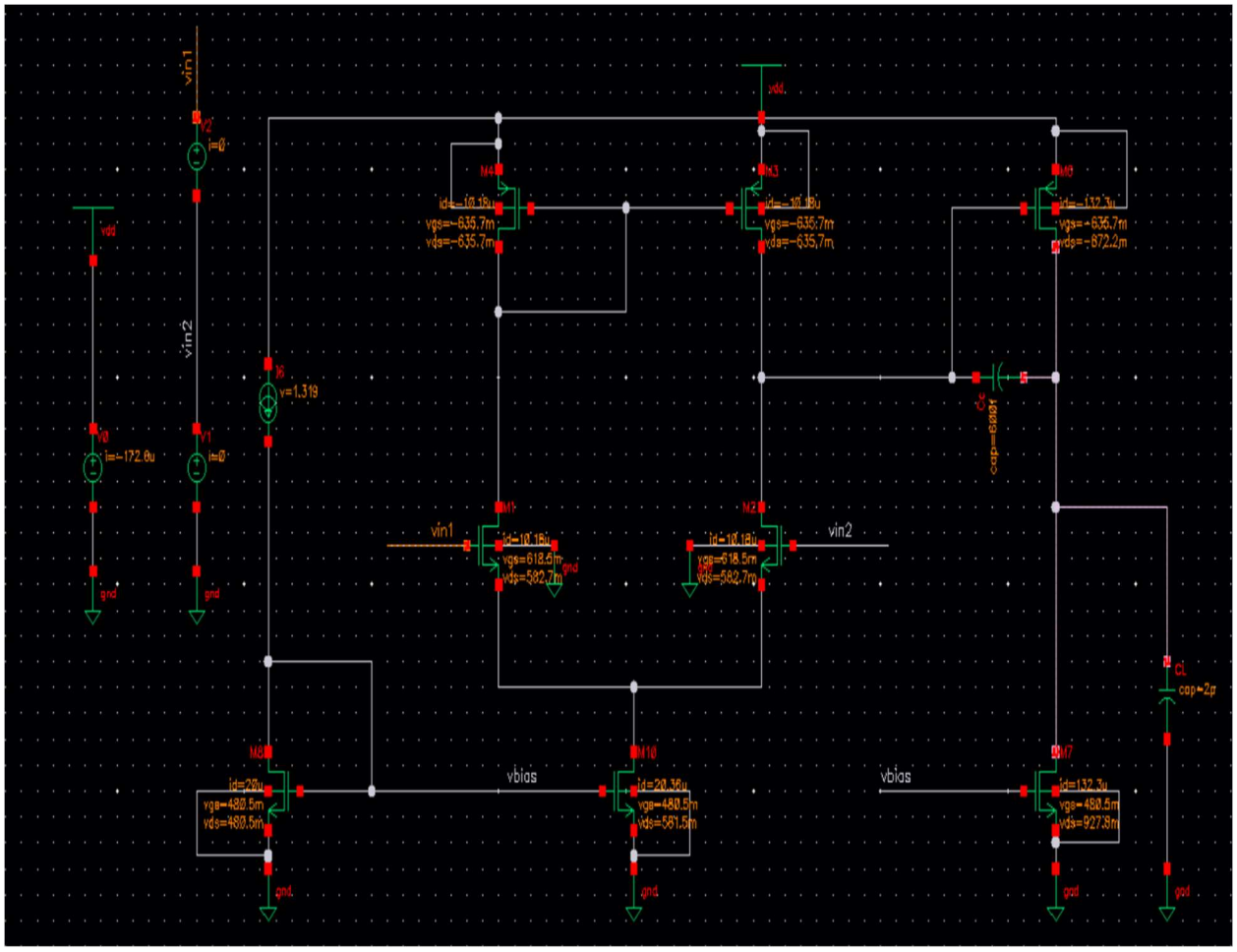
Self Project Report

- Design of a two-stage op-amp having the following specifications: Gain : 60 dB, Phase Margin : 60 deg. Gain Bandwidth Product = 30 MHz at 180 nm CMOS technology.

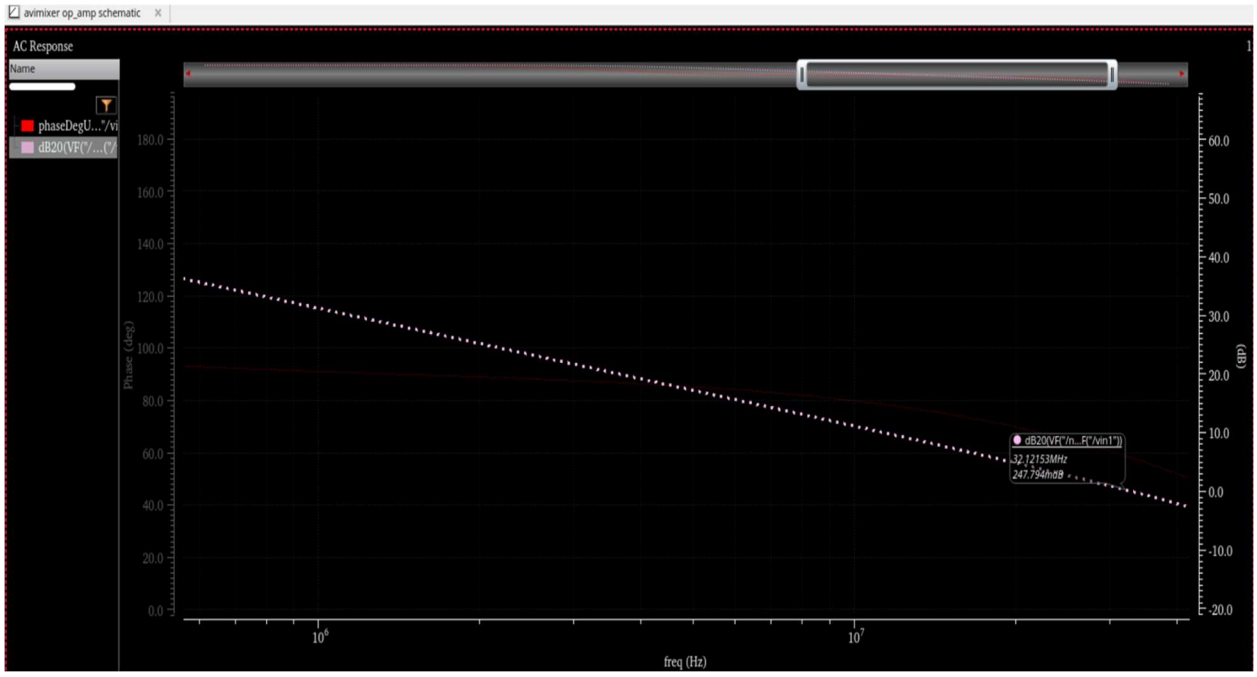
  Tool Used: Cadence Virtuoso.

  Circuit Design:

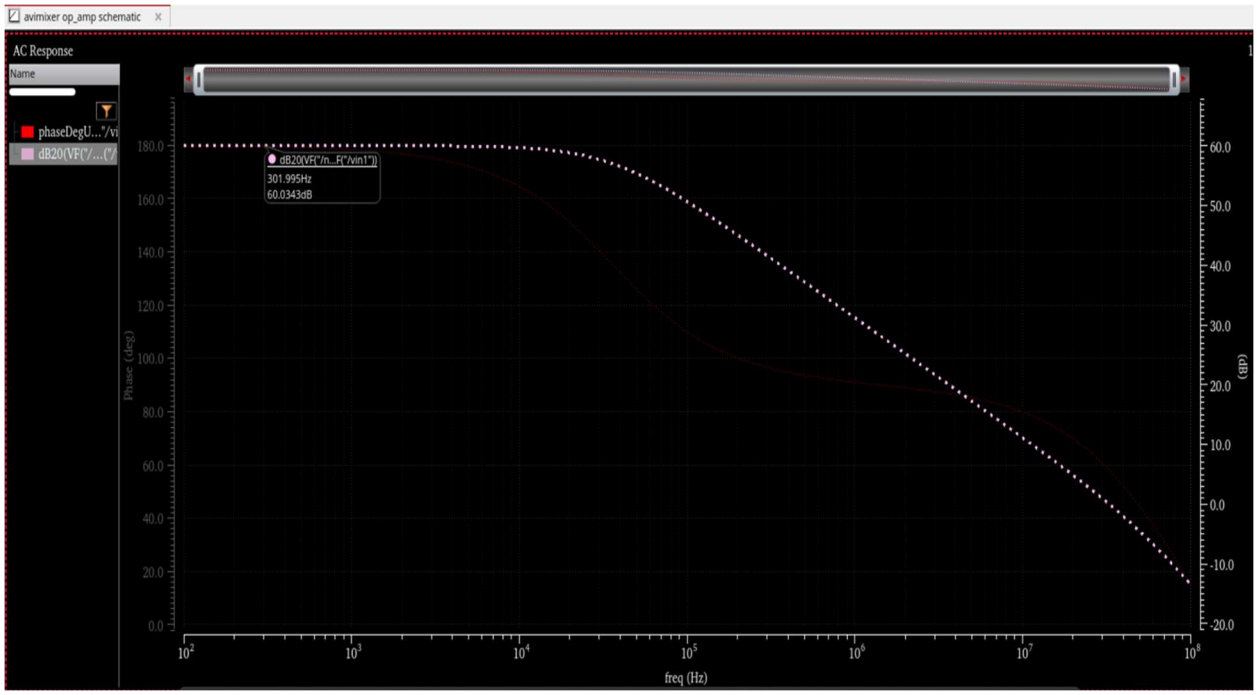


Simulation results for circuit operation at ICMR=1.6V

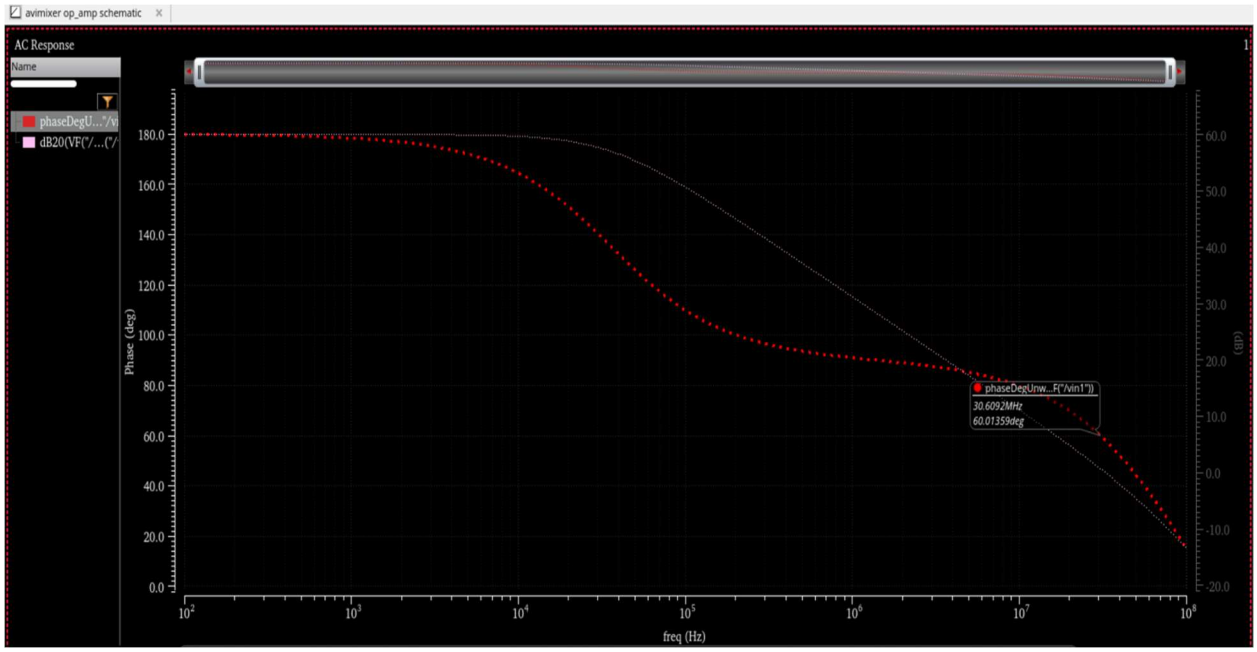
Plot for Gain Bandwidth Product estimation.



Plot for Gain estimation (Low frequency gain).

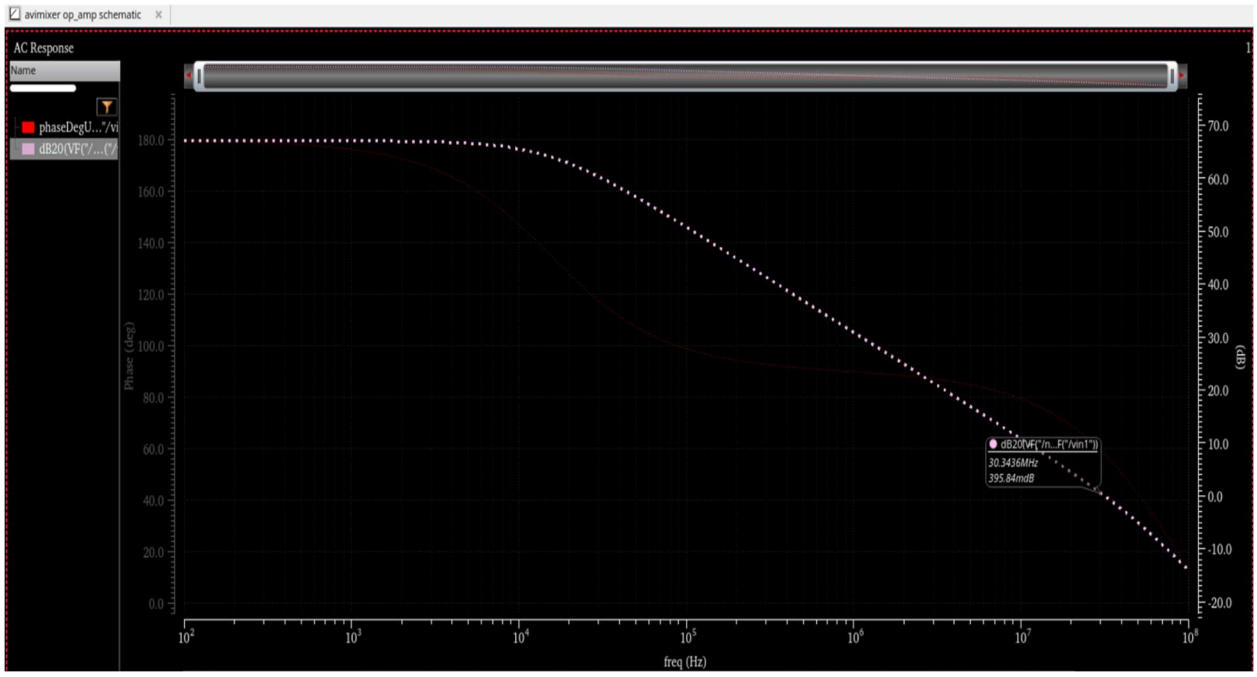


Plot for Phase margin estimation.

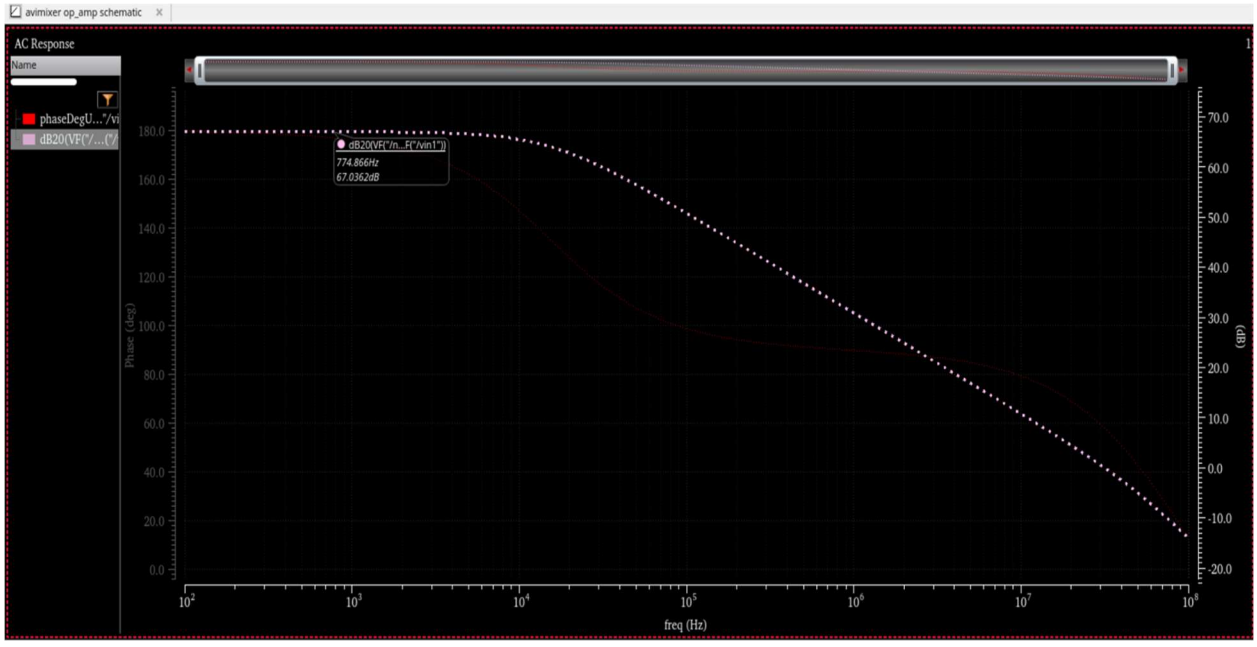


Simulation results for circuit operation at ICMR=0.8V

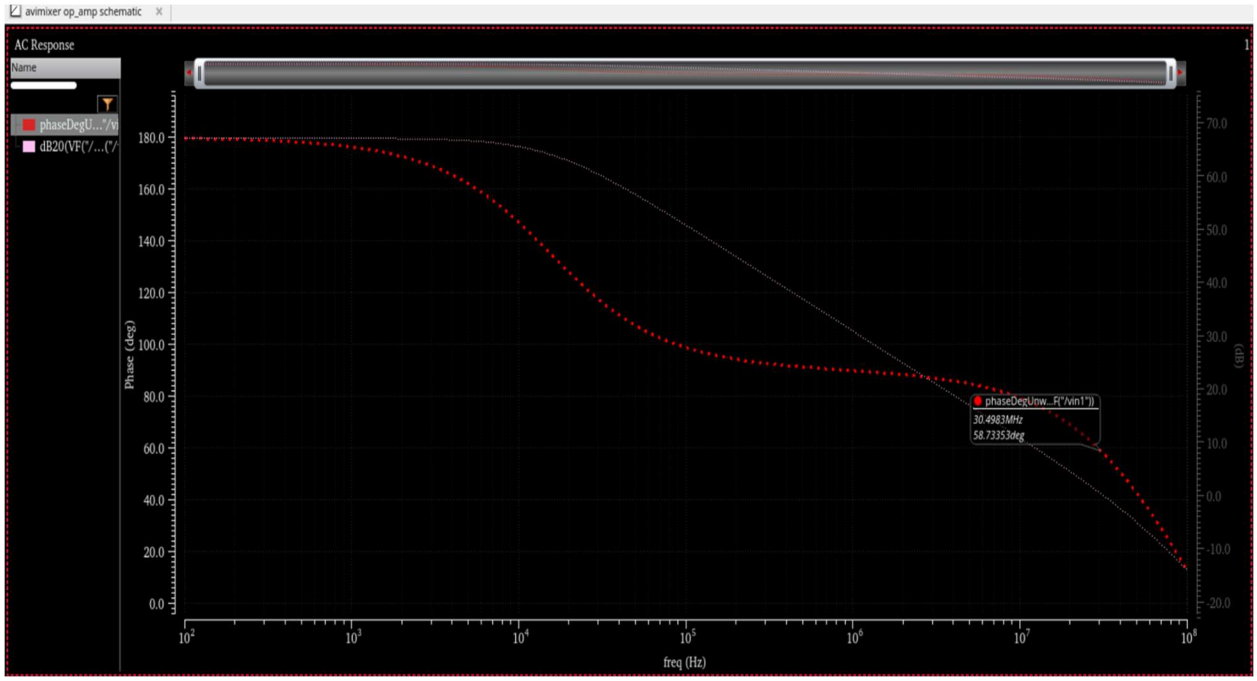
Plot for Gain Bandwidth Product estimation.



Plot for Gain estimation (Low frequency gain).

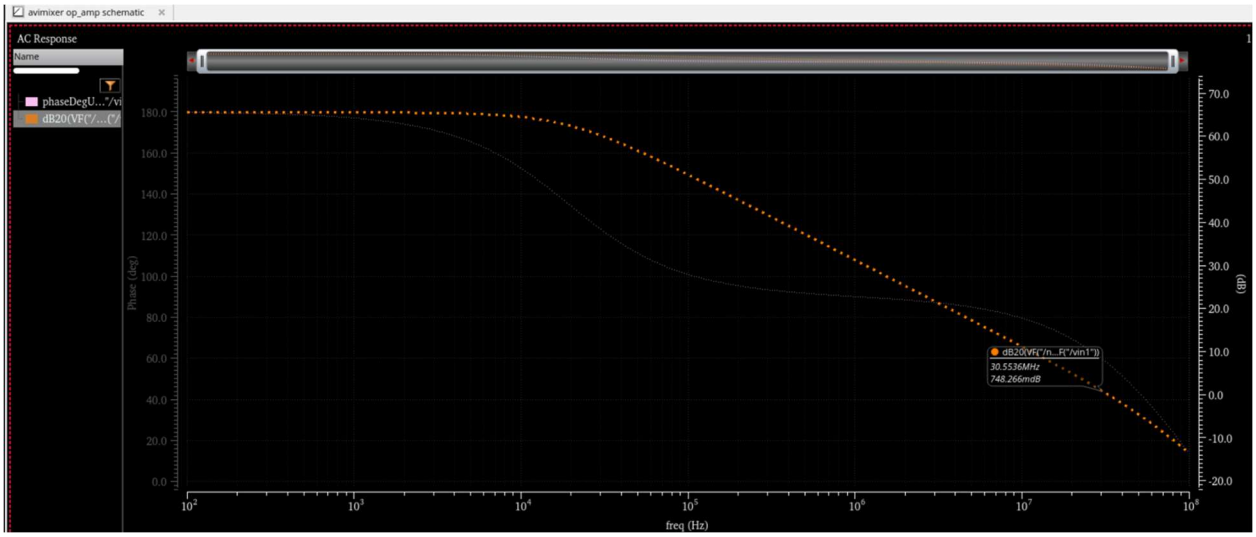


Plot for Phase margin estimation.

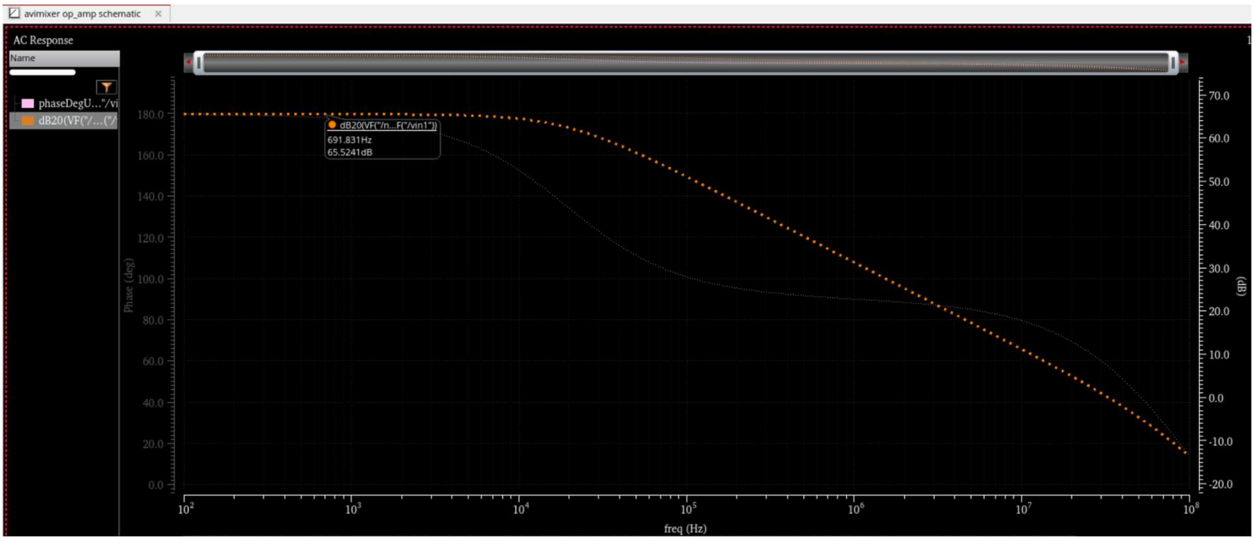


Simulation results for circuit operation at ICMR=1.2V

Plot for Gain Bandwidth Product estimation.



Plot for Gain estimation (Low frequency gain).



Plot for Phase margin estimation.