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A Miniaturized 0.78-mW/cm^2 Autonomous Thermoelectric Energy-Harvesting Platform for Biomedical Sensors

Dejan Rozgić, *Student Member, IEEE*, and Dejan Marković, *Member, IEEE*

***Abstract*—In order to use thermoelectric energy harvesters (TEHs) as a truly *autonomous energy* source for size-limited sensing applications, it is essential to improve the power conversion efficiency and energy density. This study presents a thin-film, array-based TEH with a surface area of 0.83 cm^2. The TEH autonomously supplies a power management IC fabricated in a 65-nm CMOS technology. The IC utilizes a single-inductor topology with integrated analog maximum power point tracking (MPPT), resulting in a 68% peak end-to-end efficiency (92% converter efficiency) and less than 20-ms MPPT. In an in-vivo test, a 645-μW regulated output power (effective 3.5 K of temperature gradient) was harvested from a rat implanted with our TEH, demonstrating true energy independence in a real environment while showing a 7.9 $\times$ improvement in regulated power density compared to the state-of-the-art. The system showed autonomous operation down to 65-mV TEH input.**

***Index Terms*—Boost converter, cold startup, compound harvester platform, conversion efficiency, ILRO, in-vivo, low power, MPPT, native NMOS, positive feedback, thermoelectric harvester.**

I. Introduction

HARVESTING thermal energy and its usage as a potential source for miniaturized electronic systems, has attracted a lot of attention in recent years. Many studies showed that extracting thermal energy can potentially supply hundreds of microwatts of useful power. Even though the power levels are adequate, such harvesters produce very low voltage levels, 10's–100's of mV, which are insufficient to power CMOS electronics. The focus of the research community [1]–[9] has been on improving the harvester's efficiency and low-power circuit design. Their main goal was to achieve high efficiency of processing circuits and to reduce the number of off-chip components, so that the system is optimized for size, power and cost. However, prior work lacks power density, with state-of-the-art power density below 200 μW/cm^2. Equivalently, a 1 mW of power would require a 5-6 cm^2 surface area, which is unacceptable for minimally-invasive implantable devices. The TEH conversion efficiency and power density need to be improved in order to have a *miniaturized autonomous energy* source. Also it is necessary to miniaturize the thermoelectric transducer and integrate it with the power management IC. Previous designs lack a system-level design and optimization approach, which is offered here.

Four major obstacles prevent autonomous thermal energy usage, as described below. First, since the output voltage from the transducer (that is responsible for thermal-to-electrical energy conversion) can be very low, harvesting systems should have a cold startup ability, i.e. the circuit should trigger (startup) its operation without any stored energy. A few prior designs have demonstrated this ability for thermal harvesters, [1]–[7]. Their startup units require off-chip components, which makes them unattractive for miniaturization. Some designs require a battery [1] or the output storage element to be charged to certain voltage [2], which can be used as the initial trigger. No prior work has reported an *autonomous-integrated* startup, *from a fully-discharged device*. A mechanical off-chip switch [3] is used in the boost converter design that is able to harvest energy even from a 30 mV voltage input. The use of a mechanical (motion based) switch is not autonomous and hence has limited utility. Further, it achieves peak efficiency at lower voltages; the range of high efficiency (above 50%) is quite narrow, with the efficiency dropping at higher voltages. In order to reduce the startup voltage, the authors in [6], showed post-fabricated trimmed oscillator operation down to 90 mV. Transformer based cold startup was demonstrated in [4]; however this method requires a large volume to accommodate the transformer, limiting the practical usage of the system and affecting the maximum available efficiency. To facilitate startup, the authors in [7] have recently proposed a multiple-ambient-sources-harvesting approach, where the system would start operation by using one of the energy sources and then continue to harvest higher power from another source. A pre-calibration scheme and explicit control over inductive peaking current were employed to improve efficiency; however this approach requires RF-assisted startup, which does not qualify as a fully autonomous TE self-start. Second, maximum power point tracking (MPPT) scheme has to be implemented to match the impedance of the harvester's circuit with that of the heat source, in order to maximize the available power. It is important to note that most of prior research focused on increasing converter efficiency [1]–[9], demonstrating sub-100 mV operation limited to a controlled lab

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The authors are with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA (e-mail: dejanrozgic@yahoo.com; dejan@ee.ucla.edu).

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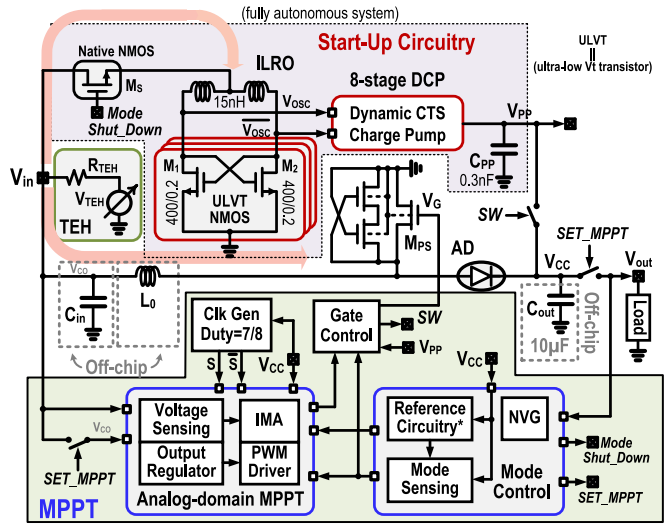

Fig. 1. Proposed thermoelctric harvesting architecture.

environment. References [2]–[4] are rare exceptions that report end-to-end efficiencies. Still, their PCB + TEG systems occupy a large area and harvesting in natural environments (where temperature differences are <3 K) would be very difficult and unreliable. Third, providing a stable thermal gradient, with minimal heat leakage in a small footprint, is very challenging and it further hindered previous attempts at truly autonomous energy harvesting. Lastly, the number of off-chip parts has to be reduced for better miniaturization.

This paper addresses the aforementioned challenges related to thermal harvesting from low input voltages, but takes into account miniaturization demands for biomedical implants. The rest of the paper is organized as follows.

The overall system, presented in Section II, features an on-chip startup CMOS circuit that is assembled with TE platform capable of extracting autonomous power. Section III describes our power management solution that makes power extraction efficient and agnostic to the harvester environment. With the fast closed-loop control techniques, described in Section IV, the low-power PM circuitry achieves high efficiency across a wide range of load currents and PVT. The high efficiency is due to accurate detection of inductor current zero-crossing and low-power comparator design. A miniaturized, custom TEH platform is described in Section V. Together with a 65 nm CMOS chip, the platform was tested in-vivo on a rat. Measurement results, discussed in Section VI, are the new state-of-the-art in autonomous thermoelectric harvesting. Our system achieves the highest level of integration, including both the PCB (circuit innovation) and TEH (materials, physics, mechanical, assembly, and surgery).

II. System Architecture

Fig. 1 shows the proposed system-level single-inductor hybrid-type architecture. A thermo-electric harvester, to a first-order approximation, is depicted as a DC-voltage source, V_{TEH}, with its internal resistance, R_{TEH}. The system comprises of an analog-domain MPPT circuit, a cold startup block based on inductive-load ring oscillator (ILRO) and mode controller. Charge transfer is done through the main boost branch comprised of an off-chip inductor, active diode AD, main boost switch $\mathrm{M_{PS}}$ and a storage element $\mathrm{C_{OUT}}$. Active diode implementation is crucial for an efficient and low-leakage power delivery. The details of the boost operation will be discussed in Section III. During the self-startup mode, an ILRO, a charge-transfer-switch (CTS) charge pump, and native NMOS mode switch with negative V_T, are employed. Once the startup block charges the output voltage (V_{CC}) to an intermediate level (0.8 V), a negative voltage generator (NVG) shuts down the startup block and the boost converter transitions to the MPPT Mode. To extract maximum power, the MPPT block is enabled; the active control of $\mathrm{M_{PS}}$ periodically turns the switch off whenever the inductor current reaches zero in the falling charge-transfer operation. The MPPT operation is detailed in Section IV. In the MPPT mode, a dedicated output regulation unit is used for output voltage control. Since the main boost switch ($\mathrm{M_{PS}}$) carries 10's of mA of current, active body control is employed to prevent reverse current flow and to mitigate the leakage current.

III. Power Management and Timing Control

A. Inductive Load Ring Oscillator (ILRO)

As mentioned before, starting up CMOS circuits with sub-100 mV input presents a difficult task in cold startup circuit design. Below 100 mV, active circuitry (transistors) operates in weak inversion (WI). In order to decrease the startup voltage, circuit designers usually connect the harvester output directly to some kind of an oscillator which acts as the system activation unit. Such oscillators demand either bulky off-chip components or their transistors require some post-fabrication tuning. Motivated by the work in [10], we leverage the fact that the inductive-load ring oscillator (ILRO) architecture can push the oscillation amplitude above the supply rails, allowing it to be triggered with very low input voltages, Fig. 2(a). We employed a 2-stage ILRO due to its simplicity and the good trade-off between the performance (low-voltage startup) and active chip area. Using the EKV Model [11], and the small-signal equivalent circuit for ILRO, Fig. 2(b), it can be shown that the minimum startup voltage for a 2-stage ILRO is half of the startup voltage for a classical CMOS inverter-based oscillator. The lower bound for the classical oscillator startup that operates in subthreshold region is described in [12] and given by:

$$V_{\mathrm{DD}}\ (\min) = 2\phi_t \ln(1+n), \tag{1}$$

where $\phi_t = kT/q$ is the thermal voltage and n represents the subthreshold slope.

Analog high-performance (native-depleted) transistors have threshold voltages around zero, resulting in a high current drive and high output gain. Thus their ILRO implementation can produce high output frequencies while supplied with low input voltages. The upper bound for the oscillator frequency is dictated by the transistor's unity-gain frequency f_T and by the load attached to the output. In a 65 nm technology, f_T for the native

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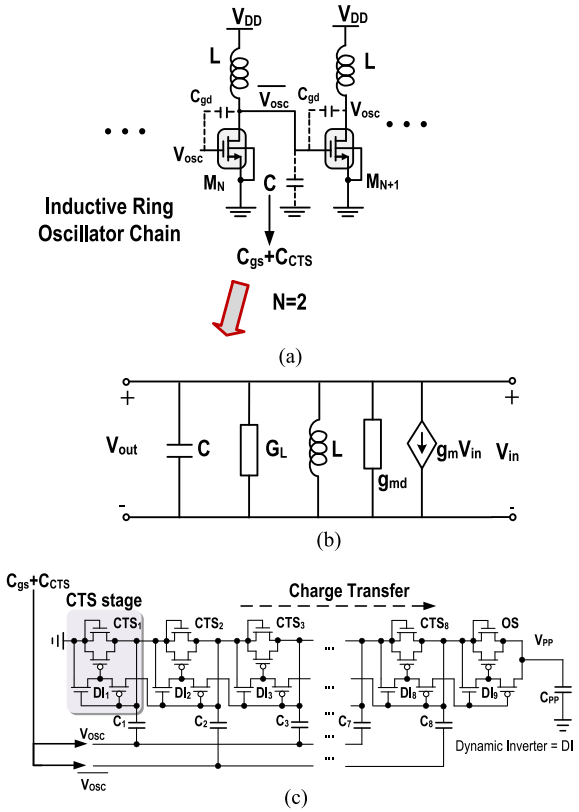

Fig. 2. (a) Inductive-load ring oscillator chain and its (b) small-signal circuit equivalent. (c) Schematic of 8-stage CTS charge pump.

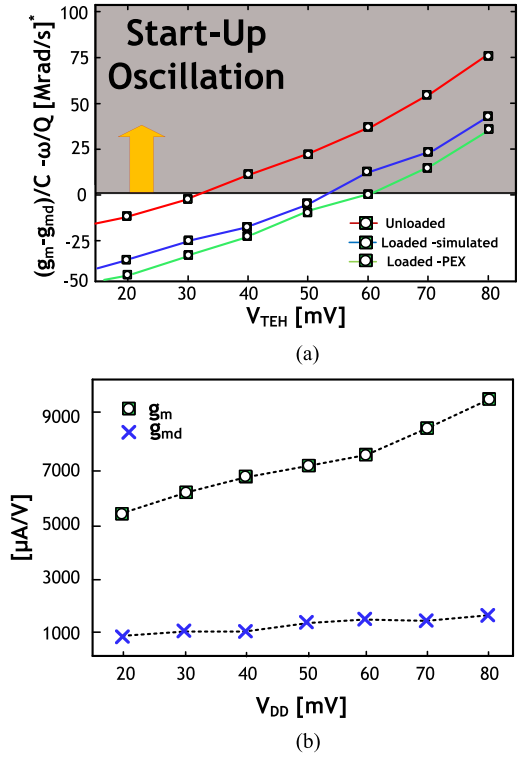

Fig. 3. (a) Simulated startup condition for a different $V_{\rm TEH}$; (b) Simulated gate and drain transconductances of the ULVT transistors ($V_S = V_B = 0$).

transistors is in the 100 MHz–1 GHz range, for $V_{\rm GS}$ of several 10's of mV (10 mV-40 mV). To derive the relationship between the minimum startup voltage for the ILRO and the transistor's geometry, we refer to Fig. 2(b), [10]–[11]. The single-stage transfer characteristic implies:

$$\frac{V_o}{V_{\rm in}} = -\frac{g_m}{g_{\rm md}+G_L}\frac{1}{1-j{\rm tan}\varphi}. \quad (2)$$

The g_m, $g_{\rm md}$ and $g_{\rm ms}$ represent the gate, drain and source transconductances of the transistor. The G_L denotes the inductor losses.

The phase shift φ for the single stage is assumed to be π without lost of generality. Assuming that $Q = \frac{\omega C}{G_L}$ is the quality factor, the Barkhausen's criterion for oscillation startup is:

$$\frac{g_m - g_{\rm md}}{C} - \frac{\omega}{Q} > 0 \quad (3)$$

The capacitance C in (3), which represents the ILRO load, is given as $C = C_{\rm CTS} + C_{\rm DS}$, where $C_{\rm CTS}$ is the input capacitance of the CTS charge pump and $C_{\rm DS}$ is the equivalent drain-source capacitance of the ILRO transistor.

The EKV model of the transistor in WI [11], implies the relationship between $g_{\rm md}$, $g_{\rm ms}$, g_m and the drain-source voltage is given by (4)–(5):

$$n\, g_m = g_{\rm ms} - g_{\rm md}, \quad (4)$$

$$\frac{g_{\rm ms}}{g_{\rm md}} = e^{\frac{V_{ds}}{\varphi_t}}. \quad (5)$$

From (2), (4) and (5), the minimum supply voltage needed for ILRO startup is given by:

$$V_{\rm DD}\,({\rm min}) = V_{\rm DS}\,({\rm min}) = \phi_t\ \ln\left[1 + n\left(1 + \frac{G_L}{g_{\rm md}}\right)\right]. \quad (6)$$

In the ideal case, the minimum supply voltage for oscillations to occur is $\phi_t \ln(1+n)$, which is exactly one-half of the minimum supply voltage needed to startup an inverter-based ring oscillator. Fig. 3(a) shows the simulated startup condition (for sustained oscillations) in terms of the minimum harvester voltage ($V_{\rm TEH}$) for the oscillator using a 65 nm technology.

In order to get more insight into the properties of the native MOS transistor, Fig. 3(b) plots g_m and $g_{\rm md}$ transconductances versus drain-source voltage $V_{\rm DS}$ that is swept from 0 to 80 mV.

The ILRO is built with inductors with $L \approx$ 15 nH and transistors with W/L = 2400 μm/0.2 μm. The inductor was picked such that its G_L has the lowest possible value within the expected frequency of operation (300 to 500 MHz). Additional headroom allocated for PVT variation and layout parasitics marginally increased the startup voltage and contributed to the drop in oscillation frequency from 350 MHz (designed) to 300 MHz (measured).

The minimum voltage needed to start the oscillation was measured to be 65 mV, closely matching the value of 60 mV obtained from PEX simulations. The efficiency of ILRO is 15% for the minimum startup voltage (simulations showed $\rm I_{DC-ILRO} \approx$ 0.13 mA @ $\rm V_{IN}$ = 60 mV, $\rm I_{DC-ILRO} \approx$ 0.39 mA @ $\rm V_{IN}$ = 100 mV).

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B. Charge-Transfer-Switch Charge Pump

The design goal for the CTS charge pump (CP) is to achieve sufficient output DC voltage and to be able to supply the control circuitry while minimizing the equivalent input capacitance. The schematic of the CTS charge pump in the proposed startup circuit is shown in Fig. 2(c). The dynamic CTS CP uses the backward and forward control for NMOS and PMOS pass transistors respectively. This scheme employs the high voltages generated in the succeeding stage to control the NMOS transistor and low voltages generated in preceding stage for the PMOS transistor. The body effect in the last stage is successfully eliminated by PMOS CTS. The CTS CP shifts the charge stage-by-stage synchronously with negligible voltage drop. The pass transistors in the charge pump are completely turned off by $V_{\rm OSC}$ and completely turned on by higher voltages from the following stage. This leads to higher efficiency since the reverse current flow is significantly reduced. The CTS also uses low-V_T (≈ 0V) transistors and their aspect ratio increases in consecutive stages in order to keep the output impedance low. Our 8-stage CTS charge pump shows 41% and 71% simulated power efficiency for $\mathrm{V_{OSC}} = 100\,\mathrm{mV_{pk-pk}}$ and $\mathrm{V_{OSC}} = 500\,\mathrm{mV_{pk-pk}}$, respectively.

C. Active Diode With Low-Voltage Drop

Since the current from the harvester flows through the diode, in all operating modes, its realization should be energy efficient and yet it should show sufficient performance. Using off-chip Schottky diodes would prevent the reverse current leakage, but their threshold voltage is bounded to 0.2 V-0.3 V and they would occupy extra PCB space. For area-limited applications, active diode implementation is a must, provided that static power is minimized. Previous solutions on active diodes [13]–[14] show fast circuits consisting of comparators, which with help of feedback actively control the diode (NMOS/PMOS) switch. The advantage of these approaches is that the diode will achieve almost zero current switching and the circuit will compensate any delay in the switch response. On the other hand, these implementations consume a lot of power in comparators and auxiliary circuitry; for biomedical applications this approach does not offer a good trade-off between design needs and power consumption. Our active diode schematic is shown in Fig. 4. The circuit is designed so that the bias current I_B presents a very small fraction of the forward current I_F; this ratio is dictated by transistor geometry. During the conduction period ($V_S > V_{\rm out} + V_{\rm DROP}$), the bias current exists and the bulk of M_D is tied to the highest available potential to mitigate the current leakage though M_D. During the blocking period, both bias and conduction currents drop down to zero due to the positive feedback in the circuit. Transistors M_{R1} and M_{R2} act as large resistors and they additionally limit the static current consumption. If the forward currents are low, transistor M_D operates in subthreshold regime and with proper sizing of M_D, M_1 and M_2, the voltage drop $V_{\rm DROP}$ can be very low, [15]. If the forward currents are high (10's of mA), the voltage drop (normally 10's of mV) is inversely proportional to the forward current. This simple design approach can reach the performance similar to the ideal Schottky diode, but with lower power. The active diode can carry 10's of mA of forward current while providing sufficiently fast signal switching.

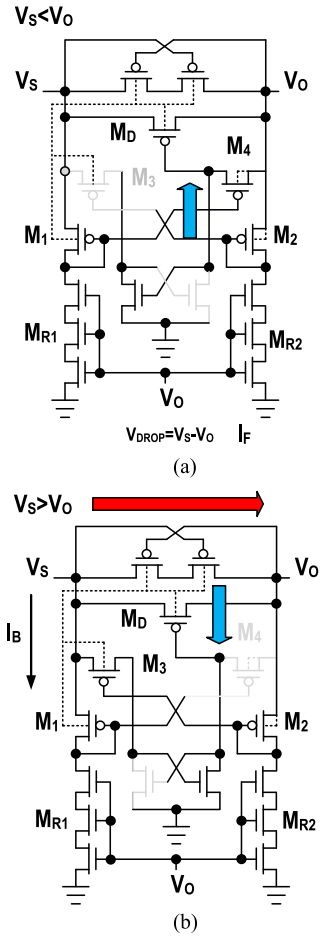

Fig. 4. Active diode (AD) during (a) ON and (b) OFF states.

D. Startup Mode and Relevant Waveforms

As previously explained, the inductive-load ring oscillator was employed due to its low voltage startup and compact area. Bulky off-chip inductors would additionally increase the startup time and voltage, and also increase the load at the ILRO output. At $t = 0$, since there is no accumulated energy in the system, the current flows from the harvester through the startup path. The native-NMOS transistor with large negative threshold voltage V_T is used as the mode switch; initially ($t = 0$) it is ON. Cross-coupled transistors M_{1-2} in the ILRO are realized with high-performance (HP) ultralow-V_T analog transistors. These transistors have enough voltage gain and high current drive even at low voltage supplies; our simulations showed $Q_{\rm ILRO} = 10.5$ at 300 MHz and 60 mV startup voltage.

For a main boost switch $M_{\rm PS}$, a low-V_T transistor was used, as it lowers the leakage current as compared to the native one, when the $\mathrm{M_{PS}}$ is OFF. Since the converter powers a simple control (digital) circuitry, the load current ($I_{\rm LOAD}$) is considered low. Discontinuous conduction mode (DCM) is the preferable operation mode of the boost converter if the output voltage of the harvester is low. In DCM – the boost converter can still have

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a large boosting ratio even with a light load current and low input voltage ($1+\frac{V_{\rm in}D^2}{2L_0 f_{\rm SW} I_{\rm LOAD}}$), [16]. The duty cycle is set to be $^3/_4$. The efficiency of the boost converter, during this mode, is inherently bounded by losses during conduction (P_α) due to resistance on the current path, and losses due to switching ($P_{\rm SW}$). The effective resistance on the current path is given by $R_\alpha = R_{\rm SW} + R_L + R_{\rm TEH}$, where R_L is the series resistance of the inductor and $R_{\rm SW}$ is the on-resistance of the main boost switch.

The power (P_R) accumulated in the inductor during the current rising can be approximated with

$$P_R = \frac{1}{2}\frac{L_0 i_{\rm peak}^2}{t_R}, \tag{7}$$

where $i_{\rm peak}$ is the inductor current at the end of the rising period t_R. The current i_R can be expressed as

$$i_{\rm peak} = \frac{V_{\rm TEH}}{R_\alpha}\left(1-e^{-\frac{R_\alpha}{L_0}t_R}\right). \tag{8}$$

Substituting (8) in (7) yields

$$P_R = \frac{L_0 {V_{\rm TEH}}^2}{{R_\alpha}^2}\frac{\left(1-e^{-\frac{R_\alpha}{L_0}t_R}\right)^2}{2t_R}. \tag{9}$$

The falling time t_F in DCM during the current drop can be approximated with

$$t_F = \frac{V_{\rm TEH}}{R_\alpha}\frac{L_0}{V_{\rm CC}+V_{\rm DROP}} \approx \frac{V_{\rm TEH}}{R_\alpha}\frac{L_0}{V_{\rm CC}}, \tag{10}$$

if we assume $V_{\rm DROP} \ll V_{\rm CC}$. In order to maximize the average power P_R delivered during one period, main switch ON-resistance and the inductor ESR have to satisfy $R_{\rm SW}+R_L \ll R_{\rm TEH}$. Larger switch will mitigate the ON resistance and result in a higher dynamic power dissipation. Preservation of energy during the startup mode gives us relation between the energy accumulated in the inductor when $M_{\rm PS}$ is turned-on and the energy dissipated on the diode during its forward bias (t_F) and energy delivered to the load during the whole period:

$$\frac{1}{2}L_0 i_{\rm peak}^2 \geq E_{\rm ESR}|_{V_{\rm CC}=0.8\,V} + E_{\rm DIODE}|_{V_{\rm CC}=0.8\,V} + V_{\rm CC} I_{\rm LOAD} T_S|_{V_{\rm CC}=0.8\,V}. \tag{11}$$

With maximizing power P_R (i.e. $\frac{dP_R}{dt_R}=0$) and given (7)–(11) we can determine the lower bound of the inductance L_0 and desired DCM period T_S. We employed $T_S = 80\ \mu$s and $L_0 = 150\ \mu$H (footprint: 6 mm x 5.6 mm). Note that L_0 does not have a linear impact on the footprint; the footprint is more sensitive to R_L than to L_0. Fig. 5 shows the power distribution during one converter cycle after parameter optimization. Out of 27% total power loss, 22% is in the conduction loss. Simulation results indicate an available load current close to 0.4 μA, which is sufficient to drive the auxiliary control circuits.

Fig. 6 shows the startup mode during both phases. After voltage $V_{\rm PP}$ passes 0.3 V, the thyristor-based oscillator (TRO) will start driving the buffer in the gate-control (GC) block which will conduct charging/discharging of the power switch $M_{\rm PS}$. In the charging phase, the startup block is turned OFF since the current

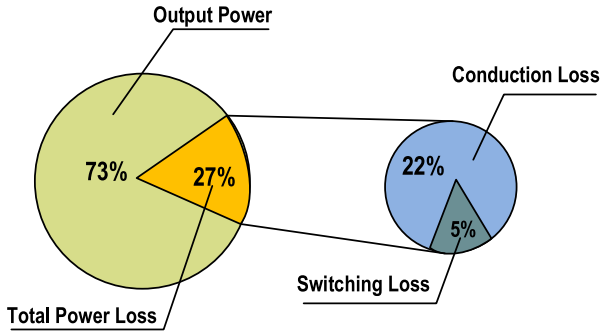

Fig. 5. Simulated power distribution after design optimization.

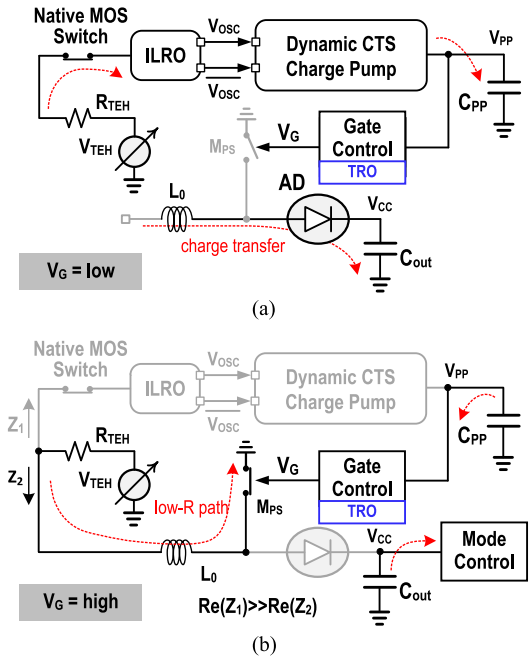

Fig. 6. Active circuitry during the startup mode in (a) discharging and (b) charging phases (adapted from [17]).

flows through the path of lower resistance (Z_2 in this case). In the discharging phase (V_G is low), the energy stored in L_0 is transferred through AD to the output capacitance $C_{\rm PP}$. Concurrently, the current from the harvester closes the loop through ILRO again; starts oscillations and the charge pump additionally recharges the auxiliary capacitance $C_{\rm PP}$. Control circuitry that is biased from $C_{\rm PP}$ consumes less than 100 nA over one period. The startup block is turning on periodically while the output voltage $V_{\rm CC}$ keeps increasing.

The true single-phase latch (TPSC) keeps the MPPT controller in idle mode during the startup phase. Post-layout simulated waveforms during startup mode are shown in Fig. 7. The MPPT controller becomes active after the output voltage is boosted to 0.8 V.

IV. MPPT Mode and Timing Diagrams

The MPPT mode requires a low-power comparator scheme that can achieve adequately fast state transitioning. In order to

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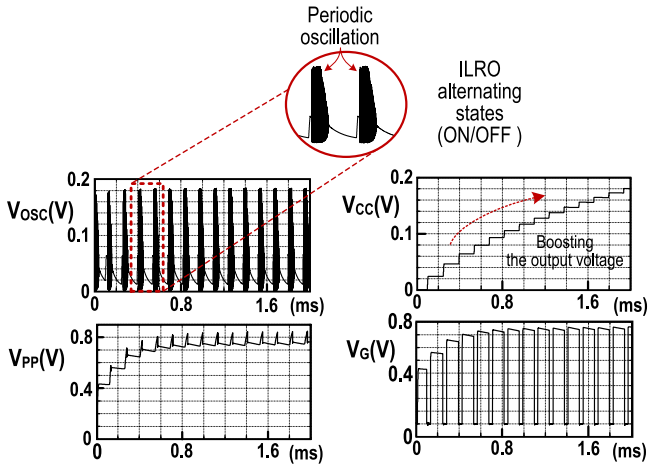

Fig. 7. PEX-simulated startup for a different V_{TEH}. (adapted from [17]).

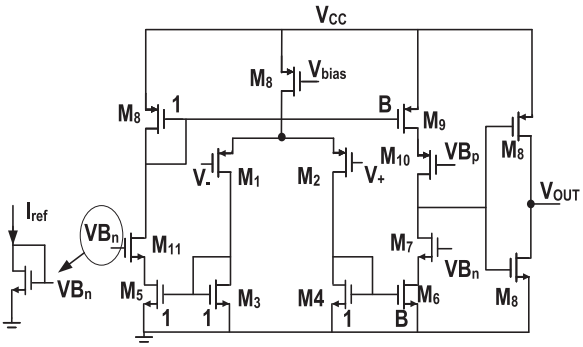

Fig. 8. Two-stage comparator design.

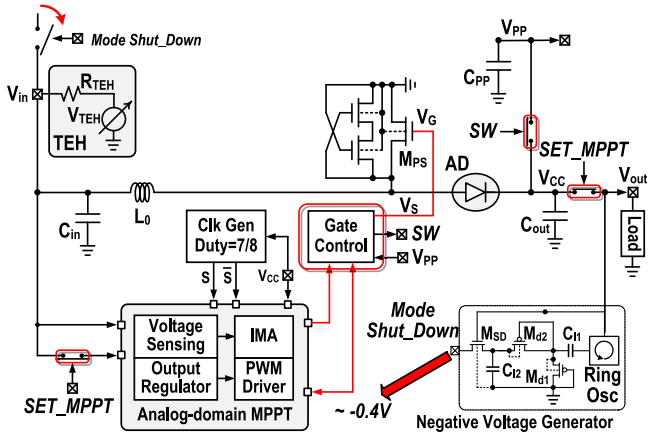

Fig. 9. Activation of MPPT block and shut-down of low-voltage starter.

satisfy these requirements, a two-stage OTA-based comparator is employed, as shown in Fig. 8.

The comparator is designed so that the current consumption is less than 470 nA for a supply voltage of 1.8 V while achieving switching frequency of 0.1 MHz.

The maximum power point (MPP) of a thermoelectric harvester is attained when the input voltage is at one half of the open-circuit voltage. Because the MPP changes the value with

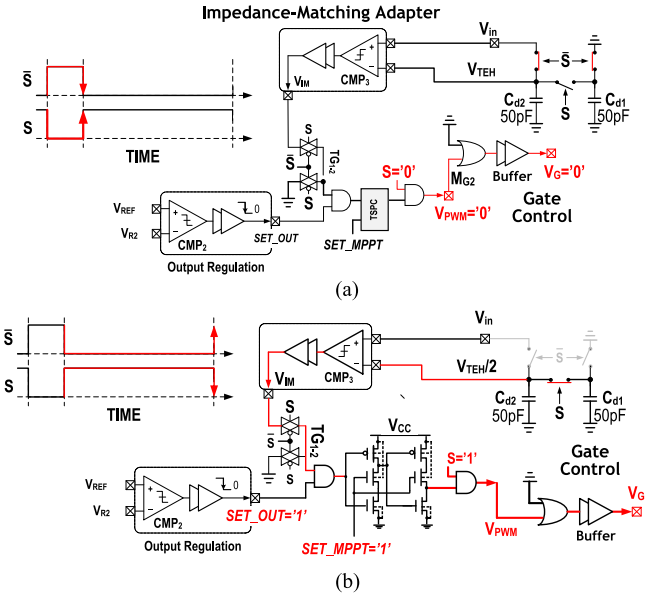

Fig. 10. MPPT operation: a) open-circuit condition, b) feedback loop during the PWM phase.

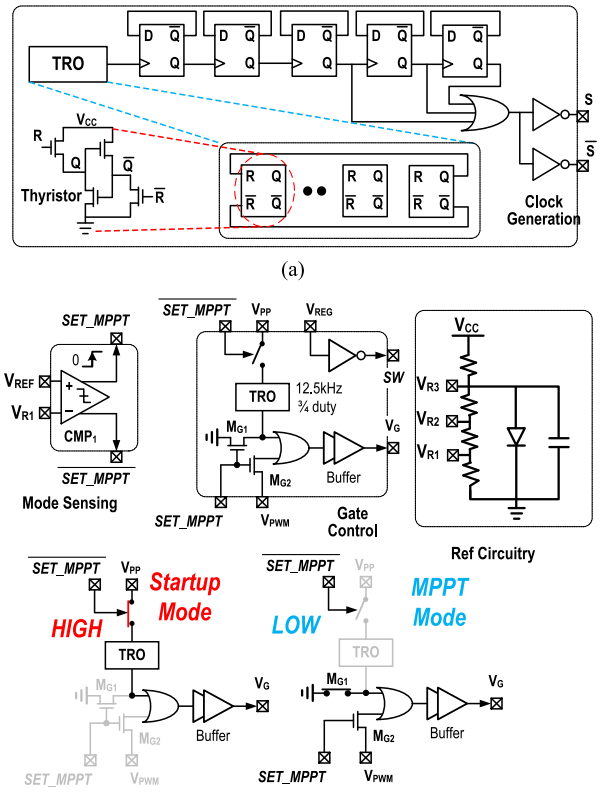

Fig. 11. (a) Reference and clock generation, (b) Gate control block during startup (left) and MPPT (right) modes.

the environment conditions such as the pressure, temperature fluctuations and also it varies with load requirements, a control circuit for MPP tracking is employed to sense half of the open-circuit voltage and to adaptively follow the MPP.

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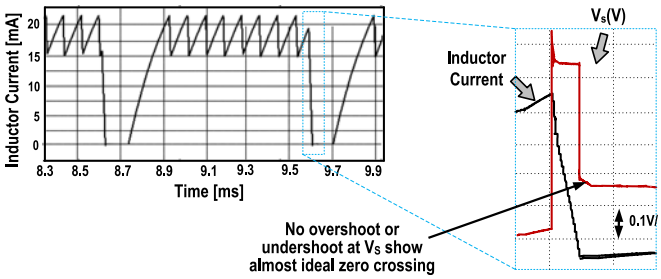

Fig. 12. Inductor switching waveform for V_S at V_{TEH} = 180 mV showing almost perfect zero switching.

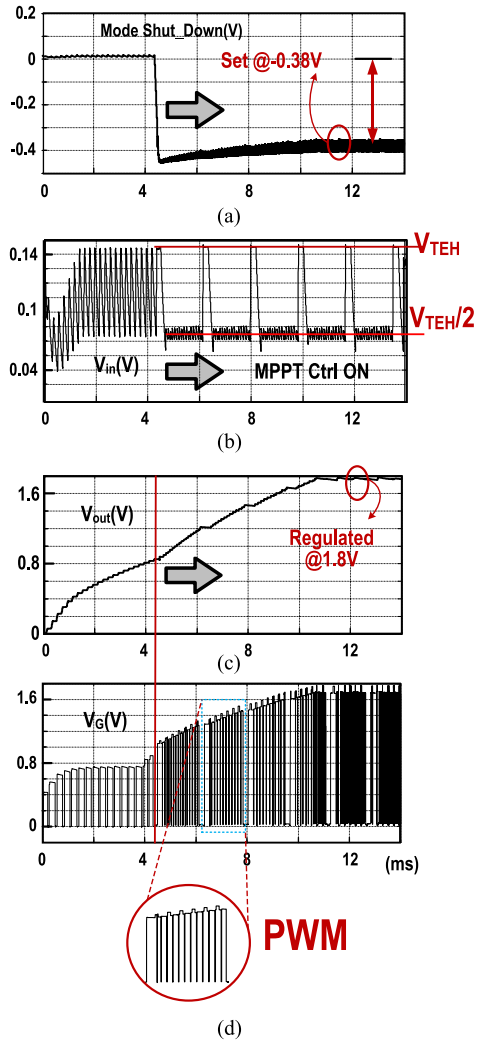

Fig. 13. Relevant waveforms during MPPT operation: (a) shut-down voltage, (b) input voltage, (c) output voltage, (d) gate voltage.

The maximum output power, $P_{\max}$, can be expressed as:

$$P_{\max} = \frac{{V_{\rm TEH}}^2}{4R_{\rm TEH}}, \text{ with } V_{\rm in} = \frac{V_{\rm TEH}}{2}, \tag{12}$$

The MPPT loop and all active circuits during this mode are shown in Fig. 9. After the activation of the MPPT controller (SET_MPPT = high), the negative voltage generator produces

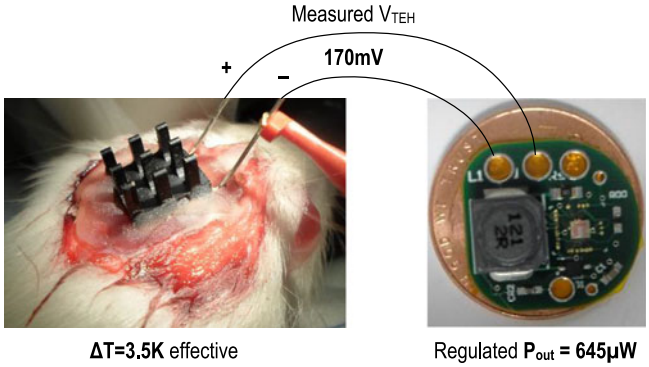

Fig. 14. Implanted TEH module shows 170 mV in-vivo, with 645 μW regulated output power (adapted from [17]).

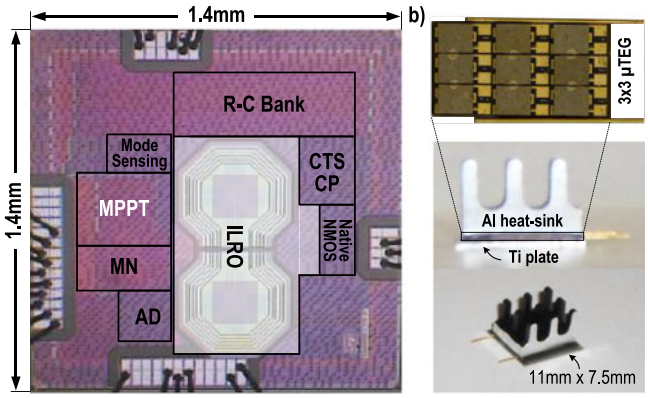

Fig. 15. (a) Chip micrograph, (b) Fabricated compound TEH platform.

−0.4 V at its output to turn-off the native transistor (the mode switch) and the startup block. A clock generator outputs complementary signals S and $\bar{S}$ with a 7/8 duty ratio and a 600 μs period. When S = low, the open-circuit voltage $V_{\rm TEH}$ is sampled, while the PWM and GC blocks keep signals $V_{\rm PWM}$ and V_G at zero, Fig. 10(a). During this period, the active diode prevents the reverse current flow from output capacitor $C_{\rm OUT}$. When S = high, the capacitive divider gives $V_{\rm TEH}/2$ by sharing the charge between the capacitors C_{d1} and C_{d2}.

CMP$_3$ dynamically matches the input voltage $V_{\rm in}$ and $V_{\rm TEH}/2$, by accommodating the pulse width of the gate voltage V_G through the feedback loop formed by CMP$_3$, inductor, the PWM and GC blocks. For precise control, it is important to minimize offset of CMP$_3$ comparator. The energy stored in inductor is transferred to $C_{\rm OUT}$ during the $\bar{S}$ phase, Fig. 10(a).

Fig. 10(b) shows the active circuitry in the feedback loop when S is high. If the input voltage is higher than $V_{\rm TEH}/2$, CMP$_3$ will turn-on the main boost switch $M_{\rm PS}$ through TG$_1$, TPSC and GC blocks. As the current through inductor keeps increasing, the input voltage is decreasing. After the input voltage reaches $V_{\rm TEH}/2$, the MPPT controller turns off the main switch $M_{\rm PS}$. Potential V_S becomes higher than the output voltage, and the energy stored in the inductor is transferred into $C_{\rm OUT}$ via AD. Then the current through the inductor starts to decrease, while $V_{\rm in}$ goes further below $V_{\rm TEH}$. After a full period, the input voltage will go up while the inductor current will go down; this

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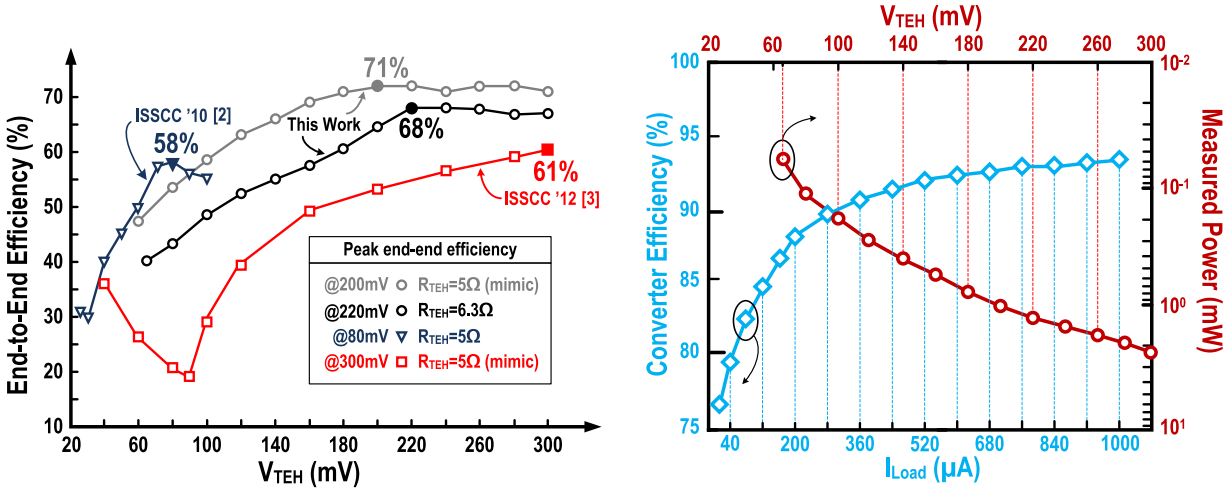

(a) (b)

Fig. 16. (a) End-to-end efficiency comparison with state-of-the-art. (b) Measured converter efficiency as a function of the output load current (left vertical axis), and measured output power (right vertical axis) as a function of the source voltage.

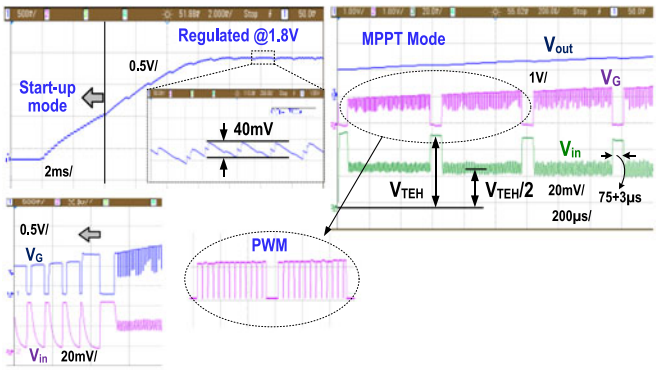

Fig. 17. Measured lab waveforms show $V_{\mathrm{TEH}} = 65$ mV and regulation to 1.8 V in less than 20 ms (adapted from [17]).

sequence starts repeating periodically, after V_{in} becomes higher than $V_{\mathrm{TEH}}/2$.

Due to the fast voltage sensing ($C_{d1} = C_{d2} = 50$ pF) and comparator fast transition, CMP_3 enables the system to find MPP very quickly; less than 20 ms is needed for complete MPP regulation. The fast feedback-loop response results in a small voltage ripple at V_{in} with a small (2 nF) input capacitance C_{in} and short settling time (3 μs). The amount of ripple is dependent on the input capacitance (C_{in}). The regulated output of the TEH is kept at its MPP with negligible voltage ripple. Any voltage fluctuations at the harvester side (up to 50 Hz) can be captured by the feedback loop in MPPT controller. The input signal periodically moves between V_{TEH} and $V_{\mathrm{TEH}}/2$ confirming the correct impedance matching. Until the output voltage doesn't reach 1.8 V, which is the target value (to power neural recording interfaces), MPPT mode is active. Comparator CMP_2 keeps the output voltage at the desired value by dynamically alternating the control signal SET_OUT. Auxiliary circuitry and MPPT controller consume less than 2.9 μA during active mode and 0.07 μA during idle mode, which directly translates into high converter efficiency. Circuit details of auxiliary blocks used in MPPT block and GC are shown in Fig. 11. The clock generation block uses thyristor-based cells, while the reference on the chip employs simple, low power diode-based circuitry.

The measured inductor current and the voltage V_{S} at the inductor current zero-crossing are shown in Fig. 12. The potential at the node V_S shows no undershoots or overshoots while crossing zero which implies almost perfect zero detection during $\bar{S}$ period. Fig. 13 shows the simulated waveforms during MPPT control. With this MPPT regulation scheme, we can approximate (to a first order) the available average load current during one period as:

$$I_{\mathrm{LOAD,avg}} \approx \gamma B f\left(L_0, D, f, R_\alpha\right) \frac{V_{\mathrm{TEH}}}{2R_{\mathrm{TEH}}} \frac{L_0}{T}, \qquad (13)$$

where $B = \frac{V_{\mathrm{TEH}}}{V_{\mathrm{CC}}}$ is the reciprocal boosting ratio, $f = (1 - e^{\frac{D R_\alpha}{f L_0}})^2$ and γ depends on the input ripple and the speed of the feedback loop [16], [18]. As (15) implies, the higher output current and boosting ratio require higher inductance value.

V. Compound TEH Platform

We have designed and fabricated compound THE module (Fig. 14) in order to meet the stringent anatomical and biophysical confinements of living subjects including but not limited to rats. The animal's cerebrovascular system is directly in contact with the bottom part of the TEH platform which is made of bio-friendly material – titanium. At the bottom titanium plate, we have arranged 3×3 thermo-electrical elements (μTEGs [19]); each μTEG behaves as an independent voltage source. The μTEG array is attached to the titanium plate with a thin layer of thermo-conductive glue.

By serially stacking three μTEGs and connecting these stacks in parallel the output power can be increased while maintaining the equivalent source impedance of a single μTEG source. Post-fabrication measurements of our TEH structure showed

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TABLE I
COMPARISON WITH STATE-OF-THE-ART THERMAL ENERGY HARVESTERS

Reference	[2]+	[3]	[4]++	[5]	[7]+++	[22]	[23]	[24]	[25]+	This work
Process	0.13 μm	0.35 μm	0.13 μm	65 nm	0.13 μm	0.18 μm	65 nm	0.18 μm	0.13 μm	65 nm
Startup mechanism	External voltage	Mechanical	White noise	Electrical	RF-Kick startup	No Start-Up Unit	Electrical	Electrical	Electrical	Electrical
Min $V_{start-up}$	650 mV	35 mV	40 mV	50 mV	220 mV		80 mV	350 mV	150 mV	65 mV
Regulated V_{out}	1 V	1.8 V	2 V	1.2 V	1.2 V	0.5 V	0.7 V-1 V	1.8 V	1.8 V	1.8 V
Peak efficiency	63% e-e	58% e-e	61% e-e	N/A	N/A	N/A	N/A	N/A (80% cnv)	N/A	68% e-e
end-end (conv.)	(75% cnv)	(91% cnv)	(N/A cnv)	(73% cnv)	(83% cnv)	(83.6% cnv)	(73% cnv)	w/o regulation	(73% cnv)	(92% cnv)
Off-chip L+C+R	1 + 3 + 0	3 + 4 + 0	2 + 5 + 0	3 + 4 + 0	1 + 2 + 0	1 + 3 + 0	4 + 2 + 0	0 + 7 + 4	0 + 6 + 0	1 + 2 + 0
Regulated Power Density @ΔT = 4 K (μW/cm^2)	22	34	N/A**	162	80*	N/A**	N/A**	128	N/A**	1285
Tracking Time	N/A	~20 ms	~20 s	~25 ms	~ 50 s	N/A	~20 ms	< 180 ms	N/A	< 20 ms
In-Vivo	NO	YES	NO	NO	YES	NO	NO	NO	NO	YES

Vstart-up refers to VTEH (e-e) end-to-end (cnv) converter.
(+) no MPPT (++) uses transformer (+++) operation down to10 mV, but need 220 mV for the startup.
(*) Harvested Power During In-Vivo experiment without reporte.d area/volume of their system (**) Partial Solutions without In-Vivo experiment and system reported.

an equivalent 6.3 Ω of internal impedance. Slight increase in impedance is due to the bond wires and Ohmic contacts. Also, 11 mm $\times$ 7.5 mm heat sink is utilized, which is large enough to cover all three TEGs, while the bottom plate extends 1 mm on both sides to accommodate skull-fixing screws. Further, in order to confine the heat flow and prevent unwanted heat leakage on the side, the exposed space between the heat sink and the bottom plate is filled with a biocompatible insulator. By controlling the output resistance, we have an explicit control over the power delivered to the load. Compared to standard animal head-stages, our design occupies a smaller volume and does not present a burden to animal behavior.

VI. EXPERIMENTAL RESULTS

The proposed low-power, boost-converter for TE harvesting applications was implemented in a 65 nm CMOS technology. Fig. 15 shows the micrograph of the chip with the MPPT controller occupying 0.06 mm^2 while the ILRO-based startup block takes 0.65 mm^2 of the chip area. As suggested in [10], [20], designing the Colpitt's-based or multi-stage ILRO would require more on-chip inductance, with inevitable increase in the chip area. For bench-top evaluation, a voltage DC-source together with serial resistance was employed to mimic the TEH. The peak end-to- end efficiency is defined as the ratio between the maximum available power delivered to the load during the impedance matching ($V_{\rm in} = V_{\rm TEH}$ /2) and the maximum available power from the thermo-electric harvester

$$\text{Peak End to End Efficiency} = \frac{P_{\text{out}|V_{\text{out}}=1.8\ V}}{P_{\text{in}|V_{\text{in}}=V_{\text{TEH}}/2}}. \qquad (14)$$

The chip-verification comprises of two parts: cold startup, and MPPT operation with mode change. Peak end-to-end efficiency is 68% at $V_{\rm TEH} = 220$ mV, outperforming prior art, as shown in Fig. 16. Measured waveforms during the startup mode and the MPPT control (Fig. 18) imply *fully autonomous* operation down to $V_{\rm TEH} = 65$ mV. In our bench-top setup, we measured the efficiency for $V_{\rm TEH}$ from 60 to 300 mV.

$V_{\rm TEH}$ is sampled when $\bar{S}$ is high and stays around $V_{\rm TEH}/2$ when $\bar{S}$ is low. In Fig. 17, $V_{\rm TEH}$ and $V_{\rm IN}$ are 65 mV and 32 mV, respectively, demonstrating the functionality of the MPPT control. In the MPPT mode, the main contributors to energy loss are the inductor resistance and switching losses associated with the $M_{\rm PS}$ switch, as predicted by simulations. In order to demonstrate fully-autonomous operation, we also conducted in-vivo testing. Collaborators from the UCLA Department of Neurology have provided us with adequate infrastructure for the in-vivo test. There was no craniotomy on the animal (for microelectrode insertion). The entire experiment lasted about 20 minutes, after which the animal got stitched and returned to its habitat, fully recovered. Our experiment was far less invasive than a typical animal surgery involving craniotomy and cementing of the head stage. The heat sink is only 9 mm tall and it is smaller and lighter than head-caps used in animal neuroscience, hence it does not negatively impact the animal behavior. It is necessary to ensure thermal flow through a small area, hence the need for a thermal antenna. In fact, our TEH heat-sink is much less invasive than head-caps used today. We have demonstrated feasibility of our technology in a neuroscience application. Further opportunities exist in environmental monitoring and similar areas.

The harvesting platform is mounted on the head of a rat and temperature gradient of 3.5 K is measured while the system was able to harvest 645 μW regulated output power, with 61% end-to-end and 92% converter efficiencies, Fig. 17. The power level indicates that TE harvester outputs $V_{\rm TEH} = 170$ mV at stable state. The keys to the improved efficiency lie in integrated power-efficient startup unit, the compact TEH source, and the fast fully-analog MPPT controller. Our fully-autonomous thermoelectric harvester shows a 7.9 $\times$ improvement in regulated power density from a 0.83 cm^2 surface area (see Table I) relative to the current state-of-the-art. With one storage cap and only one off-chip inductor, the mote-PCB paves the road to the new level of miniaturization. The compound TEH together with a small PCB occupies less than 1 cm^3 of volume and weighs less than 3 g. TEH platform presented in this work is the new state-of-the-art in the factor and power density levels.

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With the presented approach, elimination of bulky batteries in size-constrained neural recording sensors becomes possible and their integration presents the future work.

VII. Conclusion

This paper demonstrated a fully-integrated, electrical startup boost converter for autonomous thermo-electric harvesting. A standalone thermoelectric platform integrates our efficient power management IC with customized TEH into a single micro-system. We fabricated our TEH with tiny μTEGs, which have a great power levels (measured 645 uW end-to-end), and with customized and optimized platform we were able to maintain stable temperature gradient over a 9 mm thin platform. We have shown: 1) the most efficient single-ambient-source circuitry reported to date (68% vs. 61% in prior work) while achieving 2) the most compact PCB + TEG reported to date ($6.3\times$ smaller than prior art) and additionally providing 3) the first demonstration of fully autonomous TEG operation in real environment (vs. lab-bench). We require only 1 off-chip inductor and two small off-chip capacitors. Overall, this leads to $\sim 6\times$ smaller PCB footprint than previous work from [3] and [5]. Our analog MPPT minimizes energy loss and achieves $<$20 ms output regulation (very important requirement in the event of temperature fluctuations).

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References

[1] I. Doms, P. Merken, C. V. Hoof, and R. P. Mertens, "Capacitive power management circuit for micropower thermoelectric generators with a 1.4 μA controller," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2824–2833, Oct. 2009.

[2] E. J. Carlos *et al.*, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, Apr. 2010.

[3] Y.K. Ramadass *et al.*, "A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 333–341, Jan. 2010.

[4] J.-P. Im, S.-W. Wang, S.-T. Ryu, and G.-H. Cho, "A 40 mV transformer-reuse self-startup boost converter with MPPT control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3055–3067, Dec. 2012.

[5] H.-Y Tang, P.-S. Weng, P.-C. Ku, and L.-H. Lu, "A fully electrical startup batteryless boost converter with 50 mV input voltage for thermoelectric energy harvesting," in *Proc. IEEE Symp. VLSI Circuits Dig. Tech. Papers*, 2012, pp. 196–197.

[6] P.-H. Chen *et al.*, "Startup techniques for 95 mV step-up converter by capacitor pass-on scheme and VTH-tuned oscillator with fixed charge programming," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. *1252–1260*, May 2012.

[7] A. Shrivastava, N. E. Roberts, O. U. Khan, D. D. Wentzloff, and B. H. Calhoun, "A 10 mV-input boost converter with inductor peak current control and zero detection for thermoelectric and solar energy harvesting with 220 mV cold-start and 14.5 dBm, 915 MHz RF kick-start," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. *1820–1832*, May 2015.

[8] T. Torfs *et al.*, "Wearable autonomous wireless electroencephalography system fully powered by human body heat," in *Proc. IEEE Sensors*, Oct. 2008, pp. 1269–1272.

[9] W. Jung *et al.*, "A 3 nW fully integrated energy harvester based self-oscillating switched capacitor DC-DC converter," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 398–399.

[10] M. B. Machado, M. C. Schneider, and C Galup-Montoro, "On the minimum supply voltage for MOSFET oscillators," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 61, no. 2, pp. 347–357, Feb. 2013.

[11] C. Enz, F. Krummenacher, and E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *J. Analog Integr. Circuits Signal Process.*, vol. 8, pp. 83–114, Jul. 1995.

[12] J. D. Meindl and A. J. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1515–1516, Oct. 2000.

[13] H.-M. Lee and M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications", *IEEE Trans. Circuits Syst.—I: Regular Pap.*, vol. 58, no. 8, Aug. 2011.

[14] C.-S. A. Gong, "An active-diode-based CMOS rectifier for biomedical power harvesting applications," *Int. J. Circuit Theory Appl.*, vol. 39, no. 5, pp. 439–449, 2011.

[15] C. van Liempd, S. Stanzione, Y. Allasasmeh, and C. van Hoof, "A 1 μA-to-1 mA energy-aware interface IC for piezoelectric harvesting with 40 nA quiescent current and zero-bias active rectifiers," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 76–77.

[16] E. Rogers, "Understanding boost power stages in switch mode power supplies," *Appl. Rep., Tex. Instrum.*, 1999.

[17] D. Rozgić and D. Marković, "A 0.78 mW/cm2 autonomous thermoelectric energy-harvester for biomedical sensors," in *Proc. Symp. VLSI Circuits*, Jun. 2015, pp. 278–279.

[18] R.W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.

[19] Laird Technology, [Online]. Available: http://lairdtech.com, eTEG Series PG37.

[20] A. M. Niknejad and H. Hashemi, *mm-Wave silicon Technology 60 GHz and Beyond*. New York, NY, USA: Springer, 2008.

[21] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, "A 1.1 nW energy-harvesting system with 544 pW quiescent power for next-generation implants," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2812–2824, Dec. 2014.

[22] P.-H. Chen and P.-Y. Fan, "An 83.4% peak efficiency single-inductor multiple-output based adaptive gate biasing DC-DC converter for thermoelectric energy harvesting," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 62, no. 2, pp. 405–412, Feb. 2015.

[23] C. Veri *et al.*, "An 80 mV startup voltage fully electrical DC–DC converter for flexible thermoelectric generators," *IEEE Sensors J.*, vol. 16, no. 8, pp. 2735–2742, Apr. 15, 2016.

[24] S. Carreon-Bautista, L. Huang, and E. S. Sinencio, "An autonomous energy harvesting power management unit with digital regulation for IoT applications," *IEEE J. Solid-State Circuits*, vol. 51, no. 6, pp. 1457–1474, Jun. 2016.

[25] J. Kim, P. K. T. Mok, and C. Kim, "A 0.15 V input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 414–425, Feb. 2015.

[26] A. Zurbuchen *et al.*, "Towards batteryless cardiac implantable electronic devices—The swiss way," *IEEE Trans. Biomed. Circuits Syst.*, accepted for publication.

[27] X. Wang *et al.*, "A high efficiency CMOS charge pump for low voltage operation," in *Proc. ASICIEEE 8th Int. Conf.*, 2009, pp. 320–323.

[28] S. Lineykin and S. Ben-Yaakov, "Modeling and analysis of thermoelectric modules," *IEEE Trans. Ind. Appl.*, vol. 43, no. 2, pp. 505–512, Mar. 2007.

[29] A. Shrivastava, Y. K. Ramadass, S. Khanna, S. Bartling, and B. H. Calhoun, "A 1.2 W SIMO energy harvesting and power management unit with constant peak inductor current control achieving 83–92% efficiency across wide input and output voltages," in *Proc. Symp. VLSI Technol. Circuits*, 2014, pp. 1–2.

[30] E. E. Aktakka and K. Najafi, "A micro inertial energy harvesting platform with self-supplied power management circuit for autonomous wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 2027–2029, Sep. 2014.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

[31] M. B. Machado, M. C. Schneider, and C. Galup-Montoro, "Analysis and design of ultra-low-voltage inductive ring oscillators for energy-harvesting applications," in *Proc. IEEE 4th Latin Am. Symp. Circuits Syst.*, Mar. 2013, pp. 1–4.

[32] P. Feng, Z. Yiqi, and L. Xiaoming, "A high efficiency charge pump circuit for low power applications," *J. Semicond.*, , vol. 31, no. 1: 015009, 2010.

Dejan Rozgić (S'12) received the Dipl.Ing. and M.S. degrees in electrical engineering from the University of Belgrade, Belgrade, Serbia, in 2009 and 2011, respectively. In 2011, he joined the University of California, Los Angeles, CA, USA, where he is currently working toward the Ph.D. degree in the Department of Electrical Engineering. His research interests include characterization and integration of post-CMOS devices, low-power circuit design, and energy harvesting/processing circuits.

Dejan Marković (S'96—M'06) received the Dipl.Ing. degree from the University of Belgrade, Belgrade, Serbia, in 1998 and the M.S. and Ph.D. degrees from the University of California, Berkeley, CA, USA, in 2000 and 2006, respectively, all in electrical engineering. In 2006, he joined the faculty of the Electrical Engineering Department at the University of California, Los Angeles, CA, where he is currently a Professor. His current research is focused on implantable neuromodulation systems, domain-specific architectures, embedded systems, energy harvesting, and design methodologies. Dr. Marković co-founded Flex Logix Technologies, a semiconductor IP startup, in 2014. He received an NSF CAREER Award in 2009. In 2011, he was a co-recipient of ISSCC Jack Raper Award for Outstanding Technology Directions. Most recently, he received 2014 ISSCC Lewis Winner Award for Outstanding Paper.