SYMBIOSIS INTERNATIONAL (DEEMED UNIVERSITY)

(Established under section 3 of the UGC Act, 1956)

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Seat No.						

Institute: (0701) SYMBIOSIS INSTITUTE OF TECHNOLOGY, PUNE
Programme: (070122, 070124) BACHELOR OF TECHNOLOGY (COMPUTER SCIENCE, INFORMATION TECHNOLOGY)
Batch: 2017-21, 2018-22, 2019-23
Semester: III
Course: Digital Electrincs and Logic Design
Course Code: 0701220305 CS, 0701240305 IT
Date: 12/6/2021 **Maximum Marks:** 45
Day: Saturday **Time:** 3:00 to 4:30 pm

Instructions:

1. **All questions are compulsory.**
2. **Draw neat diagrams wherever necessary.**
3. **Use of non-programmable calculators is allowed.**
4. **Make suitable assumptions wherever required.**

Q.1	**a)**	Perform the following:	**8**	**CO1**
		i) $(B25)_{16}$ - $(67)_{16}$ = $()_{16}$ Hexadecimal subtraction using16's complement.		
		ii) $(456)_{10}$ - $(542)_{10}$ = ($)_{10}$BCD subtraction using 10's complement.		
		iii) $(111110.1)_2 \div (0101)_2$= ($)_2$ Binary division.		
		iv) $(636)_8$-$(345)_8$ = ($)_8$ Octal subtraction using 8's complement.		
Q.2	**a)**	Solve the following equation using algebraic simplification. Realize the answer using NOR gates only: Y=A'B'C'D'+ A'B'C'D+A'B'CD+A'B'CD'	**4**	**CO2**
Q.3	**a)**	Solve the equation using k –map: Y= ∑m(0, 1, 5, 9, 10, 13, 14) + d(3, 4, 7, 11, 15)	**3**	**CO3**
	b)	Convert the following expression into standard SOP form: Y=AB+ABC'+BC'	**3**	**CO3**
Q.4	**a)**	Design 1:8 demultiplexer using 1: 4 demultiplexer circuits using truth table.	**6**	**CO4**
	b)	Design 4 bit binary to gray code convertor along with Truth table and K-map.	**5**	**CO4**

Q.5	**a)**	Explain JK flip flop with preset and clear input. Also draw the truth table. What is the major drawback of JK flip flop?	**6**	**CO5**
	b)	Draw and explain the circuit diagram of 4-bit Serial In/Parallel out (SISO) shift register.	**6**	**CO5**
	c)	Compare sequential and combinational circuits.	**4**	**CO5**

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