Institute: (0701) SYMBIOSIS INSTITUTE OF TECHNOLOGY, PUNE
Programme: (070122, 070124) BACHELOR OF TECHNOLOGY
(COMPUTER SCIENCE, INFORMATION TECHNOLOGY)
Batch: 2015-19, 2016-20
Semester: III
Course: Digital Electrincs and Logic Design
Course Code: 0701220305CS, 0701240305IT
Date: 12/6/2021   **Maximum Marks: 60**
Day : Saturday   **Time: 3:00 to 5:30 pm**

Instructions:
1. All questions are compulsory.
2. Draw neat diagrams wherever necessary.
3. Use of non-programmable calculators is allowed.
4. Make suitable assumptions wherever required.

Q.1	**a)**	Perform the following:	**5**	**CO1**
		i) $(AF8)_{16} - (75)_{16} = (\quad)_{16}$ Hexadecimal subtraction using 16's complement.		
		ii) $(589)_{10} - (432)_{10} = (\quad)_{10}$ BCD subtraction using 10's complement.		
	b)	What are the different universal gates? Explain any one universal gate with truth table.	**5**	**CO1**
Q.2		Define any three characteristics of digital ICs.	**6**	**CO2**
Q.3	**a)**	Design full adder using half adder along with truth table and K-map.	**5**	**CO3**
	b)	Simplify the Boolean function using K-map:	**5**	**CO3**
		$Y = \pi M(1, 2, 3, 5, 6, 7, 8, 10, 12, 13, 14, 15)$		
	c)	Simplify the given expression using Boolean laws:	**4**	**CO3**
		$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$$		
Q.4	**a)**	Explain Jk flip flop with preset and clear input. Also draw the truth table. What are the drawbacks of SR flip flop?	**7**	**CO4**

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b) Describe 4-bit parallel in/serial out shift register (SISO). Show the waveform for serial output with the data input bits 1011 and clock shift/load.   **7**   **CO4**

c) Compare sequential and combinational circuits.   **6**   **CO4**

Q.5 Draw and explain ASM chart for mod 4 up counter with the condition that there exist an input signal W and if W=1, the count is incremented by 1 otherwise it remains same.   **5**   **CO5**

Q.6 Explain different components of PLA with diagram.   **5**   **CO6**

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