AMD
XILINX

FPGA Design Flow using Vivado 2021.2

Course Objectives

- After completing this course, you will be able to:
  - Describe general FPGA architectures
  - Understand the Vivado design flow
  - Create and debug HDL designs
  - Synthesize and implement HDL designs
  - Utilize the available synthesis and implementation reports to analyze a design (utilization, timing, power, etc.)
  - Configure FPGAs and verify hardware operation
  - Create and apply I/O and timing constraints
  - Use the Project Manager to navigate through the design flow
  - Identify file sets (HDL, XDC, simulation)
  - Analyze designs by using the cross-selection capabilities, Schematic viewer, and Hierarchical viewer

Course Outline
Day 1

The course consists of the following modules:

- 7-Series Architecture Overview
- Vivado Design Flow
- Lab 1: Vivado Design Flow
- Synthesis Technique
- Lab 2: Synthesizing a RTL Design
- Implementation and Static Timing Analysis
- Lab 3: Implementing the Design

Course Outline
Day 2

- IP Integrator
- Lab 4: Using the IP Catalog and IP Integrator
- Xilinx Design Constraints
- Lab 5: Xilinx Design Constraints
- Hardware Debugging
- Lab 6: Hardware Debugging

Prerequisites

- Basic HDL knowledge (VHDL or Verilog)
- Digital design knowledge and experience

Platform Support

- Vivado Design Suite: System Edition 2021.2
- Xilinx University boards
  - Boolean, PYNQ-Z2
- Supported Operating Systems
  - Microsoft Windows Professional/Enterprise 10.0 1903 Update; 10.0 1909 Update; 10.0 2004 Update: 10.0 20H2 Update; 10.0 21H1 Update
  - Red Hat Enterprise Workstation/Server 7.4, 7.5, 7.6, 7.7, 7.8, 7.9, 8.1, 8.2, 8.3, and 8.4 (64-bit), English/Japanese
  - SUSE Linux Enterprise 11.4 and 12.3 (64 Bit)
  - Amazon Linux 2 AL2 LTS (64-bit)
  - Ubuntu Linux 16.04.5 LTS; 16.04.6 LTS; 18.04.1 LTS; 18.04.2 LTS, 18.04.3 LTS; 18.04.4 LTS; 18.04.5 LTS; and 20.04 LTS, 20.04.1 LTS, 20.04.2 LTS (64-bit), English/Japanese

Note on target board/device

The labs are written for PYNQ-Z2 and Boolean

- PYNQ-Z2 targets the XC7Z020clg400-1 and Boolean targets the XC7S50CSGA324-1

Thank You

Disclaimer and Attribution

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