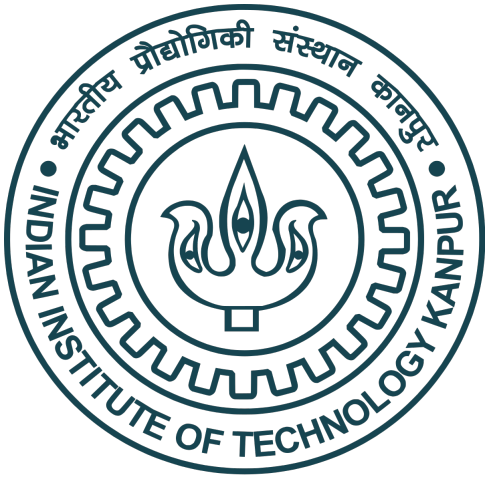
CS422: COMPUTER ARCHITECTURE




# Assignment 4

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# 1 Details

- Predicated calls have been used for finding the contents of the caches because an instruction does not proceed into the memory phase until it is verified to be present on the correct path.
- At least 2 hits = No. of cache blocks which experienced atleast two hits after being inserted into the L2 cache / No. of cache blocks which experienced atleast one hits after being inserted into the L2 cache
- The accesses of L1 and L2 caches equals the number of cache blocks for which L1 and L2 caches were queried.
- If multiple cache blocks were queried in an instruction, the a new query started only when a query prior to it has completed and changed the cache accordingly.

# 2 PART A:

This the part in which both L1 and L2 caches followed the LRU replacement policy:

| Benchmark | L1 accesses | L2 accesses | L1 misses | L2 misses | Dead-on-fill (%) | Atleast 2 hits (%) |
|---|---|---|---|---|---|---|
| **perlbench** | 561870744 | 787790 | 787790 | 16609 | 6.647 | 0 |
| **bzip2** | 683880208 | 8427660 | 8427660 | 4460227 | 67.7879 | 51.5819 |
| **gcc** | 482747215 | 10033754 | 10033754 | 2061671 | 91.2297 | 38.066 |
| **mcf** | 525252590 | 68263713 | 68263713 | 33531132 | 61.0142 | 18.0528 |
| **soplex** | 500168617 | 19194900 | 19194900 | 18511091 | 98.012 | 22.1247 |
| **hmmer** | 623357683 | 3275344 | 3275344 | 1619535 | 95.3465 | 29.167 |
| **omnetpp** | 562158859 | 13648256 | 13648256 | 10194607 | 81.1605 | 36.3331 |
| **xalancbmk** | 496786032 | 12211109 | 12211109 | 2236553 | 61.8799 | 51.8737 |

# 3 PART B:

This is the part in which the L1 cache followed the LRU replacement policy and the the L2 cache followed the SRRIP replacement policy.

| Benchmark | L1 misses | L2 misses |
|---|---|---|
| **perlbench** | 787790 | 16609 |
| **bzip2** | 8429497 | 4511072 |
| **gcc** | 10033448 | 2047868 |
| **mcf** | 68265559 | 34433797 |
| **soplex** | 19191167 | 18460824 |
| **hmmer** | 3269039 | 1559042 |
| **omnetpp** | 13645390 | 10177162 |
| **xalancbmk** | 12208560 | 2165992 |

# 4 PART C:

This is the part in which the L1 cache followed the LRU replacement policy and the the L2 cache followed the NRU replacement policy.

| Benchmark | L1 misses | L2 misses |
|---|---|---|
| **perlbench** | 787803 | 16639 |
| **bzip2** | 8428036 | 4480695 |
| **gcc** | 10033998 | 2068242 |
| **mcf** | 68265120 | 33754516 |
| **soplex** | 19195369 | 18515492 |
| **hmmer** | 3275633 | 1603309 |
| **omnetpp** | 13649593 | 10209162 |
| **xalancbmk** | 12212040 | 2242698 |

# 5 Analysis:

The difference in the number of L1 cache misses for different L2 cache replacement policies occurred because in an inclusive cache setup when an entry is evicted from the L2 cache, it is invalidated from the L1 cache as well if it is present in the L1 cache. Thus the different order of eviction of objects from the L2 cache gives rise to difference in the L1 cache misses.