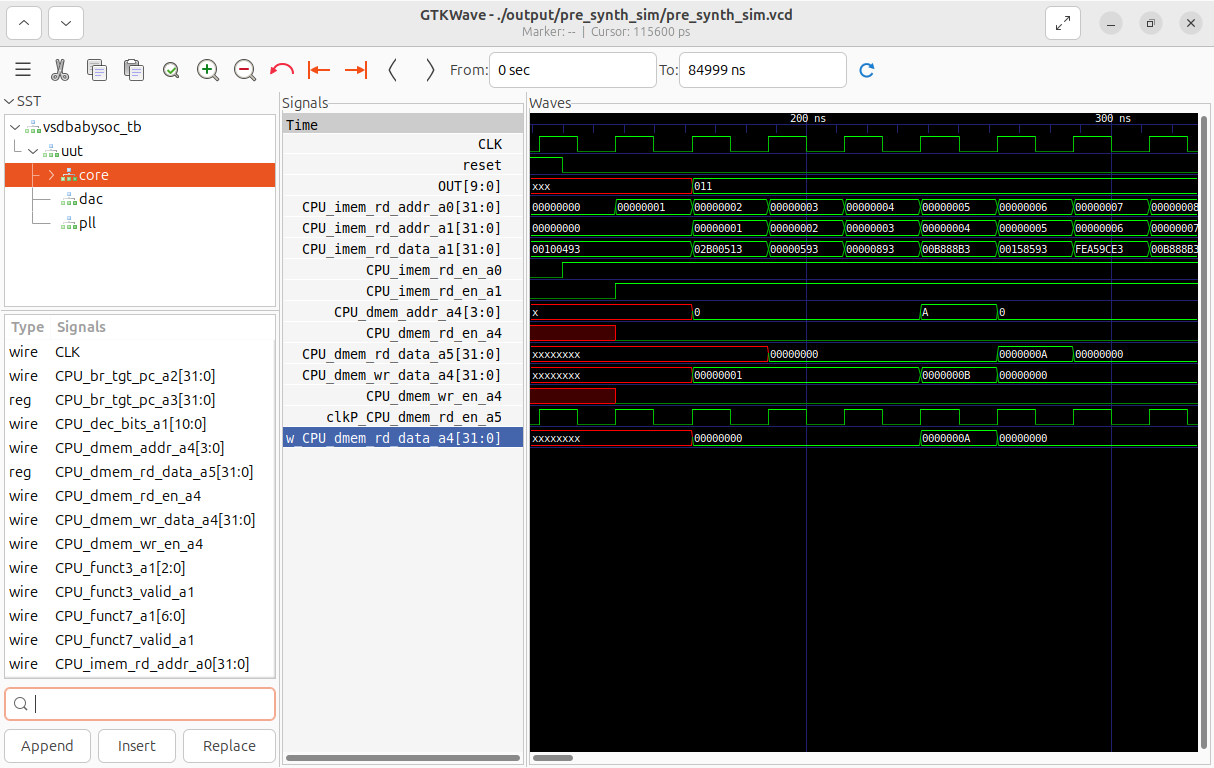
1. VSDBabySoC
   1. We have a RTl top vsdbabysoc!
   2. Comprise of three digital components
      1. CPU “RISC-V core”
         1. Inputs
            1. CLK
            2. RESET
         2. Output
            1. 10 bit to DAC input.
         3. This core is preloaded with instructions and data memory[REG VAl].
         4. As soon as reset is lifted and the clock is fed to this core via PLL.
            1. Core starts executing the instructions one by one and we see output values on the core’s output port.
            2. We see rd\_en == 1, post reset.

Instruction fetch begins.

imem address increment by 1 at each +ve clk edge!

Next we see data mem being read by the core’s logic to perform the fetch instruction.

And Output values are generated at fixed intervals.



* + 1. PLL
       1. Responsible for clock generation for the SoC.
       2. Inputs
          1. VCO\_IN

Input voltage

Not used.

* + - * 1. ENB\_CP

Enable for cp

Not used

* + - * 1. ENB\_VCO

Enable for clk

After reset when ENB\_VCO is made 1. CLK start

* + - * 1. REF

Ref clock

* + - 1. Output
         1. CLK

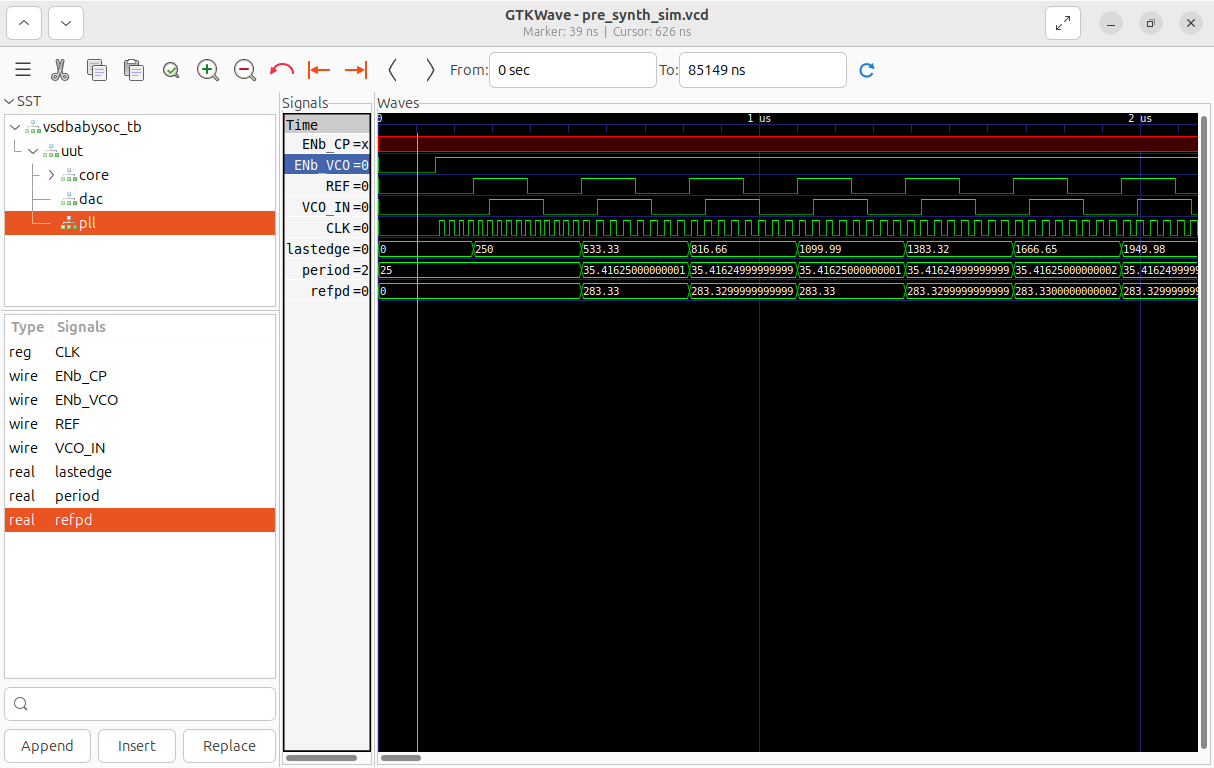
Output of PLL

Generated after use of REF and internal real variables

period, lastedge, refpd - when ENB\_VCO is 1’b1.

Input of core.

* + - * 1. We can observe no CLK generated until ENB\_VCO is 0.



* + 1. DAC 10Bit
       1. Digital to analog converter
       2. Inputs
          1. 10 bit D from core
          2. VREFL
          3. VREFH
       3. Output
          1. OUT 10 bits.
       4. Input is def by the core and it generated analog output.

