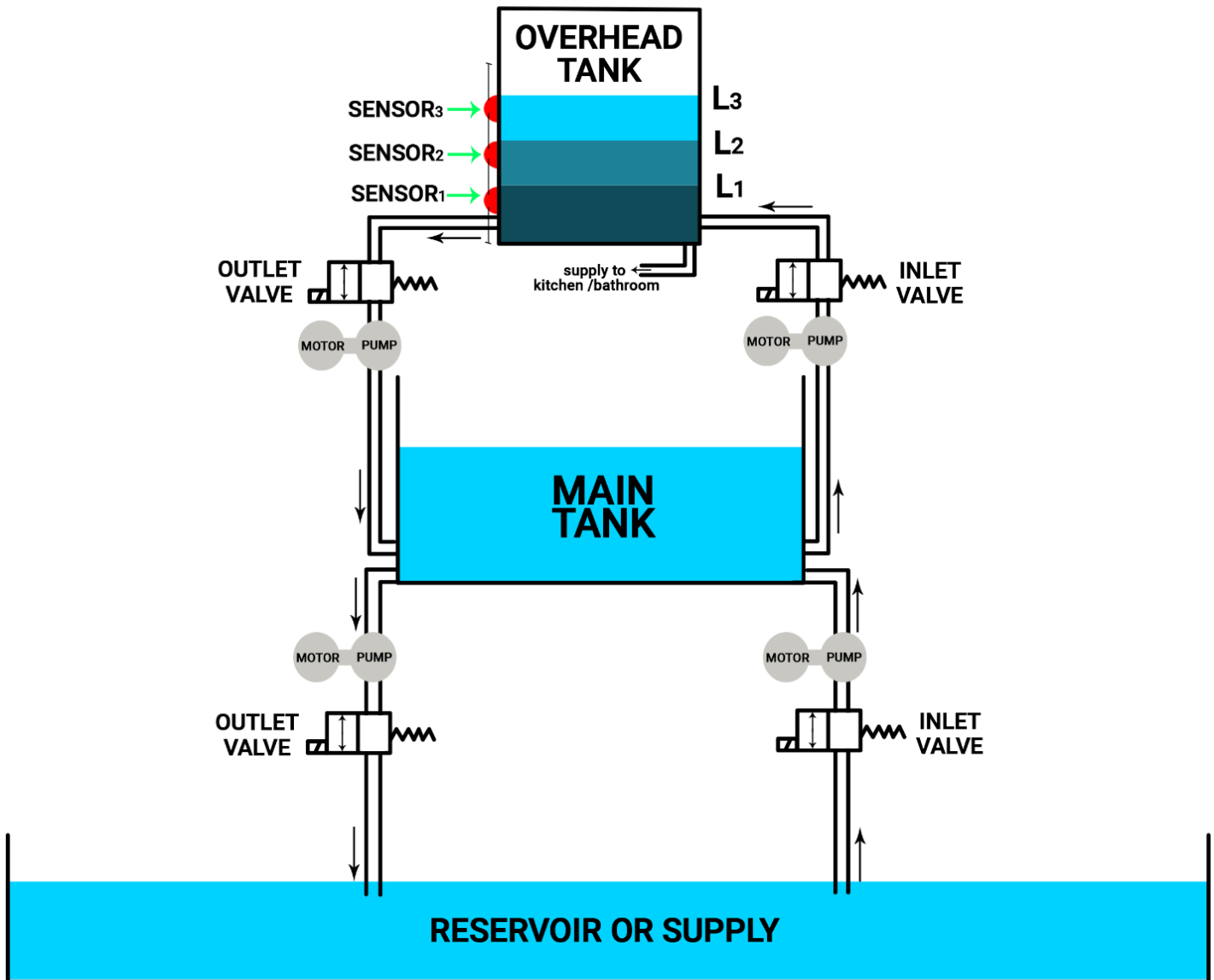


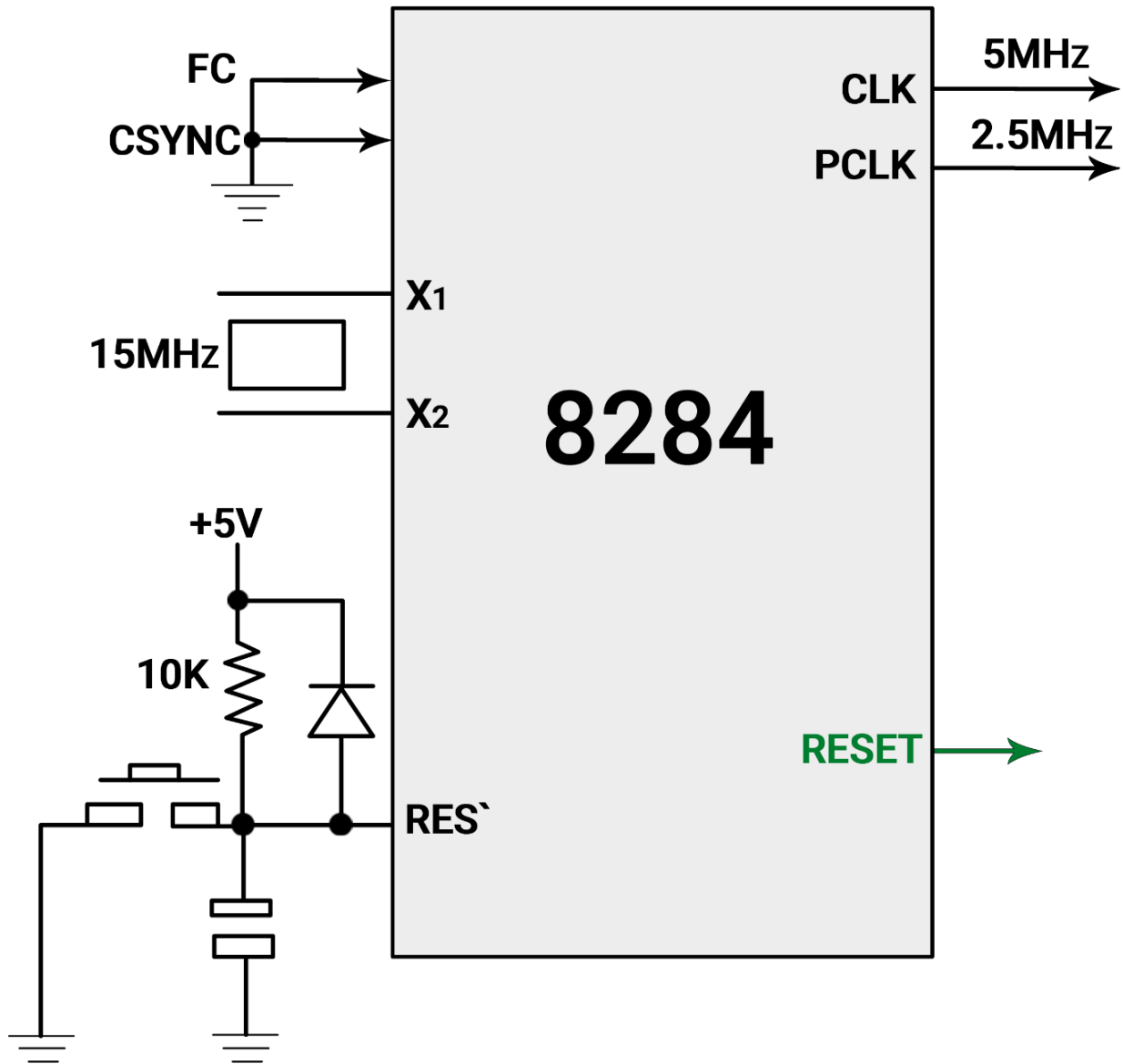
CONTENTS

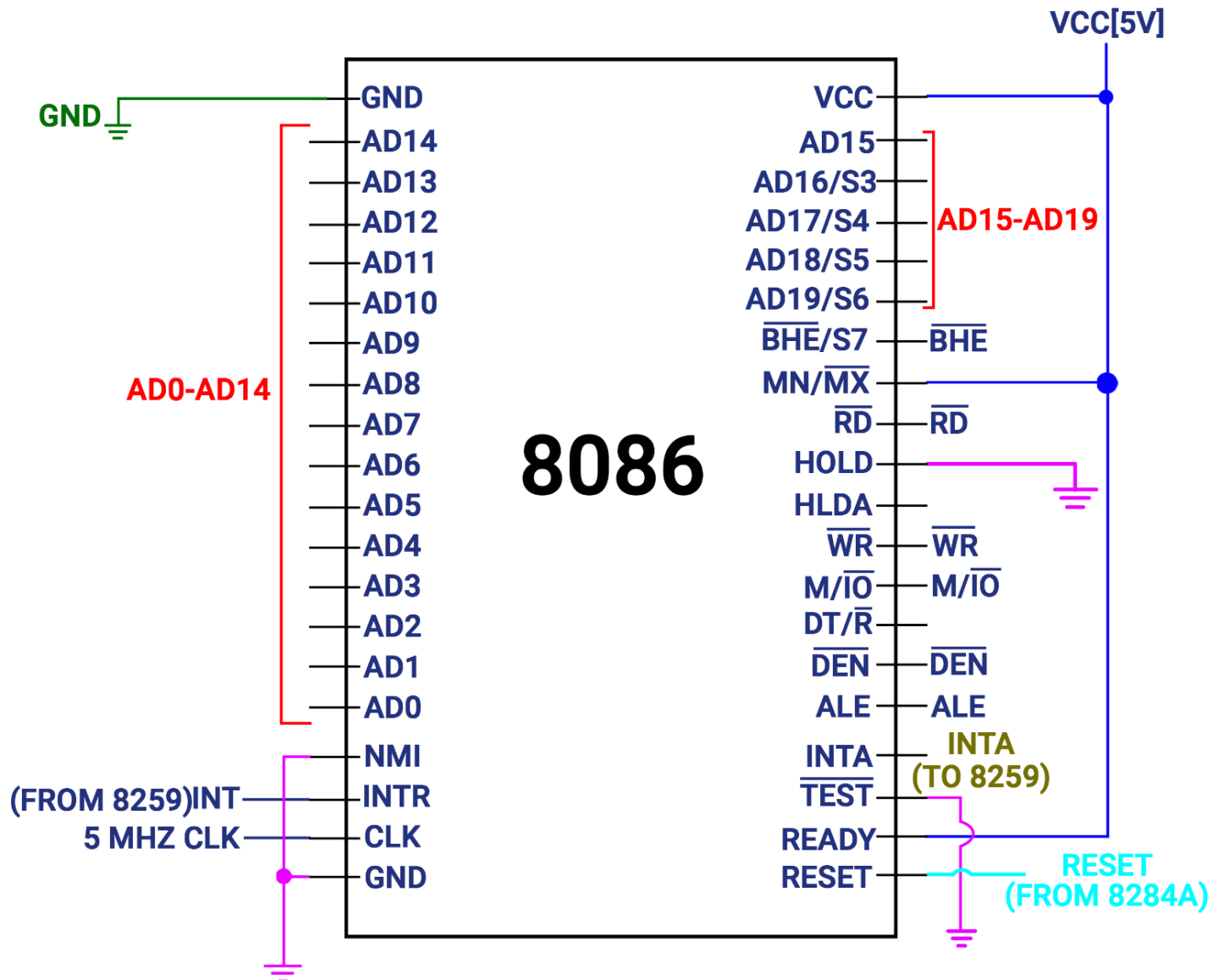
Diagrams of :

- 1.system design
- 2..8284
- 3. 8086
- 4. Address bus
- 5. Data bus
- 6. Control bus
- 7. Memory map
- 8. Memory decoding
- 9. Memory interfacing
- 10. One hour clock
- 11. I/O decoding
- 12. 8255A
- 13. Sensors
- 14. Relay
- 15. Display
- 16. 8259

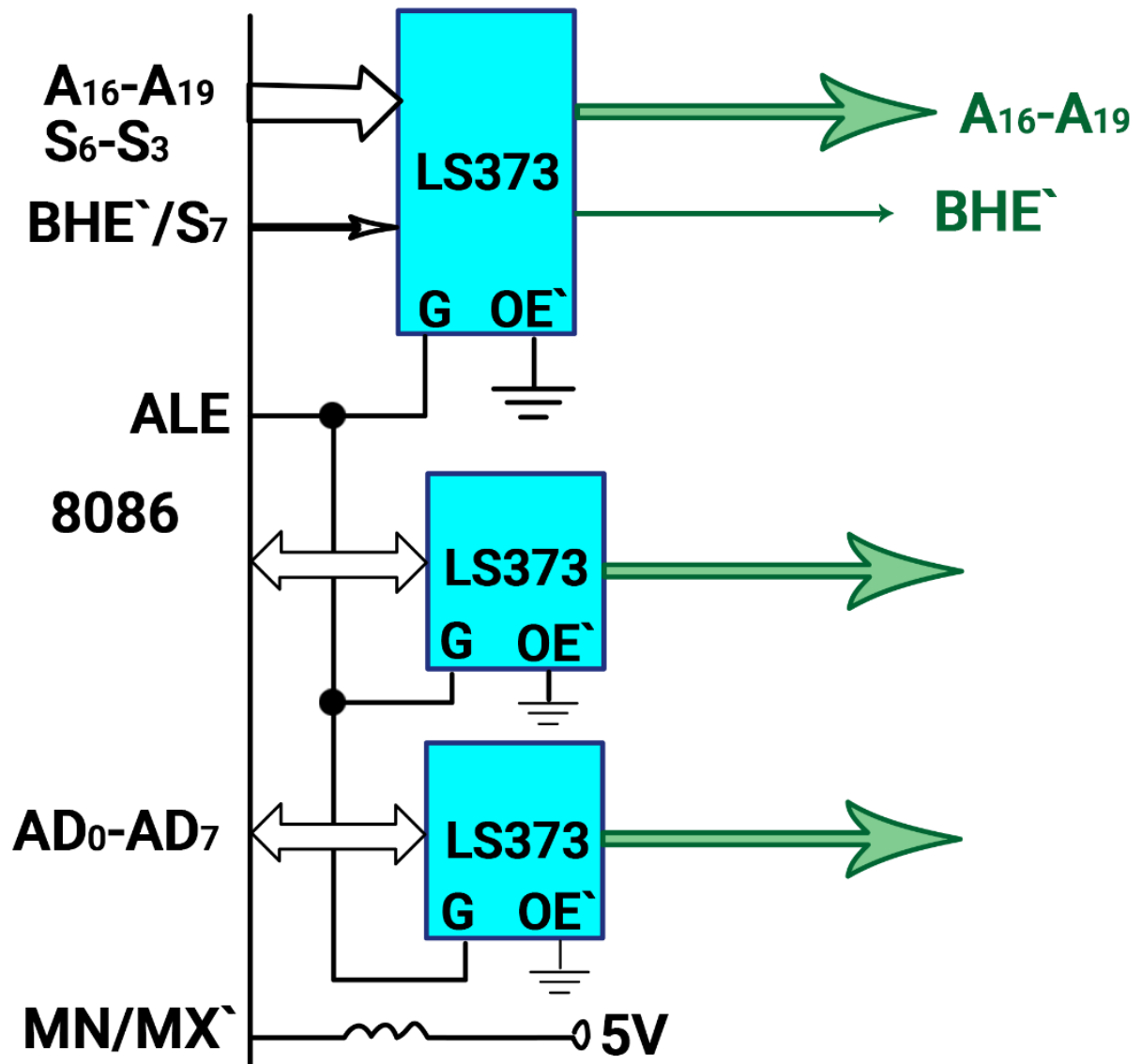
SYSTEM DESIGN



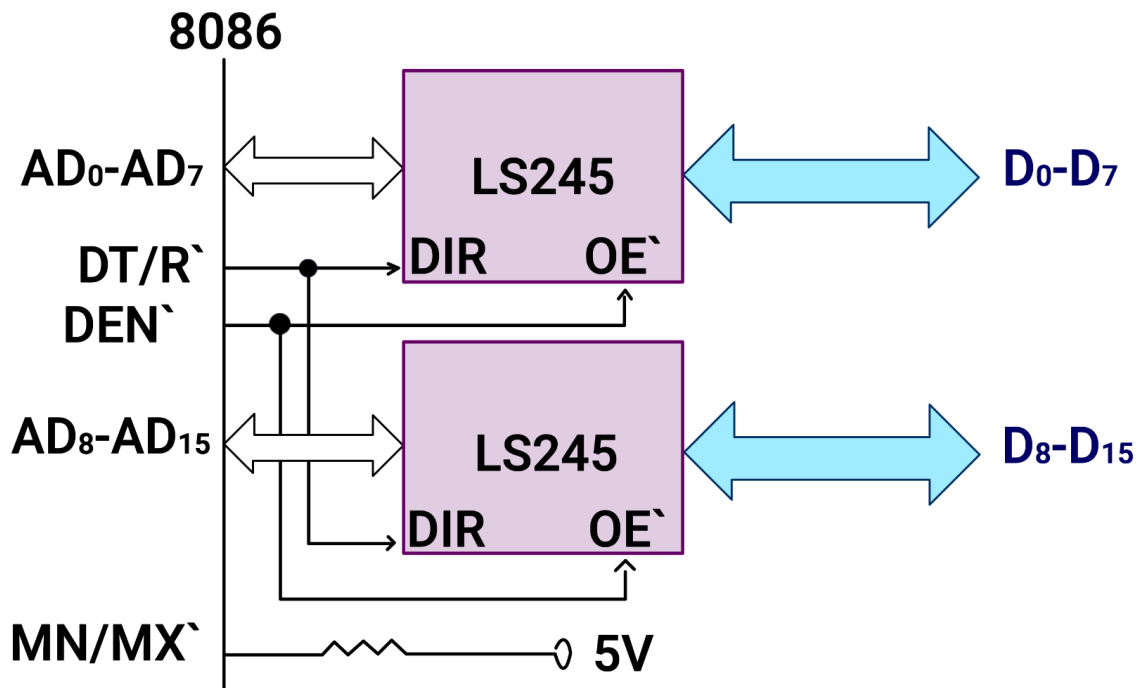




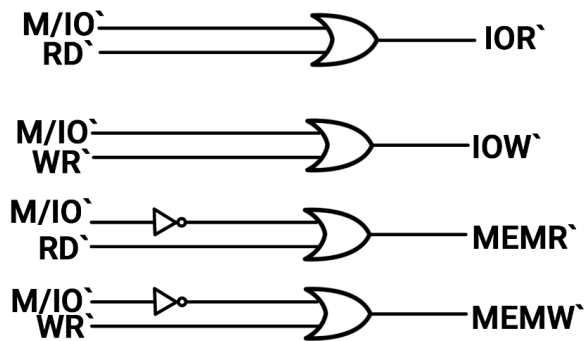
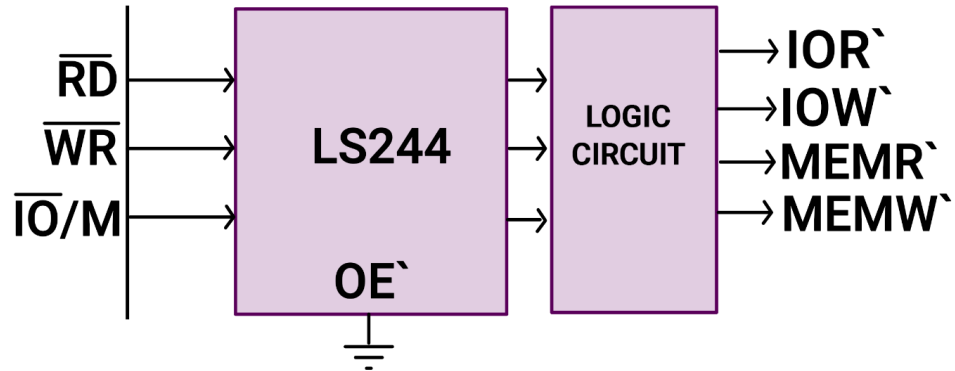
ADDRESS BUS OF 8086



DATA BUS OF 8086



CONTROL BUS OF 8086



Memory Map

ROM1 - E : 00000 - 00FFE

ROM1 - 0 : 00001 - 00FFF

RAM1 - E : 01000 - 01FFE

RAM1 - 0 : 01001 - 01FFF

ROM2 - E : FF000 - FFFFE

ROM2 - 0 : FF001- FFFFF

ROM1

[illegible]

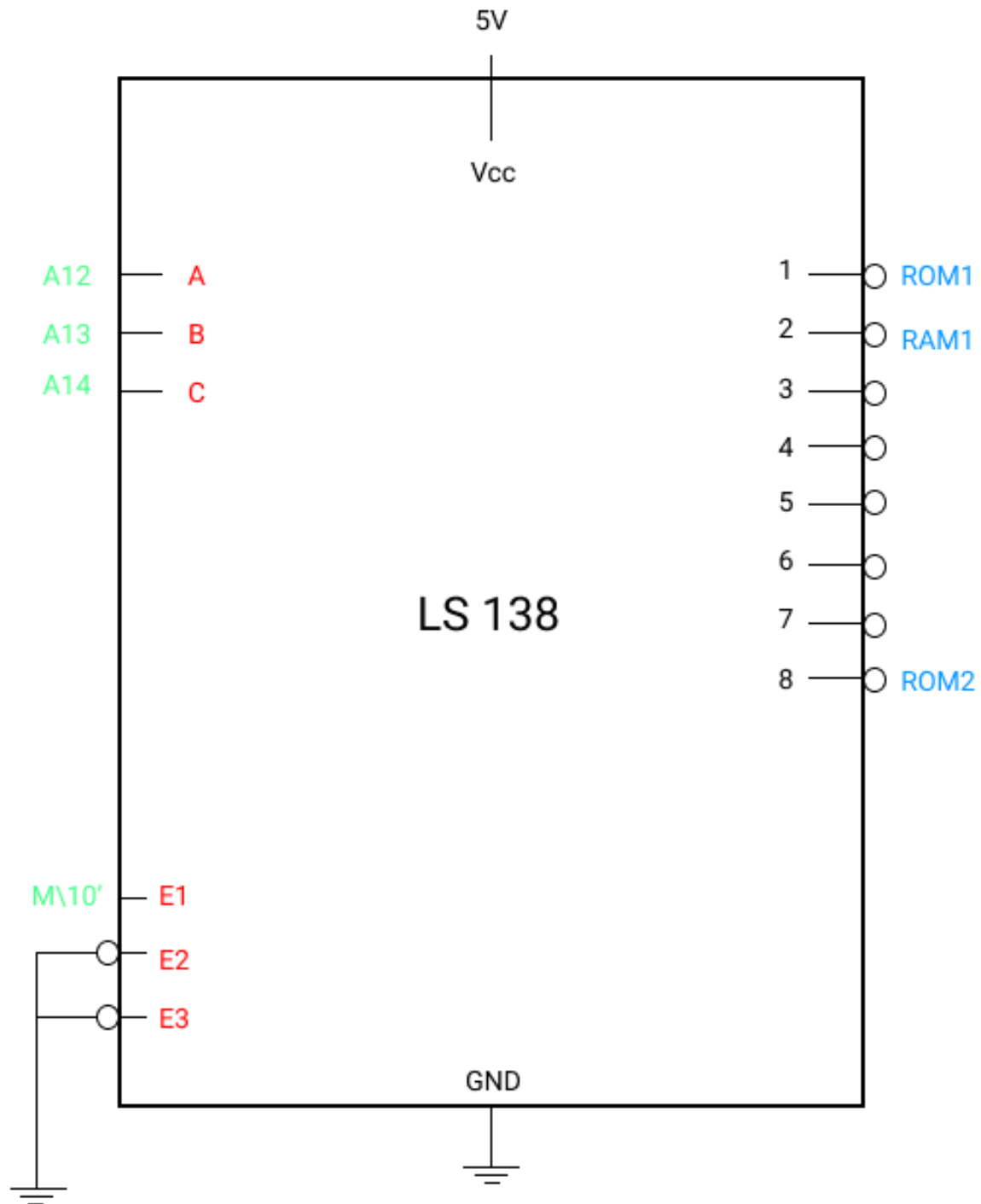
RAM1

[illegible]

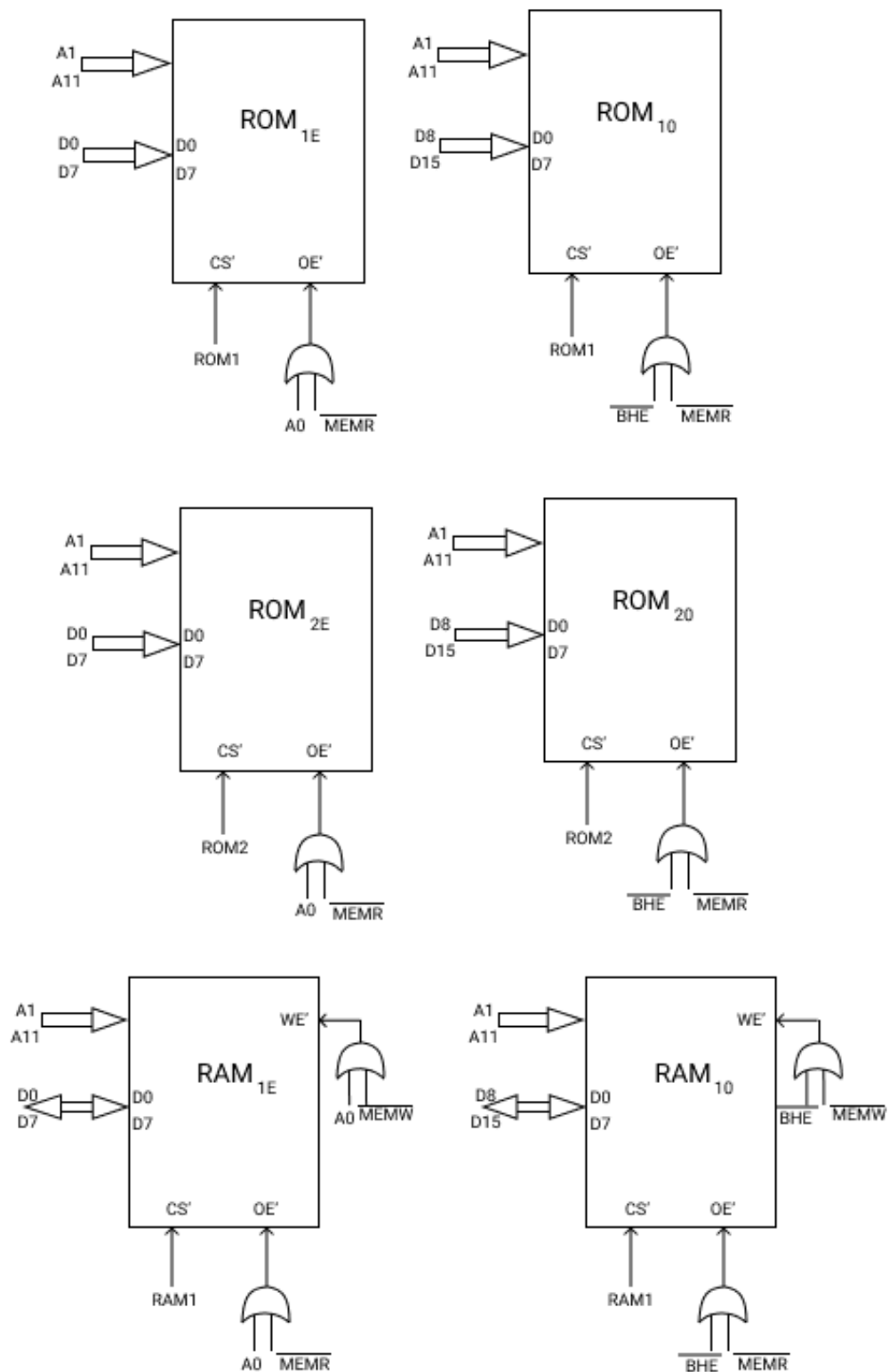
ROM2

[illegible]

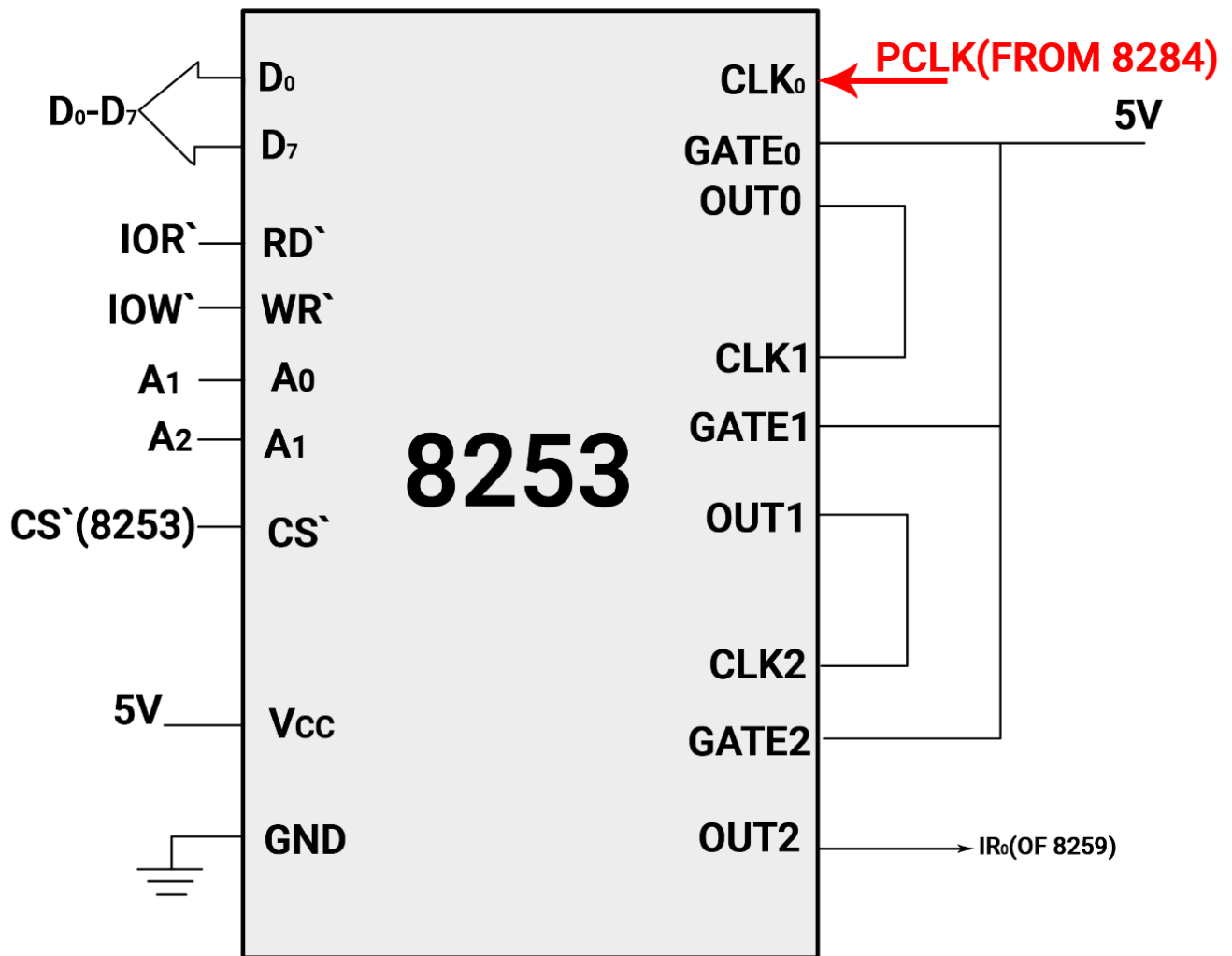
Memory Decoding Circuit



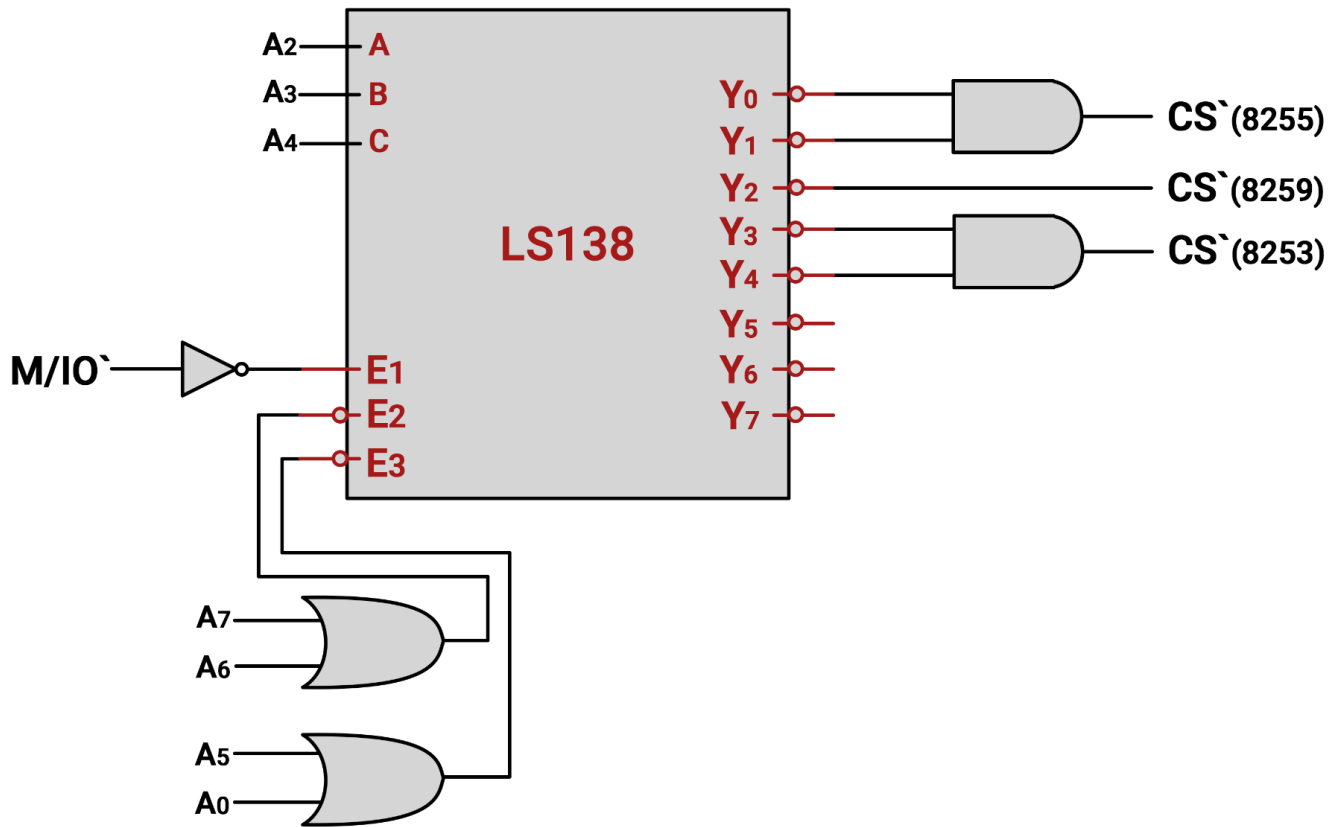
Memory Interfacing Circuit

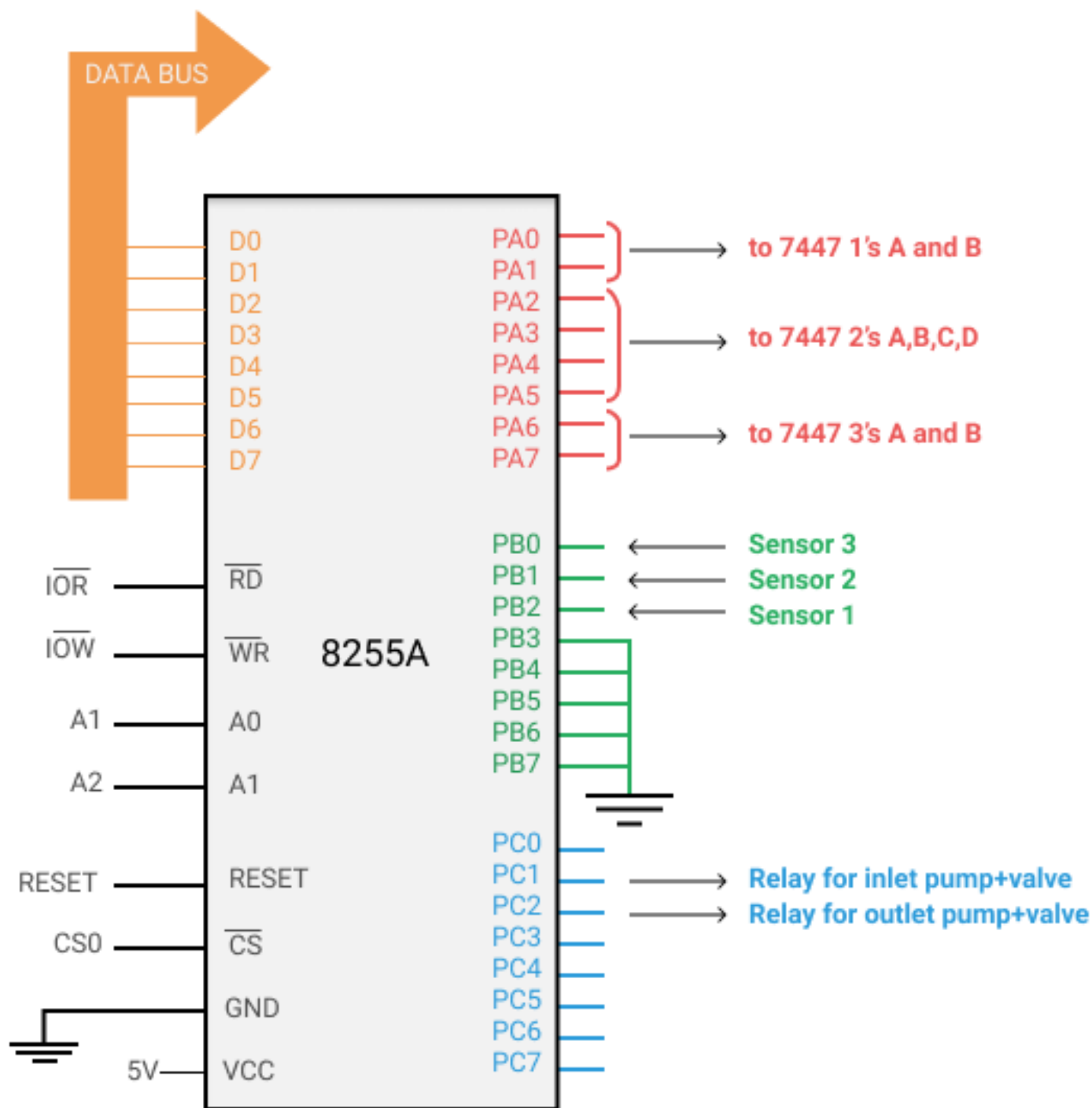


ONE-HOUR CLOCK

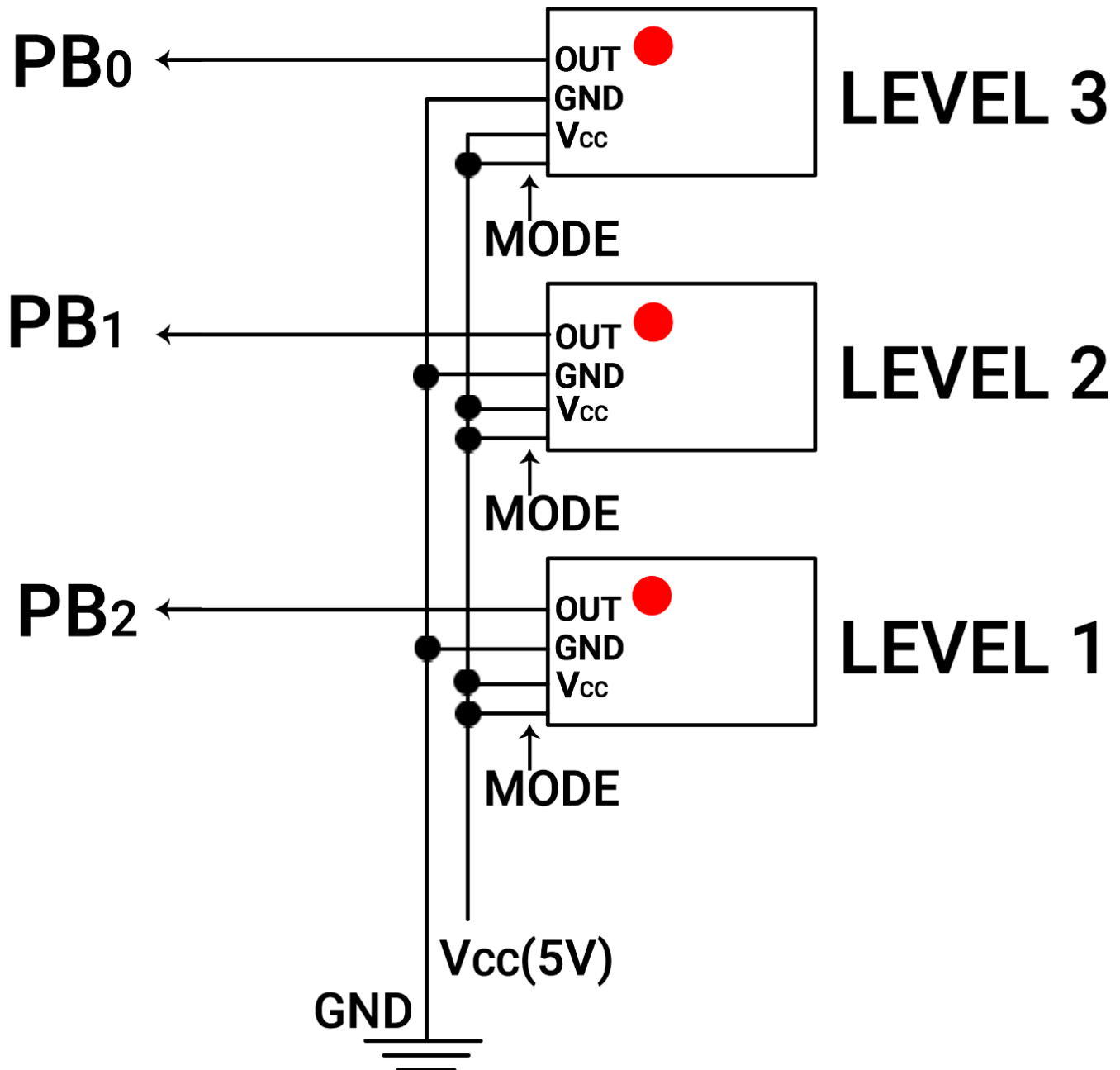


I/O DEVICES DECODING CIRCUIT

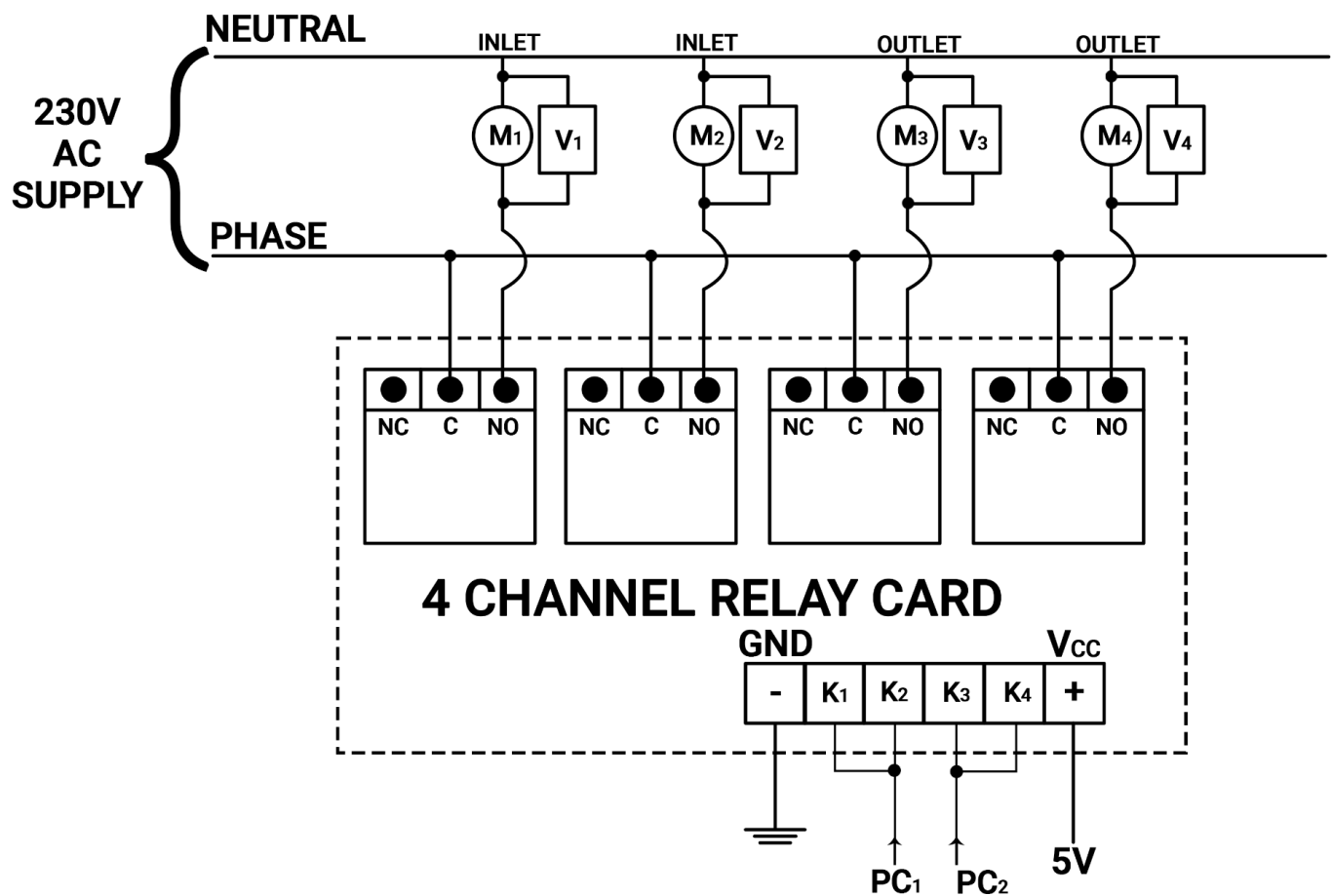




XKC Y25 T12V WATER LEVEL SENSORS



8255A Relay



8255A Display

