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Tunnel field-effect transistors with germanium/strained-silicon hetero-junctions for low power applications

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ABSTRACT

We have studied a simple structure n-channel tunnel field-effect transistor with a pure-Ge/strained-Si hetero-junction. The device operation was demonstrated for the devices fabricated by combining epitaxially-grown Ge on strained-silicon-on-insulator substrates. Atomic-layer-deposition-Al_2O_3-based gate stacks were formed with electron cyclotron resonance plasma post oxidation to ensure the high quality metal–oxide–semiconductor interface between the high-k insulator and Ge. While the gate leakage current and drain current saturation are well controlled, relatively higher minimum subthreshold swing of 125 mV/dec and lower I_{ON}/I_{OFF} ratio of 10^3–10^4 were obtained. It is expected that these device characteristics can be improved by further process optimization.

1. Introduction

Conventional metal–oxide–semiconductor field-effect transistors (MOSFETs) have encountered power dissipation challenges due to device size miniaturization [1,2]. Lower threshold voltage (V_{th}) is required to reduce the supply voltage (V_{DD}) without the increase in leakage current. However, since the sub-threshold swing (SS) in MOSFETs is limited to 60 mV/dec at room temperature by the switching mechanism of thermionic emission [3], the off leakage current exponentially increases with decreasing V_{th}. In order to overcome this limitation, tunnel field-effect transistors (TFETs) using band-to-band tunneling current have been proposed [4]. With proper S/D doping and gate alignment, TFETs can achieve steep SS below 60 mV/dec which can potentially offer low off current and V_{DD} [5]. However, TFETs with homo-junction, reported to date, still have not shown satisfactory results and have difficulties in simultaneously obtaining high I_{ON}/I_{OFF} ratio and steep SS, because of the limitation in physical properties of single material such as the bandgap [6,7]. Thus, SiGe-source/Si-channel hetero-junctions have attracted much attention because the smaller bandgap of the SiGe-source and the band-offset of the hetero-junction can increase the tunneling possibility and the larger bandgap of the Si channel and drain can suppress the leakage current [8]. Furthermore, introducing the pure-Ge source and the strain effect in the source and the channel are expected to boost the TFET performance [9].

In this work, a simple structure n-channel TFET with a pure-Ge/strained-Si (sSi) hetero-junction is proposed and fabricated. The device characteristics are also demonstrated.

2. Experimental

Fig. 1 shows the process flow and the schematic cross-section of the fabricated device structure. Biaxially tensile strained-silicon-on-insulator (sSOI) (100) substrates with a sSi thickness of 15 nm and 0.8% strain, obtained by a layer transfer and a Smart Cut technique [10], were used for the starting material. The drain regions were formed by phosphorus ion implantation with 10 keV and ion dose of 4×10^{14} cm^{-2}, followed by activation annealing at 900 °C for 30 s.

An in-situ thermal treatment prior to Ge epitaxy is essential for obtaining high epitaxial film quality [11]. In this study, a HF-terminated sSOI substrate was annealed at 850 °C for 20 min in an ultra-high vacuum chamber. A 31-nm-thick Ge was grown on the thermal-treated sSOI substrate by molecular beam epitaxy at 200 °C and a chemical solution of diluted hydrogen peroxide was used to etch and pattern the Ge layer.

Two-step 10-nm-Al_2O_3 atomic layer deposition was formed with electron cyclotron resonance plasma post oxidation to ensure the high quality MOS interface between the high-k insulator and Ge [12]. 20-nm-thick Ta was deposited as the gate metal, followed by Ni and Al deposition for the source contact and the contact pad, respectively. Here, the Ni was selected as a contact metal with the Ge because it has good thermal stability with the Ge even after an additional annealing process [13] and it induces a Fermi-level pinning with a Ge at a level close to the valence band edge of a Ge that is suitable for nTFET operation [14].

3. Results and discussion

The proposed device structure is shown in Fig. 2(a) and the band diagrams near the Ge-source/sSi-channel in the off-state and the on-state are schematically illustrated in Fig. 2(b) and (c), respectively. The proposed structure features are as follows: the combination of

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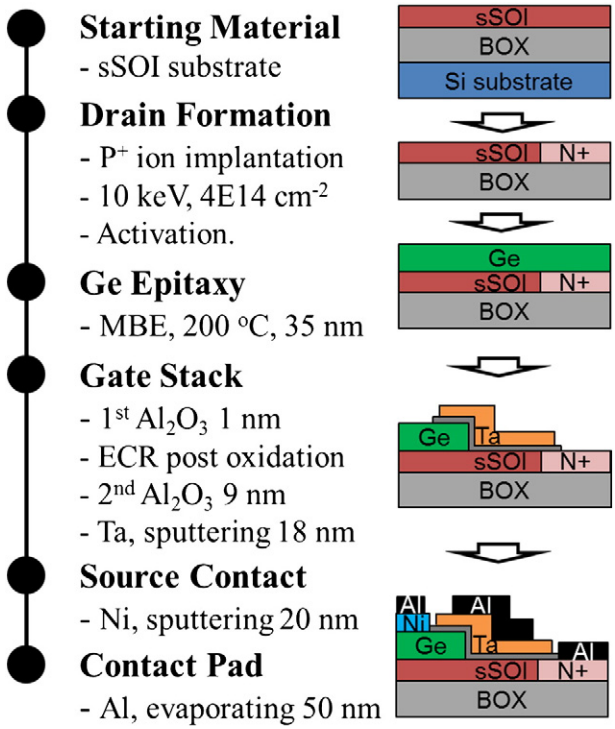

Fig. 1. Process flow and cross-sections of device structure.

100% pure-Ge with the small bandgap energy (E_g) as the source and sSi with biaxial tensile strain as the channel leads to type-II staggered hetero-structure, as shown in Fig. 2(b). In the off-state condition (i.e. the gate voltage is zero or negative), the effective tunneling width between valence band edge of source and conduction band edge of channel decreases enough as a consequence to the band-to-band tunneling that is suppressed. On the other hand, in the on-state condition, the effective tunneling width increases by positively biased gate voltages and therefore, carriers existing below valence band edge of Ge-source can tunnel to state above conduction band of silicon-channel. The proposed structure allows us to reduce the tunneling width and to increase the tunneling probability [8] without significant decrease in the bandgap causing the increase in the leakage current. As a result, enhancing the tunneling current with maintaining small leakage current can be obtained by the proposed device structure. Recently, a similar structure to the one in Fig. 1(a) has been reported and the TFET performance has been demonstrated [15]. This structure employed a 0.8%-tensily-strained SOI channel, a $Si_{0.5}Ge_{0.5}$ source and epitaxially-grown Si as a capping layer between the SiGe/high-k interface, which could lead to an increase in the tunneling width and equivalent oxide thickness (EOT). Our device structure with the pure-Ge source and ultrathin Ge oxide interfacial layers formed by the post plasma process [12] in the Ge gate stacks is expected to improve the TFET properties, because of the smaller tunneling width, the superior MOS interface and the thinner EOT.

Fig. 3(a) indicates the reflection high electron energy diffraction (RHEED) patterns taken along the <110> direction from the thermal-treated sSOI substrate, which allows a direct measurement of the surface structure. The (2×1) reconstruction caused by desorption of bonded oxygen atoms from the silicon surface [16] was obtained. The streaks of RHEED pattern in Fig. 3(b) confirm the layer by layer growth of Ge [17]. Arrows indicate initial (1×1) silicon positions and the distance between streaks of Ge became slightly smaller than that of Si suggesting larger lattice constant [18].

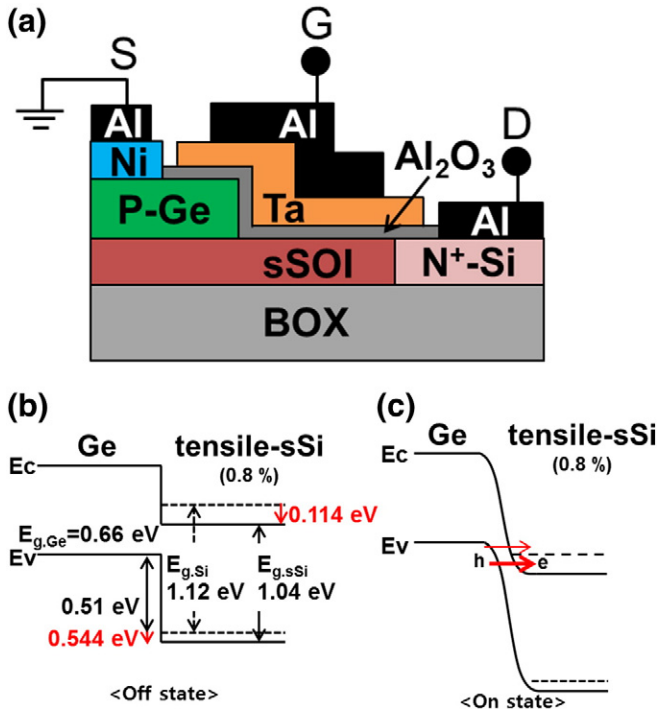

Fig. 2. (a) Proposed device structure and band diagrams of Ge-source/sSi-channel hetero-junction in (b) off-state ($V_G \leq 0$) and (c) on-state ($V_G > 0$). Dashed lines indicate the band diagrams of unstrained Si.

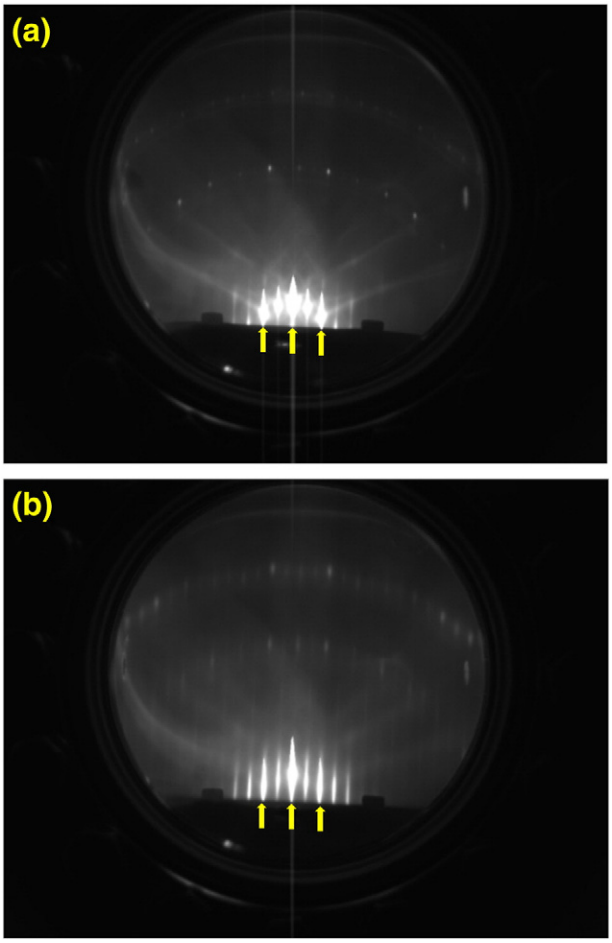

Fig. 3. Reflection high electron energy diffraction images recorded along <110> direction (a) of a sSOI surface after thermal treatment for 20 min, and (b) of a Ge surface after 31 nm growth at 200 °C. Arrows indicate initial (1×1) silicon positions.

The material properties of the pure-Ge grown on sSOI substrate were characterized by Raman spectroscopy using an argon laser with 488 nm wavelength and the detectable depth in Si and Ge are 569 and 19 nm, respectively [19]. Fig. 4(a) shows the Raman spectrum of the sSOI substrate. Here, the relationship between Raman shift ($\Delta\omega$) and the biaxial strain (ε_{xx}) on silicon is given by [20]

$$\Delta\omega = -733\varepsilon_{xx}. \quad (1)$$

The biaxial tensile strain of 0.8% was confirmed. Fig. 4(b) shows the Raman spectrum of the pure-Ge layers, where the peak located at 300 cm^{-1} is identical to that of the bulk Ge [21]. This result indicates that the grown pure-Ge layers were fully relaxed due to the large lattice mismatch between Ge and Si [22].

Fig. 5 shows a transmission electron microscopy image near the source region of the fabricated device. It is confirmed that uniform interface between Ge and the insulator was formed, although many defects that resulted from the lattice mismatch (Fig. 4(b)) are seen in the Ge layer. The Ge and sSOI thickness are found to be 31 nm and 11 nm, respectively. The sSOI thickness was thinned from the initial thickness of 15 nm, because of wet chemical treatment for cleaning. The thickness slope in the right hand region of the Ge layer is also attributed to the chemical process, used to etch the patterned Ge layers, because of the isotropic etching property. This is not critical to the present devices because the device size is several tens of micrometers. However, a highly-controlled etching process may be required for devices with sub-micron size.

Fig. 6 shows the drain current–gate voltage (I_d–V_g) and the gate current–gate voltage (I_g–V_g) characteristics of a fabricated device.

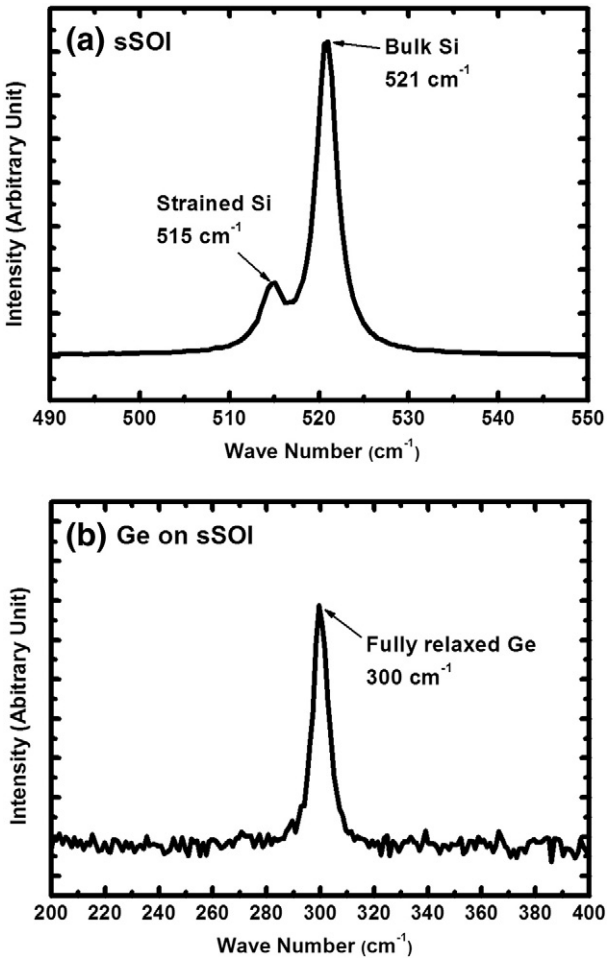

Fig. 4. Raman spectrum of the (a) sSOI substrate and (b) grown pure-Ge layers.

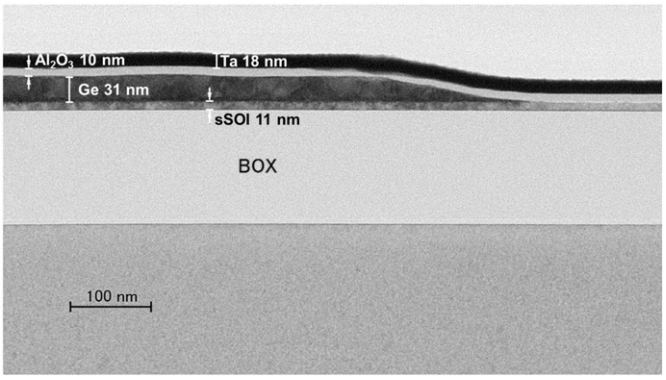

Fig. 5. Transmission electron microscopy image near the source region of the fabricated device.

While the gate leakage current and drain current saturation seem to be well controlled, relatively higher minimum subthreshold swing (SS_{min}) of 125 mV/dec and lower I_{ON}/I_{OFF} ratio of 10^3–10^4 were obtained. The series resistance of the source/drain regions could cause the device performance degradation, as the strong saturation of I_{ON} is seen in Fig. 6(a). The estimated series resistance (R_{SD}) by circular transmission line method [23] of source/drain is 967.7 kΩ (R_S = 80.6 kΩ, R_D = 887.05 kΩ) and it might be caused by undoped Ge of source and unoptimized implanted sSOI of drain. Such high R_{SD} can degrade the

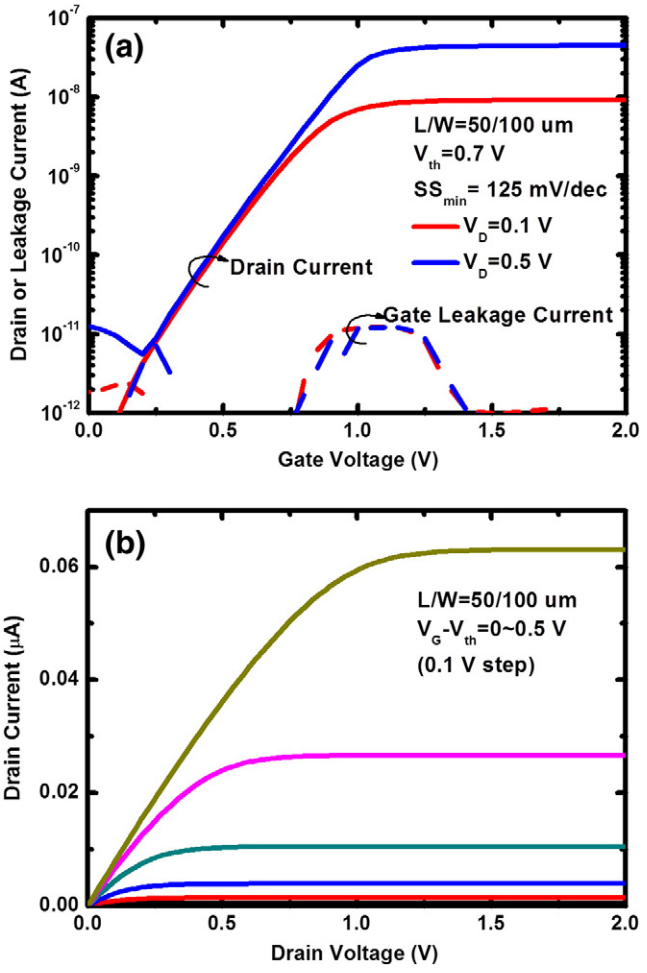

Fig. 6. I–V characteristics of the fabricated device. (a) I_d–V_g and I_g–V_g characteristics. (Solid and dashed lines stand for drain currents and gate leakage currents, respectively). (b) Output characteristics.

level of saturation current. The band-to-band tunneling of TFET is sensitive to EOT and the thinnest EOT is required for small SS below MOSFET's limit [24]. However, in this study, thick Al_2O_3 of 10 nm was used to confirm the operation in proposed device structure and it may cause high SS value. The output characteristics in Fig. 6(b) show good saturation, though the current level is low. Therefore, further process optimization can lead to improvement in the device characteristics.

4. Conclusion

N-channel TFETs using the hetero-junction composed of pure-Ge and tensile sSi have been proposed and demonstrated. The device operation was demonstrated for the devices fabricated by combining epitaxially-grown Ge on strained-SOI substrates with Al_2O_3-based Ge gate stacks.

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References

[1] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, N. Sugiyama, IEEE Trans. Electron. Devices 55 (2008) 21.
[2] E. Pop, Nano Res. 3 (2010) 147.
[3] S. Salahuddin, S. Datta, Tech. Dig. IEEE Int. Electron. Devices Meet. (2008) 693.
[4] O.M. Stuetzer, Proc. Inst. Radio Eng. 40 (1952) 1377.
[5] A.C. Seabaugh, Q. Zhang, Proc. IEEE 98 (2010) 2095.
[6] F. Mayer, L. Royer, J.-F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, S. Deleonibus, Tech. Dig. IEEE Int. Electron. Devices Meet. (2008) 163.
[7] A.M. Ionescu, H. Riel, Nature 479 (2011) 329.
[8] O.M. Nayfeh, C.N. Chleirigh, J. Hennessy, L. Gomez, J.L. Hoyt, D.A. Antoniadis, IEEE Electron. Device Lett. 29 (2008) 1074.
[9] S. Saurabh, M.J. Kumar, Jpn. J. Appl. Phys. 48 (2009) 064503.
[10] B. Ghyselen, Solid State Electron. 48 (2004) 1285.
[11] A. Ishizaka, Y. Shiraki, J. Electrochem. Soc. 133 (1986) 666.
[12] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, S. Takagi, IEEE Trans. Electron. Devices 59 (2012) 335.
[13] K. Park, B.H. Lee, D. Lee, D.-H. Ko, K.H. Kwak, C.-W. Yang, H. Kim, J. Electrochem. Soc. 154 (2007) 557.
[14] T. Nishimura, K. Kita, A. Toriumi, Appl. Phys. Lett. 91 (2007) 123123.
[15] Q.T. Zhao, J.-M. Hartmann, S. Mantl, IEEE Electron. Device Lett. 32 (2011) 1480.
[16] A. Ramstad, G. Brocks, P.J. Kelly, Phys. Rev. B 51 (1995) 504.
[17] L.T. Vinh, V.A. Fortuna, Y. Zheng, D. Bouchier, C. Guedj, G. Hincelin, Thin Solid Films 294 (1997) 59.
[18] A. Ichimiya, P.I. Cohen, Reflection High Energy Electron Diffraction, Cambridge University Press, Cambridge, 2004.
[19] D.E. Aspnes, A.A. Studna, Phys. Rev. B 27 (1983) 985.
[20] C.-Y. Peng, C.-F. Huang, Y.-H. Yang, C.-Y. Lai, S.-T. Chang, C.W. Liu, J. Appl. Phys. 105 (2009) 083537.
[21] J.H. Parker Jr., D.W. Feldman, M. Ashkin, Phys. Rev. 155 (1967) 712.
[22] R. People, J.C. Been, Appl. Phys. Lett. 47 (1985) 322.
[23] D.K. Schroder, Semiconductor Material and Device Characterization, 3rd edition A John Wiley & Sons, Inc., 2006.
[24] D.K. Mohata, R. Bijesh, Y. Zhu1, M.K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J.M. Fastenau, D. Loubychev, A.K. Liu, T.S. Mayer, V. Narayanan, S. Datta, Proc. Symp. VLSI Tech. Dig. (2012) 53.