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Investigation on the interface resistance of Si/GaAs heterojunctions fabricated by surface-activated bonding

Investigation on the interface resistance of Si/GaAs heterojunctions fabricated by surface-activated bonding

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The electrical properties of p-GaAs/n^+-Si, p^+-Si/n-GaAs, p^+-GaAs/n^+-Si, p^+-Si/n^+-GaAs, n^+-Si/n^+-GaAs, and p^+-Si/p^+-GaAs junctions fabricated by surface-activated bonding (SAB) were investigated. An amorphous layer with a thickness of 3 nm was found across the bonding interface without annealing. The current–voltage (I–V) characteristics of p^+-GaAs/n^+-Si, p^+-Si/n^+-GaAs, n^+-Si/n^+-GaAs, and p^+-Si/p^+-GaAs junctions showed excellent linearity. The interface resistance of n^+-Si/n^+-GaAs junctions was found to be 0.112 $\Omega\cdot cm^2$, which is the smallest value observed in all the samples. The resistance decreased with increasing annealing temperature and decreased to 0.074 $\Omega\cdot cm^2$ after the junction annealing at 400 °C. These results demonstrate that n^+-Si/n^+-GaAs junctions are suitable for the connection of subcells in the fabrication of tandem solar cells. © 2015 The Japan Society of Applied Physics

1. Introduction

III–V multijunction solar cells, which have reportedly produced high conversion efficiencies in comparison with other solar cell structures,[1–6] are promising practical candidates for next-generation solar cells. III–V/Si tandem cells would provide high efficiency,[7,8] low cost, mechanical robustness, and lightweight cells, relative to conventional Si and III–V multijunction cells. The direct epitaxial growth of III–V compounds on Si substrates would be the most desirable approach, but the hetero junction formed by epitaxial deposition typically introduces a substantial crystalline defect density because of the differences in crystal lattice and thermal expansion coefficient.[9,10]

One way to solve these differences is to perform surface-activated bonding (SAB),[11–13] in which surfaces of substrates are activated by the fast atom beams of Ar prior to bonding. It can accommodate the lattice mismatch between the bonding substrates and has enabled substrate bonding without heating. There are a few reports on SAB-based InGaP/Si, GaN/Si, and GaInP/GaAs/Si tandem solar cells.[14–16]

The ohmic properties of SAB-based Si/Si, Si/GaAs, and Si/InGaP p–n junctions were reported.[17,18] The interfacial conductivity of junctions was found to be improved by increasing the doping concentration of the bonding semiconductor. The reduction in electrical resistance across the interface connecting the subcells is very important for realizing a high-efficiency hybrid tandem cell by SAB. The interface resistance could lead to significant losses in multijunction solar cell operation. A resistance of 0.13 $\Omega\cdot cm^2$ has been found in p^+-GaAs/n^{++}-Si junctions, which resulted in the loss of 0.063 mV/cm^2 in two-junction tandem solar cells.[17] This value is markedly larger than those previously reported (3.92×10^{-4} $\Omega\cdot cm^2$) for InGaAs/Ge tunnel junctions in InGaP/InGaAs/Ge triple-junction solar cells.[19] Thus, it is necessary to further reduce the resistance of the bonding interface.

Although heating of samples is not required during SAB, the annealing process is necessary for forming good ohmic contacts in the electrode fabrication of multijunction solar cells. The effects of the annealing process on the electrical behavior of the Si/GaAs junctions have not yet been reported.

Table I. Carrier concentration and thickness of substrates.

Type		Carrier concentration (cm^{-3})	Thickness (μm)
p^+-Si		2.64×10^{19}	525
n^+-Si		2.61×10^{19}	525
n^+-GaAs	Epitaxial layer	$\sim1\times10^{19}$	0.4
	Substrate	$\sim1\times10^{18}$	340
p^+-GaAs	Epitaxial layer	$\sim1\times10^{19}$	0.4
	Substrate	$\sim1\times10^{18}$	340
n-GaAs	Epitaxial layer	$\sim1\times10^{17}$	0.4
	Substrate	$\sim1\times10^{18}$	340
p-GaAs	Epitaxial layer	$\sim1\times10^{17}$	0.4
	Substrate	$\sim1\times10^{18}$	340

In this work, we studied the effects of junction polarity and the annealing process on the electrical properties of Si/GaAs junction. The structural properties of the interfaces were examined by field emission scanning electron microscopy (FE-SEM) and transmission electron microscopy (TEM). We characterized their electrical properties by current–voltage (I–V) measurements and evaluated the relationship between the electrical properties and the depletion layer thickness.

2. Experimental methods

We used six types of substrates for SAB experiments. Their carrier concentrations are shown in Table I. The Hall measurements at room temperature revealed that the resistivities and carrier concentrations were 0.003 $\Omega\cdot cm$ and ($N_A=$) 2.64×10^{19} cm^{-3}, and 0.002 $\Omega\cdot cm$ and ($N_D=$) 2.64×10^{19} cm^{-3} for the p^+-Si and n^+-Si substrates, respectively. Before bonding, the Al/Ni/Au, Ti/Au, AuZn/Ti/Au, and AuGe/Ni/Ti/Au multilayers were evaporated on the back sides surfaces of p^+-Si, n^+-Si, p^+-GaAs and p-GaAs, and n^+-GaAs and n-GaAs substrates, respectively. The ohmic contacts of p^+-Si, p^+-GaAs, p-GaAs, n^+-GaAs, and n-GaAs substrates were formed by rapid thermal annealing at 400 °C for 60 s in N_2 gas ambient. p-GaAs/n^+-Si, p^+-Si/n-GaAs, p^+-GaAs/n^+-Si, p^+-Si/n^+-GaAs, n^+-Si/n^+-GaAs, p^+-Si/p^+-GaAs, p^+-Si/n^+-Si, n^+-Si/n^+-Si, p^+-Si/p^+-Si, n-GaAs/n-GaAs, p-GaAs/p-GaAs, p^+-GaAs/n^+-GaAs, n^+-GaAs/n^+-GaAs, and p^+-

GaAs/p^+-GaAs junctions were fabricated by SAB.[11–13] The n^+-Si/n^+-GaAs junctions were annealed separately at 100, 200, 300, and 400 °C for 300 s in N_2 gas ambient. All the samples were diced into 4 mm^2 pieces. *I–V* measurements were performed using an Agilent B2902A Precision Measurement Unit at room temperature. The bonding interfaces of the Si/GaAs junctions were investigated by FE-SEM (JEOL JSM6500F) and TEM (JEOL JEM-2100).

3. Results and discussion

3.1 Results

Figures 1(a) and 1(b) show FE-SEM and TEM images of the cross section of the Si/GaAs interface without annealing. As shown in Fig. 1(a), a straight line can be clearly recognized at the center of the sample. This line corresponds to the interface between Si and GaAs. In addition, we found in Fig. 1(b) that an amorphous layer of ~3 nm thickness was formed at the interface. More importantly, no structural defects such as cracks were observed at the interface.

Figure 2 shows the *I–V* characteristics of p^+-GaAs/n^+-Si, p^+-Si/n^+-GaAs, n^+-Si/n^+-GaAs, and p^+-Si/p^+-GaAs junctions measured between −0.1 and 0.1 V at room temperature. We found that the *I–V* characteristics shown in this figure revealed linear properties. The interface resistances of p^+-GaAs/n^+-Si, p^+-Si/n^+-GaAs, n^+-Si/n^+-GaAs, and p^+-Si/p^+-GaAs junctions were estimated to be 0.196, 0.132, 0.112, and 1.887 Ω·cm^2, respectively, by least-squares fitting at approximately 0 V. The resistance of n^+-Si/n^+-GaAs junctions is smaller than that of p^+-Si/p^+-GaAs junctions. The n^+-Si/n^+-GaAs junctions showed the smallest interface resistance among all the samples.

Figure 3(a) shows the *I–V* characteristics of n^+-Si/n^+-GaAs junctions without and with annealing at 100, 200, 300, and 400 °C measured between −0.1 and 0.1 V at room temperature. We found that, in the bias voltage range for measurements, the *I–V* characteristics of five samples showed excellent linearity. The interface resistances were found to be 0.112, 0.098, 0.087, 0.082, and 0.074 Ω·cm^2 for the junctions without and with annealing at 100, 200, 300, and 400 °C, respectively, by least-square fitting at approximately 0 V. The resistances of the respective samples at various annealing temperatures are shown in Fig. 3(b). It was found that the interface resistance decreases with increasing annealing temperature.

The *I–V* characteristics of n^+-Si/n^+-Si, p^+-Si/n^+-Si, p^+-Si/p^+-Si, n^+-GaAs/n^+-GaAs, p^+-GaAs/n^+-GaAs, and p^+-GaAs/p^+-GaAs junctions measured between −0.1 and 0.1 V at room temperature are shown in Fig. 4. It was found that the *I–V* characteristics in this figure showed excellent linearity. By least-squares fitting at approximately 0 V, the interface resistances of n^+-Si/n^+-Si, p^+-Si/n^+-Si, p^+-Si/p^+-Si, n^+-GaAs/n^+-GaAs, p^+-GaAs/n^+-GaAs, and p^+-GaAs/p^+-GaAs junctions were determined to be 0.034, 0.076, 0.206, 0.046, 1.010, and 3.429 Ω·cm^2, respectively. Note that the resistance of p–p junctions is larger than that of n–n junctions.

Figure 5 shows the *I–V* characteristics of n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions measured at room temperature. It was found that the *I–V* characteristics of n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions revealed symmetrical relationships versus voltage under both reverse- and forward-bias voltages. We determined that the interface resistances of n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions were 5.824 and 17664.97 Ω·cm^2, respectively, by least-squares fitting at approximately 0 V.

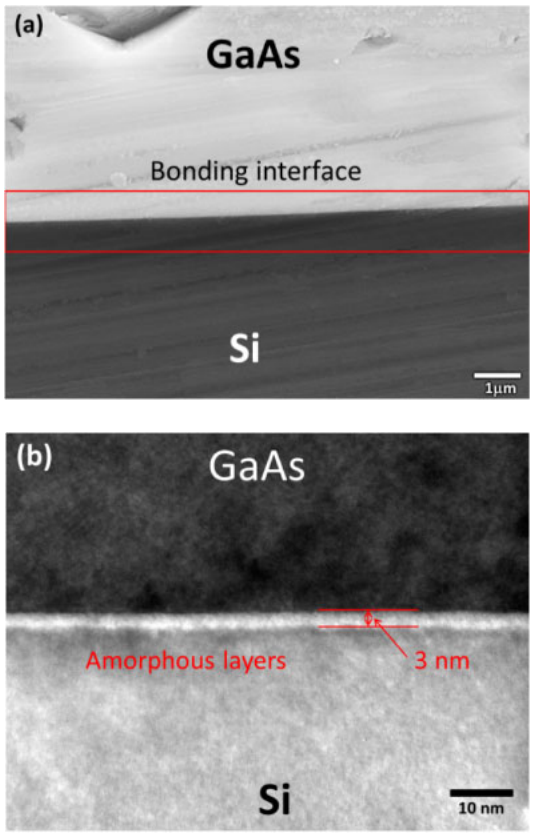

Fig. 1. (Color online) Cross-sectional FE-SEM (a) and TEM (b) images of the Si/GaAs interface.

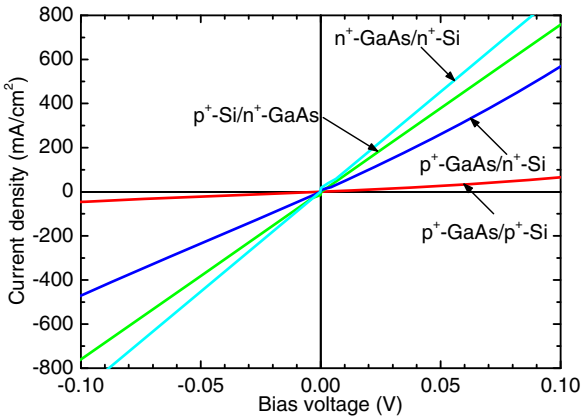

Fig. 2. (Color online) *I–V* characteristics of p^+-GaAs/p^+-Si, p^+-Si/n^+-GaAs, p^+-GaAs/n^+-Si, and n^+-GaAs/n^+-Si junctions measured at room temperature.

The *I–V* characteristics of p-GaAs/n^+-Si and p^+-Si/n-GaAs junctions measured at room temperature are shown in Fig. 6. It was found that both the curves revealed rectifying properties as expected for a p–n junction diode. Note that the magnitude of the current increased as the junctions were more deeply reverse biased for both the p-GaAs/n^+-Si and p^+-Si/n-GaAs junctions. In addition, the magnitude of the current of the p-GaAs/n^+-Si junctions was larger than that of the p^+-Si/n-GaAs junctions at the bias voltages.

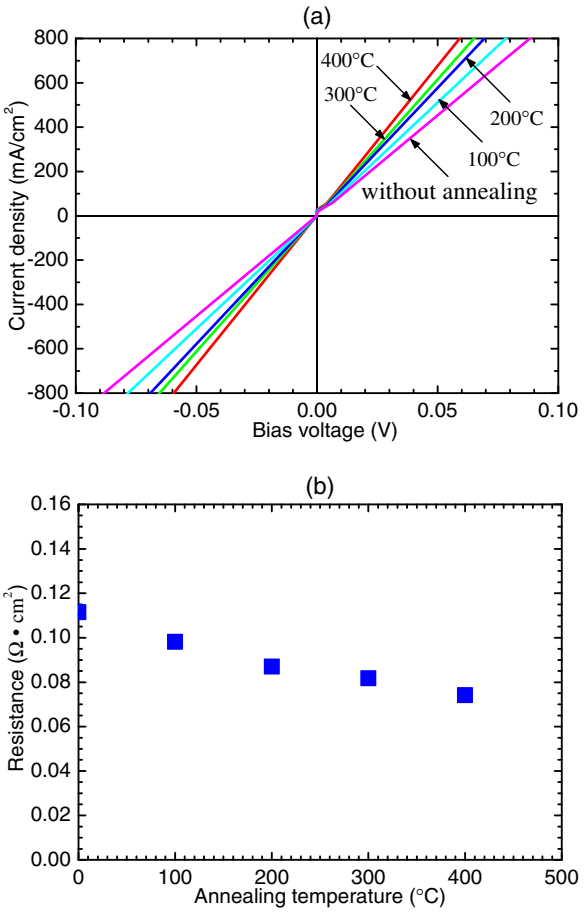

Fig. 3. (Color online) (a) *I–V* characteristics of n^+-Si/n^+-GaAs junctions without and with annealing at 100, 200, 300, and 400 °C measured at room temperature and (b) resistances of the respective samples at various annealing temperatures for n^+-Si/n^+-GaAs junctions.

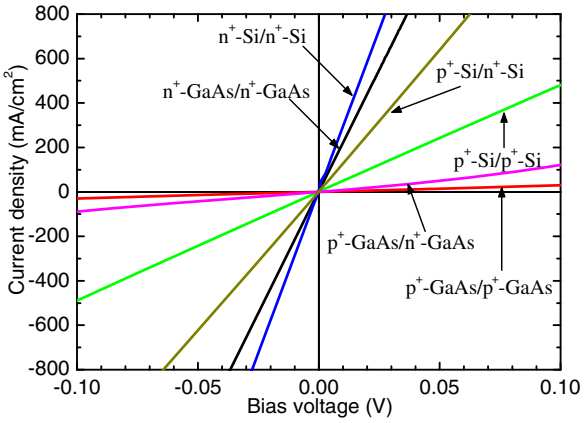

Fig. 4. (Color online) *I–V* characteristics of n^+-Si/n^+-Si, p^+-Si/n^+-Si, p^+-Si/p^+-Si, n^+-GaAs/n^+-GaAs, p^+-GaAs/n^+-GaAs, and p^+-GaAs/p^+-GaAs junctions measured at room temperature.

3.2 Discussion

In the present work, the Ar atom fast beam irradiation in SAB is assumed to induce the interface states. Such interface states should be distributed in the amorphous layer, which would likely be due to the Ar atom fast beam irradiation. The existence of electronic interface states is unavoidable at a bonding interface [because of the dangling bonds formed by

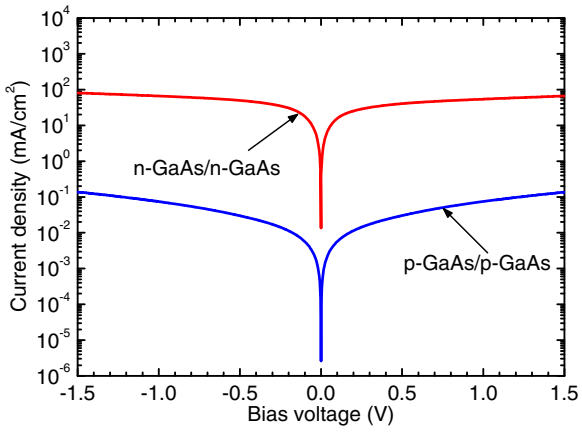

Fig. 5. (Color online) *I–V* characteristics of n-GaAs/n-GaAs and p-GaAs/p-GaAs junctions measured at room temperature.

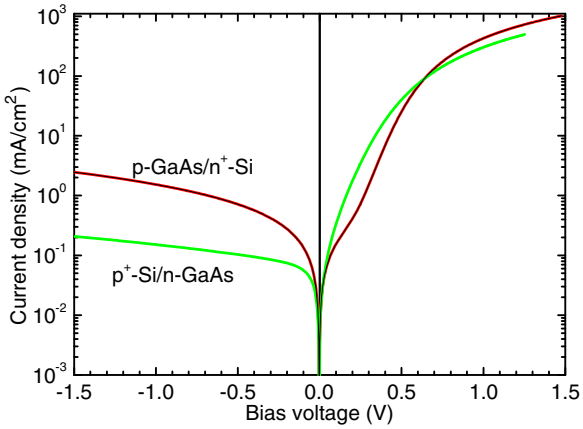

Fig. 6. (Color online) *I–V* characteristics of p-GaAs/n^+-Si and p^+-Si/n-GaAs junctions measured at room temperature.

a combination of different lattice structures]. The amorphous layer with a thickness of about 3 nm is observed at the Si/GaAs interface, [Fig. 1(b)]. A similar amorphous layer at the interface was also observed in the Si/Si,[20,21] Si/SiC,[22] and GaP/GaAs[23] junctions fabricated by SAB. For n^+-Si/n^+-GaAs, n^+-Si/n^+-Si, and n^+-GaAs/n^+-GaAs (p^+-Si/p^+-GaAs, p^+-Si/p^+-Si, and p^+-GaAs/p^+-GaAs) junctions, acceptor-like (donor like) defect states with energies below (above) the Fermi level should be formed at the interface, which can introduce a negative charge (a positive charge) at the interface. Consequently, a potential barrier and depletion layers exist in the conduction band (valence band) of the bonding interface. The high defect density and semiconductor doping concentration could reduce the barrier height and the thickness of the depletion layer.[24,25] Therefore, in high-impurity-concentration n–n and p–p junctions, the depletion layer thickness is extremely small, which enables the carriers to tunnel across the barrier of the bonding interface.

The conduction and valence band offsets are $\Delta E_c = 0.593\,\text{eV}$ and $\Delta E_v = 0.293\,\text{eV}$, respectively, which were determined from the results of previous experiments on p-Si/n-GaAs junctions fabricated by SAB.[26] As the valence band offset is significantly smaller than the conduction band offset, the injection of holes should be more effective in p^+-Si/p^+-GaAs junctions than that of electrons in n^+-Si/n^+-

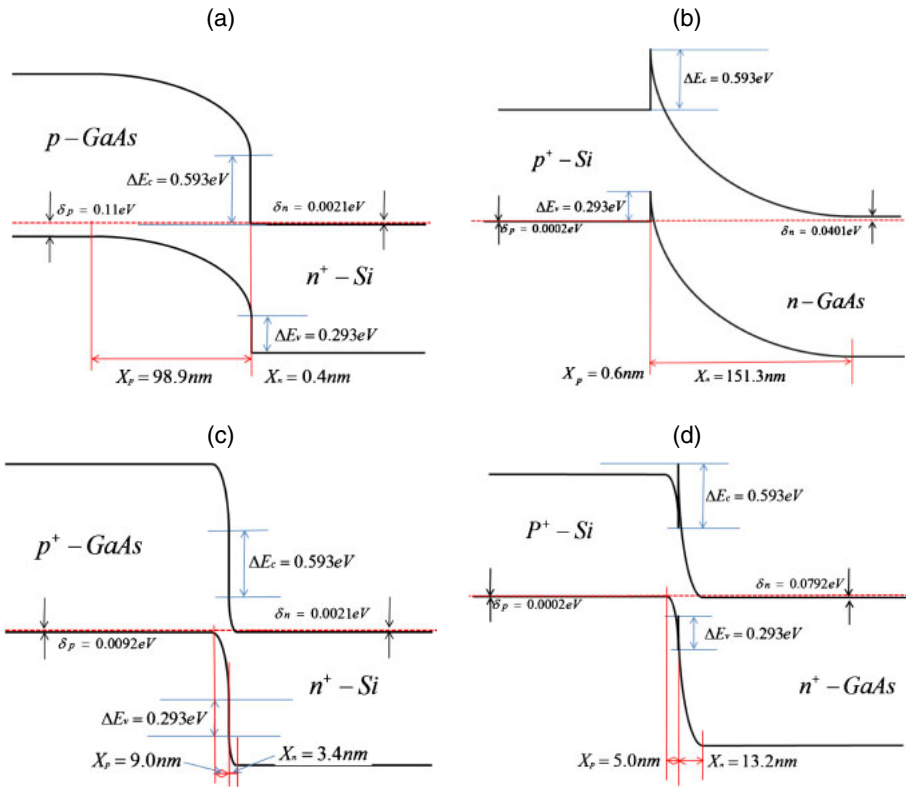

Fig. 7. (Color online) Schematic energy-band diagrams of (a) p-GaAs/n$^+$-Si, (b) p$^+$-Si/n-GaAs, (c) p$^+$-GaAs/n$^+$-Si, and (d) p$^+$-Si/n$^+$-GaAs junctions.

GaAs junctions. However, we found that the electrical conductivity in p$^+$-Si/p$^+$-GaAs junctions was significantly lower than that in n$^+$-Si/n$^+$-GaAs junctions. In addition, we also found that the resistances of p$^+$-Si/p$^+$-Si, p$^+$-GaAs/p$^+$-GaAs, and p-GaAs/p-GaAs junctions are surprisingly larger than those of n$^+$-Si/n$^+$-Si, n$^+$-Si/n$^+$-Si, n$^+$-GaAs/n$^+$-GaAs, and n-GaAs/n-GaAs junctions. This may be attributed to the difference in barrier height between the p–p and n–n junctions. It was reported that the barrier heights of n-Si/n-Si and p-Si/p-Si junctions were determined to be 0.15 and 0.4 eV, respectively, which decreased as the annealing temperature increased.[27)] The main reason for the difference in barrier heights should be that the interface state charge on the n–n (p–p) junctions decreased (increased) after the implantation of Ar ions. A similar result was observed in the p-Si and n-Si Schottky diodes, in which the substrates were implanted with Ar ions.[28,29)]

The existence of the amorphous layer across the bonding interface is assumed to be related to the interface resistance. A few reports indicated that the thickness of the amorphous layer decreased with increasing annealing temperature and the layer finally disappeared after annealing at a certain temperature.[23,30)] The annealing temperature can result in a sharp reduction in interface resistance, which eventually saturates after a certain period of annealing. A similar change was observed in the n-GaAs/n-GaAs and n-Si/n-GaAs junctions fabricated by direct wafer bonding[31)] and SAB,[32)] respectively. The observed rapid reduction in interface resistance should result from the recrystallization of the amorphous layer at the interface during annealing. The reduced interface resistance is assumed to be attributed to the reduction in interface state density. The improvement of the electrical conductivity of n–n and p–p junctions fabricated by SAB was reported to be related to the interface state density, which decreased with increasing annealing temperature.[27,33)] A similar behavior has also been reported for n-GaAs/n-GaAs fabricated by direct wafer bonding.[34)] In addition, the reverse-bias leak current dependence of amorphous layer thickness, which was attributed to the behavior of the interface state density, has been reported for the p-Si/n-SiC junctions fabricated by SAB.[23)] These results imply that the electrical conductivity of the bonding interface markedly depends on the amorphous layer thickness at the bonding interface.

Figures 7(a) and 7(b) show the energy-band diagrams of the p-GaAs/n$^+$-Si and p$^+$-Si/n-GaAs junctions, respectively, at zero bias voltage and room temperature. These diagrams are based on the carrier concentrations of the respective substrates shown in Table I. Note that these diagrams are based on the assumption that there are no additional charges located at the interfaces. The total thicknesses of the depletion layer in the p-GaAs/n$^+$-Si and p$^+$-Si/n-GaAs junctions are estimated to be 99.3 and 151.9 nm, respectively. The thickness of the depletion layer in the p$^+$-Si/n-GaAs junctions is much larger than that in the p-GaAs/n$^+$-Si junctions. The difference mentioned above between the p-GaAs/n$^+$-Si and p$^+$-Si/n-GaAs junctions might be related to their depletion layer thicknesses. The electrical characteristics of the p-GaAs/n$^+$-Si junctions are consequently assumed to be affected more largely by the interface states formed in the amorphous layer than those of the p$^+$-Si/n-GaAs junctions. Actually, the facts that, in the *I–V* characteristics of the p-GaAs/n$^+$-Si and p$^+$-Si/n-GaAs junctions, the magnitude of the reverse-bias current increases owing to the larger reverse bias and the depletion layer thickness is almost zero in both

the n^+-Si and p^+-Si substrates suggest that the tunneling process dominates the electrical transport properties across the Si/GaAs interfaces. A similar behavior was also observed at the p-Si/n-Si and p^--Si/n^+-Si junctions fabricated by SAB.[20)]

The total thicknesses of the depletion layers in the p^+-GaAs/n^+-Si and p^+-Si/n^+-GaAs junctions are similarly determined to be 12.4 and 18.7 nm at zero bias voltage, respectively, as shown in Figs. 7(c) and 7(d). The depletion layers of the p^+-GaAs/n^+-Si and p^+-Si/n^+-GaAs junctions are considerably narrower than those of conventional p–n junctions, which enables the carriers to tunnel across the depletion layer. The carriers of the p^+-GaAs/n^+-Si junctions tunneling across the depletion layer should be more effective than those of the p^+-Si/n^+-GaAs junctions. In contrast, the experimental data showed that the resistance of the p^+-GaAs/n^+-Si junctions is slightly higher than that of the p^+-Si/n^+-GaAs junctions. The difference in conductivity between the p^+-GaAs/n^+-Si and p^+-Si/n^+-GaAs junctions might be related to the interface state charges of the bonding interface. The fact that, in the *I*–*V* characteristics of the n^+-Si/n^+-Si, p^+-Si/p^+-Si, n^+-GaAs/n^+-GaAs, and p^+-GaAs/p^+-GaAs junctions, the interface resistance of the n^+-GaAs/n^+-GaAs junctions is comparatively close to that of the n^+-Si/n^+-Si junctions, whereas that of the p^+-GaAs/p^+-GaAs junctions is surprisingly larger than (approximately fifteen times as large as) that of the p^+-Si/p^+-Si junctions, suggests that a large number of positive charges are formed at the p^+-GaAs/p^+-GaAs interfaces. It is assumed consequently that the depletion layers in the p^+-GaAs substrates, which are formed by the interface charges, affect the carriers across the p^+-GaAs/n^+-Si interfaces.

Given that the annealing (typically at 400 °C)[34,35)] process is required for forming good ohmic contacts on GaAs, it is notable that the two substrates were firmly bonded to each other after annealing at 400 °C. It is also noteworthy that the interface resistance of the n^+-Si/n^+-GaAs junctions decreased to 0.074 Ω·cm^2, suggesting that the SAB-based Si/GaAs junctions are anticipated to play a significant role in fabricating devices operating for high-power and high-frequency applications, and that the n^+-Si/n^+-GaAs junctions are suitable for the connection of tandem subcells.

4. Conclusions

We fabricated p-GaAs/n^+-Si, p^+-Si/n-GaAs, p^+-GaAs/n^+-Si, p^+-Si/n^+-GaAs, n^+-Si/n^+-GaAs, and p^+-Si/p^+-GaAs junctions by SAB and measured their electrical properties at room temperature. The current–voltage characteristics of p^+-GaAs/n^+-Si, p^+-Si/n^+-GaAs, n^+-Si/n^+-GaAs, and p^+-Si/p^+-GaAs junctions showed ohmic properties. The interface resistances were estimated to be 0.196, 0.132, 0.112, and 1.887 Ω·cm^2 for p^+-GaAs/n^+-Si, p^+-Si/n^+-GaAs, n^+-Si/n^+-GaAs, and p^+-Si/p^+-GaAs junctions, respectively. The differences in electrical properties between p-GaAs/n^+-Si and p^+-Si/n-GaAs junctions, and between p^+-GaAs/n^+-Si and p^+-Si/n^+-GaAs junctions might be related to their depletion layer thicknesses. The interface resistance of n^+-Si/n^+-GaAs junctions decreases with increasing annealing temperature. It was reduced to 0.074 Ω·cm^2 after the junction annealing at 400 °C. These results suggest that SAB-based n^+-Si/n^+-GaAs junctions can be used for fabricating hybrid tandem cells.

Acknowledgment

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