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GaN MOSFET with a gate SiO_2 insulator deposited by silane-based plasma-enhanced chemical vapor deposition

Jin-Ping Ao[1,*], Katsutoshi Nakatani[1], Yuji Sogawa[1], Shiro Akamatsu[1], Young Hyun Kim[1], Takahiro Miyashita[2], Shin-ichi Motoyama[2], and Yasuo Ohno[1]

[1] Institute of Science and Technology, The University of Tokushima, 2-1 Minami-Josanjim, 770-8506 Tokushima, Japan
[2] Research and Development Department, SAMCO Inc., 7-25-3 Nishi-Gotanda Shinagawa-ku, 141-0031 Tokyo, Japan

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* Corresponding author: e-mail jpao@ee.tokushima-u.ac.jp, Phone: +81 88 656 7442, Fax: +81 88 656 7442

GaN metal-oxide-semiconductor field-effect transistors (MOSFETs) with a silane-based SiO_2 insulator deposited by plasma-enhanced chemical vapor deposition (PECVD) were demonstrated using an AlGaN/GaN heterostructure field-effect transistor (HFET) structure as the source and drain regions. Operation up to a gate voltage of 15 V was realized at an ignorable gate leakage current. To investigate the effects of annealing on the device performance, the samples were thermally treated at 850 or 1000 °C for 10 minutes in oxygen or nitrogen ambient. We found that the electron mobility and the interface state density were improved by a thermal treatment at 1000 °C in nitrogen ambient. A maximum field-effect mobility of approximately 137 $cm^2\ V^{-1}\ s^{-1}$ at an interface state density of $2.21\times10^{11}\ cm^{-2}\ eV^{-1}$ was obtained.

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1 Introduction Normally, the operation mode of AlGaN/GaN heterostructure field - effect transistors (HFETs) is depletion-mode (D-mode), because the conduction channel exists after the epitaxial growth due to the spontaneous and piezoelectric polarization charge effects in the AlGaN/GaN heterostructure [1]. However, for the application in the field of power electronics, devices with enhancement-mode (E-mode) are the key elements for realizing safe operation and reducing power consumption owing to the normally-off operation. E-mode devices are also attractive for developing single-power systems and realizing low-power direct-coupled logic by the combined use of E- and D-mode devices [2].

To achieve E-mode operation in the AlGaN/GaN HFET systems, fluorine implantation, gate recess etching and gate cap layer were introduced to deplete the existing electron channel [3-5]. However, among the most technologies mentioned above, a serious problem is that the gate leakage current will increase under positive bias. This is another important point for E-mode operation is the suppression of gate leakage current even during positive gate bias. Considering this, we have another choice by developing metal - oxide - semiconductor (MOSFET) structures like those on silicon.

To achieve E-mode MOSFETs on GaN, a high-quality channel with high carrier mobility and few interface states, and a method to realize source and drain contact are the critical technologies. GaN MOSFETs with insulators of MgO, SiO_2, HfO_2, SiN and Al_2O_3 have been reported to show E-mode operation [6-11]. However, the channel carrier mobility is still low. We have reported the performance and characteristics of a GaN MOSFET with tetraethylorthosilicate (TEOS) SiO_2 as the gate insulator [12]. Device operation up to a gate voltage of 10 V was realized at a low gate leakage current. Unfortunately, the maximum field-effect mobility is only approximately 45 $cm^2\ V^{-1}\ s^{-1}$ at an interface state density of $1.02\times10^{13}\ cm^{-2}\ eV^{-1}$. In this paper, we will report the performance and characteristics of a GaN MOSFET with a gate oxide deposited by silane-based plasma-enhanced chemical vapor deposition (PECVD) and an AlGaN/GaN heterostructure as the source and drain structure. We found that the performance on mobility and interface density has been improved by thermal treatment at high temperature.

2 Device fabrication The GaN MOSFET was developed on an AlGaN/GaN HFET structure grown on a sapphire (0001) substrate, including a buffer layer, a 3 μm

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i-GaN layer, and a 24 nm u-AlGaN layer with Al composition ratio of 25 %. The sheet resistance of the wafer is about 490 Ω/□. In the MOSFET structure, the two-dimensional gas (2DEG) layer was used as the ohmic contact layer for drain and source electrodes, and the semi-insulating buffer layer was used as the channel layer by removing the AlGaN layer, as shown in Fig. 1.

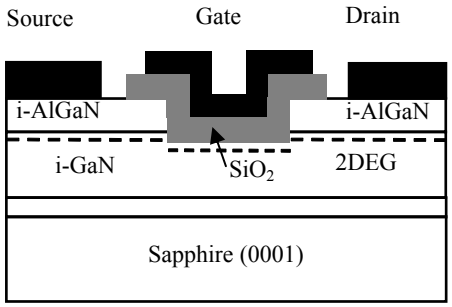

Figure 1 Device structure of the GaN MOSFET.

The device fabrication process was started from device isolation by inductively coupled plasma etching for an approximate 100 nm depth with $SiCl_4$ and Cl_2 gases. The AlGaN layer in the channel region was also recessed with the same system using a very slow etching rate to avoid etching damage. The etching depth was 40 nm with an etching rate of 1.2 nm/min. After these dry etching processes, the samples were cleaned using chemicals such as acetone and methanol, followed by a wet treatment with HNO_3:BHF = 1:1 solution. Next, a SiO_2 insulator with thickness of around 100 nm was deposited using SAMCO PD-220LC system. Three kinds of the samples were then thermally treated at 850 or 1000 °C for 10 min in N_2 or O_2 ambient. After the gate insulator patterning, ohmic contact was formed using Ti/Al/Ti/Au with annealing temperature of 850 °C for 1 min in N_2 ambient. Finally, Ni/Au was deposited as the gate electrode.

3 Device evaluation Measurements showed that the sheet resistance and the contact resistance had no obvious degradation after process for the devices only treated in Ohmic annealing process (marked as N_2/850/1), at 1000 °C for 10 min in N_2 ambient (marked as N_2/1000/10), and 850 °C for 10 min in O_2 ambient (marked as O_2/850/10), respectively. Degradation in both sheet resistance and contact resistance was found for the device treated at 1000 °C for 10 min in O_2 ambient (marked as O_2/1000/10). Capacitance-voltage measurement and step profile measurement by AFM showed that the thickness and permittivity of the oxide were 112.3 nm and 4.44, respectively. Figure 2 shows the gate leakage current with gate bias from -30 V to 15 V for the N_2/1000/10 device. The gate leakage current is suppressed below 10^{-10} A.

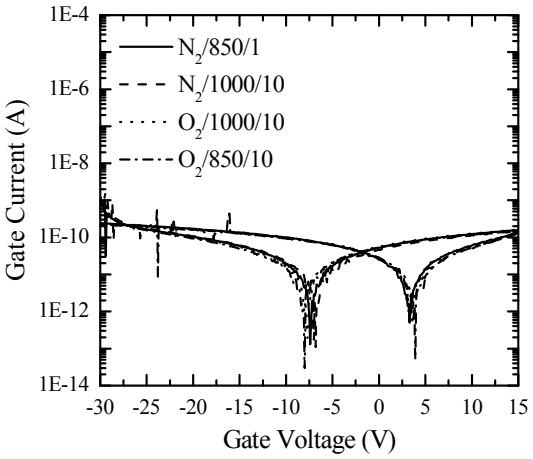

Figure 2 Gate leakage currents of the devices with gate biases from -30 to 15 V.

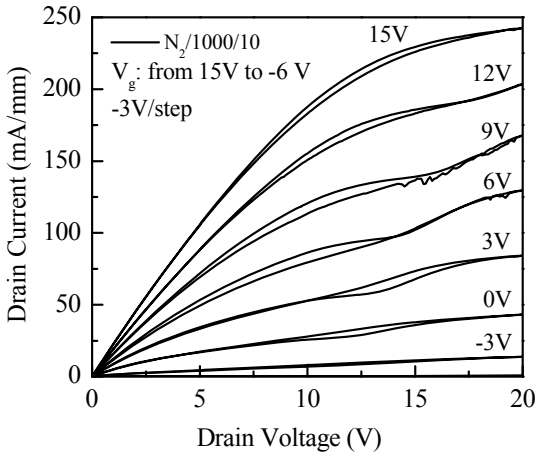

Figure 3 Current-voltage characteristics of the device at drain voltages from 0 to 20 V and gate voltages from 0 to 15 V.

Figure 3 shows the current-voltage (I-V) characteristics of a device which was treated in N_2 at 1000 °C for 10 minutes. The gate length and the gate width of the device are 3 μm and 50 μm, respectively, with the drain-source distance of 21 μm. It should be mentioned that the gate length is defined as the edge-to-edge distance in the recess region. The overlap lengths of SiO_2 and gate metal on AlGaN are 6 μm and 3 μm, respectively. Operation of drain current enhancement was confirmed up to a gate voltage of 15 V. Maximum drain current density of about 240 mA/mm and transconductance of about 15 mS/mm were obtained at drain voltage of 20 V and gate voltage of 15 V from the transfer characteristics, as shown in Fig. 4. The threshold voltage is about -3.5 V.

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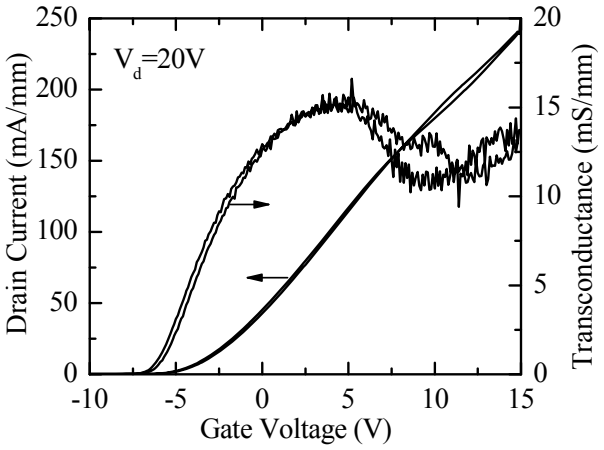

Figure 4 Drain current and transconductance of the device at drain voltage of 20 V.

Figure 5 shows the subthreshold characteristics of four kinds of ring-type transistors with inner electrode radius of 56 μm and the gate length of 100 μm. For all the devices, operation of drain current enhancement was confirmed up to a gate voltage of 15 V. The threshold voltages of the samples which were treated in O_2 ambient were found to have positive shift. Especially, the threshold voltage of the sample treated in O_2 at 1000 °C is about 1.0 V. The negative threshold voltage is considered to be mainly due to the existing interface state considering that a semi-insulating GaN layer is used as the surface channel. To move the threshold to the positive side, an improved interface with low interface state density is desired. Furthermore, a P-type GaN substrate is necessary to get a positive threshold voltage.

To investigate the interface characteristics of the SiO_2-GaN MOS structure, subthreshold swing and interface state were estimated. The subthreshold swing, which is the gate voltage (V_G) needed to reduce the drain current (I_{DS}) by one decade, is defined as:

$$S = \frac{dV_G}{d\log I_{DS}}. \tag{1}$$

The measured subthreshold swings were 0.249 V/dec (N_2/850/1), 0.212 V/dec (N_2/1000/10), 0.189 V/dec (O_2/850/10), 0.209 V/dec (O_2/1000/10), respectively. The equivalent circuit of a MOS structure can be expressed as the oxide capacitance C_{OX} connected in series with a parallel connection of the depletion capacitance C_D and the interface-related capacitance C_{it}. In this case, the subthreshold swing can be expressed as

$$S = (\ln 10)\left(\frac{kT}{q}\right)\left(1+\frac{C_D}{C_{OX}}+\frac{C_{it}}{C_{OX}}\right), \tag{2}$$

where k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge.

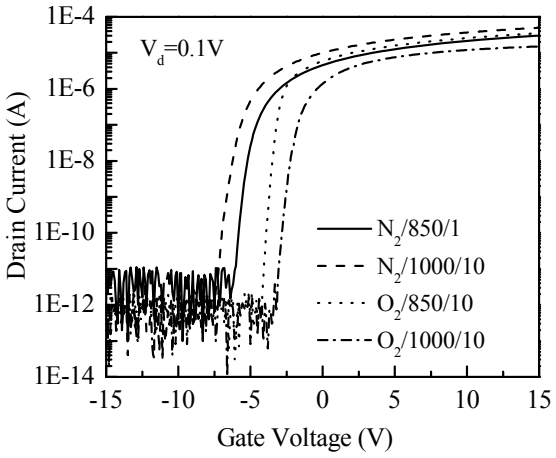

Figure 5 Subthreshold characteristics of the devices with different thermal treatment conditions.

Using Eq. (2) and assuming that the depletion capacitance is zero, we estimated that the densities of the interface state between SiO_2 and GaN were 3.32×10^{11} (N_2/850/1), 2.21×10^{11} (N_2/1000/10), 1.57×10^{11} (O_2/850/10), and 2.16×10^{11} (O_2/1000/10) cm^{-2} eV^{-1}, respectively. Theoretically, for a Si MOSFET with a SiO_2 thickness of 50 nm and a carrier concentration of 1×10^{16} cm^{-3} on a p-type substrate, the calculated subthreshold swing is 0.189 V/dec without any interface state. The minimum subthreshold swing will reach 59.6 mV/dec at room temperature assuming that the oxide thickness is zero and carrier concentration is also zero. As shown in Eq. (2), the subthreshold swing will increase by the existence of the interface-related capacitance C_{it}. If the interface state is below 10^{10} cm^{-2} eV^{-1}, the affect can be ignored in the above calculation case. In our GaN MOSFET case, the depletion capacitance is assumed as zero considering that the carrier concentration is extremely low in the semi-insulating substrate, so the affect on subthreshold swing comes mainly from the interface state. In this experiment, the subthreshold swing and interface state density were improved by thermal treatment. A low subthreshold swing of 0.189 V/dec and a low interface state density of 1.57×10^{11} cm^{-2} eV^{-1} were obtained even though the thickness of the oxide is 112.3 nm. A very good SiO_2-GaN interface was achieved.

Capacitance and conductance measurement showed that the field-effect mobilities were 108 and 79 cm^2/Vs, respectively, for the devices treated at 850 °C and 1000 °C in oxygen, as shown in Fig. 6. For the devices treated at Ohmic annealing condition and 1000 °C in nitrogen ambient, the measured mobilities were 110 and 137 cm^2/Vs, respectively. Obviously, channel mobility and interface characteristics were improved through thermal treatment in N_2 ambient. The mobility was degraded by treating in O_2 ambient even though the interface was improved. This is considered to be due to the oxygen diffusion into the channel.

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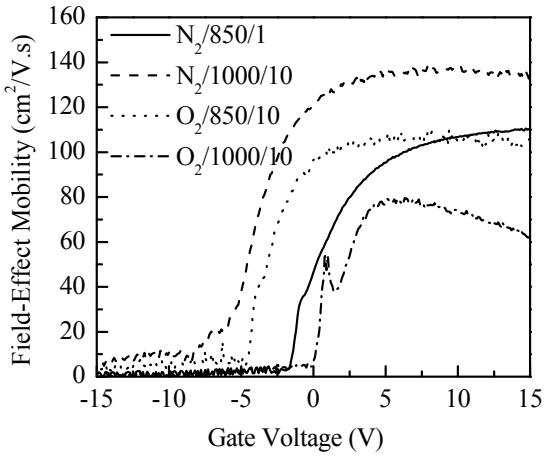

Figure 6 Measured field-effect mobilities of the devices.

4 Conclusion GaN MOSFETs with a silane-based SiO_2 insulator were developed on an AlGaN/GaN HFET structure. Operation up to a gate voltage of 15 V was realized at a low gate leakage current. Device characteristics such as electron mobility and interface state were improved by thermal treatment at 1000 °C in nitrogen ambient. The maximum field-effect mobility is approximately 137 cm^2 V^{-1} s^{-1} at an interface state density of 2.21×10^{11} cm^{-2} eV^{-1}.

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