

Wafer-Level Electroluminescence Metrology for InGaN Light-Emitting Diodes

Jong-In Shim, *Member, IEEE*, Dong-Pyo Han, and Dong-Soo Shin, *Member, IEEE*

Abstract—We present a reliable and fast characterization system that measures the electroluminescence (EL) of light-emitting diodes (LEDs) at the epi-wafer level. This “EL Q-check system” requires simple pre-processes for the measurement, circumventing the full chip-fabrication processes. The developed EL Q-check system consists of three parts: a CO₂ laser for p-GaN ablation, a diamond knife for delineating the measurement area on the wafer and isolating the damaged area during the CO₂ laser ablation, and the actual EL measurement on the wafer. The accuracy and the usefulness of the EL Q-check system are experimentally tested with eleven LED wafers of different crystal qualities by comparing the EL performances from the proposed system with those of the fully fabricated LED chips. For this purpose, the same wafers were divided in half and test patterns and LED chips were processed, respectively. A surprisingly good correlation between the results obtained by two methods indicates that the developed EL Q-check system can be used for accurate, reliable, and fast epi-wafer evaluation.

Index Terms—Electroluminescence, metrology, light-emitting diode, epi-wafer, Q-check system.

I. INTRODUCTION

THERE has been a tremendous progress in commercial production of visible light-emitting diodes (LEDs) and laser diodes (LDs) by utilizing III-nitride compound semiconductors recently. Especially, the InGaN-based visible LEDs are replacing conventional incandescent and fluorescent lamps as general lighting sources owing to their environmental friendliness and robustness [1]–[5]. Still, the LED industry struggles with very strict requirements of higher performance with lower manufacturing costs. The drop of internal quantum efficiency (IQE) at high injection currents, a phenomenon typically known as the efficiency droop, and other issues related with the operating voltage, color bin, and long-term reliability represent some of the inherent technical challenges to overcome [6]–[9]. At the same time, the packaging and

testing costs also pose significant economic burdens for research and development of more efficient LEDs.

Typically, manufacturing processes of LED modules roughly consist of following three steps: i) the sapphire substrate processing and subsequent epitaxial growth on it by the metal-organic chemical vapor deposition (MOCVD), ii) the LED die processing by etching, photolithography, metallization, etc., and iii) the LED chip packaging with wire and die bonding, epoxy molding, etc. [10] In general, the cost for the back-end processing after epitaxial growth is known to be as high as ~90% of the total LED chip manufacturing costs. Therefore, it is very desirable to predict the electroluminescence (EL) characteristics of LED devices such as the optical power, spectrum, forward voltage, and reverse leakage current just after the MOCVD growth without the full wafer processing to save time and labor costs.

While the photoluminescence (PL), Raman spectroscopy, x-ray diffraction, and atomic force microscopes have been popularly utilized at the epitaxial wafer stage [11]–[16], they are limited to characterizing optical or crystallographic properties and insufficient to represent the actual electroluminescent characteristics of LEDs. On the contrary, a method of EL metrology for the LED epi-wafers has not yet been well developed, which is mainly due to the difficulties in forming the contact electrodes and controlling the current paths both stably and reproducibly.

Until now, two EL metrology methods known as the In-dot metrology and the wafer-edge contact metrology have been used in order to predict the EL characteristics of the LED devices at the epi-wafer stage. In the In-dot metrology, n- and p-electrodes are formed on each n- and p-type epitaxial layer by handy processes using In metal balls. Usually, the p-type layer is scratched with a diamond cutter for the n-type contact formation on the surface of the n-type layer. This method is not technically elegant in that it is destructive and sensitive to the operator's skill. However, very reliable experimental data such as the leakage current under reverse bias or the optical power at a forward current are usually achievable as the perfect electrical isolation between the p- and n-type layers can be achieved by the mechanical scratch.

On the other hand, the wafer-edge contact metrology is a nondestructive method and is commercially available [18]. This method still has some technical difficulties such as its sensitivity to achieving very reproducible electrical contacts to the p-layer only by mechanical metal probing. Also, the

Manuscript received July 25, 2016; revised August 31, 2016; accepted September 2, 2016. Date of publication September 13, 2016; date of current version September 26, 2016. This work was supported by the Industrial Strategic Technology Development Program, Development of WPE 75% LED Device Process and Standard Evaluation Technology funded by the Ministry of Trade, Industry and Energy, Korea, under Grant 10041878.

J.-I. Shim and D.-P. Han are with the Department of Electronics and Communication Engineering, Hanyang University, Ansan 426-791, South Korea (e-mail: jishim@hanyang.ac.kr).

D.-S. Shin is with the Department of Applied Physics and the Department of Bionanotechnology, Hanyang University, Ansan 426-791, South Korea (e-mail: dshin@hanyang.ac.kr).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JQE.2016.2608798

0018-9197 © 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

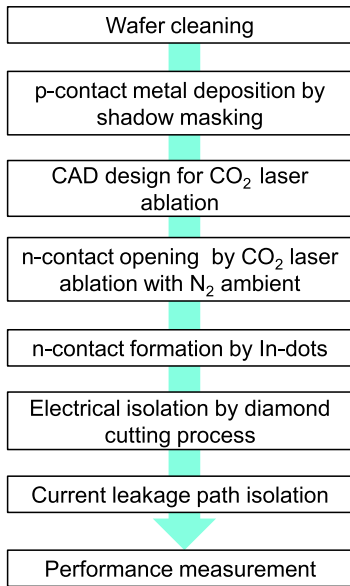


Fig. 1. The flowchart for the proposed epitaxial wafer processing.

current flowing from the p-contact area to the n-electrode may be disturbed by the randomly scattered defects over the wafer surface. Thus, there exists a need to make up for the weakness of the present EL metrologies.

In this paper, we present a reliable and fast EL characterization system at the LED epi-wafer stage, called “EL Q-check system”, which requires semi-automatic processes instead of the full chip fabrication.

This paper is organized as follows. Section II describes experimental techniques applied in our study. Detailed data from the measurements are presented in Section III. Section IV summarizes the obtained results and concludes the paper.

II. EPITAXIAL WAFER PROCESSING FOR EL Q-CHECK

For experiments, we prepared epitaxial wafers grown by MOCVD on c-plane sapphire substrates for InGaN/GaN blue LEDs. The epitaxial layer structure was a standard one for conventional blue LEDs, which consisted of an n-GaN buffer layer, five pairs of InGaN/GaN multiple quantum wells (MQWs), an AlGaIn electron blocking layer (EBL), and a p-GaN clad layer.

The wafer preparation procedure for our EL Q-check system is outlined in the flowchart shown in Fig. 1. After wafer cleaning, we make the p- and n-metal electrodes successively. Then the test LED pattern is electrically isolated from the rest of the wafer mechanically. An additional electrical isolation between p- and n-electrodes is applied. Lastly, we evaluate the EL characteristics by changing the bias level of voltage and current. Fig. 2(a) and (b) show optical microscopic images of a fabricated test LED pattern with and without current injection, respectively. In the next subsections, we describe each step in more detail.

A. P-Contact

For reliable EL characterization, one of the important technical issues is to delineate the p-type metal contact very stable and reproducibly, even with insufficient ohmic contact

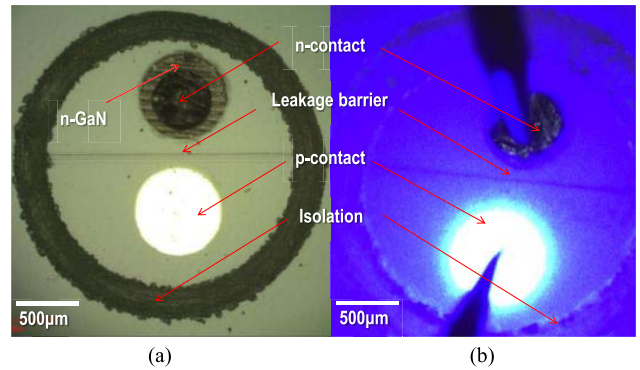


Fig. 2. (a) The image of the Q-check pattern on the wafer and (b) its EL image under forward bias.

property. The indium tin oxide (ITO) has been popularly utilized as a transparent p-type ohmic contact [19]. In our EL Q-check system, circular p-metal electrodes are formed on the surface of the epitaxial wafer by electron-beam evaporation of a 20-nm-thick ITO layer with a simple shadow mask technique as shown in Fig. 2(a).

The hole current injected from the p-electrode to the InGaN/GaN QWs is confined vertically by the p-electrode pattern without spreading laterally as shown in Fig. 2(b) because the p-GaN layer has a relatively high resistivity and is very thin compared to the n-GaN layer [20]. Thus, it is very important to form and define the p-electrode very reproducibly. In this sense, a simple shadow mask technique works well for the purpose although it requires a little processing time.

B. N-Contact

In order to make the n-electrodes, it is necessary to etch the p-GaN layer from the surface of the epitaxial wafer. Here, we use a semi-automatic approach of using CO₂-laser ablation of the p-layer instead of chemical etching or mechanical scribing with a diamond cutter to save processing time and labor. The laser ablation system is computer-controlled so that the laser's power, duty cycle, and scan speed can be adjusted precisely to achieve the desired ablation depth and pattern. After the CO₂-laser ablation of the p-GaN layer, we manually put an In ball on the n-GaN surface and heat it on a hot plate at 200 °C for 2 min to melt it thermally [21].

C. Electrical Isolation

The electrical isolation of a testing area from the remainder of the wafer is necessary in order to eliminate the current paths via various defects in other areas. Here we use a fully mechanical method of using a diamond cutter whose tip diameter is $\sim 10\ \mu\text{m}$. We circularly scribe the epitaxial layers from the surface to the sapphire substrate by the diamond cutter which is fixed to a specially designed mechanical system. An outer dark circle in Fig. 2(a) shows the scribed isolation pattern. Its schematic top and cross-sectional views are shown in Fig. 3. ITO and In ball, used as p- and n-metal electrodes, respectively, are seen in Fig. 3 as well as the mechanical scratch of the circular pattern surrounding metal electrodes

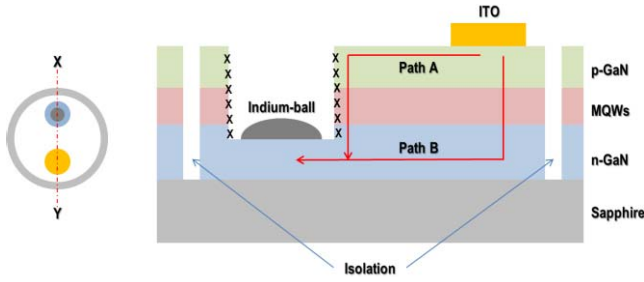


Fig. 3. The schematic top-view of the processed pattern with electrical contacts and isolation (left) and its cross-section along the x-y axis (right).

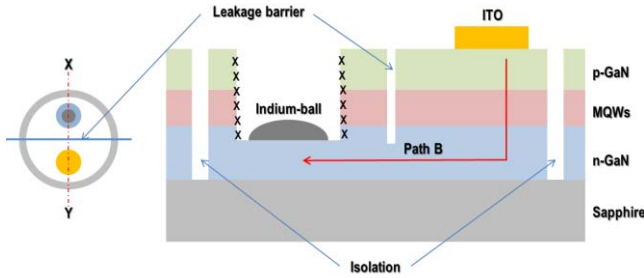


Fig. 4. The schematic top-view of the processed pattern with electrical contacts, isolation, and the leakage barrier (left) and its cross-section along the x-y axis (right).

made by the diamond cutter for a perfect electrical isolation of the testing area from the remainder of the epitaxial wafer.

D. Leakage Barrier

In Fig. 3, two current paths A and B are shown. The current path B represents a current component for the EL from the active region. On the other hand, the current path A accounts for the surface leakage current resulting from the thermal damages on the side wall, marked by x's, during the CO₂-laser ablation.

It is necessary to suppress the surface leakage current (path A) for precise evaluation of EL characteristics from the active MQW region (path B). To achieve this goal, we make a leakage barrier between the p- and n-electrodes by scratching a line from the surface to the n-GaN layer as schematically shown in Fig. 4. A diamond cutter with a tip diameter of $\sim 1 \mu\text{m}$ is used. Care must be taken during scratch in order not to introduce any damage or contamination that might cause the surface leakage. With this careful mechanical isolation technique, we can eliminate the surface leakage current via path A shown in Fig. 3.

Fig. 5 compares the I-V curves measured at different fabrication steps. The black solid line is the one after the consecutive processes of p-electrode deposition, laser ablation of p-GaN and MQW layers, and n-electrode formation on the n-GaN layer. In this case, current levels below the forward voltage of 2 V are highest among three cases and its shape is symmetric around zero bias. Such symmetric I-V curves typically indicate surface leakage currents via layers damaged during the laser ablation process [22].

The leakage current level is reduced from the black solid line to the red solid line by adding a diamond isolation process to the test region. The red solid line is measured after

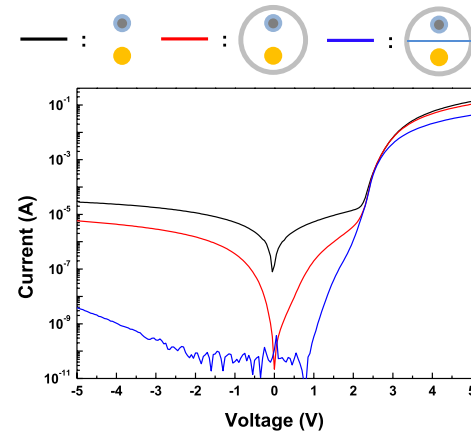


Fig. 5. The I-V characteristics measured after three different processing steps.

mechanically scribing a circle from the surface to the sapphire substrate, which can perfectly isolate the test pattern from the other region. A difference current between the black and red lines is understood as the recombination current via defects outside the test region.

We can further reduce the leakage current flowing through the surface region damaged during the laser ablation process by separating the surface region from the p-electrode region as shown by the blue line in Fig. 5. Compared to the black and red solid lines, the blue solid line is very asymmetric around zero bias and its current level at the reverse-biased region is extremely low. From the fact that its shape resembles a typical I-V curve of a GaN p-n diode, we expect that the blue solid line represents an electrical property of the bulk MQW region.

III. EXPERIMENTS AND DISCUSSION

Eleven LED wafers of different crystal qualities were prepared in order to verify the accuracy of the proposed EL Q-check system. We fabricated two different LED patterns on the same wafer, i.e., ones by the proposed EL Q-check and the others by the conventional LED chip processing. We first processed a half of each epitaxial wafer by using the EL Q-check method and measured their EL characteristics. Then, we completely removed the metal electrodes and fabricated lateral-electrode LED chips on the other half of each epitaxial wafer by the conventional LED chip processing. Fig. 6 shows a processed LED wafer where the EL Q-check and LED chip patterns fabricated in this experiment are seen in the upper and lower halves, respectively.

A. EL Spectrum

Figs. 7 (a) and (b) show an example of the normalized EL spectra measured at 1 A/cm^2 and their dominant wavelengths as a function of current density, respectively. In the EL Q-check pattern, the current flow is limited by the p-electrode size as shown in Fig. 2 (b). Thus, the current density of an EL Q-check pattern is calculated by dividing the driving current with the p-electrode size. On the other hand, the current density of a lateral LED chip is obtained by dividing the driving current with the total chip size.

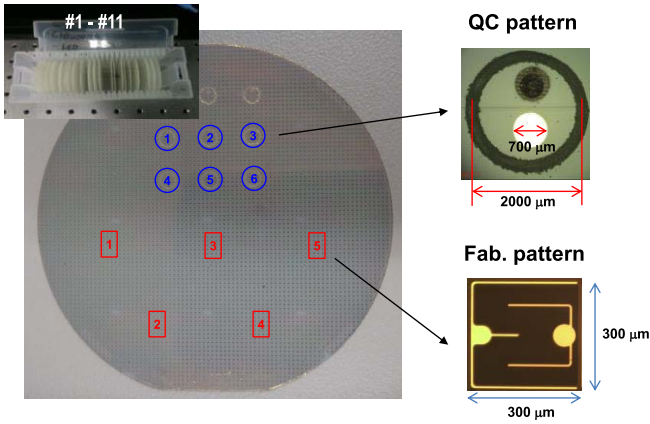


Fig. 6. Two different LED patterns are fabricated on the same wafer: the proposed EL Q-check pattern (upper half) and the conventional lateral-electrode LED pattern (lower half).

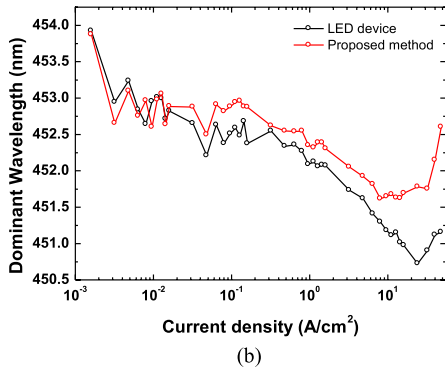
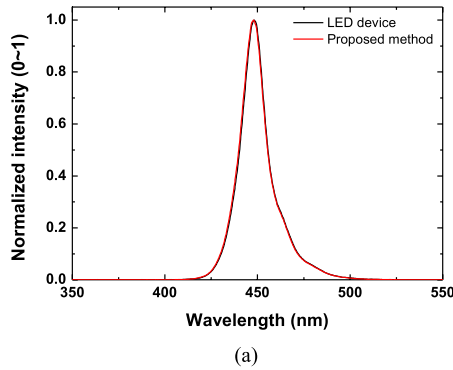


Fig. 7. (a) Normalized EL spectra at 1 A/cm² and (b) dominant wavelengths of EL spectra as a function of current density from the LED device and the proposed Q-check pattern.

As shown in Fig. 7, there is little difference in EL spectra and dominant wavelengths when the current density is less than ~ 10 A/cm². However, at high current densities $> \sim 10$ A/cm², larger red shifts are observed from the EL Q-check method. This is considered due to poorer ohmic contacts and subsequently higher heating with the EL Q-check system.

B. I-V Characteristics

Fig. 8 compares the I-V characteristics of the EL Q-check pattern and the LED pattern. The I-V curves are very similar when the bias voltage is less than 2 V. But we see relatively large differences in the I-V curves when the bias voltage is larger than that 2 V, which is due to the poor ohmic contact by

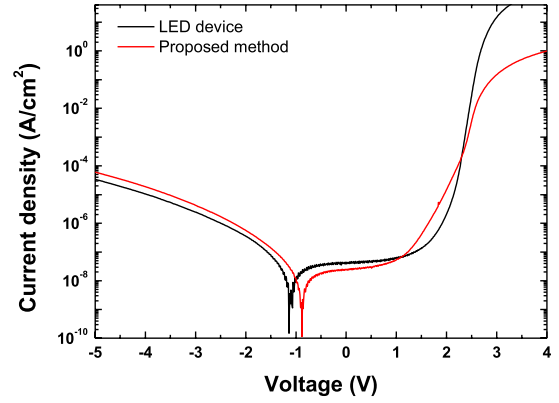


Fig. 8. The current density as a function of bias voltage for the LED device and the proposed Q-check pattern.

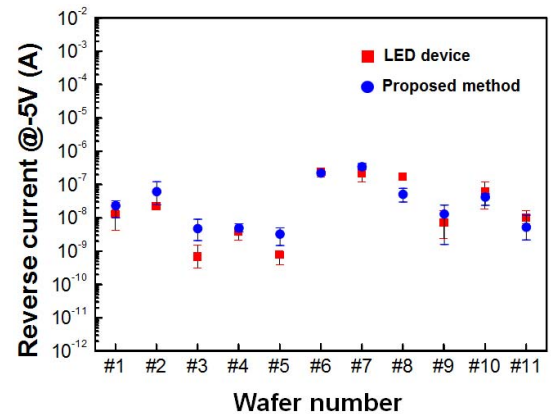


Fig. 9. Leakage currents at -5 V for the LED devices and the proposed Q-check patterns fabricated on 11 epitaxial wafers.

the EL Q-check method. It is well known that the forward I-V characteristic is greatly affected by the current flowing paths and the series resistance [23]. Thus, the proposed EL Q-check method may not be accurate for estimating the forward operating voltage at a given forward current or current density [24].

We focus on the leakage current under reverse bias which is closely related to the various types of defects. Thus, the current at a certain reverse bias is a very useful parameter to indicate defect densities of epitaxial wafers. Fig. 9 compares the leakage current at a bias voltage of -5 V from the EL Q-check and LED device patterns for 11 different epitaxial wafers. We tested five samples from each pattern and their variations are denoted by error bars for each epitaxial wafer. The leakage currents between two device patterns are almost the same, indicating that the proposed EL Q-check system is very useful to predict the leakage-current level under reverse bias.

C. Optical Power

We also compare the light output power as a function of current. In the EL Q-check pattern, the thick p-electrode pattern reflects emission light from the active layers so that most of light is emitted through sapphire substrates. Thus, we measured the optical power from the sapphire substrates for the EL Q-check pattern and from the top surface for the LED pattern. Fig. 10 shows relative optical powers from two different device patterns driven at 50 mA for 11 different

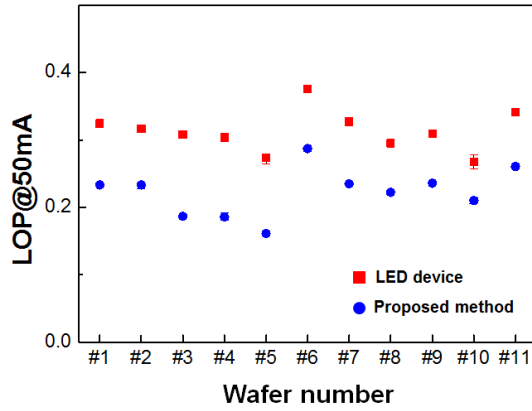


Fig. 10. Relative optical powers at a driving current of 50 mA for the LED devices and the proposed Q-check patterns fabricated on 11 epitaxial wafers.

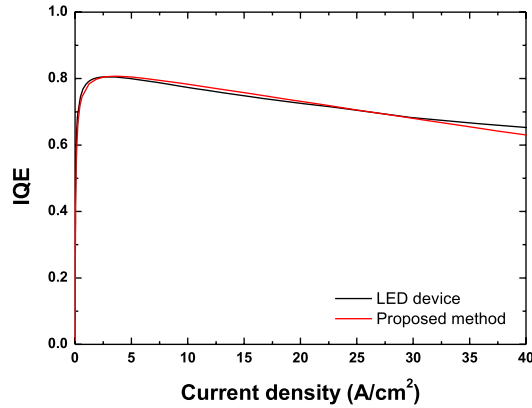


Fig. 11. The IQE as a function of current density for the LED device and the proposed Q-check pattern.

epitaxial wafers. It is clear that the variations of optical powers are quite consistent between the two device patterns.

D. IQE

The IQE is one of the most important characteristics representing the performance of InGaN-based blue LEDs. It has been known that the IQE of a blue LED is affected by many factors such as defects in epitaxial layers, the piezoelectric field, and the local potential fluctuation [25]. We have developed a simple IQE measurement method based on the ABC model and applied the method to these test patterns [26]. Fig. 11 shows an example of the IQE as a function of current density for two device patterns. Similar efficiency droop behaviors are observed between the two device patterns for other samples at high current densities.

Fig. 12 depicts the averaged IQEs at a driving current density of 55 A/cm² for 5 different LED devices and proposed EL Q-check patterns from 11 different epitaxial wafers. A very close correlation is observed across all the wafers. As Figs. 11 and 12 demonstrate, the proposed EL Q-check method should prove very reliable and useful for the IQE measurement at the epi-wafer level.

IV. CONCLUSION

We have proposed a new EL Q-check method to evaluate the electrical and optical characteristics of InGaN-based epitaxial

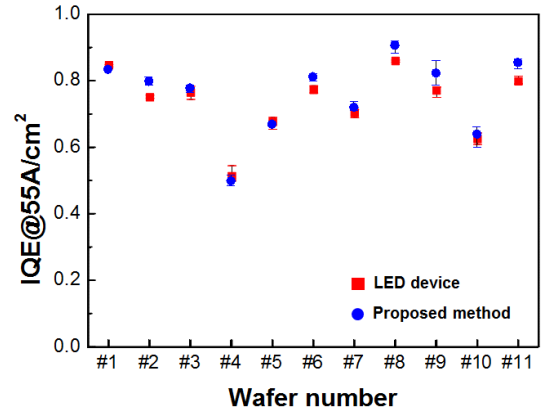


Fig. 12. The IQE as a function of current density for the LED devices and the proposed Q-check patterns fabricated on 11 epitaxial wafers.

wafer without full fabrication and packaging processes. The proposed method utilizes a CO₂ laser and a diamond cutter and can be completed within only 2-3 hours. It employs simple processes such as scribing the isolation and the leakage barrier for more accurate characterization of the epitaxial wafer. The proposed method in this study can enable the fast feedback and screening of LED epitaxial wafers to improve the LED device performance through measuring optical and electrical characteristics such as the EL spectrum, reverse leakage current, and the IQE. We have confirmed that the measured results obtained by the proposed method have very good correlations with the results obtained by LED devices obtained by full fabrication processes. We believe that our method can supply essential information about the epitaxial wafers with minimal time and labor costs and thus enable further performance improvement of LED devices in the research and development environment.

ACKNOWLEDGMENT

The authors would like to thank H. W. Ryu, Y. -J. Kim, H. S. Kim, and S. G. Kim for experimental helps, K. B. Nam and S. S. Choi for sample preparation and technical discussions.

REFERENCES

- [1] E. F. Schubert, *Light-Emitting Diode*, 2nd ed. New York, NY, USA: Cambridge Univ. Press, 2006.
- [2] Y. J. Tsao, "Solid-state lighting: Lamps, chips, and materials for tomorrow," *IEEE Circuits Devices Mag.*, vol. 20, no. 3, pp. 28–37, May/Jun. 2004.
- [3] S. Pimpitkar, J. S. Speck, S. P. DenBaars, and S. Nakamura, "Prospects for LED lighting," *Nature Photon.*, vol. 3, no. 4, pp. 180–182, 2009.
- [4] M. H. Crawford, "LEDs for solid-state lighting: Performance challenges and recent advances," *IEEE J. Sel. Topics Quantum Electron.*, vol. 15, no. 4, pp. 1028–1039, Jul./Aug. 2009.
- [5] Y. Narukawa, M. Ichikawa, D. Sanga, M. Sano, and T. Mukai, "White light emitting diodes with super-high luminous efficacy," *J. Phys. D, Appl. Phys.*, vol. 43, no. 35, p. 354002, Aug. 2010.
- [6] J. Piprek, "Efficiency droop in nitride-based light-emitting diodes," *Phys. Status Solidi A*, vol. 207, no. 10, pp. 2217–2225, Oct. 2010.
- [7] D.-P. Han, H. Kim, J.-I. Shim, D.-S. Shin, and K.-S. Kim, "Influence of carrier overflow on the forward-voltage characteristics of InGaN-based light-emitting diodes," *Appl. Phys. Lett.*, vol. 105, pp. 191114-1–191114-4, Nov. 2014.

- [8] M. Meneghini *et al.*, "Leakage current and reverse-bias luminescence in InGaN-based light-emitting diodes," *Appl. Phys. Lett.*, vol. 95, no. 17, pp. 173507-1-173507-3, Oct. 2009.
- [9] M. Meneghini, L.-R. Trevisanello, G. Meneghesso, and E. Zanoni, "A review on the reliability of GaN-based LEDs," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 323-331, Jun. 2008.
- [10] T.-Y. Seong, J. Han, H. Amano, and H. Morkoc, *III-Nitride Based Light Emitting Diodes and Applications*. New York, NY, USA: Springer-Verlag, 2013.
- [11] J.-S. Song, H. Rho, M. S. Jeong, J.-W. Ju, and I.-H. Lee, "Spatially resolved photoluminescence and Raman mapping of epitaxial GaN laterally overgrown on sapphire," *Phys. Rev. B*, vol. 81, pp. 233304-1-233304-4, Jun. 2010.
- [12] D. Kiliani, G. Micard, B. Steuer, B. Raabe, A. Herguth, and G. Hahn, "Minority charge carrier lifetime mapping of crystalline silicon wafers by time-resolved photoluminescence imaging," *J. Appl. Phys.*, vol. 110, no. 5, pp. 054508-1-054508-7, Sep. 2011.
- [13] G. Martínez-Criado, A. Cros, A. Cantarero, R. Dimitrov, O. Ambacher, and M. Stutzmann, "Optical characterization of Mg-doped GaN films grown by metalorganic chemical vapor phase deposition," *J. Appl. Phys.*, vol. 88, no. 6, pp. 3470-3478, 2000.
- [14] P. K. Kandaswamy, C. Bougerol, D. Jalabert, P. Ruterana, and E. Monroy, "Strain relaxation in short-period polar GaN/AlN superlattices," *J. Appl. Phys.*, vol. 106, no. 1, p. 013526, 2009.
- [15] M. Moseley, A. Allerman, M. Crawford, J. J. Wierer, M. Smith, and L. Biedermann, "Electrical current leakage and open-core threading dislocations in AlGaIn-based deep ultraviolet light-emitting diodes," *J. Appl. Phys.*, vol. 116, no. 5, p. 053104, 2014.
- [16] J.-H. Song *et al.*, "Role of photovoltaic effects on characterizing emission properties of InGaIn/GaN light emitting diodes," *Appl. Phys. Lett.*, vol. 95, no. 26, pp. 263503-1-263503-3, Dec. 2009.
- [17] J.-I. Shim and D.-S. Shin, "Influences of the p-GaN Growth temperature on the optoelectronic performances of GaN-based blue light-emitting diodes," *IEEE J. Quantum Electron.*, vol. 52, no. 4, Apr. 2016, Art. no. 3300208.
- [18] Bruker Inc., Madison, WI, USA. *LumiMap Electroluminescence System*, accessed on Aug. 31, 2016. [Online]. Available: https://www.bruker.com/fileadmin/user_upload/8-PDF-Docs/Electroluminescence/DS558-RevA2-LumiMap_Electroluminescence_System-Datasheet.pdf
- [19] S. J. Chang *et al.*, "Nitride-based flip-chip ITO LEDs," *IEEE Trans. Adv. Packag.*, vol. 28, no. 2, pp. 273-277, May 2005.
- [20] D. P. Han, J. I. Shim, and D. S. Shin, "Relationship between thermal and luminance distributions in high-power lateral GaN/InGaIn light-emitting diodes," *Electron. Lett.*, vol. 46, no. 6, pp. 437-438, Mar. 2010.
- [21] S. Y. Moon, J. H. Son, K. J. Choi, J.-L. Lee, and H. W. Jang, "Indium as an efficient ohmic contact to N-face n-GaN of GaN-based vertical light-emitting diodes," *Appl. Phys. Lett.*, vol. 99, no. 20, pp. 202106-1-202106-3, Nov. 2011.
- [22] H. Kim, J. Cho, Y. Park, and T.-Y. Seong, "Leakage current origins and passivation effect of GaN-based light emitting diodes fabricated with Ag p-contacts," *Appl. Phys. Lett.*, vol. 92, no. 9, pp. 092115-1-092115-3, Mar. 2008.
- [23] S. W. Lee *et al.*, "Origin of forward leakage current in GaN-based light-emitting devices," *Appl. Phys. Lett.*, vol. 89, no. 13, p. 132117, 2006.
- [24] S. Hwang and J. Shim, "A method for current spreading analysis and electrode pattern design in light-emitting diodes," *IEEE Trans. Electron Device*, vol. 55, no. 5, pp. 1123-1128, May 2008.
- [25] G. Verzellesi *et al.*, "Efficiency droop in InGaIn/GaN blue light-emitting diodes: Physical mechanisms and remedies," *J. Appl. Phys.*, vol. 114, no. 7, p. 071101, 2013.
- [26] H.-Y. Ryu, H.-S. Kim, and J.-I. Shim, "Rate equation analysis of efficiency droop in InGaIn light-emitting diodes," *Appl. Phys. Lett.*, vol. 95, no. 8, p. 081114, 2009.



Jong-In Shim (M'95) was born in Kangreung, South Korea, in 1960. He received the B.S. and M.S. degrees in electronics from Seoul National University, Seoul, South Korea, in 1983 and 1985, respectively, and the Ph.D. degree in physical electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 1992.

From 1985 to 1988, he was with the Electronics and Telecommunication Research Institute, Daejeon, South Korea, where he was involved in InGaAsP-InP semiconductor lasers. From 1992 to 1994, he joined the Optoelectronics Research Laboratory, NEC, Tsukuba, Japan, where he was involved in research on tunability and coherence of semiconductor lasers and their fabrication technology by the selective MOVPE growth. In 1994, he joined the Department of Electronic and Computer Engineering, Hanyang University, South Korea. From 2002 to 2003, he was a Visiting Researcher with the University of California at Santa Barbara, Santa Barbara, CA, USA. He is currently a Professor and leads the Semiconductor Photonics Laboratory with Hanyang University. He has authored or co-authored over 100 papers in international journals and one book. He holds 30 patents. His current research interests include optoelectronic devices for optical communication as well as solid-state lighting.

Dr. Shim has served as the General Secretary of the Optical Society of Korea and the President of the Society of LED and Solid-State Lighting, South Korea.



Dong-Pyo Han was born in Seoul, South Korea, in 1981. He received the B.S. and Ph.D. degrees in electrical engineering from Hanyang University, South Korea, in 2008 and 2015, respectively. His main research interests include characterizing and understanding semiconductor light-emitting diodes and their physical mechanisms.



Dong-Soo Shin (S'00-M'01) received the B.S. degree from Yonsei University, Seoul, South Korea, and the M.S. and Ph.D. degrees from the University of California at San Diego, La Jolla, CA, USA, in 1993, 1996, and 2001, respectively, all in physics.

From 2001 to 2003, he was a Member of Technical Staff with Agere Systems (formerly Lucent Technologies Microelectronics), Breinigsville, PA, USA, where he was involved in research and development on high-speed electroabsorption-modulated lasers and uncooled lasers. From 2003 to 2004, he was a Senior Scientist with Spatialight, Novato, CA, USA, where he was involved in microdisplays development. In 2004, he joined the Department of Applied Physics, Hanyang University, Ansan, South Korea. From 2010 to 2011, he was a Visiting Associate Research Scientist with the University of California at San Diego, where he was involved in the research of modified uni-traveling-carrier waveguide photodiodes with high power and high linearity. He is currently a Professor with Hanyang University. His main research interests include optoelectronic devices, microwave photonics, and device physics.

Dr. Shin is a member of the Optical Society of Korea and the Society of LED and Solid-State Lighting, South Korea.