Lab. 02

Logic Design Lab.

Spring 2023

Prof. ChangGun Lee

(cglee@snu.ac.kr)

TA. Seonghyeon Park

TA. Jihwan Kim

TA. Hoyong Lee

(rubis.ld.ta@gmail.com)

Contents

- **Announcement**
- **Two-bit comparator**
- **Xilinx ISE**
- **Universal Board**
- **Lab**

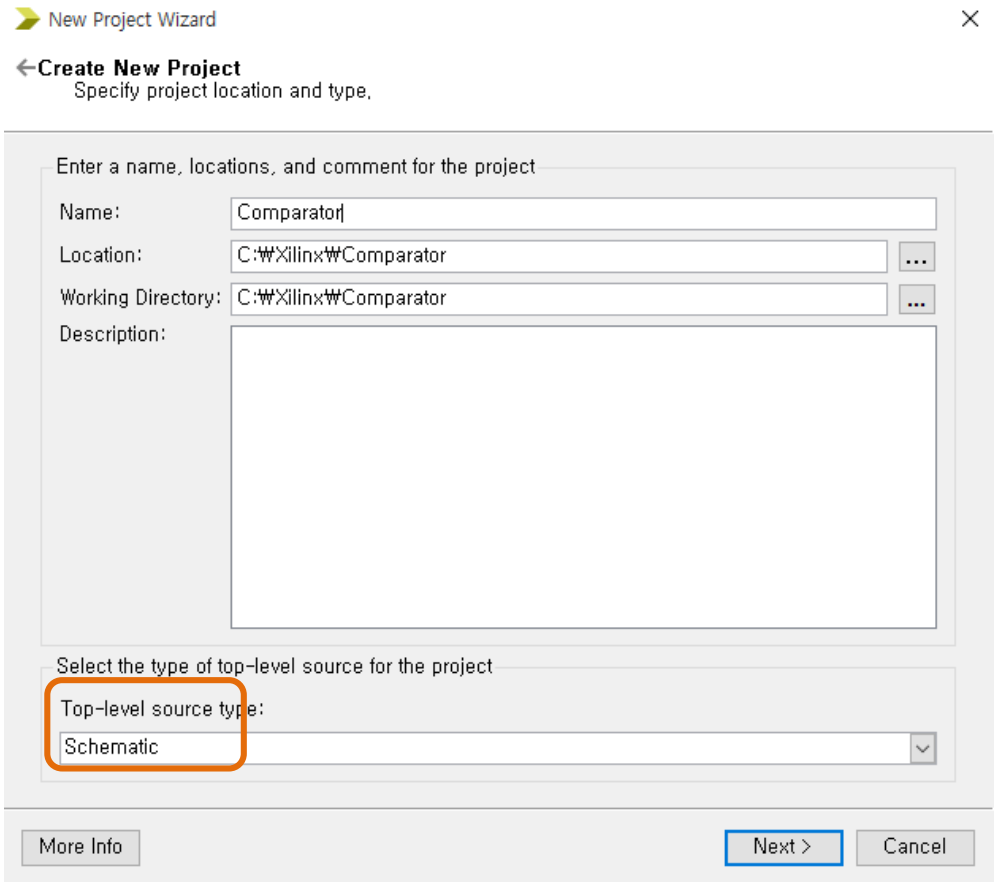
Xilinx ISE

Xilinx ISE Design Suite

- Integrated Synthesis Environment(ISE)
- Release 14.7, 2013
- Features
  - Synthesis(compile) and analysis of HDL[1)] designs.
  - Timing analysis, RTL diagram
  - Xilinx FPGA programmer

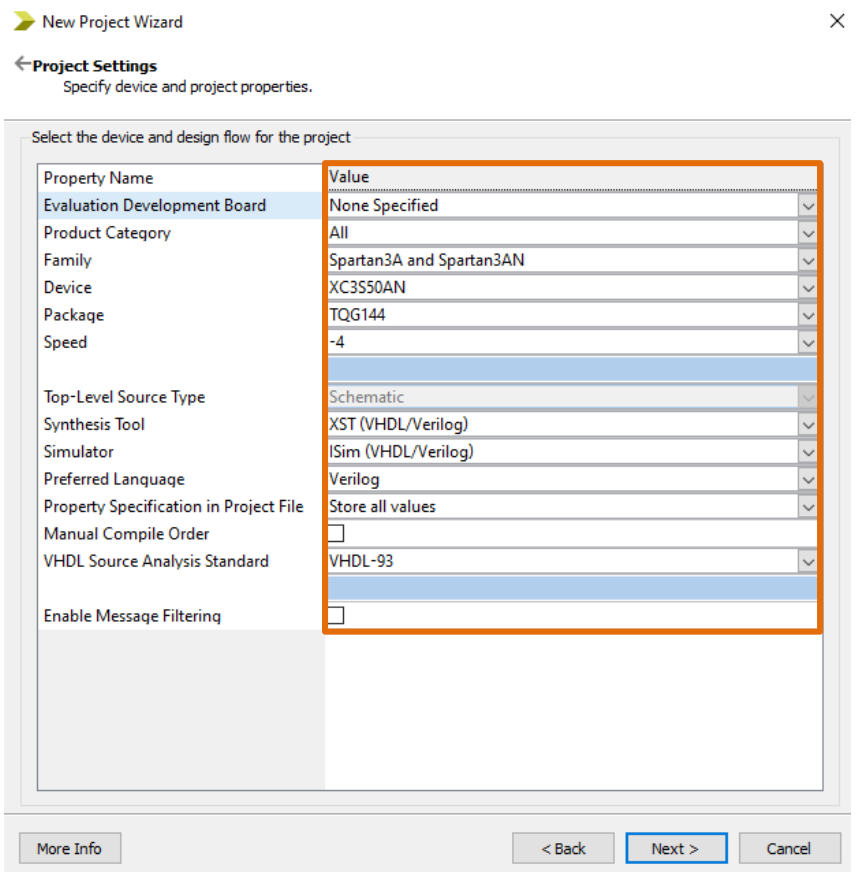
1) HDL: Hardware Description Language

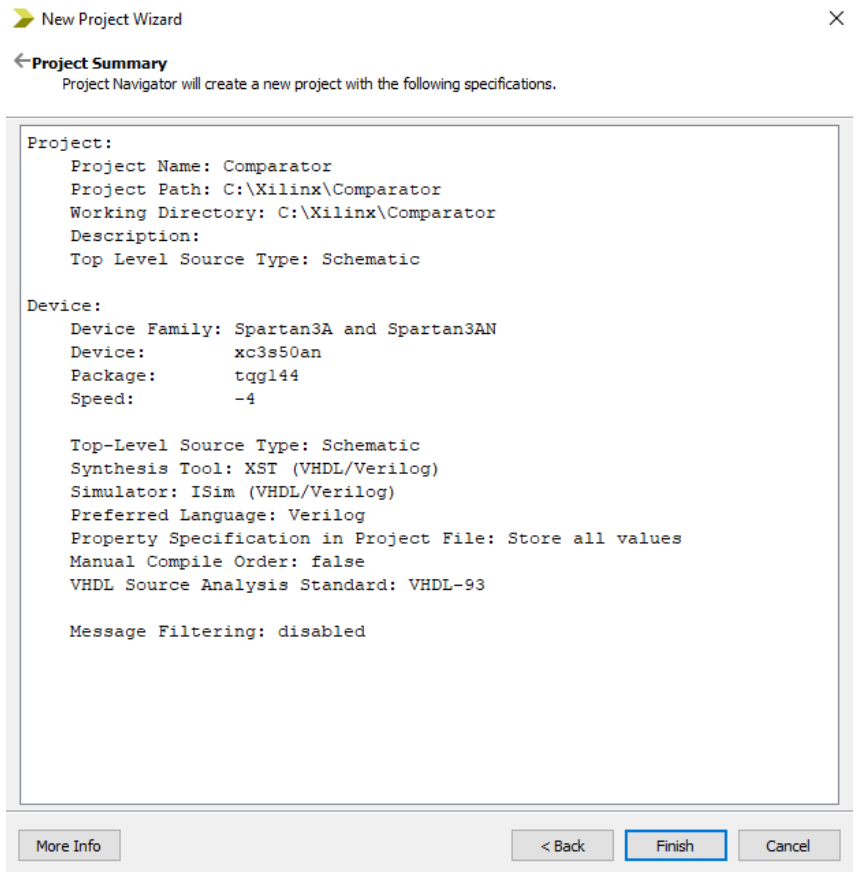
Creating New Project



- Select **File -> New Project**
- Specify **Name**, **Location**, **Working Directory**. Select **Top-level source type as Schematic.**

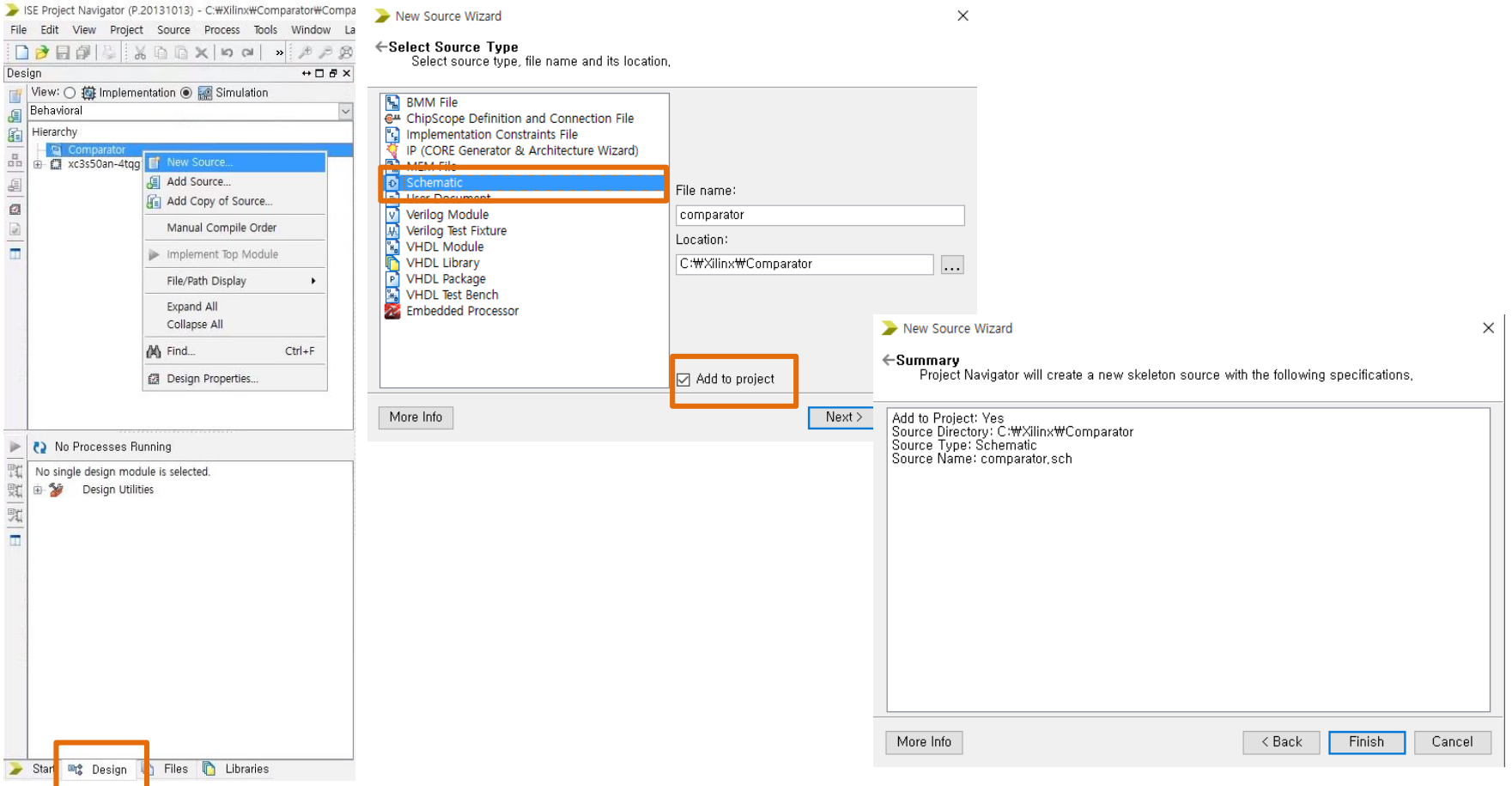
Project Settings





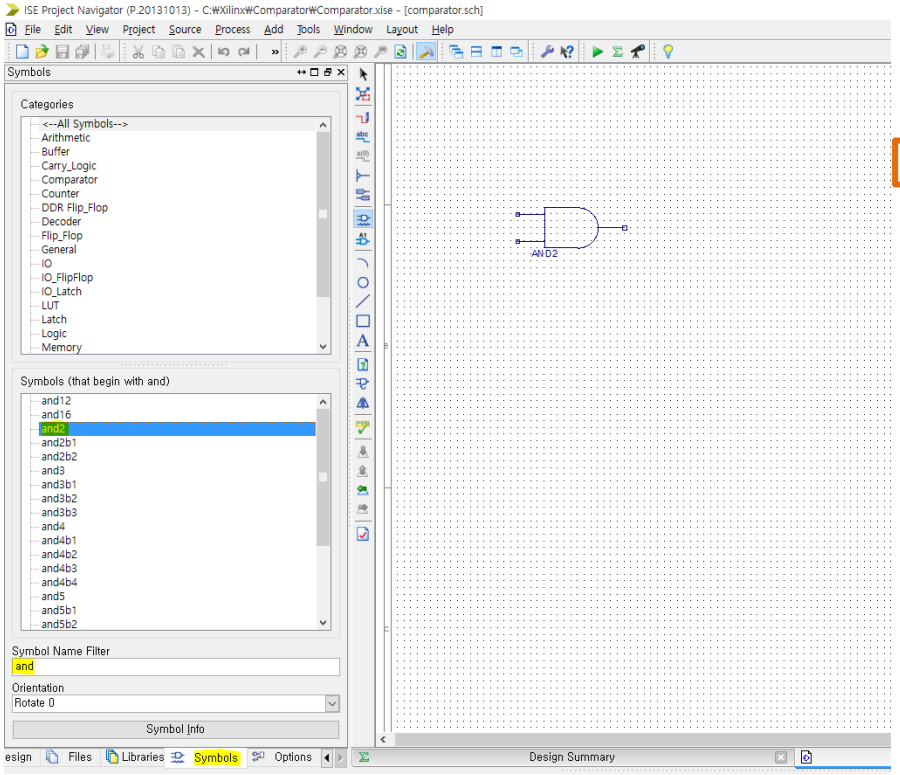
- Set **Project Settings** as **above**
- Click **Next → Finish**

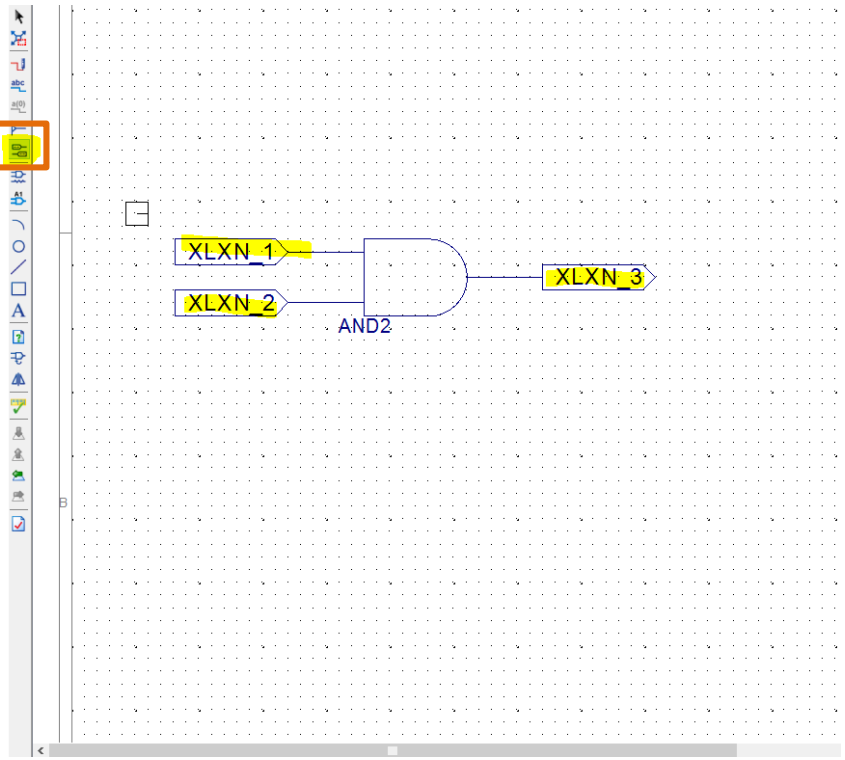
Creating Schematic



- Right-Click anywhere in Hierarchy in **Design tab**, select New Source.
- New Source Wizard window appears. Select Source Type window, select **Schematic** and type the File name. Ensure **Add to project is checked.**

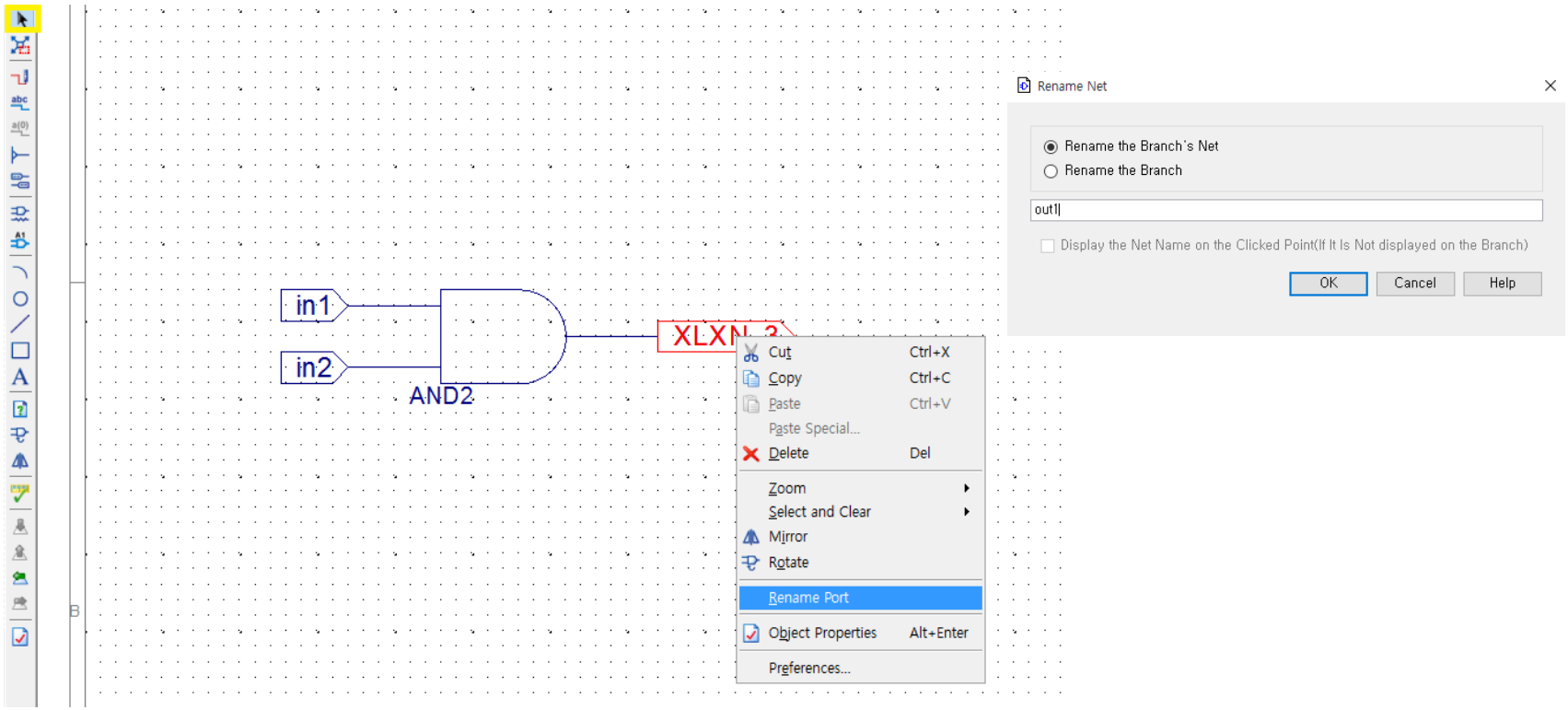
2-input-AND gate circuit (1)





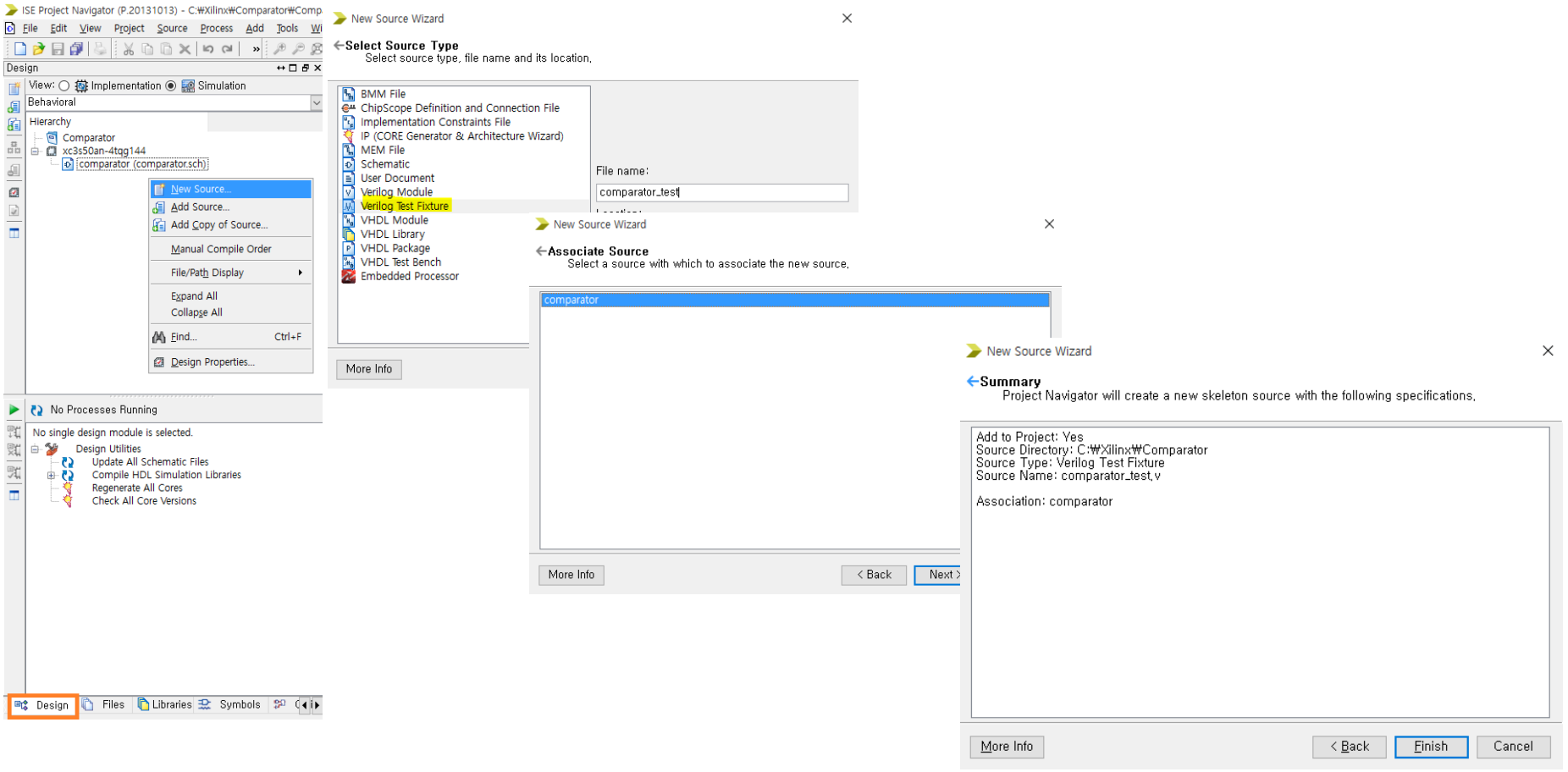
- In Symbols tab, type "and" under Symbol Name Filter.
- Select and2 under Symbols, and place it on board.
- Click **I/O Marker button** and you can add input/output markers to your circuit.

2-input-AND gate circuit (2)



- Change the names of input/output symbols.
- Save to apply changes

Creating Verilog Test Bench



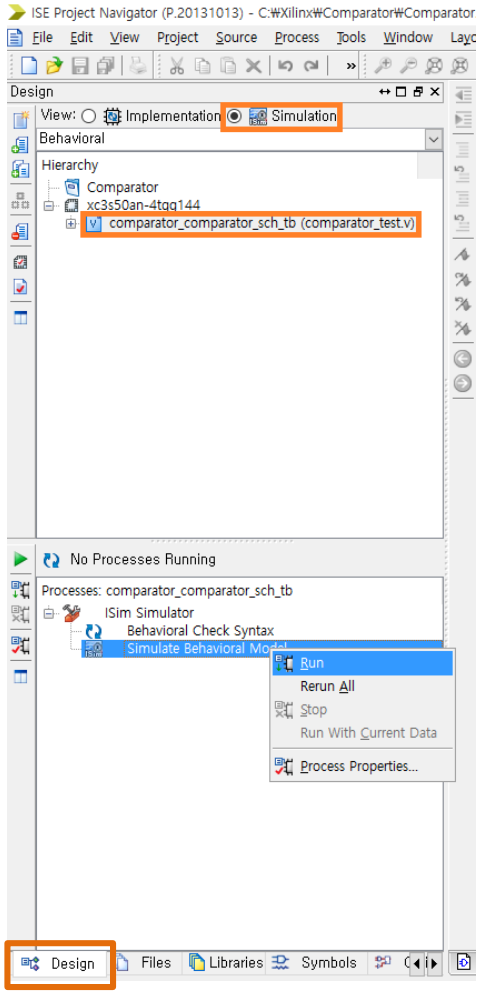
- Select New Source by right clicking inside **Design tab**.
- Select Verilog Test Bench. Type the file name as above.

Schematic Simulation Code

```
1  // Verilog test fixture created from schematic
2
3  `timescale 1ns / 1ps
4
5  module comparator_comparator_sch_tb();
6
7  // Inputs
8     reg in1;
9     reg in2;
10
11 // Output
12    wire out1;
13
14 // Bidirs
15
16 // Instantiate the UUT
17    comparator UUT (
18       .in1(in1),
19       .in2(in2),
20       .out1(out1)
21    );
22 // Initialize Inputs
23
24    initial begin
25       in1 = 0;
26       in2 = 0;
27       #100;
28
29       in1 = 0;
30       in2 = 1;
31       #100;
32
33       in1 = 1;
34       in2 = 0;
35       #100;
36
37       in1 = 1;
38       in2 = 1;
39    end
40 endmodule
41
```

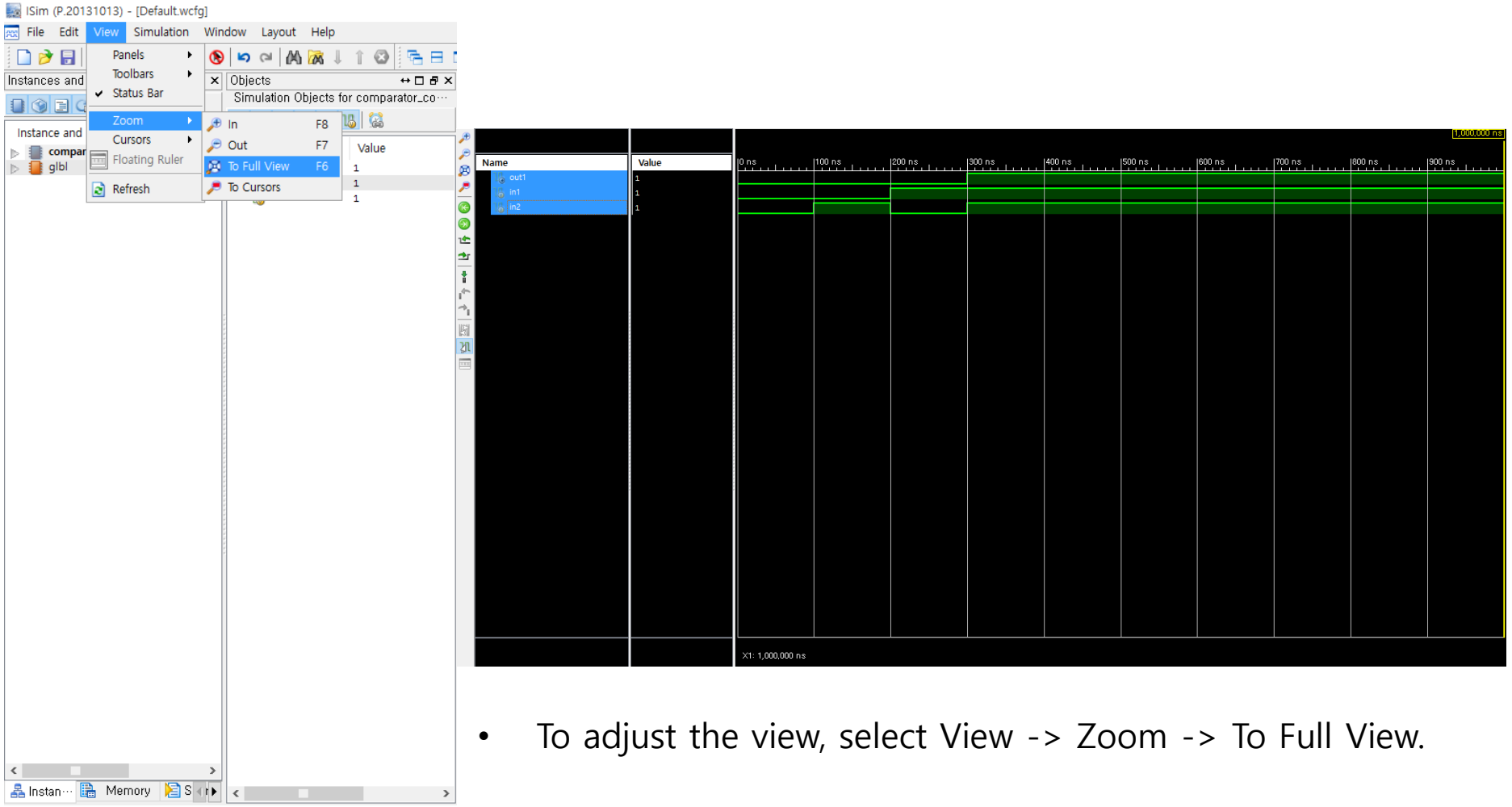
Wait for 100 ns

Simulate Behavioral Model



- Save the project
- Ensure that **Design tab** is selected, View is set to **Simulation**, and your **simulation source code is clicked**
- Double click Behavioral Check Syntax for syntax check
- Double click Simulate Behavioral Model

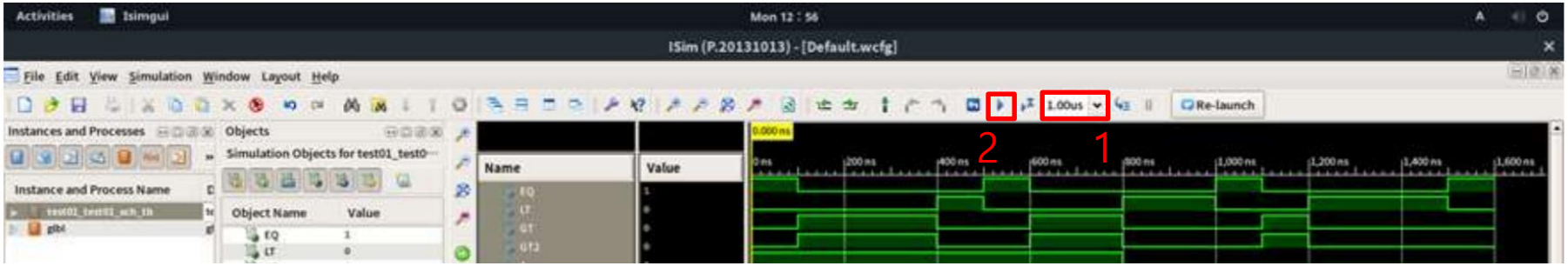
Simulation Result



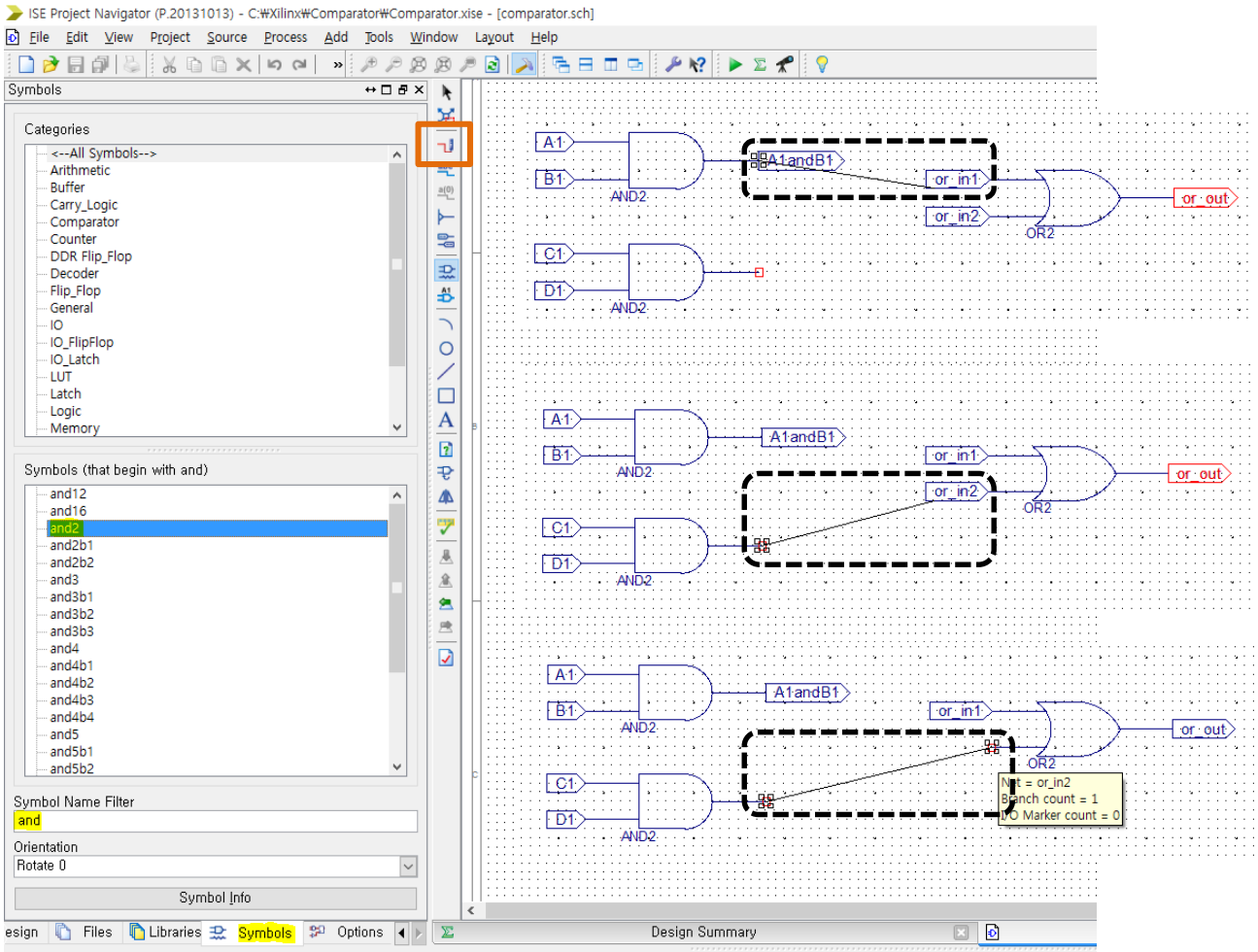
- To adjust the view, select View -> Zoom -> To Full View.

Tips : Adjust Simulation Time

- You can adjust simulation time (default : 1 us)



Tips: Connecting multiple gates



- When connecting multiple gates using **'Add Wire' button**, make sure that both two ends don't have I/O markers

Today's lab

- Implement 2-bit comparator LT, EQ, GT using Xilinx ISE Schematic. Simulate its behavior using Xilinx test bench.
- You may need to adjust simulation time to see every result.
- You should add result in report

Some problems with Xilinx

- Xilinx ISE program generates log file *.wdb
  - Sometimes, the file size grows hugely.
  - It makes disk size full, and the disk often fails to boot.

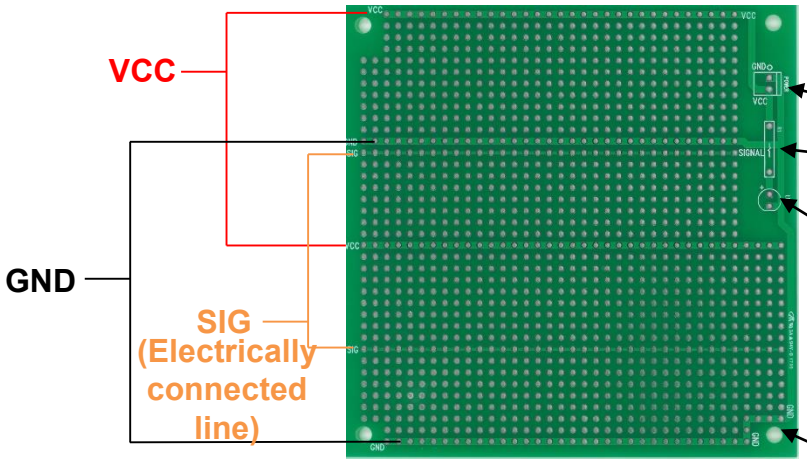
- Don't open multiple simulation windows.
- Before terminating Xilinx ISE program …
  - Exit your simulation window.
  - Clean up your temp file with Project > Cleanup Project Files

```
ohasno@310-2-26:~/Comparator$ ls -al
total 156
drwxr-xr-x  6 ohasno cseusers  4096 Mar 27 15:43 .
drwx------ 19 ohasno cseusers  4096 Mar 27 15:35 ..
-rw-r--r--  1 ohasno cseusers   125 Mar 27 15:43 comparator_comparator_sch_tb_beh.prj
-rwxr-xr-x  1 ohasno cseusers 21792 Mar 27 15:43 comparator_comparator_sch_tb_isim_beh.exe
-rw-r--r--  1 ohasno cseusers  4709 Mar 27 15:43 comparator_comparator_sch_tb_isim_beh.wdb
-rw-r--r--  1 ohasno cseusers  4359 Mar 27 15:43 Comparator.gise
-rw-r--r--  1 ohasno cseusers    18 Mar 27 15:39 comparator.jhd
-rw-r--r--  1 ohasno cseusers  1908 Mar 27 15:39 comparator.sch
-rw-r--r--  1 ohasno cseusers     0 Mar 27 15:39 comparator.schlog
```

로그 파일

Universal Board

Custom-Made Universal Board



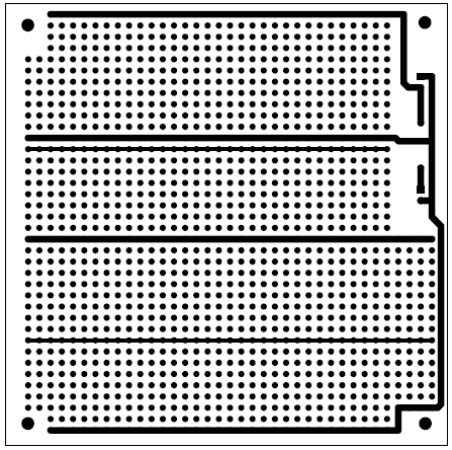
2-Pin Power Connector

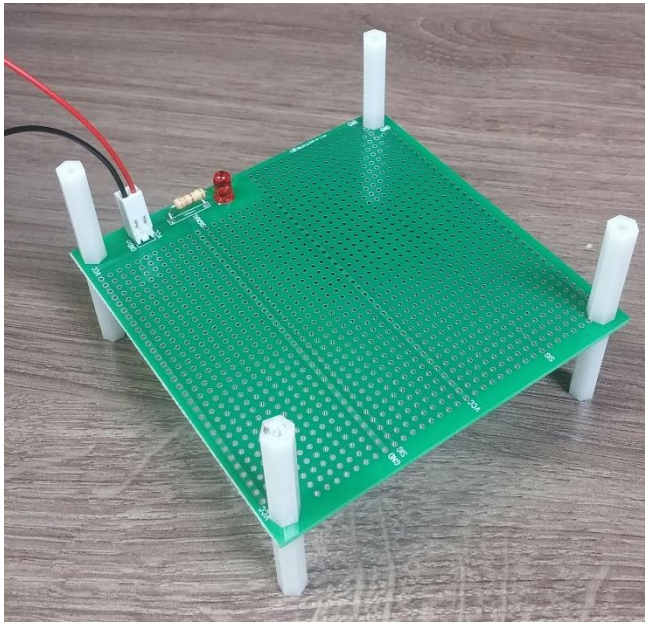
Resistor (~330Ω)

LED

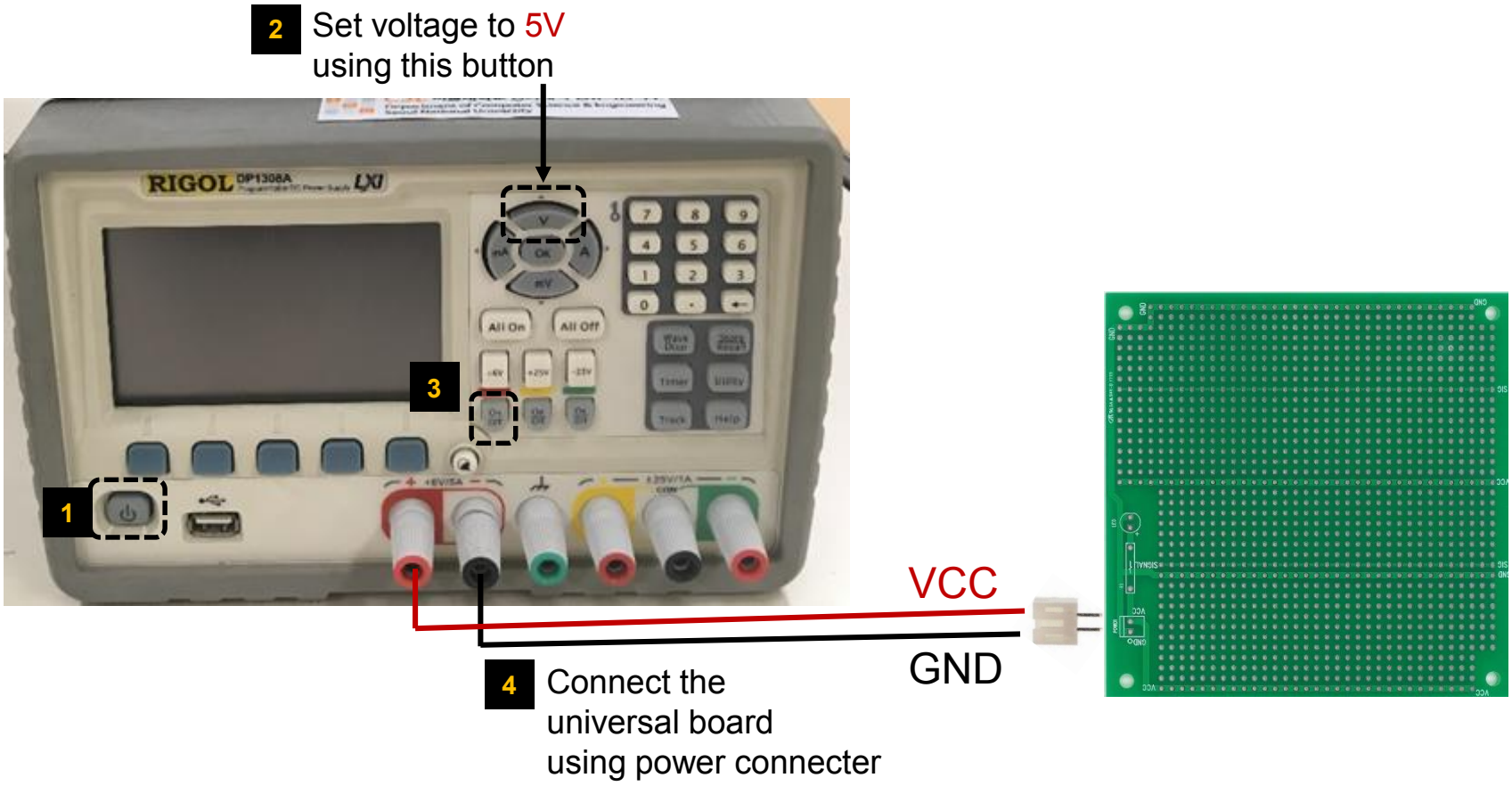
(turn on when power is connected)

PCB Support Plastic



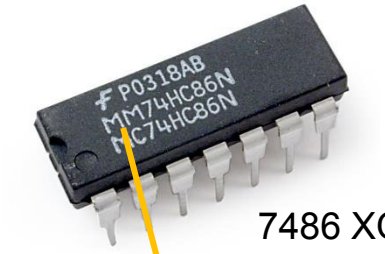


Turning it on using power supply

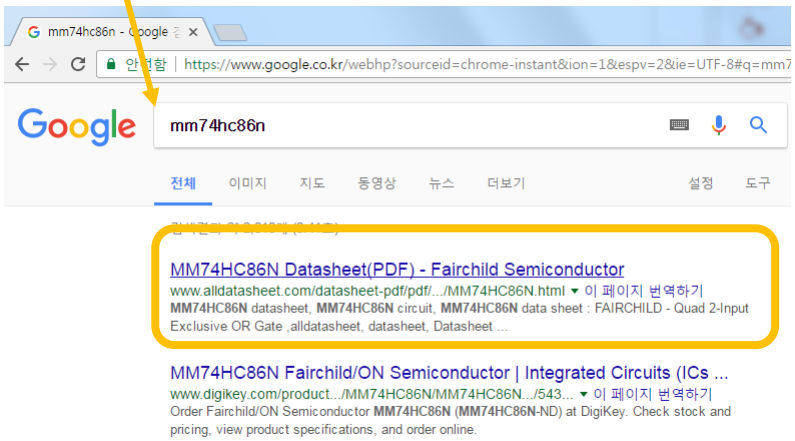


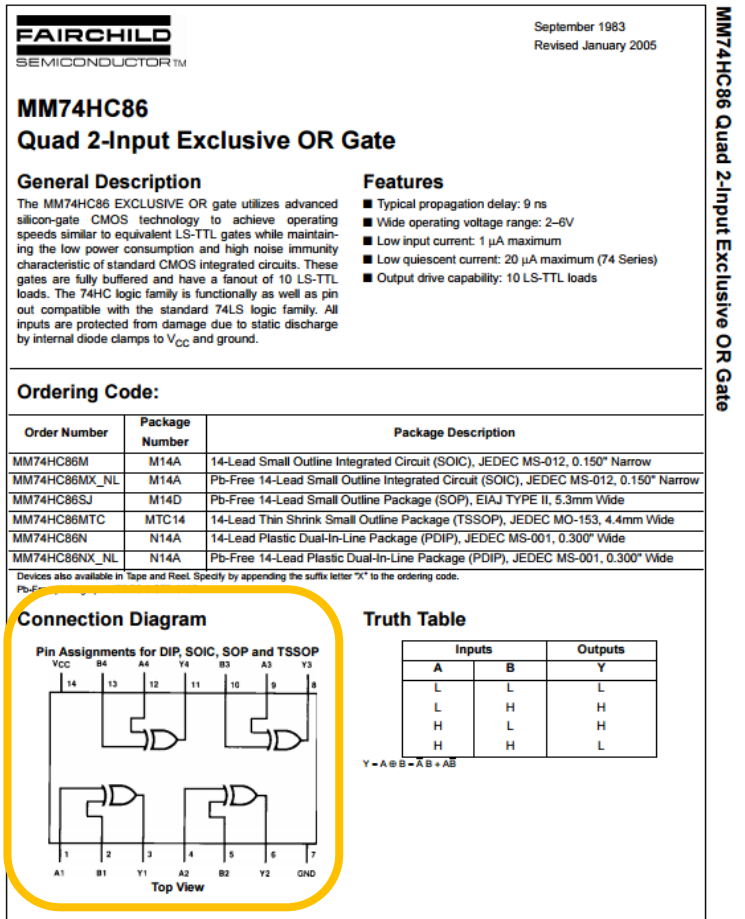
Tips: Look up the datasheet!

- NEVER trust the sorted device boxes… *Always check the product name* to confirm that you picked the right one.
- Always look up the datasheet online, double check its pin mapping.



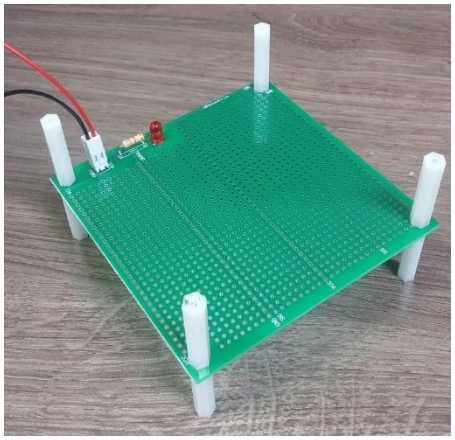
7486 XOR gate



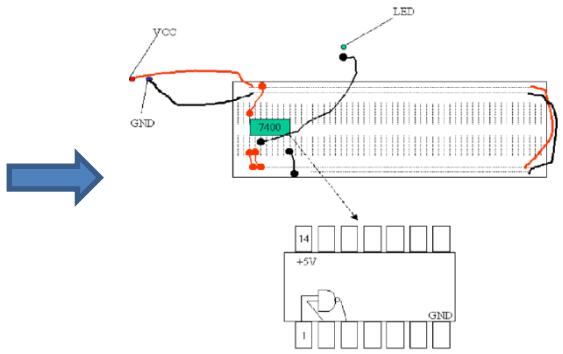


Insight

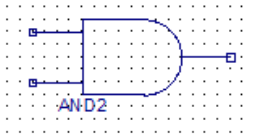
- Xilinx to the rescue!
  - Thanks to Xilinx, you don't need to solder or use a breadboard when implementing the circuit.
  - In the past, without Xilinx,
    hardware design was much more challenging than now.



Soldering



Breadboard



Xilinx

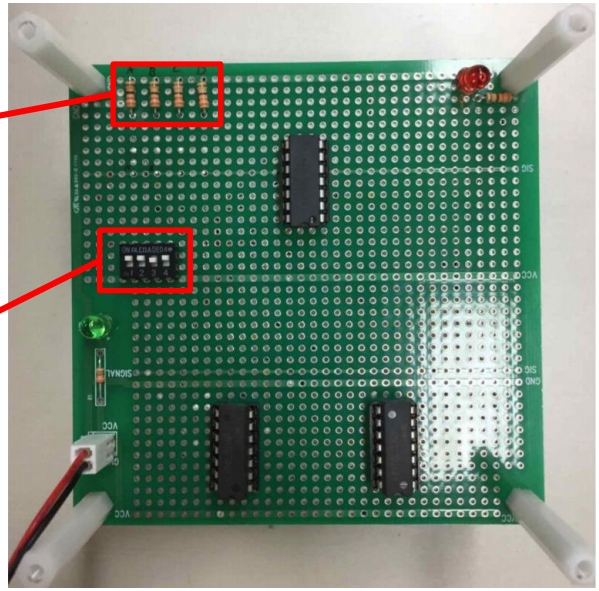
Homework

1. [TEAM]

Implement 2-bit comparator GT logic on the universal board, using DIP switch and primitive logic gates(INV, AND, OR, XOR, NAND…).
Try your best to minimize the number of logic gates/chips used.

Pull-down Resistor

DIP Switch (For 4 input)

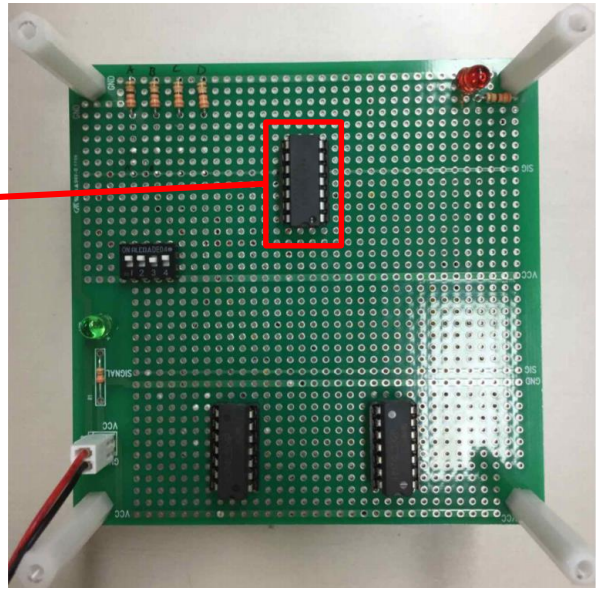


Homework

Tips

- You should solder chip socket, not on gate directly!
- Remove the sheath from the wire and use it.

Chip Socket
+
Gate



Homework

2. [Individual]

Draw a circuit diagram for the below formula using ONLY NOR and NOT gates. You can draw it by hand or using any of a computer program.

- Y = A(B+CD)

3. [Individual]

Y = AB + ABC + A'B + AB'C

(1) Make a truth table

(2) Minimize # of operators

(3) Draw a circuit diagram

Homework

- Write a report
  - Either in Korean or in English
  - Your report should include:
    - Lab result (Not only homework)
    - Through discussion
    - Homework (if there is any)
  - # of pages doesn't matter
  - Documents should be submitted as PDF file.
  - **Due :**
    Class 001 – April, 17th (Before class begin at 7:00pm)
    Class 002 – April, 18th (Before class begin at 7:00pm)
    Class 003 – April, 20th (Before class begin at 7:00pm)