

# Lab. 06

Logic Design Lab.

Spring 2023

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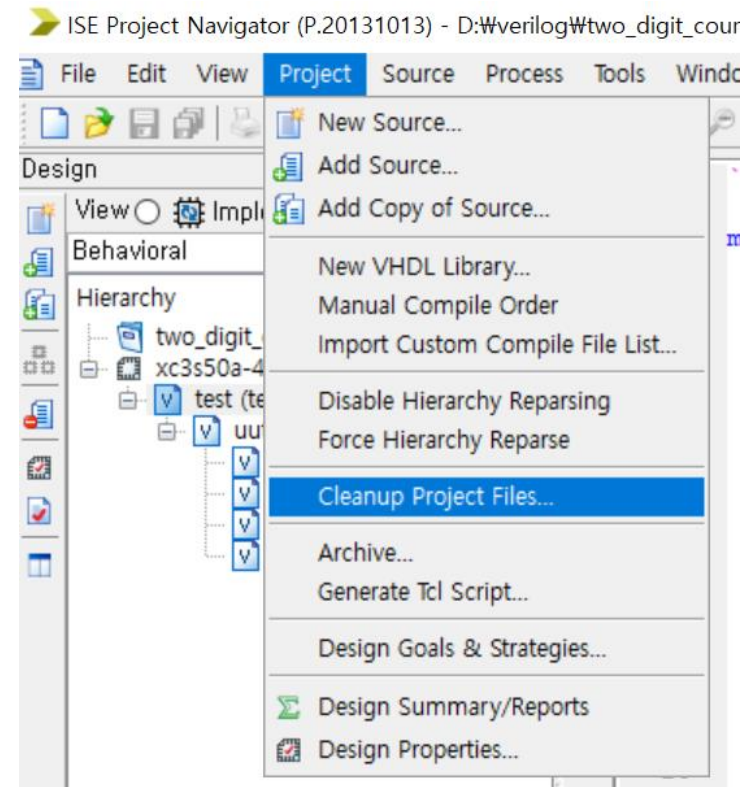
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# Announcement

- Do not open multiple simulation window
- Before exiting the Xilinx ISE program, take the following two steps:
  - Close the simulation window
  - Project → Cleanup Project Files...
- There is an issue where the log file becomes abnormally large in certain situations. In this case, the log file runs out of disk space and cannot use the computer normally.



# Sequential logic

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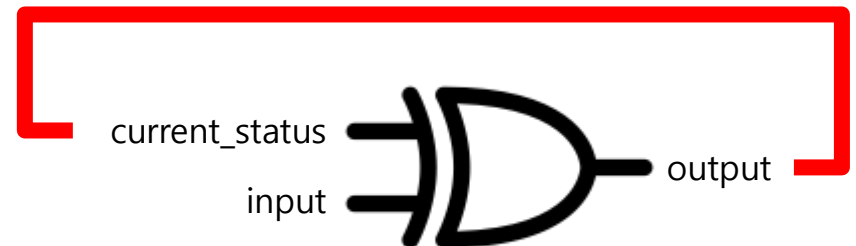
# Sequential logic (1)

- Output is determined by both of **current state** and **input**
- To save current state, **feedback** is used to implement storage

## Example > sequential logic

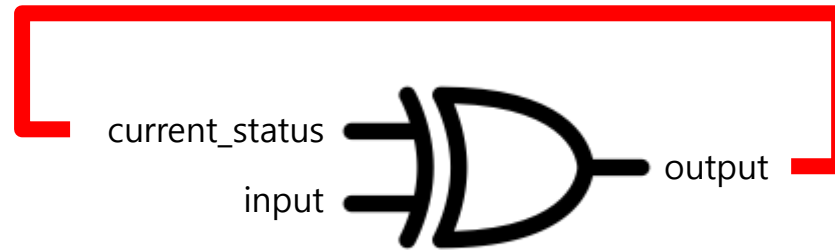
If **input == 0** then **hold current status**, else if **input == 1** then **toggle current status**.  
**Output is same as current status.**

current_status	input	output
0	0	0
0	1	1
1	0	1
1	1	0



# Sequential logic (2)

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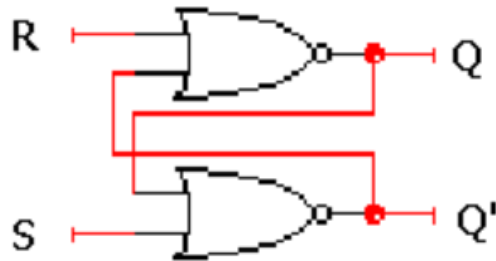


## Taxonomy ...

- Never mind, always work  
→ Latch
- Work only when it is enabled  
→ Gated latch
- Work only when it is edge triggered  
→ Flip-flop

# R-S Latch

- R-S latch is a **1 bit memory** with cross-coupled gates.



S	R	Q
0	0	hold
0	1	0
1	0	1
1	1	unstable

S	R	Q(t)	Q(t+Δ)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

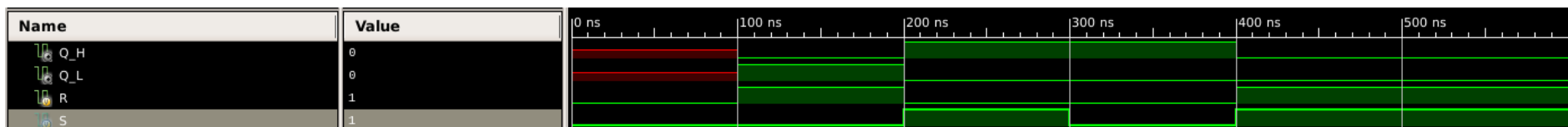
hold

reset

set

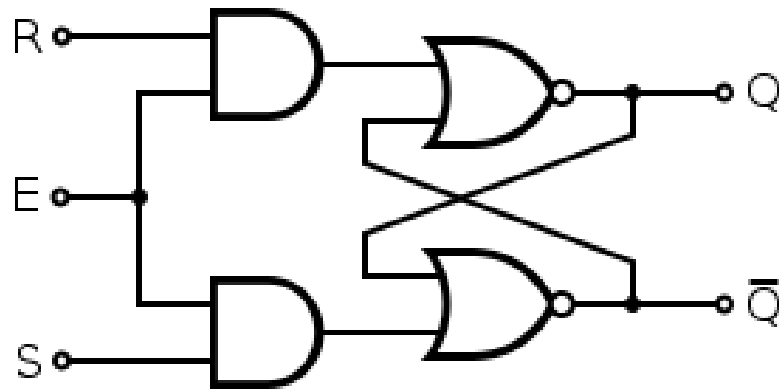
not allowed

Q	RS	00	01	11	10
0			1	X	
1		1	1	X	

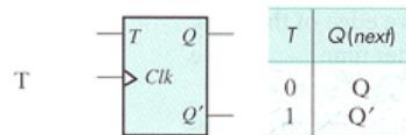
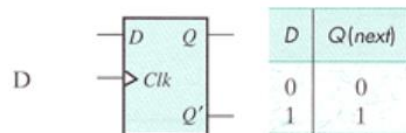
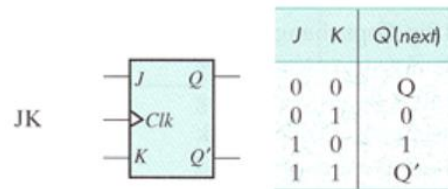
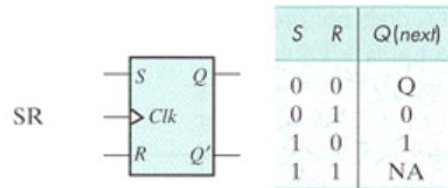


# Gated R-S Latch

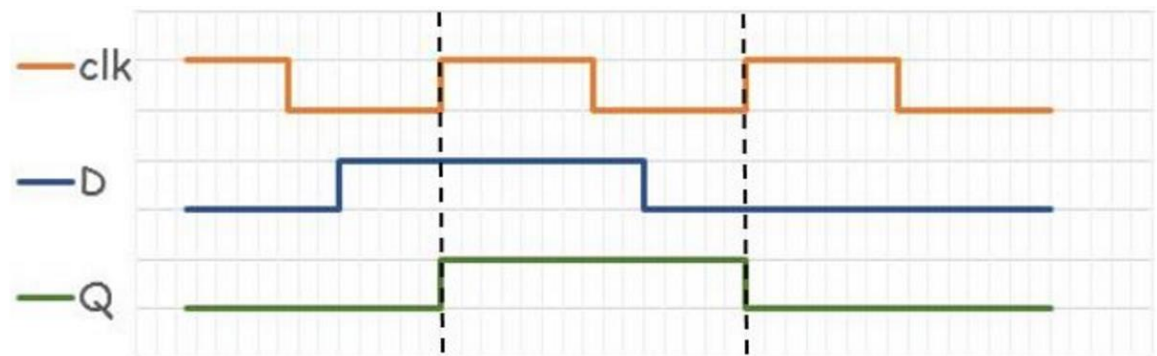
- R and S(inputs) matter only when E(enable) = 1
- Otherwise, hold current state



# Flip-Flops



D FlipFlop





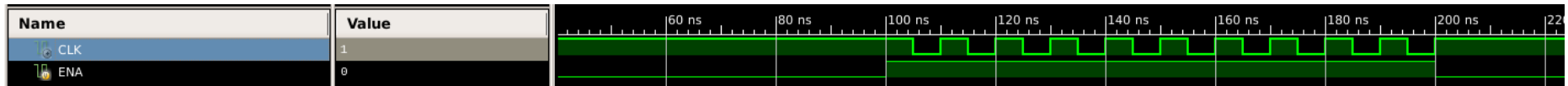
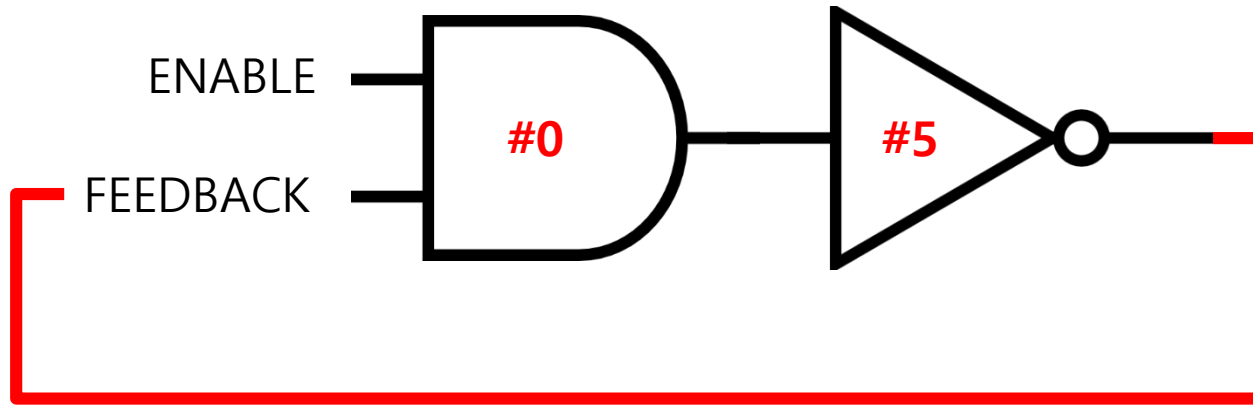
# Clock

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- Provide **timing** to sequential logic (ex. Flip-Flop)

74LS74 DatasheetCEG 360/560 - EE 451/651 Section I - 74

# Simple Oscillator



How to implement gate delay ?

**Example >**

```
wire tmp;  
assign #5 tmp = tmp & 1;
```

# Homework

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# Homework

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1. Implement the following in Verilog and simulate the behavior.

(1) a R-S latch

(2) a gated R-S latch using (1)

(3) a Simple Oscillator(the clock period is free)

(4) a R-S Flip-Flop(Edge-triggered) using above modules

Include Source codes(modules) and simulation result.

Explain that the modules you implement work well.

No need to attach testbench code.

2. (Optional) Explain the different Flipflops(SR, D, JK, etc.) and how they differ from each other.

# Report

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- Write a report
  - Either in Korean or in English
  - **Your report should include**
    - discussion
    - Homework (if there is any)
  - # of pages doesn't matter
  - Documents should be submitted as PDF file(**less than 25Mb**)
  - **Attach source code and waveform screenshot**
  - Due :
    - Class 001 - May, 22<sup>th</sup> (Before class begin at 7:00pm)
    - Class 002 - May, 23<sup>th</sup> (Before class begin at 7:00pm)
    - Class 003 - May, 25<sup>th</sup> (Before class begin at 7:00pm)