

## Lab02 Report

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### 1. Lab

Result:

#### (i) Minimization

LT comparator:

$$\begin{aligned}
 & A'B'C'D + A'B'CD' + A'B'CD + A'BCD' + A'BCD + AB'CD \\
 & = A'B'C'D + A'B'C + A'BC + AB'CD \\
 & = A'C + A'B'C'D + AB'CD \\
 & = A'C + B'D(A'C + AC) \\
 & = A'C + B'D(A \text{ XNOR } C)
 \end{aligned}$$

EQ comparator:

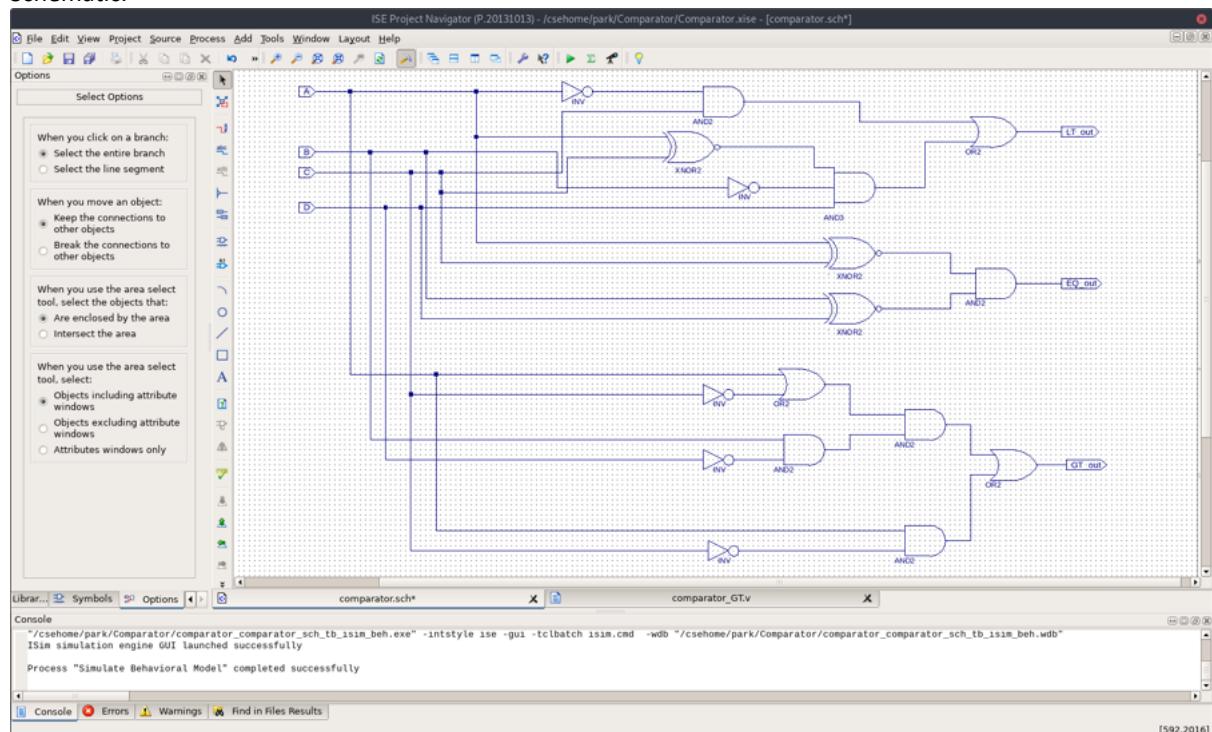
$$\begin{aligned}
 & A'B'C'D' + A'B'CD + ABCD + AB'CD' \\
 & = (A'C' + AC)B'D' + (A'C' + AC)BD \\
 & = (A'C' + AC)(B'D' + BD) \\
 & = (A \text{ XNOR } C) \cdot (B \text{ XNOR } D)
 \end{aligned}$$

GT comparator:

$$\begin{aligned}
 & A'BC'D' + AB'C'D' + AB'C'D + ABC'D' + ABC'D + ABCD' \\
 & = A'BC'D' + (AB'C'D' + AB'C'D) + (ABC'D' + ABC'D) + ABCD' + ABC'D' + ABC'D \\
 & = (A'BC'D' + ABC'D') + AB'C' + ABC' + (ABCD' + ABC'D') \\
 & = BC'D' + AC' + ABD' \\
 & = BD'(A + C') + AC' \\
 & = ((A + C') \cdot (B \cdot D')) + (A \cdot C')
 \end{aligned}$$

#### (ii) Schematic

Using these minimizations, we implemented the schematic of 2 bit-comparators LT, EQ and GT using Xilinx ISE Schematic.



#### (iii) Simulation code

And then we used the following schematic simulation code, utilising the inputs A, B, C, D and the outputs LT, EQ, and GT. We gave all possible 16 input combinations, each at a 100ns interval.

ISE Project Navigator (P\_2013l013) - /csehome/park/Comparator/Comparator.xise - [comparator\_GT.v]

```

1 // Verilog test fixture created from schematic /csehome/park/Comparator/comparator.sch - Thu Apr 13 20:24:13 2023
2
3 `timescale 1ns / 1ps
4
5 module comparator_comparator_sch_tb();
6
7 // Inputs
8 reg A;
9 reg B;
10 reg C;
11 reg D;
12
13 // Output
14 wire EQ_out;
15 wire LT_out;
16 wire GT_out;
17
18 // Bidirs
19
20 // Instantiate the UUT
21 comparator UUT (
22   .EQ_out(EQ_out),
23   .A(A),
24   .B(B),
25   .D(D),
26   .LT_out(LT_out),
27   .C(C),
28   .GT_out(GT_out)
29 );
30 // Initialize Inputs
31 initial begin
32   A = 0;

```

Start Design Files

comparator.sch\* comparator\_GT.v

Console

Process "Simulate Behavioral Model" completed successfully

Started : "Launching ISE Text Editor to edit comparator\_GT.v".

Console Errors Warnings Find in Files Results

In 5 Col 1 Verilog

ISE Project Navigator

```

1 // Verilog test fixture created from schematic /csehome/park/Comparator/comparator.sch - Thu Apr 13 20:24:13 2023
2
3 `timescale 1ns / 1ps
4
5 module comparator_comparator_sch_tb();
6
7 // Inputs
8 reg A;
9 reg B;
10 reg C;
11 reg D;
12
13 // Output
14 wire EQ_out;
15 wire LT_out;
16 wire GT_out;
17
18 // Bidirs
19
20 // Instantiate the UUT
21 comparator UUT (
22   .EQ_out(EQ_out),
23   .A(A),
24   .B(B),
25   .D(D),
26   .LT_out(LT_out),
27   .C(C),
28   .GT_out(GT_out)
29 );
30 // Initialize Inputs
31 initial begin
32   A = 0;
33   B = 0;
34   C = 0;
35   D = 0;
36   #100;
37
38   A = 0;
39   B = 0;
40   C = 0;
41   D = 1;
42   #100;
43
44   A = 0;
45   B = 0;
46   C = 1;
47   D = 0;
48   #100;
49
50   A = 0;
51   B = 0;
52   C = 1;
53   D = 1;
54   #100;
55
56   A = 0;
57   B = 1;
58   C = 0;
59   D = 0;
60   #100;
61
62   A = 0;
63   B = 1;
64   C = 0;
65   D = 1;
66   #100;
67
68   A = 0;
69   B = 1;
70   C = 1;
71   D = 0;
72   #100;
73
74   A = 0;
75   B = 1;
76   C = 1;
77   D = 1;
78   #100;
79
80   A = 1;
81   B = 0;
82   C = 0;
83   D = 0;
84   #100;
85
86   A = 1;
87   B = 0;
88   C = 0;
89   D = 1;
90   #100;
91
92   A = 1;
93   B = 0;
94   C = 1;
95   D = 0;
96   #100;
97
98   A = 1;
99   B = 0;
100  C = 1;
101  D = 1;
102  #100;
103
104  A = 1;
105  B = 1;
106  C = 0;
107  D = 0;
108  #100;
109
110  A = 1;
111  B = 1;
112  C = 0;
113  D = 1;
114  #100;
115
116  A = 1;
117  B = 1;
118  C = 1;
119  D = 0;
120  #100;
121
122  A = 1;
123  B = 1;
124  C = 1;
125  D = 1;
126  #100;
127
128 endmodule

```

ISE Project Navigator

Design View Implementational Simulation

Behavioral Hierarchy

Comparator xc3s50an-4tg144 comparator\_comparator.sch UUT - comparator (comp)

No Processes Running

Processes: comparator\_comparator, iSim Simulator, Behavioral Check Syn..., Simulate Behavioral...

ISE Project Navigator

Design View Implementational Simulation

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ISE Project Navigator

Design View Implementational Simulation

Behavioral Hierarchy

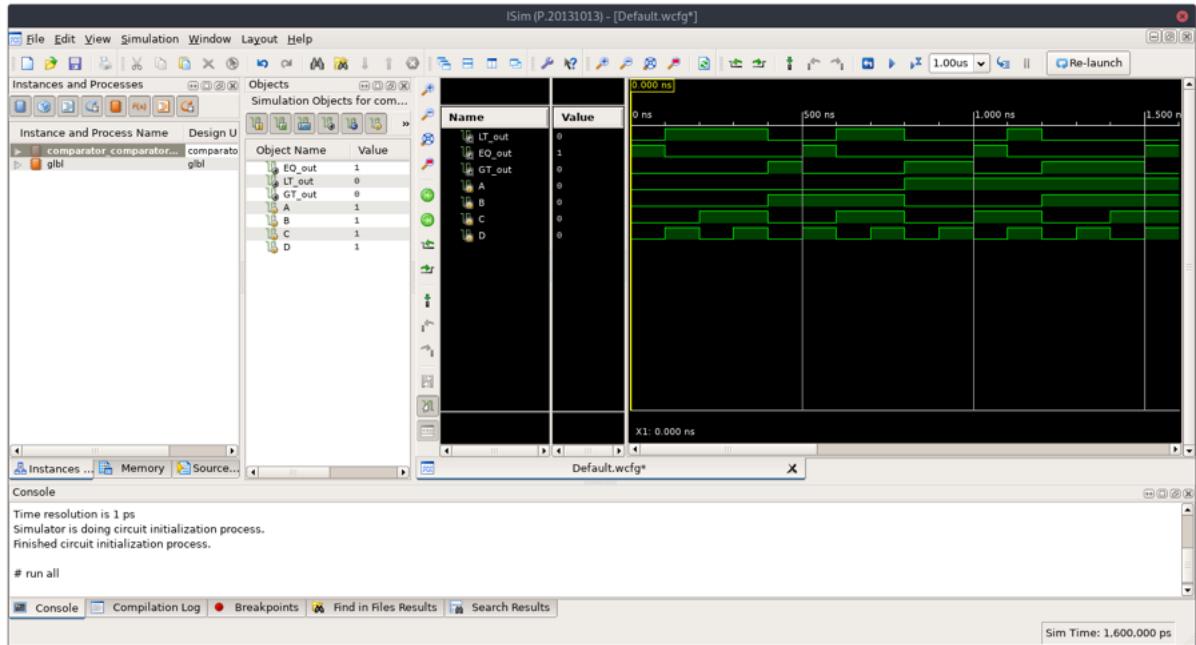
Comparator xc3s50an-4tg144 comparator\_comparator.sch UUT - comparator (comp)

No Processes Running

Processes: comparator\_comparator, iSim Simulator, Behavioral Check Syn..., Simulate Behavioral...

(iii) Simulation result:

The simulation result was as follows:



Discussion:

The expected output of the 2-bit comparators are as follows:

Input				Output		
A	B	C	D	LT	EQ	GT
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Comparing each of the 16 pulses to the corresponding entry to this truth table, we were able to check that all 3 comparators are correctly implemented.

## 2. Homework 1

Result:

(1) Implementing GT logic on universal board

We used the implementation from the schematic designed and tested on Xilinx.

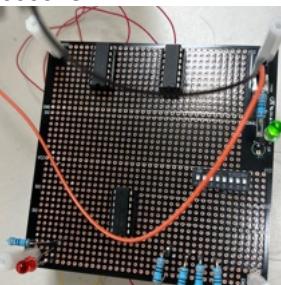
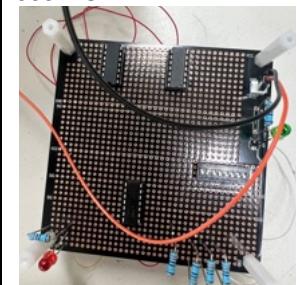
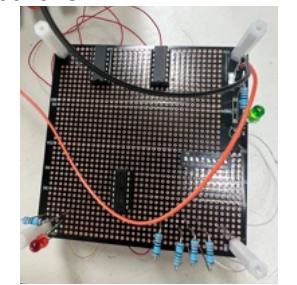
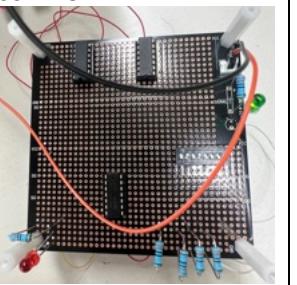
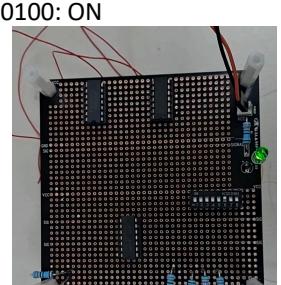
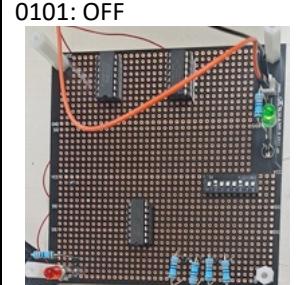
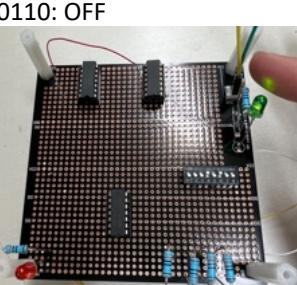
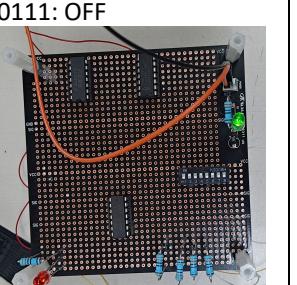
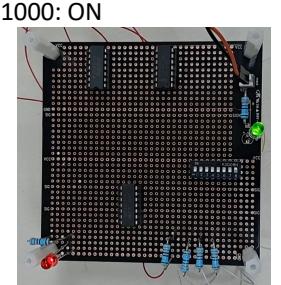
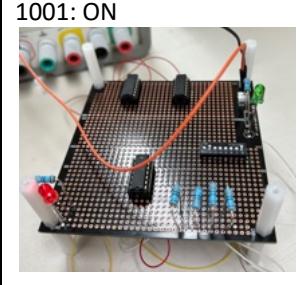
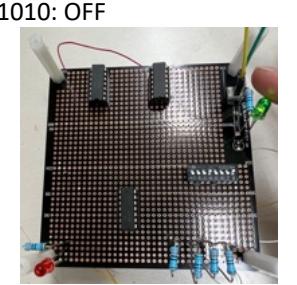
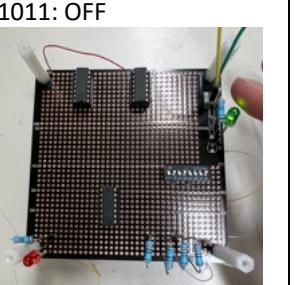
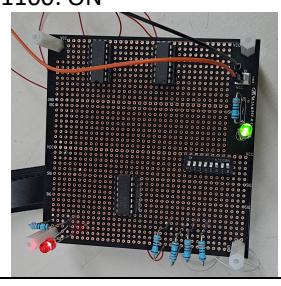
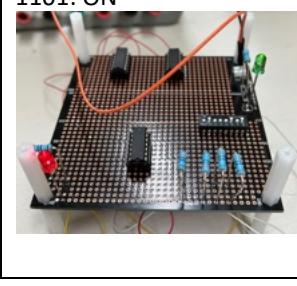
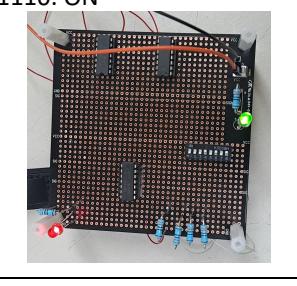
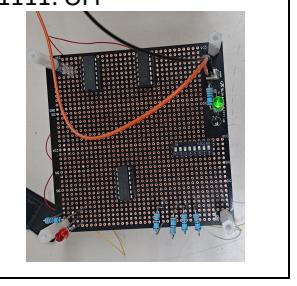
$$((A \text{ OR } \text{NOT } C) \text{ AND } (B \text{ OR } \text{NOT } D)) \text{ OR } (A \text{ AND } C')$$

We implemented it this way because this only requires the use of 3 types of gates (AND, OR, NOT) and 7 gates in total.

In addition to these gates, we used 4 pull-down resistors and a 8-input DIP switch and connected to 4-inputs. We mapped A to '8', B to '6', C to '4', and D to '2'.

## (2) Input and output

we observed if the LED was turned on or off for each of the 16 input combinations:

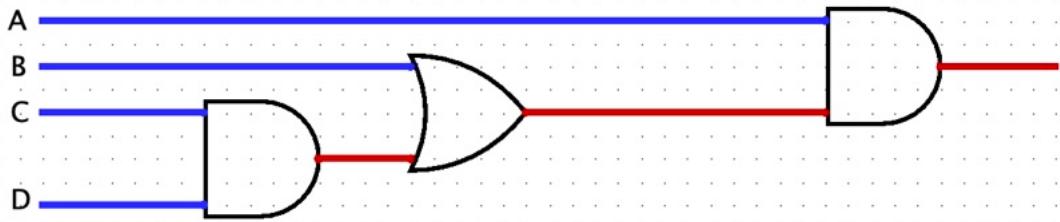
0000: OFF 	0001: OFF 	0010: OFF 	0011: OFF 
0100: ON 	0101: OFF 	0110: OFF 	0111: OFF 
1000: ON 	1001: ON 	1010: OFF 	1011: OFF 
1100: ON 	1101: ON 	1110: ON 	1111: OFF 

## Discussion:

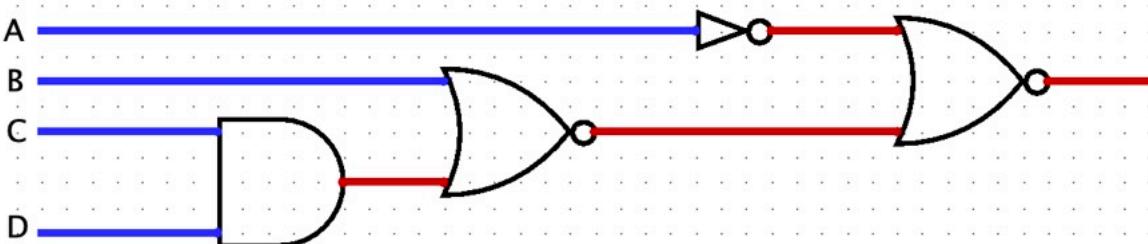
Comparing each of the 16 input combinations to the truth table of GT in the first discussion, we were able to check that the GT comparator was correctly implemented.

## 3. Homework 2

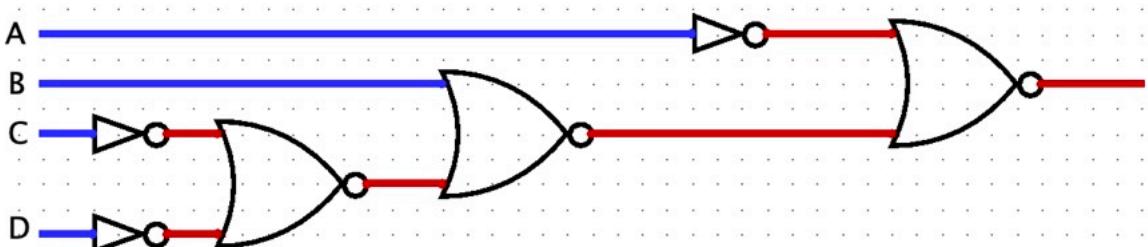
This is the circuit diagram for  $A \cdot (B + C \cdot D)$ , implemented by  $A \text{ AND } (B \text{ OR } (C \text{ AND } D))$



Since AND is equivalent to NOR with complemented inputs, replace the rightmost AND with NOR with complemented inputs:



And then, replace the remaining AND with NOR with complemented inputs:



This is a circuit diagram for the given formula, using only NOR and NOT gates.

#### 4. Homework 3

Given formula:  $AB + ABC + A'B + AB'C$

Truth table:

A	B	C	$AB + ABC + A'B + AB'C$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Minimization:

$$\begin{aligned}
 & AB + ABC + A'B + AB'C \\
 & = AB + ABC + A'B + AB'C + ABC \\
 & = AB(1 + C) + A'B + AB'C + ABC \\
 & = AB + A'B + AB'C + ABC
 \end{aligned}$$

$$\begin{aligned} &= (A + A')B + AB'C + ABC \\ &= B + AB'C + ABC \\ &= B + AC(B' + B) \\ &= B + AC(1) \\ &= B + AC \end{aligned}$$

Circuit Diagram:

