Lab. 01

Logic Design Lab.

Spring 2023

Prof. ChangGun Lee

(cglee@snu.ac.kr)

TA. Seonghyeon Park

TA. Jihwan Kim

TA. Hoyong Lee

(rubis.ld.ta@gmail.com)

Course Information

- Report/Assignment
  - Weekly Task (can be written in Korean or English)
  - Your report should include:
    - Lab Result (Must include pictures)
  - Disscussion (Concepts you learnen during the lab session, any errors you made, how to correct your errors, etc.)
  - Should be a **single PDF file** and less than 30MB
  - Should be submitted by **email** following the rules in the next slide
  - **Deadline: Before the start of the next class (before 7:00pm)**
    - Late Policy: +24h : -20% +48h: -50% +72h: -100%

Course Information

- Attendance
  - Arrive before the lecture is done: No penalty
  - After the lecture: -10%
  - Absent: -100%

Course Information

- Rules for submitting reports / assignments
  - Submission: rubis.ld.ta@gmail.com
  - Email Title:
    - LDLAB_YYMMDD_class#_team#_NAME_StudentID
  - Report File Name:
    - LDLAB_YYMMDD_team#_NAME_StudentID.**pdf**

Points will be deducted if you submit word **.doc** file!

(*YYMMDD : LAB CLASS DATE. Not the submission date.)

EX)

email title : LDLAB_200409_001_team1_John Smith_2019-88888

report file name : LDLAB_200409_001_team1_John Smith_2019-88888.**pdf**

Course Information

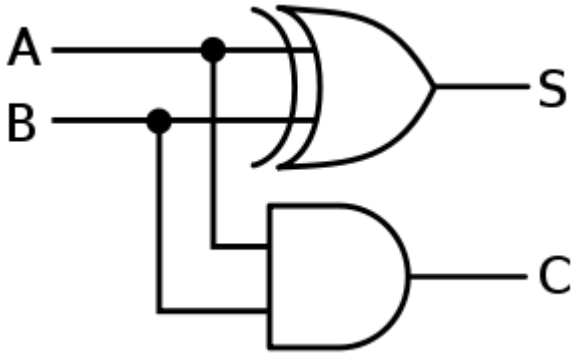
- **Cheating**
  - Zero tolerance
  - You will receive an ‘F’
- **Laboratory Manners**
  - Save materials – don’t be wasteful
  - Put all tools and materials back to their proper place
  - Clean up your desk and shut down the PC
- **“3 Strikes, 1 Out” Rule**
  - Three Warnings → -20% of entire lab grade
  - Examples of strike:
    - Dirty desk or dirty personal lab cabinet
    - Intolerable attitude

Contents

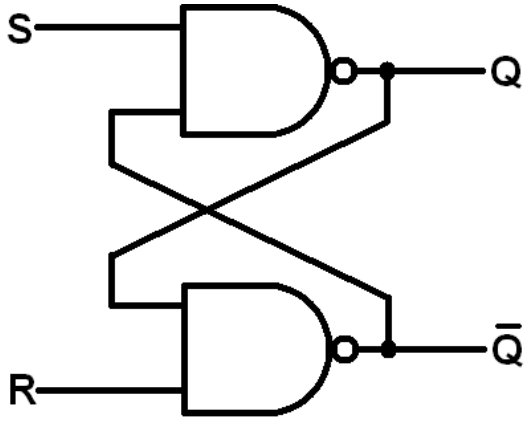
- **What you will learn:**
  - Combinational / Sequential logic circuit
  - Soldering / Prototyping
  - Schematic Design
  - Hardware Description Language (Verilog)
  - Hardware Simulation
  - Field-programmable Gate Array (FPGA) Programming
- **Final Project**
- **Practice Guideline**

What you will learn

- **Combinational and sequential logic circuit**



<Half adder>

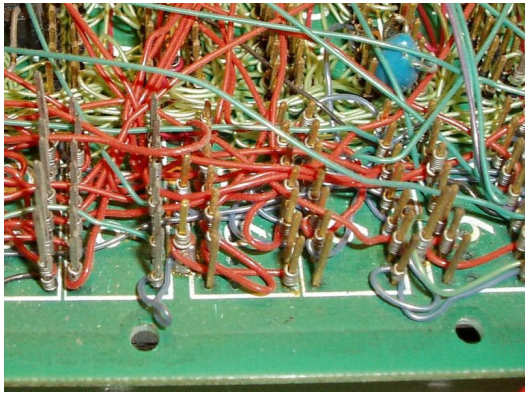


<SR Latch>

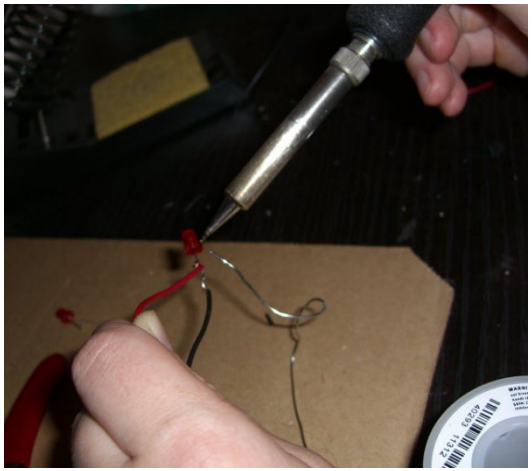
What you will learn

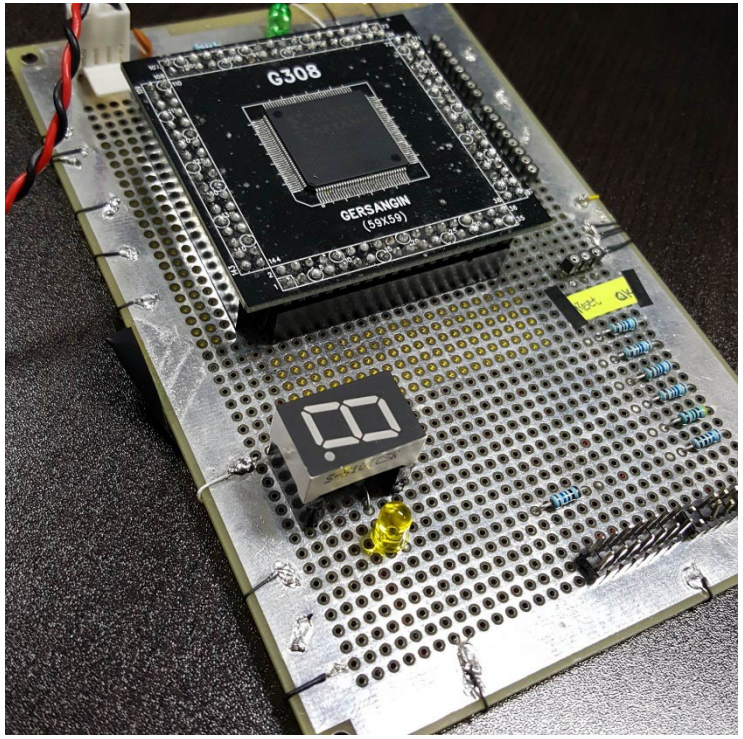
- **Soldering and prototyping**

Wire wrapping



Soldering



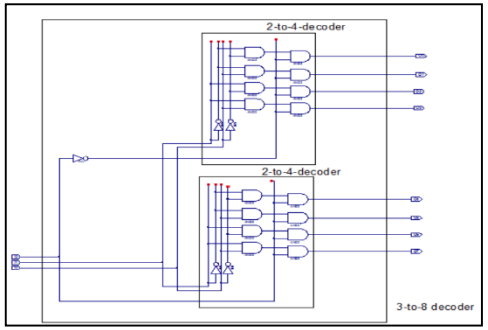


Prototyping

What you will learn

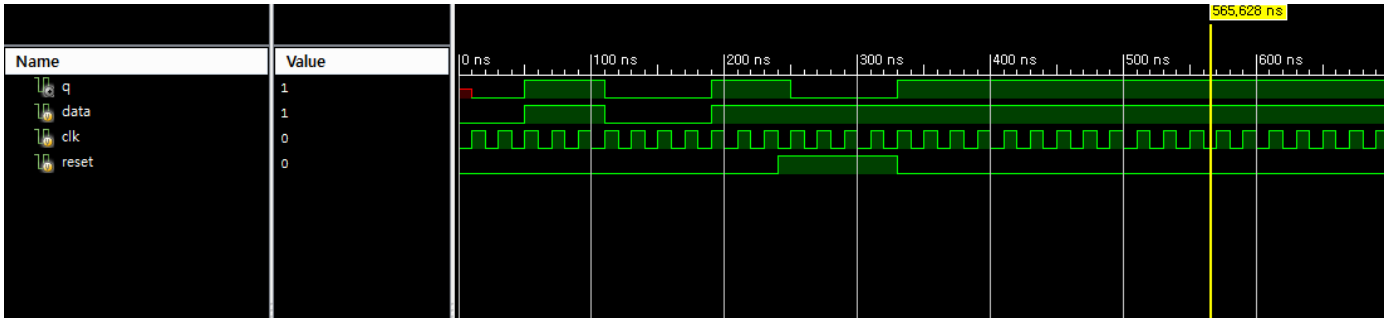
- **Computer Aided Design**

Schematic Design



Hardware Description Language

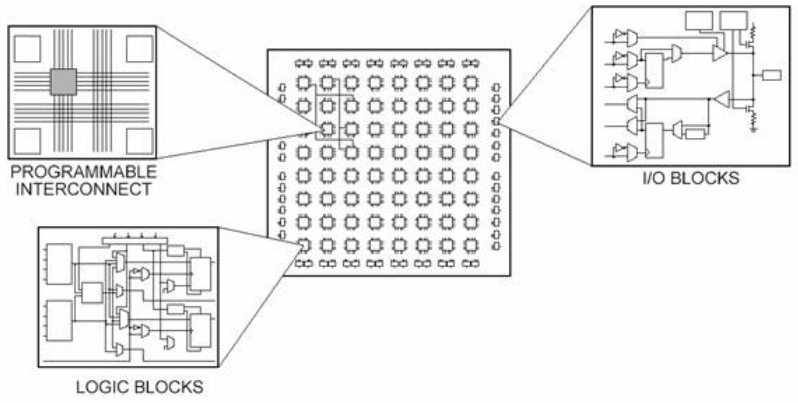
```
module seq_test_module(data, clk, reset, q);
   input data, clk, reset;
   output q;
   reg q;

   always @ (posedge clk)
   begin
      if (reset == 1)
         q <=0;
      else
         q <= data;
   end
endmodule
```



Hardware Simulation

What you will learn

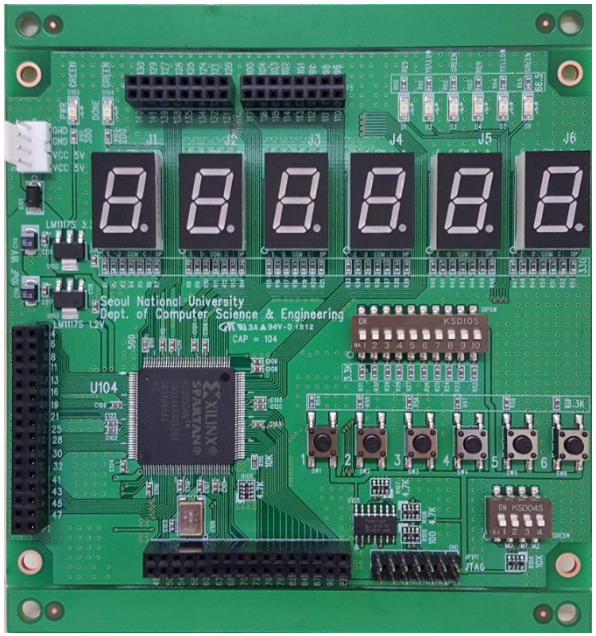
- **Field Programmable Gate Array (FPGA) Programming**



Final Project

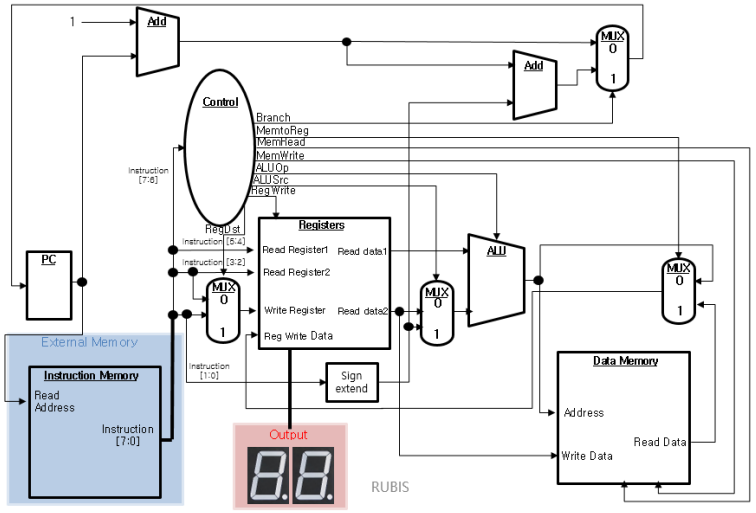
Final Project

- **You will be given:**



<Custom-made logic design board>

- **You will have to make:**

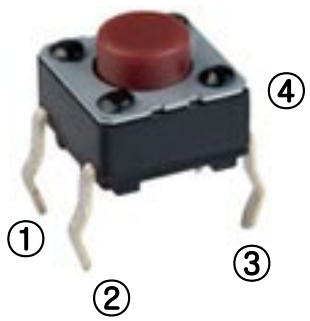


<Microprocessor>

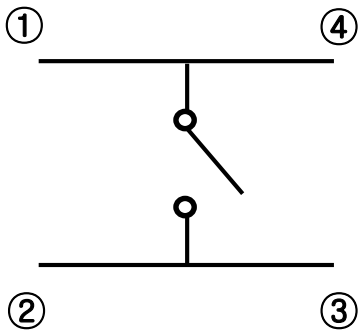
Practice Guideline

Combinational Logic Practice

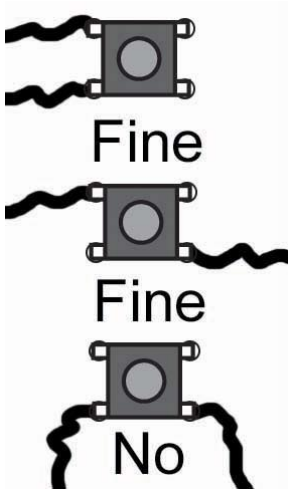
- **Tactile switches**



Tactile Switch



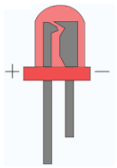
Circuit Diagram

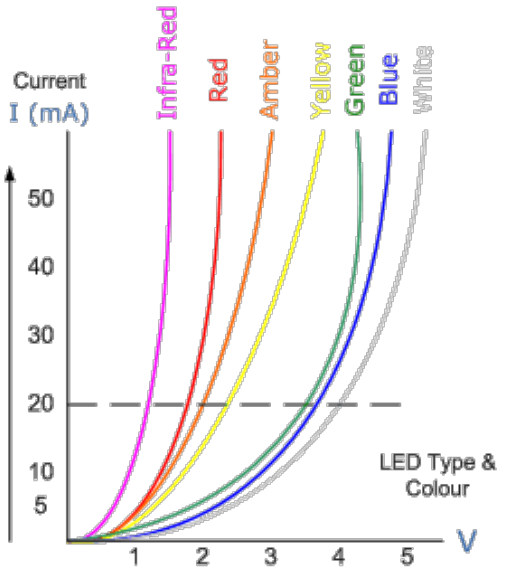


Usage

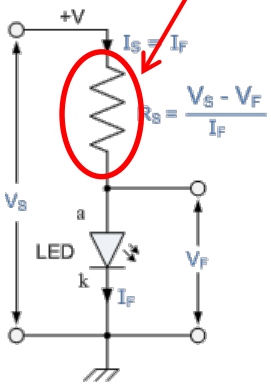
Combinational Logic Practice

- **LEDs**



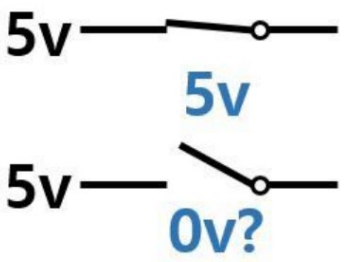


- LEDs emit colored light when passed through by forward current
- To protect LED from excessive current flow, using an appropriate resistor(around 3~400Ω) is necessary



Combinational Logic Practice

- **Floating**

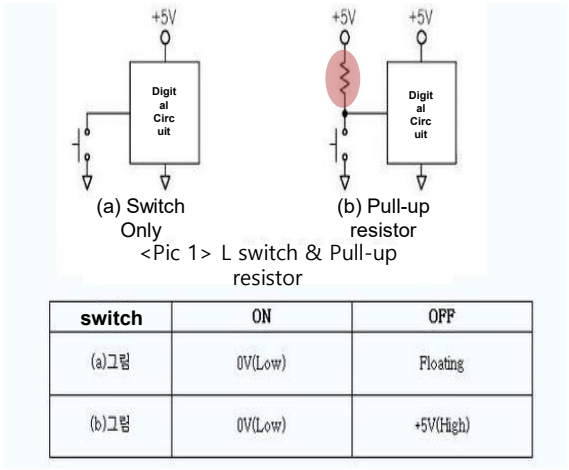


It is not 0V!

Noise Sensitive

Combinational Logic Practice

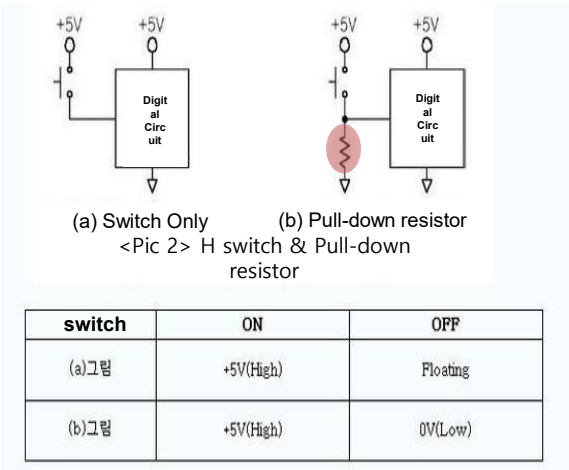
- **Pull-up & pull-down resistors**



<Pic 1> L switch & Pull-up resistor

switch	ON	OFF
(a)그림	0V(Low)	Floating
(b)그림	0V(Low)	+5V(High)

Pull-up Resistor



<Pic 2> H switch & Pull-down resistor

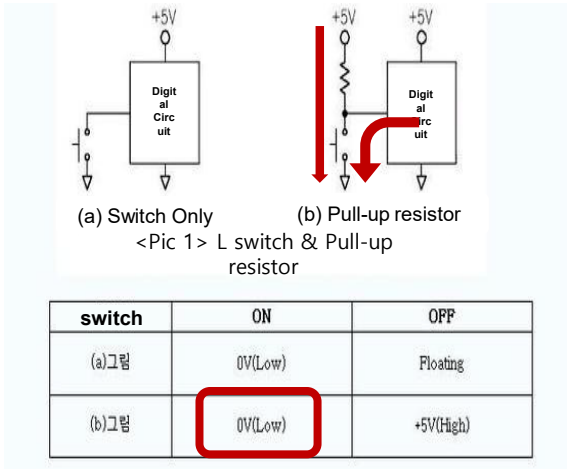
switch	ON	OFF
(a)그림	+5V(High)	Floating
(b)그림	+5V(High)	0V(Low)

Pull-down Resistor

Combinational Logic Practice

- **Pull-up & pull-down resistors**

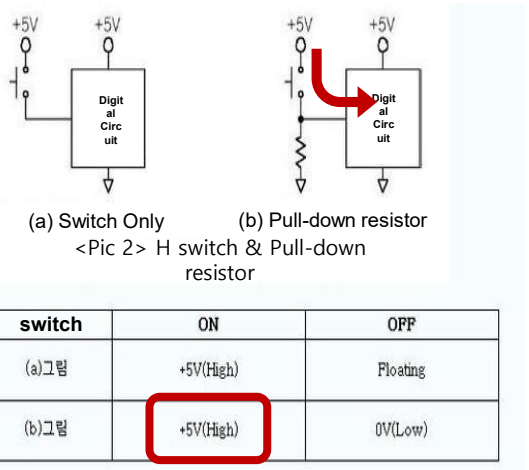
Switch on Switch off



<Pic 1> L switch & Pull-up resistor

switch	ON	OFF
(a)그림	0V(Low)	Floating
(b)그림	0V(Low)	+5V(High)

Pull-up Resistor



<Pic 2> H switch & Pull-down resistor

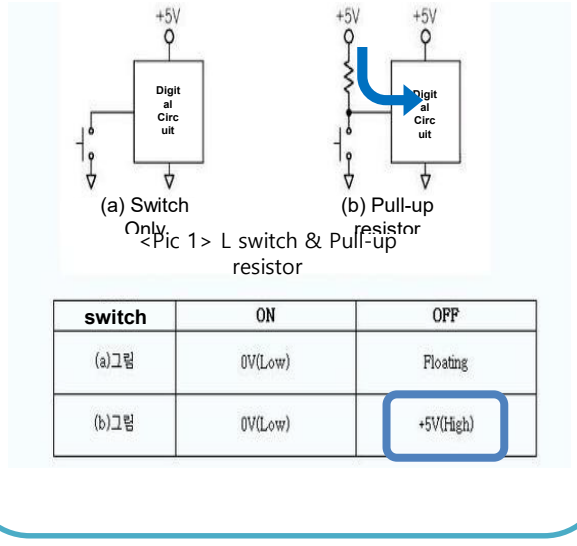
switch	ON	OFF
(a)그림	+5V(High)	Floating
(b)그림	+5V(High)	0V(Low)

Pull-down Resistor

Combinational Logic Practice

- **Pull-up & pull-down resistors**

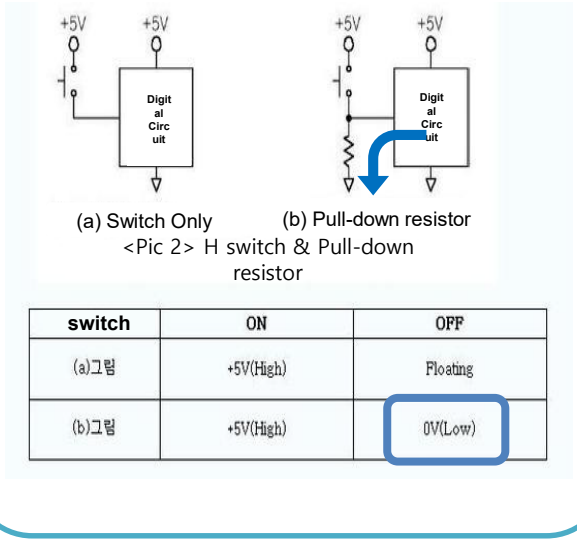
Switch on Switch off



<Pic 1> L switch & Pull-up resistor

switch	ON	OFF
(a)그림	0V(Low)	Floating
(b)그림	0V(Low)	+5V(High)

Pull-up Resistor



<Pic 2> H switch & Pull-down resistor

switch	ON	OFF
(a)그림	+5V(High)	Floating
(b)그림	+5V(High)	0V(Low)

Pull-down Resistor

Instruments

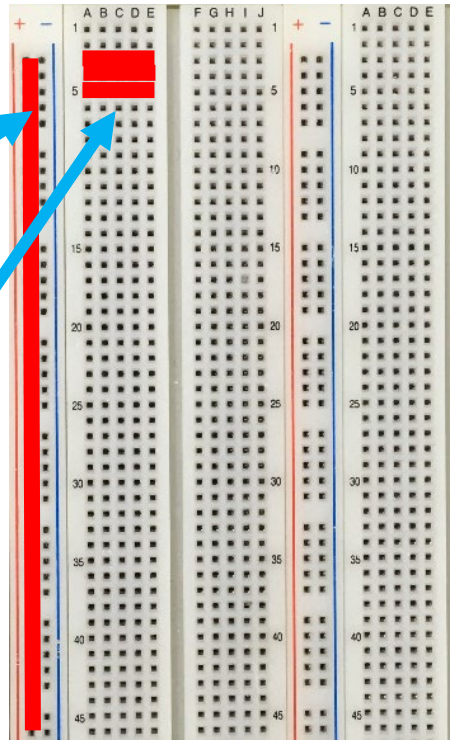
oscilloscope

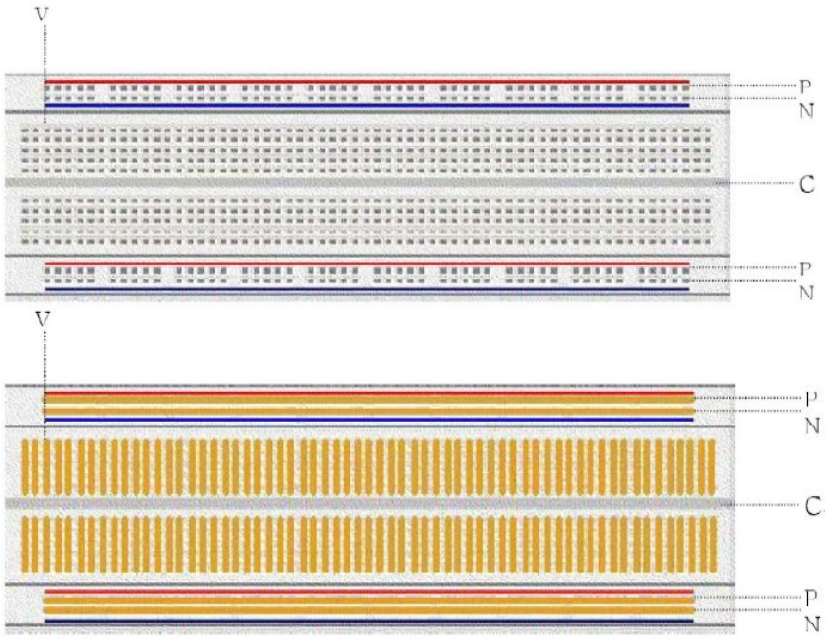
Function Generator
Multimeter
Power Supply

Breadboard

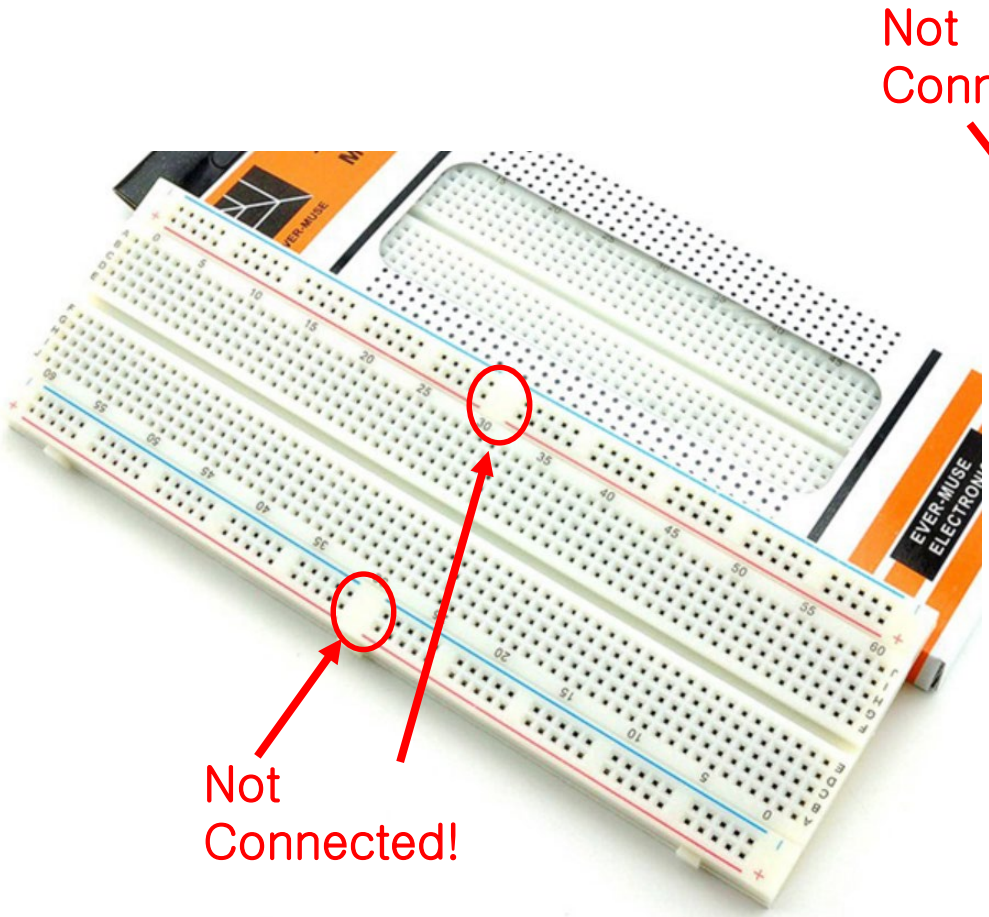
Connected vertically

Connected horizontally



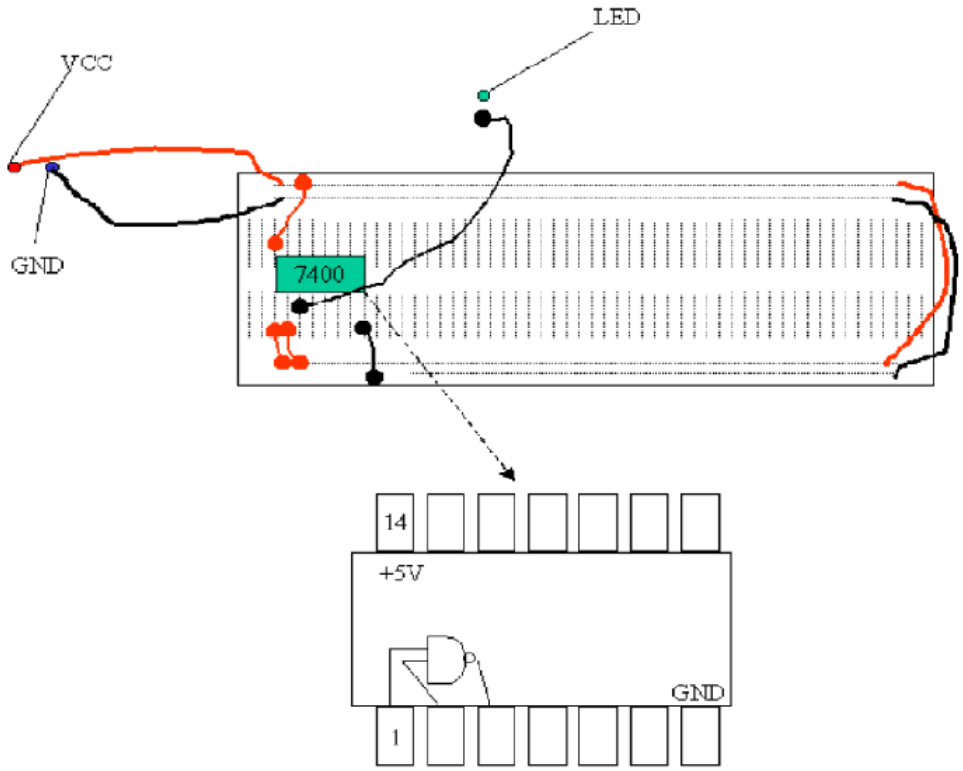


Breadboard(Separated)



Breadboard

- **Implementation guide**

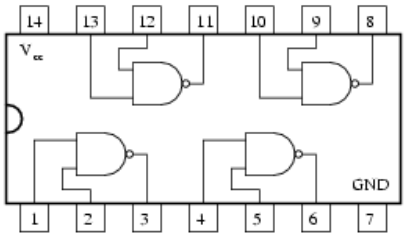


✓ A circuit using 7400 Quad 2-Input NAND gate is constructed on the bread board

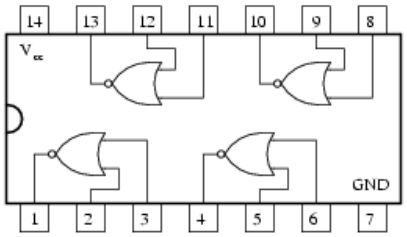
Logic Gates

- **Logic Gates**

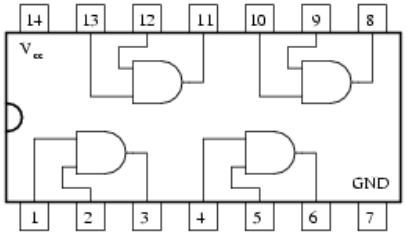
5400/7400
Quad NAND gate



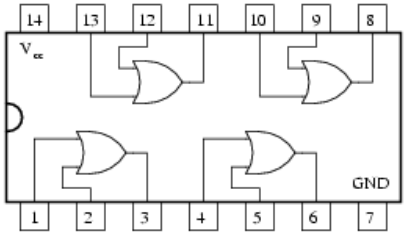
5402/7402
Quad NOR gate



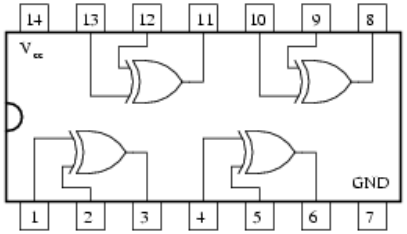
5408/7408
Quad AND gate



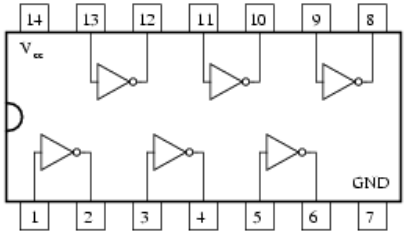
5432/7432
Quad OR gate



5486/7486
Quad XOR gate



5404/7404
Hex inverter



Tools – Solder, Soldering iron, Tip, etc

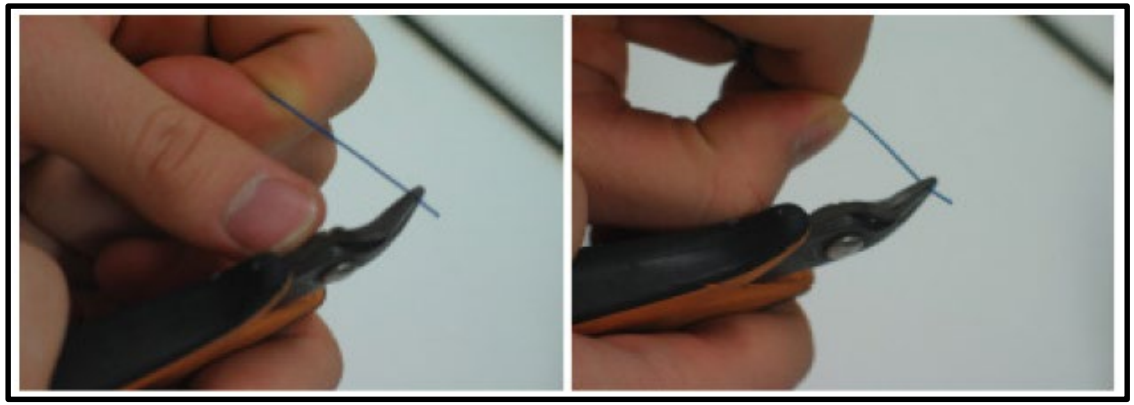
Soldering iron

Tin wire Solder Wire

Nipper Bead nipper Desolder Chip extractor Long-nose plier

Tools

- **Bead Nipper**



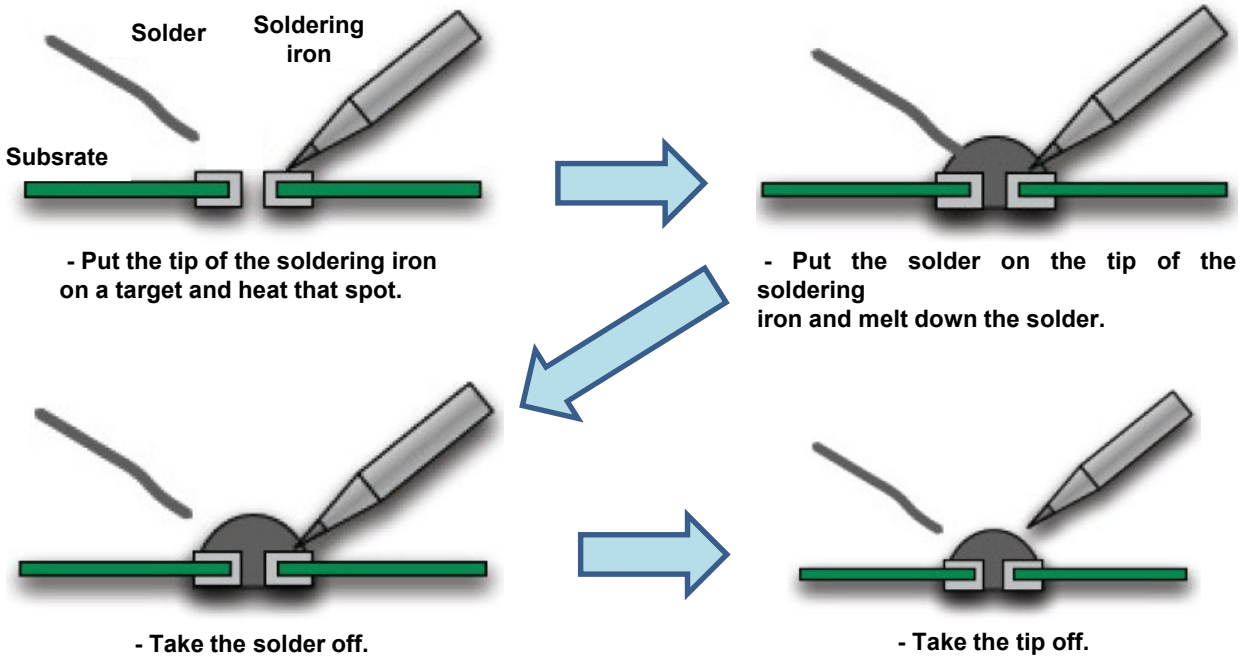
Ripping off coating

- **Extracting chips**

  - To extract IC chips, use IC Chip extractor.
  - Never extract chips using your hand

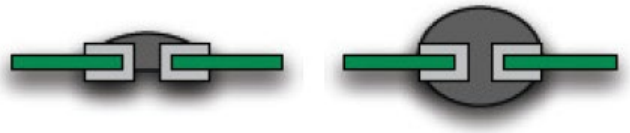
Soldering

- **Procedure**

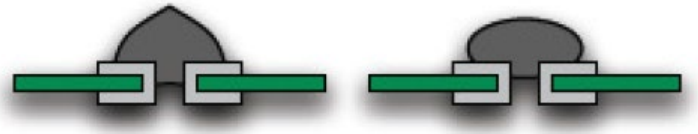


Soldering

- **Wrong cases**

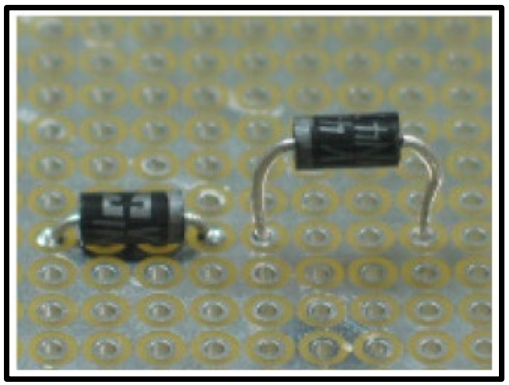


Amount of solder is wrong!



Taking a tip off is too late!

Temperature of the soldering iron is not high enough!

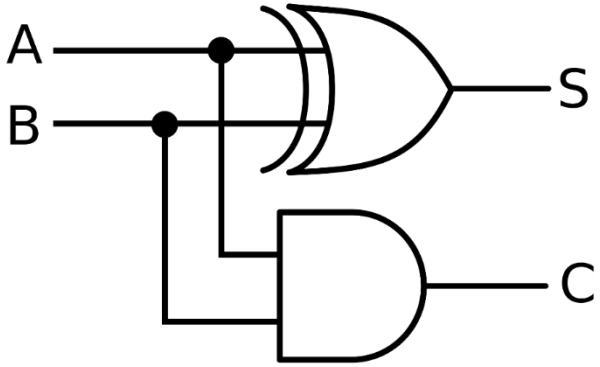


Components must be pressing against the board.

Lab

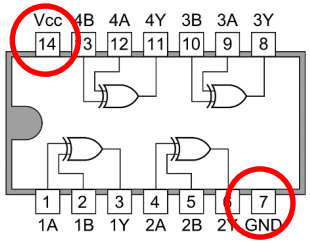
Combinational Logic Practice

- Let's implement half-adder on breadboard.

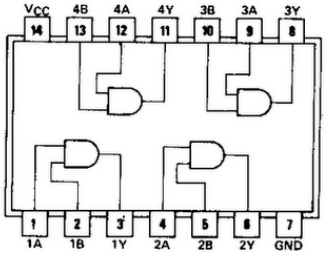


Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

7486 Quad 2-input ExOR Gates



7408



Homework

- All homework do with your team.
- Submit a report per person.

Homework

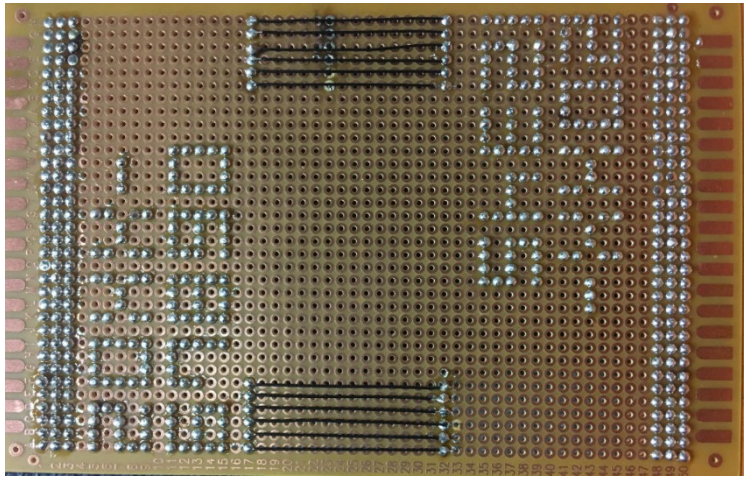
1. Half-adder
   - Disscussion (Concepts you learnen during the lab session, any errors you made, how to correct your errors, etc.)
   - Result for every case in truth table (pictures)

Homework

2. Soldering

Practice soldering and wiring as the figure below. (Soldering **3 lines** and **student ID**, and **6 slim wires** for each person)

One of you should use another board.



Homework

- Write a report
  - Either in Korean or in English
  - Must include the result and discussion of the practice
  - # of pages doesn't matter
  - Documents should be submitted as PDF file.
  - All the files should be compressed to ZIP format
    (if there are several files)
  - **Due :**
    Class 001 – April, 10th (Before class begin at 7:00pm)
    Class 002 - April, 11th (Before class begin at 7:00pm)
    Class 003 - April, 13th (Before class begin at 7:00pm)