Name: KEY

CS472 / ECE472 / CS572 / ECE572
Quiz #2
No notes or calculator should be used during this quiz.
This quiz is double-sided!

For each question below, choose the best answer.

1. (2 pts) What is a Translation Look-aside Buffer (TLB)?

   A cache that is used to quickly locate the physical address of a virtual memory page

2. (2 pts) Suppose that you are working with a computer that uses the following memory arrangement (the same hierarchy used in our lectures):
   - The CPU can communicate only with the L1 cache
   - The L1 cache can communicate with either the CPU or the L2 cache
   - The L2 cache can communicate with either the L1 cache or the main DRAM memory

   1. The L1 cache would be expected to perform faster than the L2 cache
   2. The L2 cache would generally be larger than the L1 cache

3. (2 pts) Why would a virtual memory implementation use a fully associative cache to hold page table entries?
   Because the lookup speed is critical to avoid adding a significant performance penalty for instructions that access memory
   We need a cache so that the lookup doesn't always need to occur in main memory (thereby significantly slowing any memory accesses). Technically this doesn't have to be an associative cache but we want to avoid unnecessary block replacements (since this causes a time penalty) so an associative cache is well suited.

4. (2 pts) A direct-mapped cache uses which of the following replacement policies?
   A direct-mapped cache doesn't give the designer any choice of replacement policy

FALSE 5. (1 pt) Anytime a CPU writes to a page of virtual memory, the corresponding page is immediately written to disk to avoid loss of data.

FALSE 6. (1 pt) A direct-mapped cache design guarantees that you will never have to replace blocks of data within the cache.

FALSE 7. (1 pt) A fully associative cache design guarantees that you will never have to replace blocks of data within the cache.
The probability of a block replacement is lower but we could still need to replace a block (specifically in the case when the cache is already full and we need to access a different block).