Name: Exam Key Student ID #: _____

CS472 / ECE472 / CS572 / ECE572

Fall 2018 Midterm Exam

You may use a calculator and a double-sided 8.5" x 11" notesheet.

Indicate whether the following statements are True or False.

False 1. (2 pt) Assuming that the pipeline is initially empty, a pipelined CPU can fully execute a single instruction in less time than the non-pipelined equivalent CPU.

True 2. (2 pt) The programmer's choice of compiler could have an impact on the order that instructions will be executed within the computer.

False 3. (2 pt) Anytime a CPU writes to a page of virtual memory, the corresponding page is immediately written to disk to avoid loss of data.

False 4. (2 pt) The highest addressable virtual memory location must always be less than or equal to the highest physical memory address within a computer.

True 5. (2 pt) The execution time of a benchmark program is generally considered to be a fair comparison between processors with different Instruction Set Architectures (ISAs).

True 6. (2 pt) A program's memory access patterns will have a significant impact on the hit rate of a data cache.

False 7. (2 pt) A conflict miss can never occur in a direct-mapped cache.

~~False~~ 8. ~~(2 pt) In the MIPS architecture, the machine code of a branch instruction indicates the absolute memory address that should be placed inside the program counter (PC).~~
Dropped due to possible ambiguity. I should have used the phrasing "…machine code of a branch instruction **contains** the absolute memory address"

False 9. (2 pt) As the level of associativity increases, it becomes easier to implement a least-recently-used (LRU) cache replacement policy.

~~False~~ 10. ~~(2 pt) Anytime a CPU writes to a page of virtual memory, the corresponding page is immediately written to disk to avoid loss of data.~~ (duplicate)

True 11. (2 pt) Static RAM (SRAM) is generally used to implement memory caches while dynamic RAM (DRAM) is generally used as the basis for system memory.

True 12. (2 pt) The decimal value 36.015625 can be exactly represented in IEEE 754 single precision format.

False 13. (2 pt) In a virtual memory system, a translation-lookaside buffer (TLB) miss implies that the specified memory page must be retrieved from swap space (on the HDD).

~~True~~ 14. ~~(2 pt) The MIPS ISA uses a load/store architecture that requires operands to be moved into registers before ALU operations can take place.~~
I'll give this one to students since it's possible to make the argument that an instruction such as `addi` has one operand included in the instruction and is therefore not using a register for that operand. The phrasing should have said "...requires operands to be moved from memory into registers…"

False 15. (2 pt) A write-through cache scheme implies that a cache will write changes only to the cache block (and set a dirty bit). The modified cache block will then be written to main memory only when it is replaced by a different block.

Provide the appropriate answer in the blank space.

16. (2 pts) In a pipelined CPU design, situations that prevent the next instruction stream from being executed during its designated clock cycle are called: hazards or pipeline hazards

For each of the following questions, choose the best answer.

17. (2 pts) An immediate-format MIPS instruction requires how many registers to be specified?

A. 1
B. 2
C. 3
D. 4

18. (2 pts) Which of the following is a technique that computer architects can take in order to avoid hitting the metaphorical "power wall"?

A. Decrease the clock period to reduce power consumption
B. Increase the clock frequency
C. Improve parallelization to execute multiple instructions simultaneously
D. All of the above

19. (2 pts) In a CMOS IC design, power consumption is improved by lowering which of the following?

A. The operating voltage
B. The operating frequency
C. The capacitive load
D. All of the above

20. (2 pts) Suppose that you are implementing an associative cache with N=3. Assume that the block size has been selected as 8 bytes and that there are 64 block indices in the cache (i.e. there are 64 sets of 3 blocks). The cache uses a 20 bit addressing scheme. How many bits will each individual tag occupy?
3 bits for byte offset, 6 bits for block index. 20 – 3 – 6 = 11

A. 10
B. 11
C. 12
D. 13

21. (2 pts) Suppose your coworkers at ACME Computer Design have a problem. They implemented a virtual memory system to provide each process with its own virtual address space (each page with a size of 2K). Unfortunately, the corresponding page table is ginormous. Which of the following suggestions would be wisest?

A. Remove the translation-lookaside buffer (TLB) so that all queries can go directly to main memory
B. Decrease the size of each memory page
C. Increase the size of each memory page
D. Move 90% of the memory pages into swap space (on HDD) so that additional memory is available for the page table

22. (2 pts) Which of the following statements best describes memory behavior in the MIPS architecture?

A. The stack and the heap each start at high memory addresses and work towards low addresses
B. The stack and the heap both start near the middle of main memory and they grow away from each other
C. The stack and the heap each start at low memory addresses and work towards high addresses
D. The stack starts at a high memory address, the heap starts at a low address and they grow towards each other

23. (2 pts) Suppose that the MIPS architects decided to change the instruction length and develop a CPU with sixty-four 32 bit registers. If all other features remain intact, how many bits should the machine code of an R-format instruction occupy?

A. 33
B. 34
C. 35
D. 36

For each of the following problems, assume that the main memory contents are as shown in the diagram. Each problem is independent (e.g. the memory is initialized to match the diagram prior to each question).

Contents of main memory				
Address				
0x1c20	0x8a	0x78	0x42	0x9c
0x1c24	0x97	0x3d	0xff	0x14
0x1c28	0xa3	0x67	0xda	0x81
0x1c2c	0x00	0x00	0x2f	0x18
0x1c30	0x2c	0xe2	0x22	0x71
0x1c34	0x00	0x00	0x00	0x08
0x1c38	0x9d	0x56	0x18	0xb4
0x1c3c	0xef	0x02	0xbb	0x7c
...				
...				
0xffe8	0xf7	0x35	0x21	0xc3
0xffec	0x8a	0x55	0x48	0x8d
0xfff0	0x00	0x00	0x1c	0x28
0xfff4	0x00	0x00	0x3f	0x28
0xfff8	0x2b	0x7e	0x12	0x72
0xfffc	0x13	0x48	0x15	0x13

24. (4 pts) Assume that the initial register values are as follows:
$t1 = 0x0004, $s0 = 0x0107,
$a1 = 0x1c28, $a2 = 0x1c34

```
addi   $s0, $t1, 19 s0 = 0x4+19 = 23
sub    $s0, $a1, $s0 s0 = 0x1c28-23 = 0x1c11
add    $a2, $t1, $zero a2 = 0x04+0 = 4
add    $t1, $s0, $a1 t1 = 0x1c11+0x1c28
```

After the assembly code has finished execution, what are the contents of the following registers?

$t1 = 0x3839, $s0 = 0x1c11,
$a1 = 0x1c28, $a2 = 4

25. (4 pts) Assume that the initial register values are as follows:
$t1 = 0x0004, $s0 = 0x0107,
$a1 = 0x1c28, $a2 = 0x1c34

```
     addi   $t1, $zero, 10 t1 = 10
     lw     $s0, 0($a2) s0 = 0x08 = 8
     slt    $t1, $t1, $s0 10 !< 8 → t1 = 0
     beq    $t1, $zero, L1 t1 is 0 so goto L1
     addi   $a1, $a1, 2
     j      L2
L1:
     lw     $s0, 4($a2) s0 = 0x9d5618b4
L2:
```

After the assembly code has finished execution, what are the contents of the following registers?

$t1 = 0, $s0 = 0x9d5618b4, $a1 = 0x1c28, $a2 = 0x1c34

26. (8 pts) For this problem, assume that the initial register values are as follows:
$t1 = 0x0004, $s0 = 0x0107, $s1 = 0x571, $sp = 0xfff4

```
addi   $sp, $sp, -8 adjust the stack pointer to 0xffec
lw     $s0, 0($sp) s0 = 0x8a55488d
lw     $s1, 4($sp) s1 = 0x00001c28 = 0x1c28
lw     $t1, 0($s1) t1 = 0xa367da81
addi   $s0, $zero, 255 s0 = 255 = 0xFF
or     $t1, $t1, $s0 t1 = t1 | 0xFF = 0xa367daFF
addi   $sp, $sp, 8 adjust the stack pointer back to 0xfff4
```

After the assembly code has finished execution, what are the contents of the following registers?

$t1 = 0xa367daFF, $s0 = 255, $s1 = 0x1c28, $sp = 0xfff4

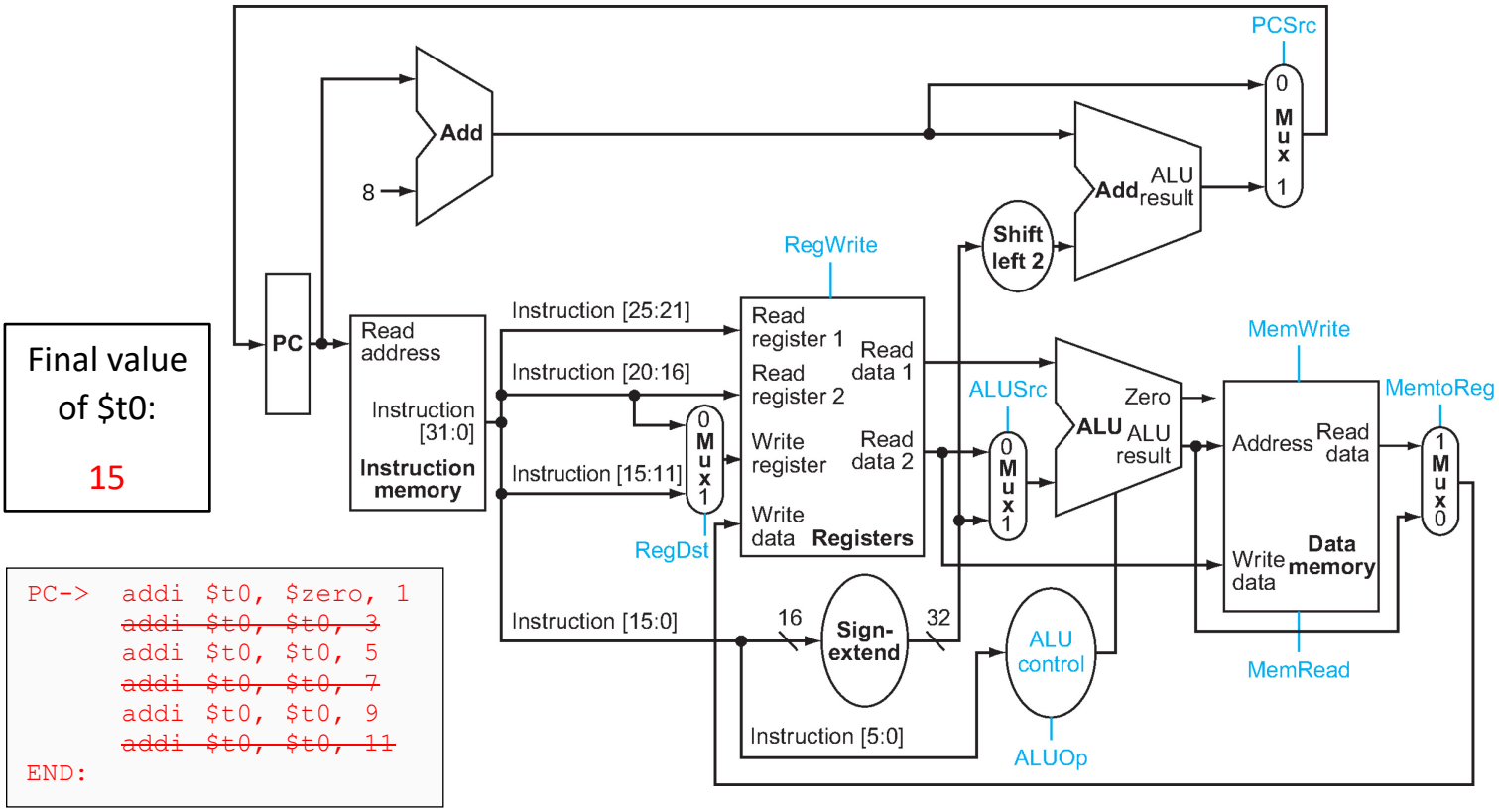
27. (7 pts) Compute the IEEE 754 single precision (32 bit) representation of the decimal value 467.625

A. What is the 1 bit value of the sign bit?
0 (positive number)

B. What is the 8 bit value of the biased exponent?
467.625 = 111010011.101
= $1.11010011101 \times 2^{8}$
8+127 = 135
= 0b10000111

C. What is the 23 bit value of the mantissa?
1101 0011 1010 0000 0000 000

28. (3 pts) Suppose that the CPU design shown below was manufactured with a defect. The input to the ADDER was intended to be 4 (corresponding to a 4 byte instruction). Unfortunately, the input was inadvertently set to 8 (as shown). All other components of the computer are still running on the assumption that each instruction occupies 32 bits. The small box below shows the sequence of 32 bit instructions that was going to be executed. Assuming the program counter (PC) was originally pointing to the first instruction, what will be the final value of $t0 after the program counter reaches the END label?



Final value of $t0:

15

```
PC->  addi  $t0, $zero, 1
      addi  $t0, $t0, 3
      addi  $t0, $t0, 5
      addi  $t0, $t0, 7
      addi  $t0, $t0, 9
      addi  $t0, $t0, 11
END:
```

29. (3 pts) In a particular computer, the instruction-cache miss rate is 3% and the data-cache hit rate is 96%. There is a miss penalty of 120 cycles that occurs when either cache is unable to immediately return the data. In a given program, suppose that 30% of the instructions involve load or store operations. If the base number of cycles per instruction (CPI) is 2 (meaning the CPI with an ideal cache) then what would be the expected CPI during this particular program?

A data-cache hit rate of 96% implies a data-cache miss rate of 4%.
The expected CPI is: 2 + (0.03*120) + (0.30*0.04*120) = 7.04

30. (10 pts) Suppose you are working with a direct-mapped cache implementation. The cache has a block size of 4 words (16 bytes). There are 16 entries in the cache. The cache uses a 16 bit address.
Implied address format: 8 bits for tag, 4 bits for block index, 4 bits for byte offset.
Note that this implies that the tag must be 0 for any byte address < 256.

A. The following chart indicated byte addresses that are requested from the initially empty cache. Addresses are accessed in sequential order (162, 139, 301, 300, etc).
You do not have to fill in this chart but you may find it useful for partial credit.

Byte Address	Block address	Block Index	Tag	Hit?
162	10	10	00000000	N
139	8	8	00000000	N
301	18	2	00000001	N
300	18	2	00000001	Y
249	15	15	00000000	N
141	8	8	00000000	Y
220	13	13	00000000	N
261	16	0	00000001	N
208	13	13	00000000	Y
172	10	10	00000000	Y

B. Complete the following table showing the final state of the cache. If a value is unknown, write a question mark in that space.

Index	Valid	Tag
0	1	00000001
1	0	?
2	1	00000001
3	0	?
4	0	?
5	0	?
6	0	?
7	0	?
8	1	00000000
9	0	?
10	1	00000000
11	0	?
12	0	?
13	1	00000000
14	0	?
15	1	00000000

How many cache hits occurred?

4

How many times were blocks replaced? (Loading into an empty slot does not count.)

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