ECE/CS 472/572 – Computer Architecture
Instructor: Prof. Lizhong Chen
Homework #1 – Due: Wednesday, April 17 at 8:30am, Hard copy

Problem 0
Read book chapter 4.1 to 4.4.

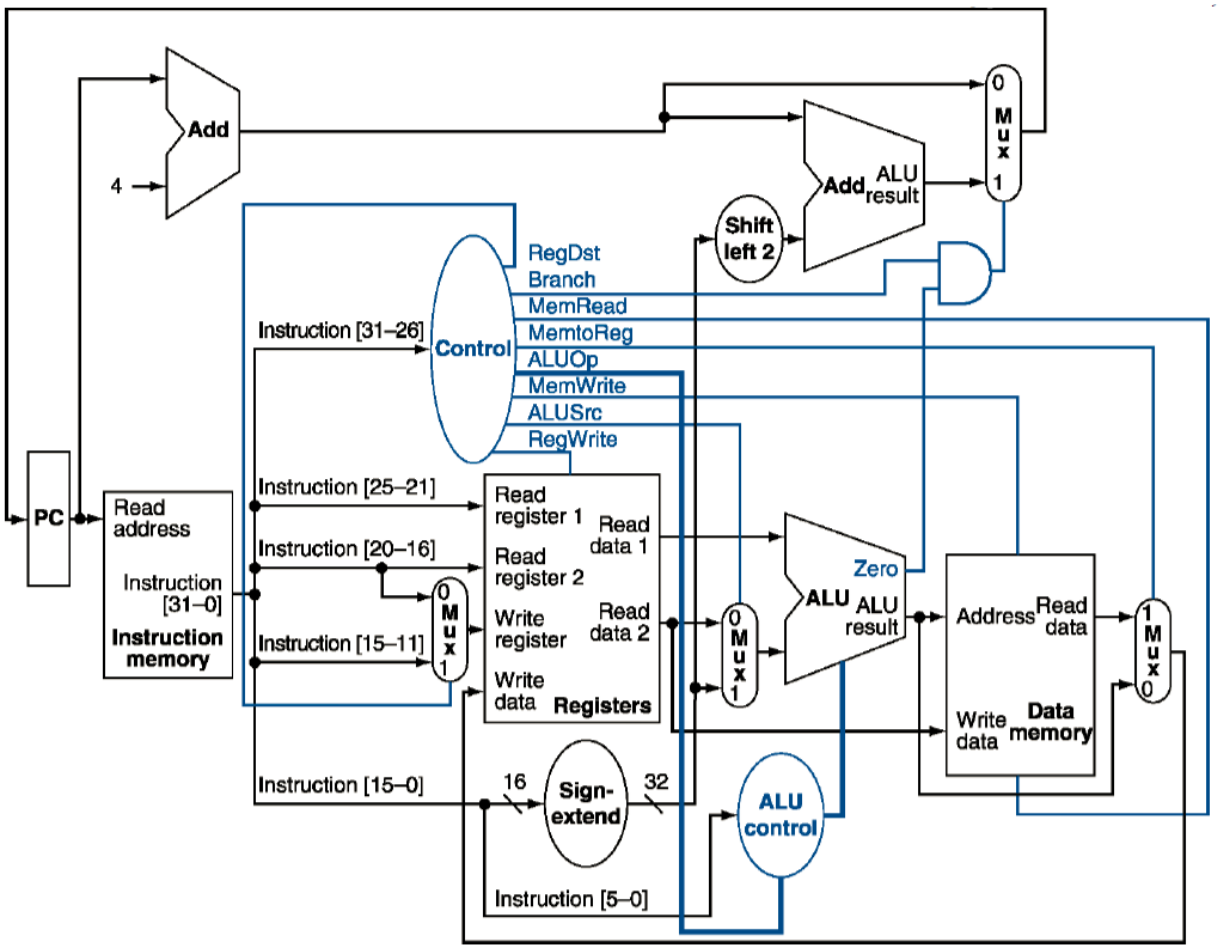

Figure 1. The basic implementation of the MIPS subset, including the necessary multiplexers and control lines

Problem 1 (30 pts)

When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. In the following problems, assume that we are starting with a datapath from Figure 1, where

Block	Delay (ps)
I-Mem	450
Add	100
Mux	20
ALU	150
Regs	250
D-Mem	550
Control blocks	100
Sign-extend	50

Note that this is a single-cycle processor, so every instruction takes one cycle to execute, and the next instruction will not start until the current instruction completes execution.

Consider the addition of a multiplier to the ALU. This addition will add 130 ps to the latency of the ALU. The result leads to fewer instructions executed since we will no longer need to emulate the MUL instruction.

1.1) What is the clock cycle time with and without this improvement? **(10 pts)**

1.2) If this improvement can result in 15% fewer number of instructions executed as we no longer need to emulate the MUL instruction. What is the speedup achieved by adding this improvement? Does this increase or decrease the performance? **(10 pts)**

1.3) If we want to achieve a speedup that is ≥ 1.3 by adding this MUL operation to ALU, what percentage of instructions should be reduced at least? **(10 pts)**

Problem 2 (35 pts)

For the problems in this exercise, assume that there are **NO** stalls in the single-cycle processor. Before executing the following code, the initial values (decimal format) of register files are listed as below

r2	r3	r4	r5	r6	r7	r8	r9	r10	r11	r31
2	0	1	6	2	4	12	7	3	8	0

```
loop1:  addi r11, r10, 4
        sw r2, 16(r7)
        nor r3, r2, r6
loop2:  lw r4, 0(r2)
        lw r8, 0(r3)
        add  r5, r4, r8
        nor  r6, r3, r5
        sw r6, 0(r2)
        addi r11, r11, -1
        bne r11, r31, loop2
        addi r9, r9, -1
        bne r9, r2, loop1
```

2.1) Please list the breakdown **percentage** of **executed** instructions (e.g., add: 10%) **(18 pts)**

op	add	addi	bne	lw	sw	nor
count/total						
percentage						

2.2) In what fraction of all cycles is the data memory used; in what fraction of all cycles is the instruction memory used? **(7 pts)**

2.3) In what fraction of all cycles is the input of the sign-extend circuit needed? What is this circuit doing in cycles in which its output is not needed? **(10 pts)**

Problem 3 (35 pts)

In this exercise we examine in detail how an instruction is executed in a single-cycle datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word:

000000 01000 00011 01011 00000 100100

Assume that data memory is all zeros and that the processor's registers (32 bits) have the following values (decimal format) at the beginning of the cycle in which the above instruction word is fetched:

r0	r1	r2	r3	r4	r5	r6	r8	r11	r18
125	-219	-56	79	134	-2	15	99	141	211

3.1) What are the outputs of the sign-extend and the "Shift left 2" unit (near the top of Figure 1) for this instruction word? **(5 pts)**

Sign-extend	Shift-left-2

3.2) What are the values of the **ALU control** unit's inputs for this instruction? **(5 pts)**

ALUOp	Instruction[5-0]

3.3) What is the new PC address after this instruction is executed (assuming the current value of PC is pc)? Highlight the path through which this value is determined **(5 pts)**

3.4) For each Mux, show the values of its data output during the execution of this instruction **(5 pts)**

3.5) For the ALU and the two add units, what are their data input values? **(5 pts)**

3.6) What are the values of all inputs for the "Registers" unit? **(10 pts)**