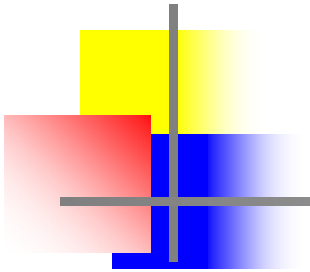


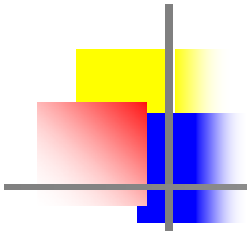
ECE201-Digital Design

(Ch.08 Register Transfer Level)

3 June 2019

by

Kyu-Seek Sohn



Contents

- Digital system = control logic + datapath
- Register Transfer Level
- Algorithmic State Machine
- Design Example : Binary Multiplier
- Home Work

A Digital System

- Control logic + datapath model

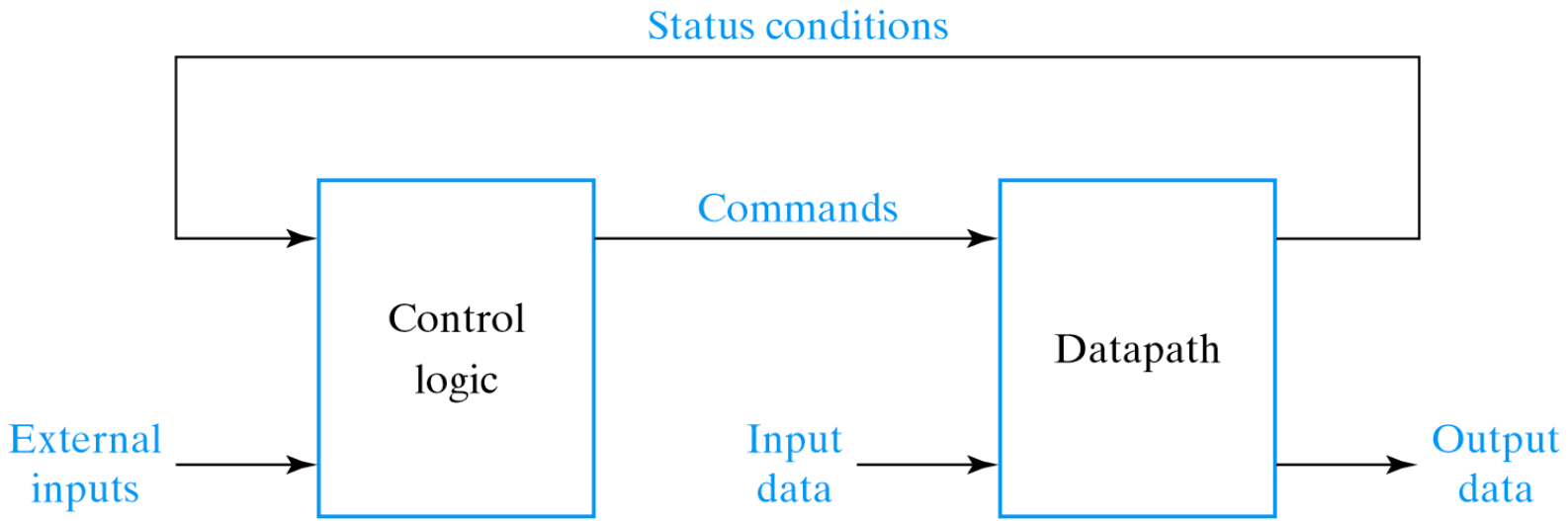
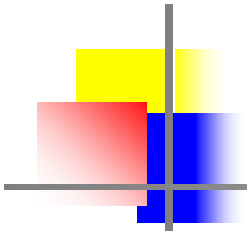
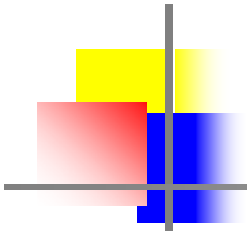


Fig. 8-2 Control and Datapath Interaction



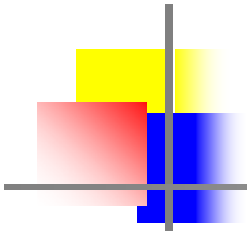
Control Logic

- Sequencing the operations in the datapath
  - Command : signals generated by the control logic
- A sequencial circuit
  - Internal state dictate the control command for the system
- Inputs
  - External inputs
  - Status conditions from the datapath
- Outputs
  - Commands to the datapath



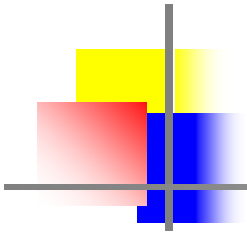
Datapath

- Data processing path
  - Series of registers along which data is manipulated
- Operations manipulating data
  - Transfer operations
  - Arithmetic operations
  - Logic operations (bit-wise)
  - Shift operations
- Outputs
  - Output data
- Inputs
  - Input data



Register Transfer Level(RTL)

- Register is :
  - Basic unit of data processing in the datapath
  - Basic component of datapath
- Operations executed on registers
  - Transfer operations
  - Arithmetic operations
  - Logical operations
  - Shift operations
  - Relational operations



Algorithmic State Machines(ASM)

- Definition
  - A special flowchart that defines digital hardware algorithms
- Use of ASM
  - To specify accurately the control sequence and datapath operations in a digital system
- Meaning of ASM
  - Timing reliationship between the state of the states of a sequential control logic
  - Event causing the state transition

Components of ASM

- State box

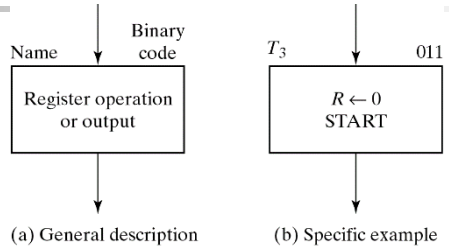


Fig. 8-3 State Box

- Decision box

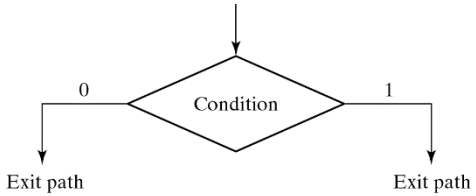


Fig. 8-4 Decision Box

- Conditional box

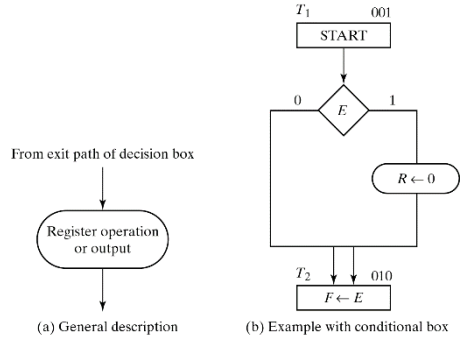


Fig. 8-5 Conditional Box

State Box

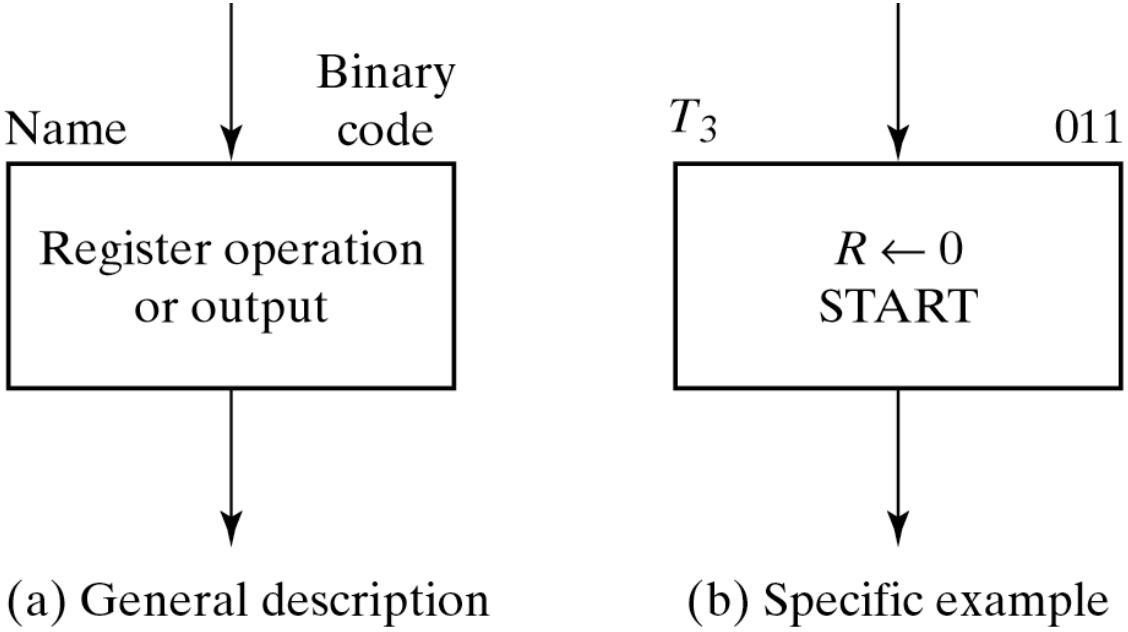


Fig. 8-3 State Box

Decision Box

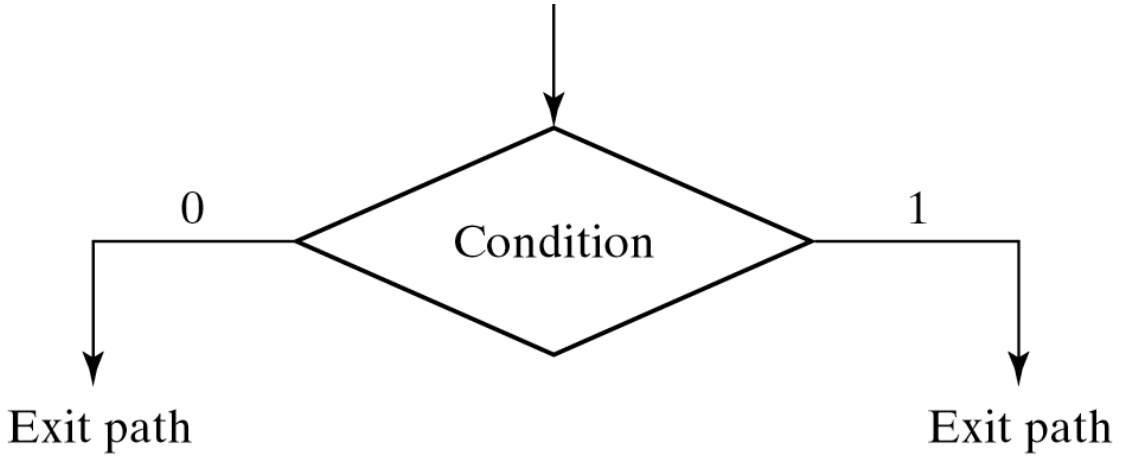


Fig. 8-4 Decision Box

Conditional Box

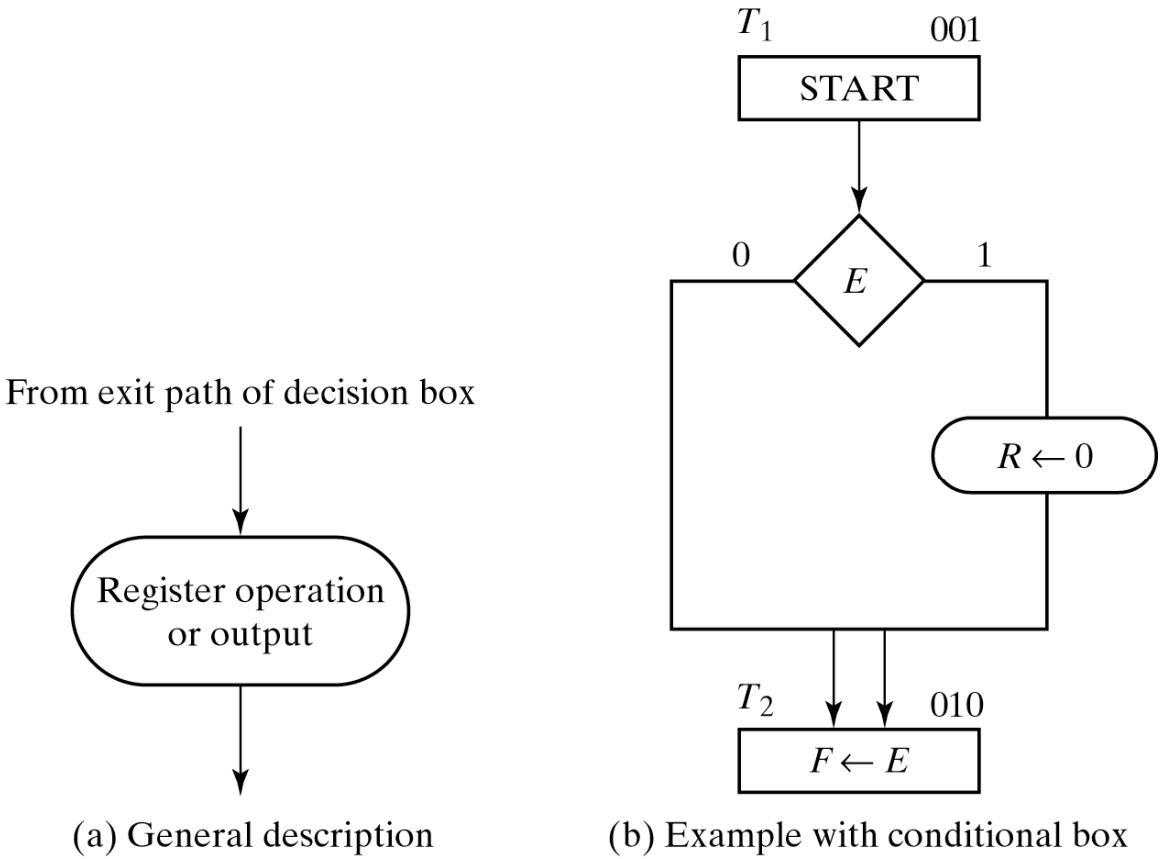


Fig. 8-5 Conditional Box

ASM Block

The operational unit executing datapath function in one time clock

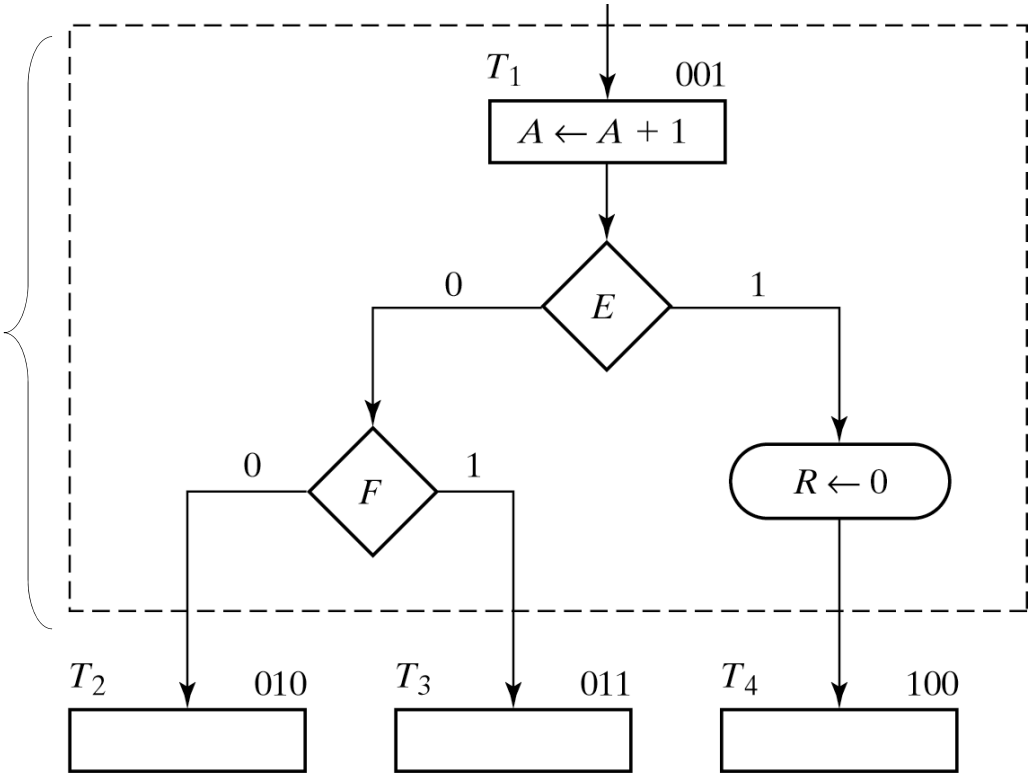


Fig. 8-6 ASM Block

Register Configuration

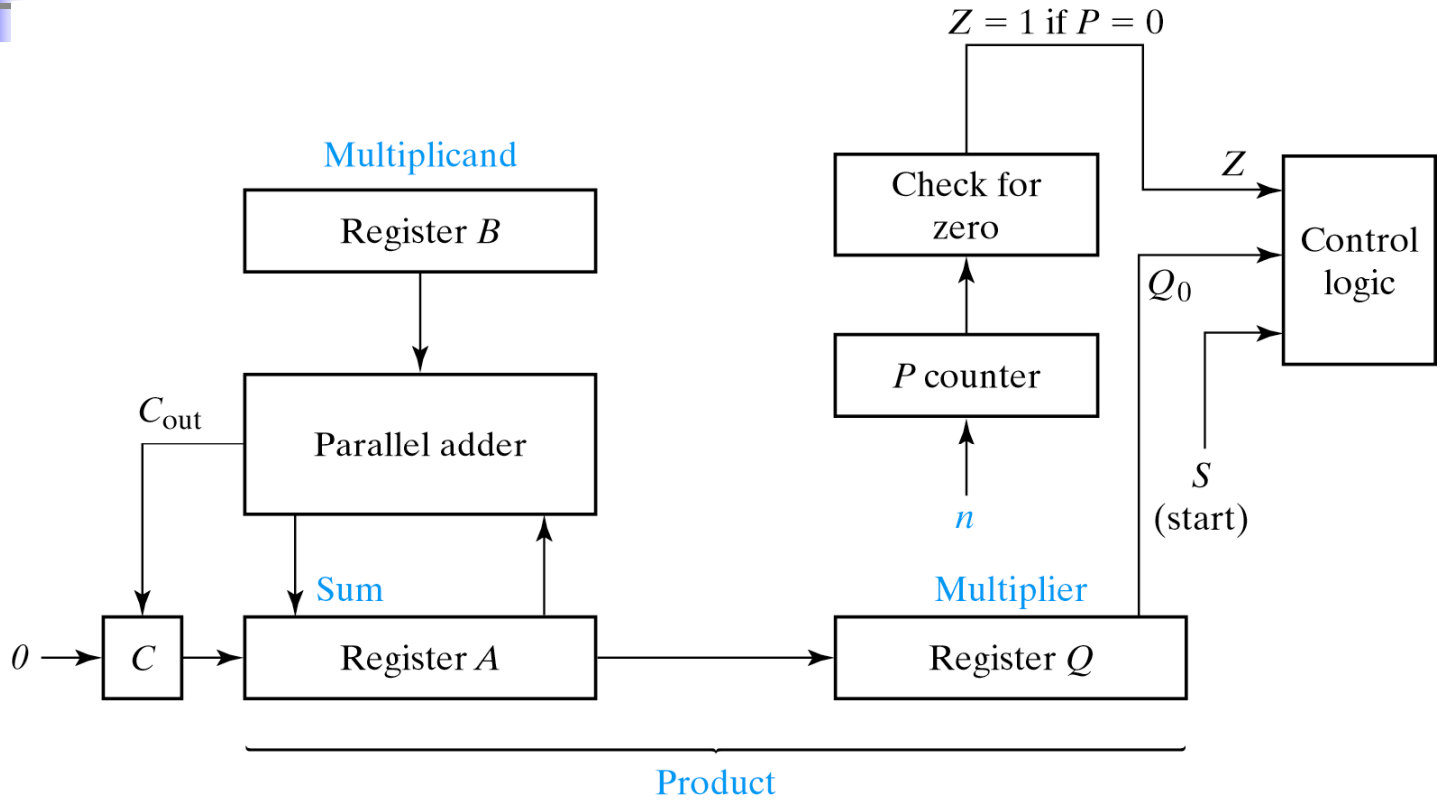


Fig. 8-13 Block Diagram of Binary Multiplier

ASM Chart of The Binary Multiplier

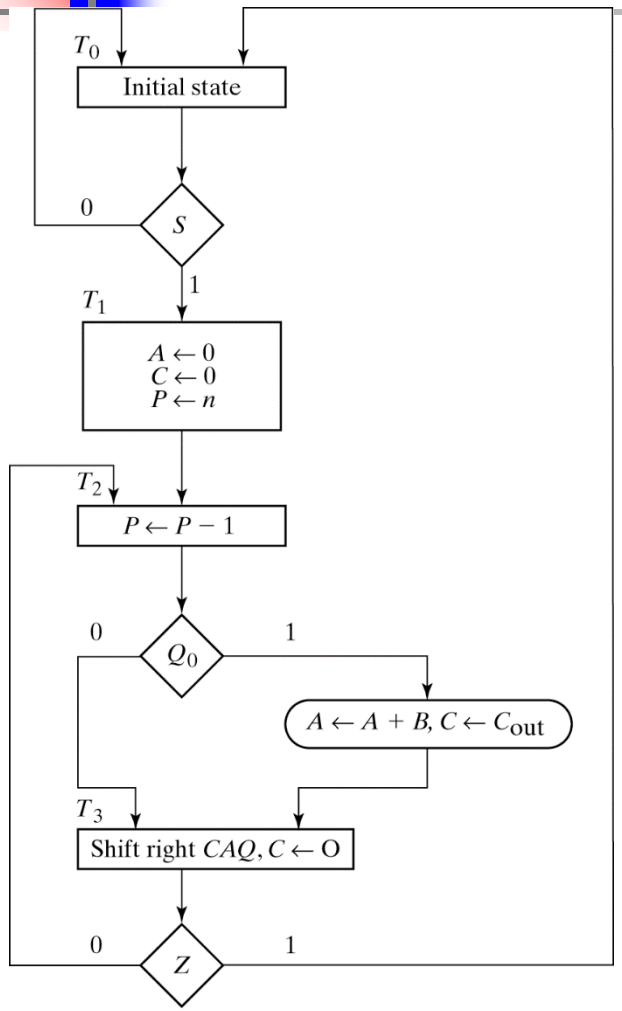
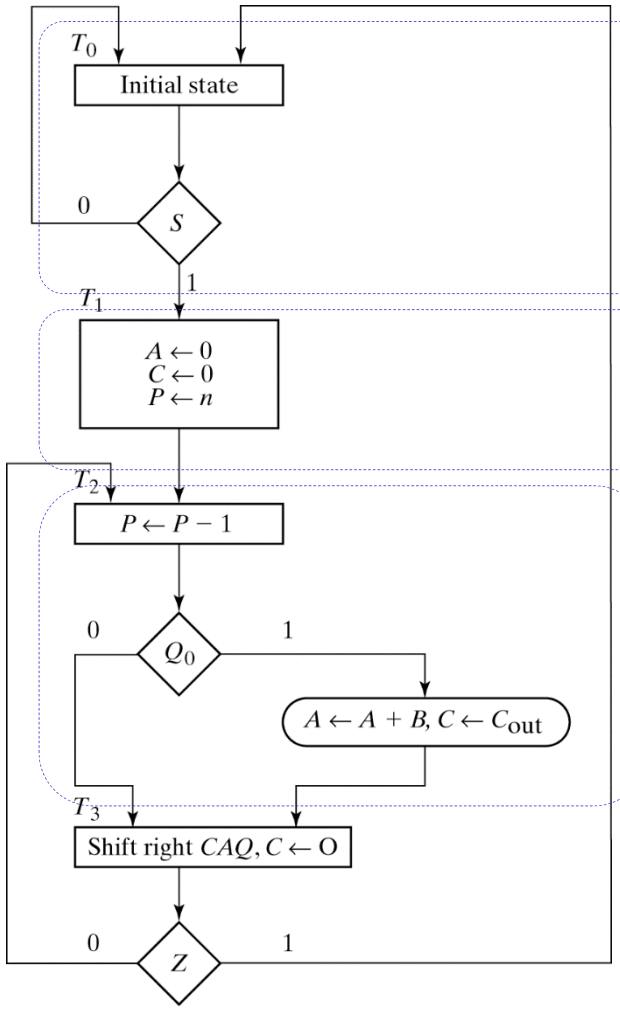


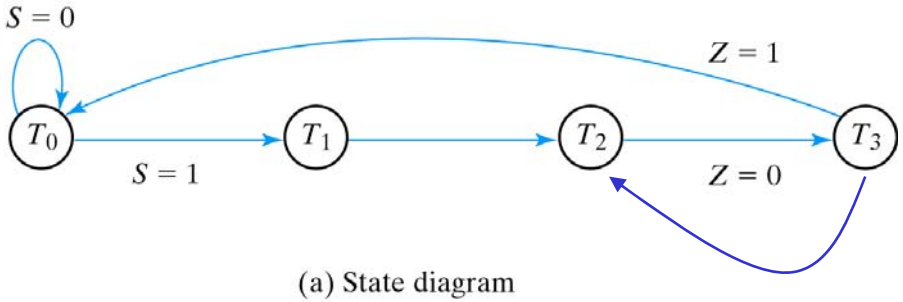
Fig. 8-14 ASM Chart for Binary Multiplier



ASM block

Fig. 8-14 ASM Chart for Binary Multiplier

Control Logic State Diagram



(a) State diagram

Z=0

T_0: Initial state

T_1: $A \leftarrow 0, C \leftarrow 0, P \leftarrow n$

T_2: $P \leftarrow P - 1$

if $(Q_0) = 1$ then $(A \leftarrow A + B, C \leftarrow C_{out})$

T_3: shift right $CAQ, C \leftarrow 0$

(b) Register transfer operations

Fig. 8-15 Control Specifications for Binary Multiplier

Control Block Diagram

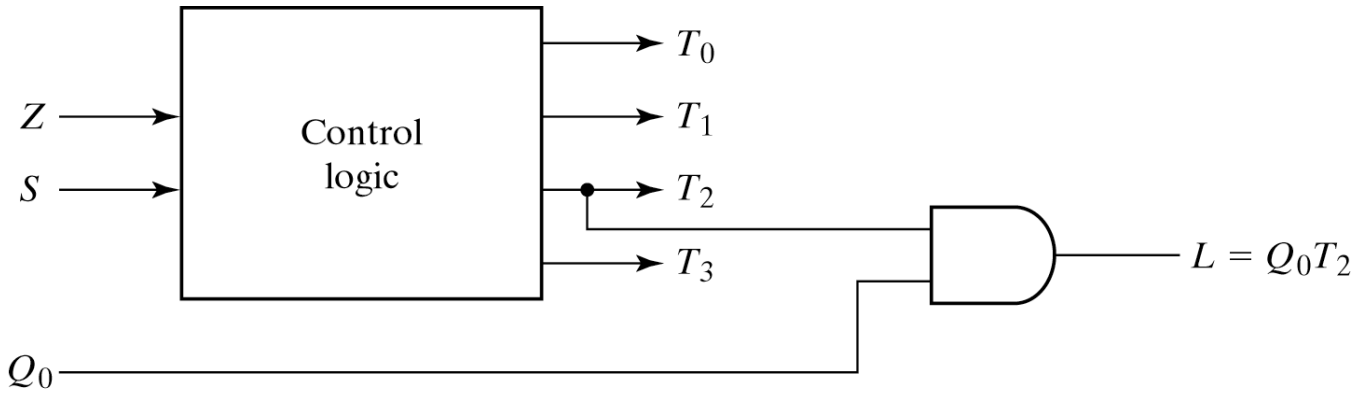


Fig. 8-16 Control Block Diagram

Sequence Register and Decoder

- State table for control circuits

Table 8-3
State Table for Control of Fig. 8-10

Present-State Symbol	Present State		Inputs			Next State		Outputs		
	G_1	G_0	S	A_3	A_4	G_1	G_0	T_0	T_1	T_2
T_0	0	0	0	X	X	0	0	1	0	0
T_0	0	0	1	X	X	0	1	1	0	0
T_1	0	1	X	0	X	0	1	0	1	0
T_1	0	1	X	1	0	0	1	0	1	0
T_1	0	1	X	1	1	1	1	0	1	0
T_2	1	1	X	X	X	0	0	0	0	1

$$D_{G1} = T_1 + T_2 + T_{3Z}' \qquad D_{G0} = T_0 S + T_2$$

Control Logic Diagram

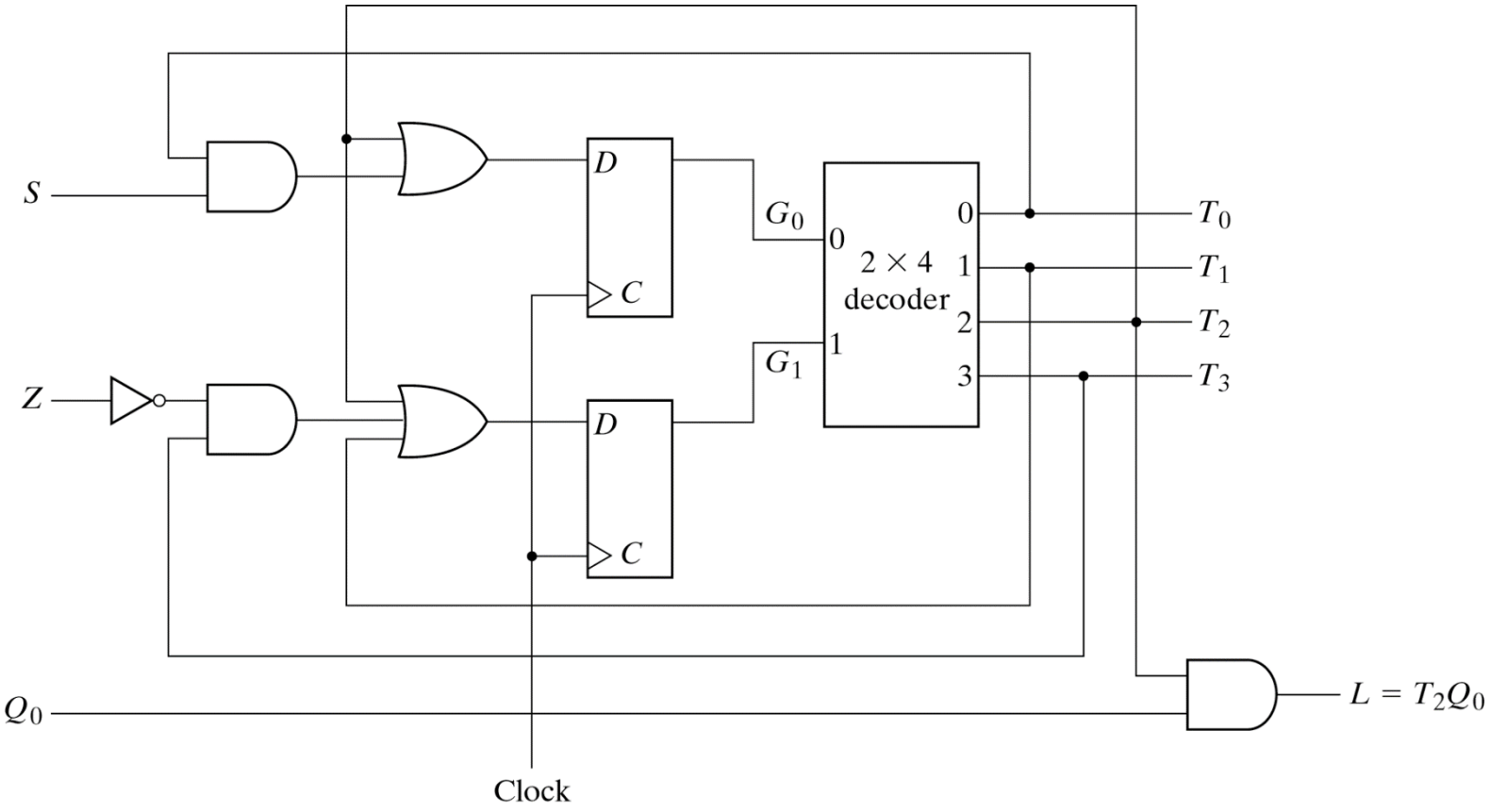


Fig. 8-17 Logic Diagram of Control for Binary Multiplier Using a Sequence Register and Decoder

One Flip-Flop per State

- State diagram ⇒ F-F input equations

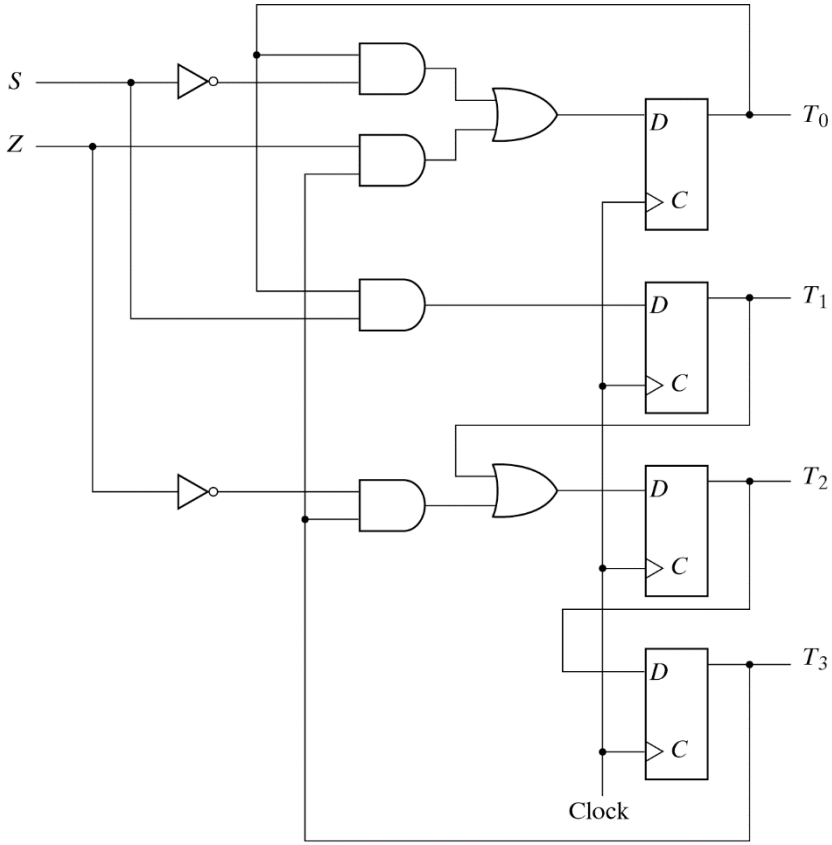


Fig. 8-18 One Flip-Flop Per State Controller