Chapter 2

1. 8

4. DPTR or PC (program counter)
5. Necessary
6. 28H, A
7. (a), (d), (f), and (g)
8. (a), (c), (d), (f), and (g)

18. No
19. They are not real code (real code produces op code). Pseudo-instructions only give instruction to the assembler and does not generate opcodes.

22. It executes whatever is at location 0000h which could be garbage in this case.
23. (a) 2 bytes
(b) 2 bytes
(c) 1 byte
(d) 2 bytes
(e) 1 byte
(f) 1byte
(g) 1 byte

27. 32K
28. 1K

34. when there is a carry from D7
35. when there is a carry from D3 to D4

37. (a) CY = 1
(b) CY = 0
(c) CY = 0

41. Bank 1

45. (a) RAM Location 04
(b) RAM Location 00
(c) RAM Location 07
(d) RAM Location 05
46. (a) RAM Location 14h
(b) RAM Location 10h
(c) RAM Location 17h
(d) RAM Location 15h

48.

Instruction	SP	Stack
ORG 0		
MOV R0,#66H	0x07	
MOV R3,#7FH	0x07	
MOV R7,#5DH	0x07	
PUSH 0	0x08	66
PUSH 3	0x09	66 7F
PUSH 7	0x0A	66 7F 5D

CLR A	0x0A	66 7F 5D
MOV R3,A	0x0A	66 7F 5D
MOV R7,A	0x0A	66 7F 5D
POP 3	0x09	66 7F
POP 7	0x08	66
POP 0	0x07	

Chapter 8

8. Low, High
9. 0000
10. 07

12.

	12 MHz	20 MHz	25 MHz	30 MHz
AT89C51	1 μs	0.6 μs	0.48 μs	0.4 μs
DS5000	0.333 μs	0.2 μs	0.16 μs	0.133 μs
DS89C4x0	83.3 ns	50 ns	40 ns	33.3 ns

41. (1) The colon starts the line.
(2) The first byte after the colon (10h) indicates that there will be 16 data bytes in this line.
(3) The next two bytes (0000h) indicate the ROM address that the first data byte should be burned into.
(4) The next byte (00h) shows that this is not the last line of the program.
(5) The next sixteen bytes are the op-codes and their operand data.
(6) And the last byte is the check-sum byte of the previous bytes in the line.

43. Calculation of the check-sum byte:
10h + 00h + 00h + 00h + 75h + 80h + 55h + 75h + 90h + 55h +75h + A0h + 55h + 7Dh + FAh + 11h + 1Ch + 75h + 80h + AAh = 761h
Dropping the carries: 61h
2's complement of 61h: 9Fh
Verification of the check-sum byte: 10h + 00h + ... + 80h + AAh + 9Fh = 800h
Dropping the carries: 00h, so 9Fh is the correct check-sum byte of the line.