PROBLEMS

SECTION 2.1: INSIDE THE 8051

1. Most registers in the 8051 are _____ bits wide.
2. Registers R0 - R7 are all _____ bits wide
3. Registers ACC and B are _____ bits wide.
4. Name a 16-bit register in the 8051.
5. To load R4 with the value 65H, the pound sign is _____ (necessary, optional) in the instruction "MOV R4,#65H".
6. What is the result of the following code and where is it kept?

```
MOV  A,#15H
MOV  R2,#13H
ADD  A,R2
```

7. Which of the following is (are) illegal?

(a) `MOV R3,#500` (b) `MOV R1,#50` (c) `MOV R7,#00`
(d) `MOV A,#255H` (e) `MOV A,#50H` (f) `MOV A,#F5H`
(g) `MOV R9,#50H`

8. Which of the following is (are) illegal?

(a) `ADD R3,#50H` (b) `ADD A,#50H` (c) `ADD R7,R4`
(d) `ADD A,#255H` (e) `ADD A,R5` (f) `ADD A,#F5H`
(g) `ADD R3,A`

9. What is the result of the following code and where is it kept?

```
MOV  R4,#25H
MOV  A,#1FH
ADD  A,R4
```

10. What is the result of the following code and where is it kept?

```
MOV  A,#15
MOV  R5,#15
ADD  A,R5
```

SECTION 2.2: INTRODUCTION TO 8051 ASSEMBLY PROGRAMMING AND
SECTION 2.3: ASSEMBLING AND RUNNING AN 8051 PROGRAM

11. Assembly language is a_____ (low, high) -level language while C is a _____ (low, high) -level language.
12. Of C and Assembly language, which is more efficient in terms of code generation (i.e., the amount of ROM space it uses)?
13. Which program produces the "obj" file?
14. True or false. The source file has the extension "src" or "asm".
15. Which file provides the listing of error messages?
16. True or false. The source code file can be a non-ASCII file.
17. True or false. Every source file must have ORG and END directives.
18. Do the ORG and END directives produce opcodes?
19. Why are the ORG and END directives also called pseudocode?
20. True or false. The ORG and END directives appear in the ".lst" file.

21. Every 8051 family member wakes up at address _____ when it is powered up.
22. A programmer puts the first opcode at address 100H. What happens when the microcontroller is powered up?
23. Find the number of bytes each of the following instructions takes.
    (a) `MOV A,#55H` (b) `MOV R3,#3` (c) `INC R2`
    (d) `ADD A,#0` (e) `MOV A,R1` (f) `MOV R3,A`
    (g) `ADD A,R2`
24. Pick up a program listing of your choice, and show the ROM memory addresses and their contents.
25. Find the address of the last location of on-chip ROM for each of the following.
    (a) DS5000-16 (b) DS5000-8 (c) DS5000-32
    (d) AT89C52 (e) 8751 (f) AT89C51
    (g) DS5000-64
26. Show the lowest and highest values (in hex) that the 8051 program counter can take.
27. A given 8051 has 7FFFH as the address of its last location of on-chip ROM. What is the size of on-chip ROM for this 8051?
28. Repeat Question 27 for 3FFH.

SECTION 2.5: 8051 DATA TYPES AND DIRECTIVES

29. Compile and state the contents of each ROM location for the following data.

```
            ORG   200H
MYDAT_1:    DB    "Earth"
MYDAT_2:    DB    "987-65"
MYDAT_3:    DB    "GABEH 98"
```

30. Compile and state the contents of each ROM location for the following data.

```
            ORG   340H
DAT_1:      DB    22,56H,10011001B,32,0F6H,11111011B
```

SECTION 2.6: 8051 FLAG BITS AND THE PSW REGISTER

31. The PSW is a(n) _____ -bit register.
32. Which bits of PSW are used for the CY and AC flag bits, respectively?
33. Which bits of PSW are used for the OV and P flag bits, respectively?
34. In the ADD instruction, when is CY raised?
35. In the ADD instruction, when is AC raised?
36. What is the value of the CY flag after the following code?

```
CLR   C             ;CY = 0
CPL   C             ;complement carry
```

37. Find the CY flag value after each of the following codes.

```
(a) MOV A,#54H      (b) MOV A,#00     (c) MOV A,#250
    ADD A,#0C4H         ADD A,#0FFH       ADD A,#05
```

38. Write a simple program in which the value 55H is added 5 times.

39. Which bits of the PSW are responsible for selection of the register banks?
40. On power-up, what is the location of the first stack?
41. In the 8051, which register bank conflicts with the stack?
42. In the 8051, what is the size of the stack pointer (SP) register?
43. On power-up, which of the register banks is used?
44. Give the address locations of RAM assigned to various banks.
45. Assuming the use of bank 0, find at what RAM location each of the following lines stored the data.
    (a) `MOV R4,#32H` (b) `MOV R0,#12H`
    (c) `MOV R7,#3FH` (d) `MOV R5,#55H`
46. Repeat Problem 45 for bank 2.
47. After power-up, show how to select bank 2 with a single instruction.
48. Show the stack and stack pointer for each line of the following program.

```
        ORG  0
MOV     R0,#66H
MOV     R3,#7FH
MOV     R7,#5DH
PUSH    0
PUSH    3
PUSH    7
CLR     A
MOV     R3,A
MOV     R7,A
POP     3
POP     7
POP     0
```

49. In Problem 48, does the sequence of POP instructions restore the original values of registers R0, R3, and R7? If not, show the correct sequence of instructions.
50. Show the stack and stack pointer for each line of the following program.

```
        ORG  0
MOV     SP,#70H
MOV     R5,#66H
MOV     R2,#7FH
MOV     R7,#5DH
PUSH    5
PUSH    2
PUSH    7
CLR     A
MOV     R2,A
MOV     R7,A
POP     7
POP     2
POP     5
```

Example 8-5

Compare the data portion of the Intel hex file of Figure 8-9 with the opcodes in the list file of the test program given in Figure 8-8. Do they match?

Solution:

In the first line of Figure 8-9, the data portion starts with 75H, the opcode for the instruction "MOV", as shown in the list file of Figure 8-8. The last byte of the data in line 3 of Figure 8-9 is 22, which is the opcode for the "RET" instruction in the list file of Figure 8-8.

Review Questions

1. True or false. The Intel hex file uses the checksum byte method to ensure data integrity.
2. The first byte of a line in the Intel hex file represents ____.
3. The last byte of a line in the Intel hex file represents ____.
4. In the TT field of the Intel hex file, we have 00. What does it indicate?
5. Find the checksum byte for the following values: 22H, 76H, 5FH, 8CH, 99H.
6. In Question 5, add all the values and the checksum byte. What do you get?

SUMMARY

This chapter began by describing the function of each pin of the 8051. The four ports of the 8051, P0, P1, P2, and P3, each use 8 pins, making them 8-bit ports. These ports can be used for input or output. Port 0 can be used for either address or data. Port 3 can be used to provide interrupt and serial communication signals. Then the design of the DS89C4x0-based trainer was shown. We also explained the Intel hex format.

PROBLEMS

SECTION 8.1: PIN DESCRIPTION OF THE 8051

1. The 8051 DIP package is a ____-pin package.
2. Which pins are assigned to V_{CC} and GND?
3. In the 8051, how many pins are designated as I/O port pins?
4. The crystal oscillator is connected to pins ____ and ____.
5. If an 8051 is rated as 25 MHz, what is the maximum frequency that can be connected to it?
6. Indicate the pin number assigned to RST in the DIP package.
7. RST is an _____ (input, output) pin.
8. The RST pin is normally _____ (low, high) and needs a _____ (low, high) signal to be activated.
9. What are the contents of the PC (program counter) upon RESET of the 8051?

10. What are the contents of the SP register upon RESET of the 8051?
11. What are the contents of the A register upon RESET of the 8051?
12. Find the machine cycle for the following crystal frequencies connected to X1 and X2.
    (a) 12 MHz (b) 20 MHz (c) 25 MHz (d) 30 MHz
13. $\overline{EA}$ stands for _____ and is an_____ (input, output) pin.
14. For 8051 family members with on-chip ROM such as the 8751 and the 89C51, pin $\overline{EA}$ is connected to _____ (V_{CC}, GND).
15. $\overline{PSEN}$ is an _____ (input, output) pin.
16. ALE is an _____ (input, output) pin.
17. ALE is used mainly in systems based on the _____ (8051, 8031).
18. How many pins are designated as P0 and what are those in the DIP package?
19. How many pins are designated as P1 and what are those in the DIP package?
20. How many pins are designated as P2 and what are those in the DIP package?
21. How many pins are designated as P3 and what are those in the DIP package?
22. Upon RESET, all the bits of ports are configured as _____ (input, output).
23. In the 8051, which port needs a pull-up resistor to be used as I/O?
24. Which port of the 8051 does not have any alternate function and can be used solely for I/O?

SECTION 8.2: DESIGN AND TEST OF DS89C4X0 TRAINER

25. Write a program to get 8-bit data from P1 and send it to ports P0, P2, and P3.
26. Write a program to get 8-bit data from P2 and send it to ports P0 and P1.
27. In P3, which pins are for RxD and TxD?
28. At what memory location does the 8051 wake up upon RESET? What is the implication of that?
29. Write a program to toggle all the bits of P1 and P2 continuously
    (a) using AAH and 55H (b) using the CPL instruction.
30. What is the address of the last location of on-chip ROM for the AT89C51?
31. What is the address of the last location of on-chip ROM for the DS89C420?
32. What is the address of the last location of on-chip ROM for the DS89C440?
33. What is the address of the last location of on-chip ROM for the DS89C450?
34. What is the fastest frequency that DS89C4x0 can run on?
35. What is the slowest frequency that DS89C4x0 can run on?
36. Calculate the machine cycle time for the DS89C430 if XTAL = 33 MHz.
37. Before we reprogram the DS89C4x0 we must _____ (dump, erase) the flash ROM.
38. True or false. In order to download the hex file into the DS89C4x0, it must be in the Intel hex file format.
39. Give two features of the DS89C4x0 that earlier 8051 and 8052 chips do not have.
40. After downloading a program, the DS89C4x0 gives the message ">GGGG". What does it mean?

SECTION 8.3: EXPLAINING THE INTEL HEX FILE

41. Analyze the six parts of line 1 of Figure 8-9.
42. Analyze the six parts of line 2 of Figure 8-9.
43. Verify the checksum byte for line 1 of Figure 8-9 and also verify that the information is not corrupted.
44. Verify the checksum byte for line 2 of Figure 8-9 and also verify that the information is not corrupted.
45. Reassemble the test program with ORG address of 100H and analyze the Intel hex file.
46. Reassemble the test program with ORG address of 300H and compare the Intel hex file with the results of Problem 45.
47. Write a program to toggle all the bits of P1 and P2 continuously with no delay and analyze the Intel hex file.

ANSWERS TO REVIEW QUESTIONS

SECTION 8.1: PIN DESCRIPTION OF THE 8051

1. From 0 to 16 MHz, but no more than 16 MHz
2. EA
3. PC = 0000
4. 0000
5. Port 0

SECTION 8.2: DESIGN AND TEST OF DS89C4X0 TRAINER

1. True
2. Pin 9
3. Low
4. Flash
5. Serial
6. a) It comes with a loader inside the chip and b) it has two serial ports
7. The SW allows to load the program or to run it.
8. 33 MHz
9. True
10. >K
11. >L
12. >D

SECTION 8.2: EXPLAINING INTEL THE HEX FILE

1. True
2. The number of bytes of data in the line
3. Checksum byte
4. 00 means this is not the last line and there are more lines of data to be followed.
5. 22H + 76H + 5FH + 8CH + 99H = 21CH. Dropping the carries we have 1CH and its 2's complement is E4H.
6. 22H + 76H + 5FH + 8CH + 99H + E4 = 300H. Dropping the carries we have 00, which means data is not corrupted.