PROBLEMS

SECTION 3.1: LOOP AND JUMP INSTRUCTIONS

1. In the 8051, looping action with the instruction "`DJNZ Rx,rel address`" is limited to ____ iterations.
2. If a conditional jump is not taken, what is the next instruction to be executed?
3. In calculating the target address for a jump, a displacement is added to the contents of register _____.
4. The mnemonic SJMP stands for _____ and it is a ___-byte instruction.
5. The mnemonic LJMP stands for _____ and it is a ___-byte instruction.
6. What is the advantage of using SJMP over LJMP?
7. True or false. The target of a short jump is within –128 to +127 bytes of the current PC.
8. True or false. All 8051 jumps are short jumps.
9. Which of the following instructions is (are) not a short jump?
   (a) JZ (b) JNC (c) LJMP (d) DJNZ
10. A short jump is a ___-byte instruction. Why?
11. True or false. All conditional jumps are short jumps.
12. Show code for a nested loop to perform an action 1000 times.
13. Show code for a nested loop to perform an action 100,000 times.
14. Find the number of times the following loop is performed.

```
        MOV  R6,#200
BACK:   MOV  R5,#100
HERE:   DJNZ R5,HERE
        DJNZ R6,BACK
```

15. The target address of a jump backward is a maximum of _____ bytes from the current PC.
16. The target address of a jump forward is a maximum of _____ bytes from the current PC.

SECTION 3.2: CALL INSTRUCTIONS

17. LCALL is a ___-byte instruction.
18. ACALL is a ___-byte instruction.
19. The ACALL target address is limited to ____ bytes from the present PC.
20. The LCALL target address is limited to ____ bytes from the present PC.
21. When LCALL is executed, how many bytes of the stack are used?
22. When ACALL is executed, how many bytes of the stack are used?
23. Why do the PUSH and POP instructions in a subroutine need to be equal in number?
24. Describe the action associated with the POP instruction.
25. Show the stack for the following code.

```
000B 120300        LCALL DELAY
000E 80F0          SJMP BACK     ;keep doing this
0010
0010 ;-------this is the delay subroutine
```

```
0300                    ORG 300H
0300          DELAY:
0300 7DFF               MOV  R5,#0FFH  ;R5=255
0302 DDFE   AGAIN:      DJNZ R5,AGAIN  ;stay here
0304 22                 RET            ;return
```

26. Reassemble Example 3-10 at ORG 200 (instead of ORG 0) and show the stack frame for the first LCALL instruction.

SECTION 3.3: TIME DELAY FOR VARIOUS 8051 CHIPS

27. Find the system frequency if the machine cycle = 1.2 µs.
28. Find the machine cycle if the crystal frequency is 18 MHz.
29. Find the machine cycle if the crystal frequency is 12 MHz.
30. Find the machine cycle if the crystal frequency is 25 MHz.
31. True or false. LJMP and SJMP instructions take the same amount of time to execute even though one is a 3-byte instruction and the other is a 2-byte instruction.
32. Find the time delay for the delay subroutine shown to the right, if the system has an 8051 with frequency of 11.0592 MHz.

```
DELAY:    MOV  R3,#150
HERE:     NOP
          NOP
          NOP
          DJNZ R3,HERE
          RET
```

33. Find the time delay for the delay subroutine shown to the right, if the system has an 8051 with frequency of 16 MHz.

```
DELAY:    MOV  R3,#200
HERE:     NOP
          NOP
          NOP
          DJNZ R3,HERE
          RET
```

34. Find the time delay for the delay subroutine shown to the right, if the system has an 8051 with frequency of 11.0592 MHz.

```
DELAY:    MOV  R5,#100
BACK:     MOV  R2,#200
AGAIN:    MOV  R3,#250
HERE:     NOP
          NOP
          DJNZ R3,HERE
          DJNZ R2,AGAIN
          DJNZ R5,BACK
          RET
```

35. Find the time delay for the delay subroutine shown to the right, if the system has an 8051 with frequency of 16 MHz.

```
DELAY:    MOV  R2,#150
AGAIN:    MOV  R3,#250
HERE:     NOP
          NOP
          NOP
          DJNZ R3,HERE
          DJNZ R2,AGAIN
          RET
```

PROBLEMS

SECTION 4.1: 8051 I/O PROGRAMMING

1. The 8051 DIP package is a ____-pin package.
2. Which pins are assigned to V_{CC} and GND?
3. In the 8051, how many pins are designated as I/O port pins?
4. How many pins are designated as P0 and which number are they in the DIP package?
5. How many pins are designated as P1 and which number are they in the DIP package?
6. How many pins are designated as P2 and which number are they in the DIP package?
7. How many pins are designated as P3 and which number are they in the DIP package?
8. Upon RESET, all the bits of ports are configured as _____ (input, output).
9. In the 8051, which port needs a pull-up resistor in order to be used as I/O?
10. Which port of the 8051 does not have any alternate function and can be used solely for I/O?
11. Write a program to get 8-bit data from P1 and send it to ports P0, P2, and P3.
12. Write a program to get 8-bit data from P2 and send it to ports P0 and P1.
13. In P3, which pins are for RxD and TxD?
14. At what memory location does the 8051 wake up upon RESET? What is the implication of that?
15. Write a program to toggle all the bits of P1 and P2 continuously (a) using AAH and 55H (b) using the CPL instruction.

SECTION 4.2: I/O BIT MANIPULATION PROGRAMMING

16. Which ports of the 8051 are bit-addressable?
17. What is the advantage of bit-addressability for 8051 ports?
18. When P1 is accessed as a single-bit port, it is designated as _____.
19. Is the instruction "`CPL P1`" a valid instruction?
20. Write a program to toggle P1.2 and P1.5 continuously without disturbing the rest of the bits.
21. Write a program to toggle P1.3, P1.7, and P2.5 continuously without disturbing the rest of the bits.
22. Write a program to monitor bit P1.3. When it is high, send 55H to P2.
23. Write a program to monitor the P2.7 bit. When it is low, send 55H and AAH to P0 continuously.
24. Write a program to monitor the P2.0 bit. When it is high, send 99H to P1. If it is low, send 66H to P1.
25. Write a program to monitor the P1.5 bit. When it is high, make a low-to-high-to-low pulse on P1.3.
26. Write a program to get the status of P1.3 and put it on P1.4.
27. The P1.4 refers to which bit of P1?
28. Write a program to get the status of P1.7 and P1.6 and put them on P1.0 and P1.7, respectively.

Review Questions

1. True or false. The 8052 is an upgraded version of the 8051.
2. True or false. The 8052 has a total of 256 bytes of on-chip RAM in addition to the SFRs.
3. True or false. The extra 128 bytes of RAM in the 8052 is physically the same RAM as the SFR.
4. Give the address for the upper RAM of the 8052.
5. Show how to put value 99H into RAM location F6H of upper RAM in the 8052.

SUMMARY

This chapter described the five addressing modes of the 8051. Immediate addressing mode uses a constant for the source operand. Register addressing mode involves the use of registers to hold data to be manipulated. Direct or register indirect addressing modes can be used to access data stored in either RAM or registers of the 8051. Direct addressing mode is also used to manipulate the stack. Register indirect addressing mode uses a register as a pointer to the data. The advantage of this is that it makes addressing dynamic rather than static. Indexed addressing mode is widely used in accessing data elements of look-up table entries located in the program ROM space of the 8051.

A group of registers called the SFR (special function registers) can be accessed by their names or their addresses. We also discussed the bit-addressable ports, registers, and RAM locations and showed how to use single-bit instructions to access them directly.

PROBLEMS

SECTIONS 5.1 AND 5.2 IMMEDIATE AND REGISTER ADDRESSING MODES / ACCESSING MEMORY USING VARIOUS ADDRESSING MODES

1. Which of the following are invalid uses of immediate addressing mode?
   (a) MOV A,#24H (b) MOV R1,30H (c) MOV R4,#60H
2. Identify the addressing mode for each of the following.
   (a) MOV B,#34H (b) MOV A,50H (c) MOV R2,07
   (d) MOV R3,#0 (e) MOV R7,0 (f) MOV R6,#7FH
   (g) MOV R0,A (h) MOV B,A (i) MOV A,@R0
   (j) MOV R7,A (k) MOV A,@R1
3. Indicate the address assigned to each of the following.
   (a) R0 of bank 0 (b) ACC (c) R7 of bank 0
   (d) R3 of bank 2 (e) B (f) R7 of bank 3
   (g) R4 of bank 1 (h) DPL (i) R6 of bank 1
   (j) R0 of bank 3 (k) DPH (l) P0
4. Which register bank shares space with the stack?
5. In accessing the stack, we must use _____ addressing mode.

6. What does the following instruction do? "MOV A,0F0H"
7. What does the following instruction do? "MOV A,1FH"
8. Write code to push R0, R1, and R3 of bank 0 onto the stack and pop them back into R5, R6, and R7 of bank 3.
9. Which registers are allowed to be used for register indirect addressing mode when accessing data in RAM?
10. Write a program to copy FFH into RAM locations 50H to 6FH.
11. Write a program to copy 10 bytes of data starting at ROM address 400H to RAM locations starting at 30H.
12. Write a program to find y where $y = x^2 + 2x + 5$, and x is between 0 and 9.
13. Write a program to add the following data and store the result in RAM location 30H.

```
        ORG   200H
MYDATA: DB    06,09,02,05,07
```

SECTION 5.3: BIT ADDRESSES FOR I/O AND RAM

14. "SETB A" is a(n) _____ (valid, invalid) instruction.
15. "CLR A" is a(n) _____ (valid, invalid) instruction.
16. "CPL A" is a(n) _____ (valid, invalid) instruction.
17. Which I/O ports of P0, P1, P2, and P3 are bit-addressable?
18. Which registers of the 8051 are bit-addressable?
19. Which of the following instructions are valid? If valid, indicate which bit is altered.

(a) SETB P1	(b) SETB P2.3	(c) CLR ACC.5
(d) CLR 90H	(e) SETB B.4	(f) CLR 80H
(g) CLR PSW.3	(h) CLR 87H	

20. Write a program to generate a square wave with 75% duty cycle on bit P1.5.
21. Write a program to generate a square wave with 80% duty cycle on bit P2.7.
22. Write a program to monitor P1.4. When it goes high, the program will generate a sound (square wave of 50% duty cycle) on pin P2.7.
23. Write a program to monitor P2.1. When it goes low, the program will send the value 55H to P0.
24. What bit addresses are assigned to P0?
25. What bit addresses are assigned to P1?
26. What bit addresses are assigned to P2?
27. What bit addresses are assigned to P3?
28. What bit addresses are assigned to the PCON register?
29. What bit addresses are assigned to the TCON register?
30. What bit addresses are assigned to register A?
31. What bit addresses are assigned to register B?
32. What bit addresses are assigned to register PSW?
33. The following are bit addresses. Indicate where each one belongs.
    (a) 85H (b) 87H (c) 88H (d) 8DH (e) 93H (f) A5H
    (g) A7H (h) B3H (i) D4H (j) D7H (k) F3H
34. Write a program to save registers A and B on R3 and R5 of bank 2, respectively.

35. Give another instruction for "CLR C".
36. In Problem 19, assemble each instruction and state if there is any difference between them.
37. Show how you would check whether the OV flag is low.
38. Show how you would check whether the CY flag is high.
39. Show how you would check whether the P flag is high.
40. Show how you would check whether the AC flag is high.
41. Give the bit addresses assigned to the flag bit of CY, P, AC, and OV.
42. Of the 128 bytes of RAM locations in the 8051, how many of them are also assigned a bit address as well? Indicate which bytes those are.
43. Indicate the bit addresses assigned to RAM locations 20H to 2FH.
44. The byte addresses assigned to the 128 bytes of RAM are _____ to _____.
45. The byte addresses assigned to the SFR are _____ to _____.
46. Indicate the bit addresses assigned to both of the following. Is there a gap between them?
    (a) RAM locations 20H to 2FH (b) SFR
47. The following are bit addresses. Indicate where each one belongs.
    (a) 05H (b) 47H (c) 18H (d) 2DH (e) 53H (f) 15H
    (g) 67H (h) 55H (i) 14H (j) 37H (k) 7FH
48. True or false. The bit addresses of less than 80H are assigned to RAM locations 20 - 2FH.
49. True or false. The bit addresses of 80H and beyond are assigned to SFR (special function registers).
50. Write instructions to save the CY flag bit in bit location 4.
51. Write instructions to save the AC flag bit in bit location 16H.
52. Write instructions to save the P flag bit in bit location 12H.
53. Write instructions to see whether the D0 and D1 bits of register A are high. If so, divide register A by 4.
54. Write a program to see whether the D7 bit of register A is high. If so, send a message to the LCD stating that ACC has a negative number.
55. Write a program to see whether the D7 bit of register B is low. If so, send a message to the LCD stating that register B has a positive number.
56. Write a program to set high all the bits of RAM locations 20H to 2FH using the following methods:
    (a) byte addresses (b) bit addresses
57. Write a program to see whether the accumulator is divisible by 8.
58. Write a program to find the number of zeros in register R2.

SECTION 5.4: EXTRA 128-BYTE ON-CHIP RAM IN 8052

59. What is the total number of bytes of RAM in the 8052 including the SFR registers? Contrast that with the 8051.
60. What addressing mode is used to access the SFR?
61. What addressing mode is used to access the upper 128 bytes of RAM in the 8052?
62. Give the address range of the lower and the upper 128 bytes of RAM in the 8052.

63. In the 8052, the SFR shares the address space with the _____ (lower) upper) 128 bytes of RAM.
64. In Question 63, discuss if they are physically the same memory.
65. Explain what is the difference between these two instructions.
(a) `MOV 80H,#99H` (b) `MOV @R0,#99H` if R0=80H
66. Which registers can be used to access the upper 128 bytes of RAM in the 8052?
67. Write a program to put 55H into RAM locations C0 - CFH of upper memory.
68. Write a program to copy the contents of lower RAM locations 60 - 6FH to upper RAM locations D0 - DFH.

ANSWERS TO REVIEW QUESTIONS

SECTION 5.1: IMMEDIATE AND REGISTER ADDRESSING MODES

1. No
2. MOV R3,#10000000B
3. Source and destination registers' sizes do not match.
4. True
5. No

SECTION 5.2: ACCESSING MEMORY USING VARIOUS ADDRESSING MODES

1. Direct; because there is no "#" sign
2. 02
3. 12H
4. E0H
5. R0 and R1

SECTION 5.3: BIT ADDRESSES FOR I/O AND RAM

1. True
2. False
3. False
4. A, B, and PSW
5. 16 bytes are bit-addressable; they are from byte location 20H to 2FH.
6. MOV A,R3
   JNB ACC.0
7. For (a), (b), and (c) use Figure 5-1. (a) RAM byte 22H, bit D4
   (b) RAM byte 24H, bit D0 (c) RAM byte 22H, bit D2
   For (d) and (e) use Figure 5-2. (d) SETB P1.5 (e) SETB ACC.6
8. RAM bytes 00 - 20H, special function registers.
9. True
10. True

SECTION 5.4: EXTRA 128-BYTE ON-CHIP RAM IN 8052

1. True
2. True
3. False
4. 80 - FFH
5. MOV A,#99H
   MOV R0,#0F6H
   MOV @R0,A