## ELEE 204 Design Project

## DUE: Monday, April 9, 2018 and Monday, April 30, 2018

Working in groups of 2-4, solve a real world problem using digital logic tools, techniques and components from this class. Find a system or process around Grove City College that would be improved by creative use of digital logic. You don't need to build the actual system, just the digital logic behind the system.

Document the problem in an objective way. Describe your design goals, assigning an appropriate priority to each (i.e. some goals are more important than others). Design a circuit diagram, aka your schematic. Then implement the design on a breadboard or on the Altera board. Perform tests to verify the design matches the problem and goals. You will likely have to simulate inputs and maybe outputs. Document your design goals, key decisions, rationale for those decisions, circuit diagram, VHDL code (if you use any), test results and an evaluation of the project. The evaluation includes how well your design solves the problem and how your overall process went. This documentation should be 3-5 pages (more is fine).

**Individually**, fill out the peer evaluation form (in the course network folder) and email me the 3rd page. Include yourself in the evaluation. This information is confidential and will not be used to alter your teammates' scores.

On the first due date, you will meet with me as a group and show me your design goals and draft design. You will discuss your specific roles on the project.

On the final due date, you will turn in the final product, including your peer evaluation.

It is a good idea to talk to me after coming up with a preliminary problem statement and a rough idea of the design approach.

## **Grading Criteria**

- clear and thorough documentation that includes all prescribed components
- an appropriate problem that illustrates your skills
- good use of digital logic principles and documentation
- meaningful description of your role and evaluation of teammates
- grammar and spelling
- working product