Sequential Circuits

Question 1: Which of the following 8 bit registers are grouped together to form 16 bit registers?
A. B and C
B. B and D
C. A and B
D. None of the above

Question 2: Which of the following flag is not present in 8085?
A. Carry
B. Zero
C. Parity
D. Trap

Question 3: In 8085 microprocessor, data-bus and address bus are multiplexed in order to
A. Increase the speed of microprocessor.
B. Reduce the number of pins.
C. Connect more peripheral chips.
D. None of the above

Question 4: ALU (Arithmetic and Logic Unit) of 8085 microprocessor consists of
A. Accumulator, temporary register, arithmetic and logic circuits
B. Accumulator, arithmetic, logic circuits and five flags
C. Accumulator, arithmetic and logic circuits
D. Accumulator, temporary register, arithmetic, logic circuits and five flags

Question 5: Which of the following statements for Intel 8085 is correct?
A. Program Counter (PC) specifies the address of the instruction last executed
B. PC specifies the address of the instruction being executed
C. PC specifies the address of the next instruction to be executed
D. PC specifies the number of instructions executed so far

Question 6: In which of the following data and address cannot be fetched simultaneously?
A. Harvard
B. Von neumann
C. Both
D. None

Question 7: In RISC instruction size is variable?

A. True
B. False

Question 8:
8085:: Address Bus : _____:: Data Bus : _____
A. 16, 16
B. 8, 16
C. 16,8
D. None of the above

Question 9: Which of the following interrupt is not present in 8085?
A. RST 7.5
B. INTA
C. TRAP
D. None of the above

Question 10: Which of the following is non maskable interrupt?
A. INTR
B. RST 6.5
C. TRAP
D. RST 7.5

Question 11: Causing a flag to became 0 is called:
A. Clearing a flag
B. Case a flag
C. Both a and b
D. None of these

Question 12: In which register instruction is decoded prepared and ultimately executed:
A. Instruction register
B. Current register
C. Both a and b
D. None of these

Question 13: Single address computer instruction has two parts:
A. The operation code
B. The operand
C. A and B

D. None of these

Question 14: Stack works on:
A. LILO
B. LIFO
C. FIFO
D. None of these

Question 15: The CPU yields control of the bus to the DMA controller via:
A. DMA acknowledge signal
B. DMA integrated signal
C. DMA implicitly signal
D. None of these

Question 16: The point where control returns after a subprogram is completed is known as the :
A. Return address
B. Main Address
C. Program Address
D. Current Address

Question 17: The processor 80386/80486 and the Pentium processor uses _____ bits address bus:
A. 16
B. 32
C. 36
D. 64

Question 18: The processor uses the stack to keep track of where the items are stored on it this by using the:
A. Stack pointer register
B. Queue pointer register
C. Both a & b
D. None of these

Question 19: The subprogram finish the return instruction recovers the return address from the:
A. Queue
B. Stack

C. Program counter
D. Pointer

Question 20: Which bus carry addresses:
A. System bus
B. Address bus
C. Control bus
D. Data bus

Question 21: _____ subsystem that transfers data between computer components inside a computer or between computers:
A. Chip
B. Register
C. Processor
D. Bus

Question 22: _____ Stores the instruction currently being executed:
A. Instruction register
B. Current register
C. Both a and b
D. None of these

Question 23: In 8085, multiplication is done by
A. MLI B
B. MUL B
C. Both A and B
D. None of the above

Question 24: Accumulator contains 4DH, what will be the value of flags after executing following instruction
ADI 59H
A. Ac = 0, P = 1, C = 0
B. Ac = 1, P = 0, C = 0
C. Ac = 1, P = 0, C = 1
D. None of the above

Question 25: What will be the value of accumulator after executing following command?

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SBI 37H borrow = 1, A=37H
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A. -1

B. FFH

C. 0377

D. All of the above

E. None of the above

Question 26: What will be the value of accumulator after executing following instructions

MVI A, 49H

MVI C, 12H

ORA C

A. 5BH

B. 5AH

C. 4AH

D. 4BH

Question 27: Bus interface unit is not responsible for

A. sends address of the memory or IO

B. supports instruction queuing

C. supports arithmetic operations

D. provides address relocation facility

Question 28: Find the status of CF, SF, and AF after the following instructions are executed.

MOV AL, 35 H

ADD AL, 0CE H

A. CF = 0, SF = 1, AF = 1

B. CF = 1, SF = 1, AF = 1

C. CF = 1, SF = 0, AF = 1

D. CF = 1, SF = 0, AF = 0

Question 29: Assume that CS register=3000 H and IP =2000 H. To fetch an instruction form the memory, find the memory address from which the next instruction will be fetched.

A. 3200H

B. 32000H

C. 3200

D.32000

Question 30: Assume that, SS=3000 H, BP=0010 H, SI=0040 H Find the physical address in following instruction.
MOV AL, [BP+SI]

A. 30050H

B. 30040H

C. 30010H

D. None of the above