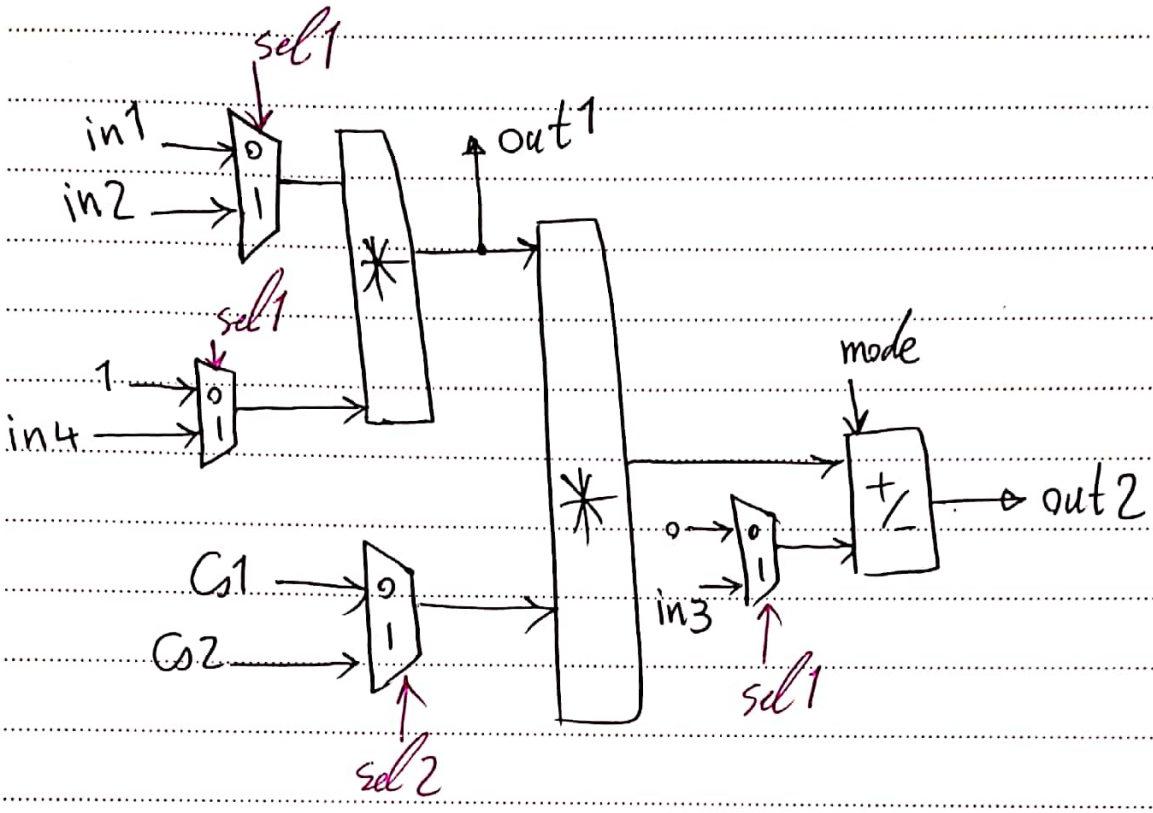
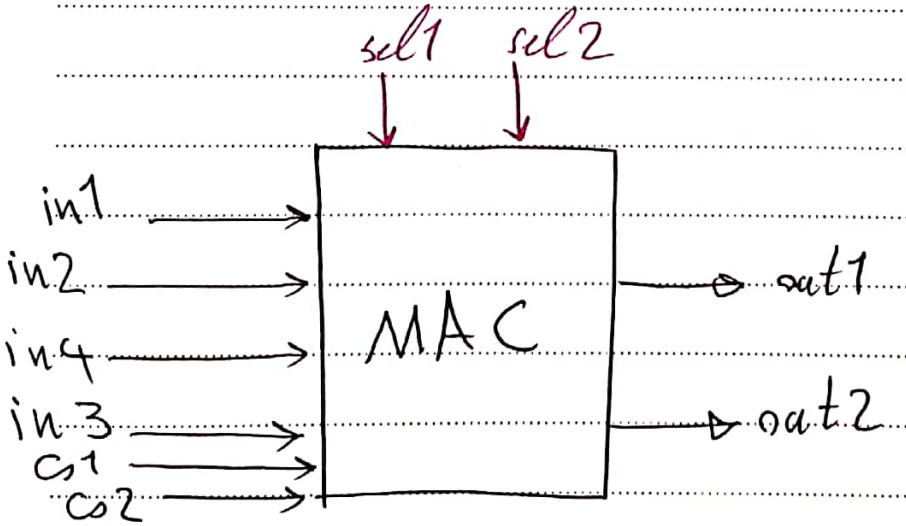
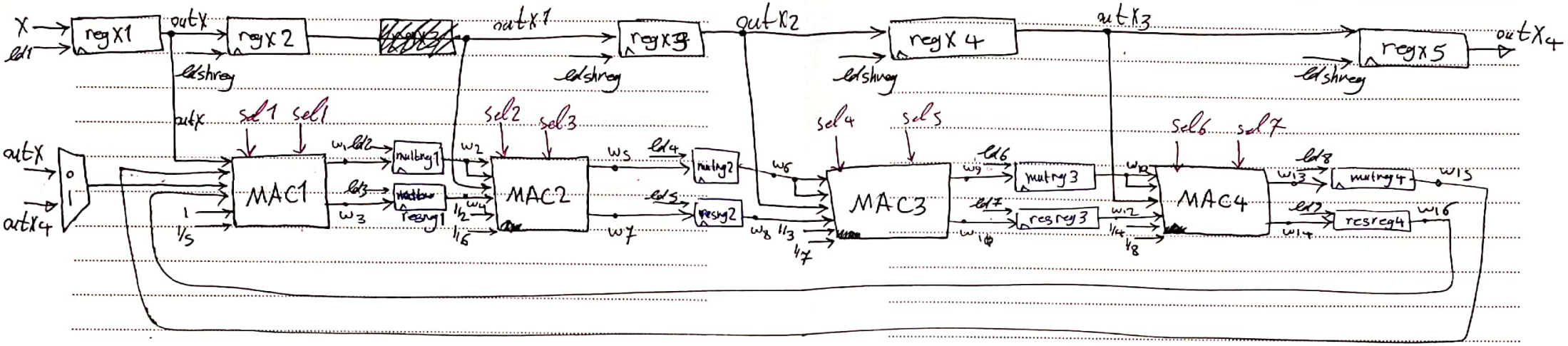
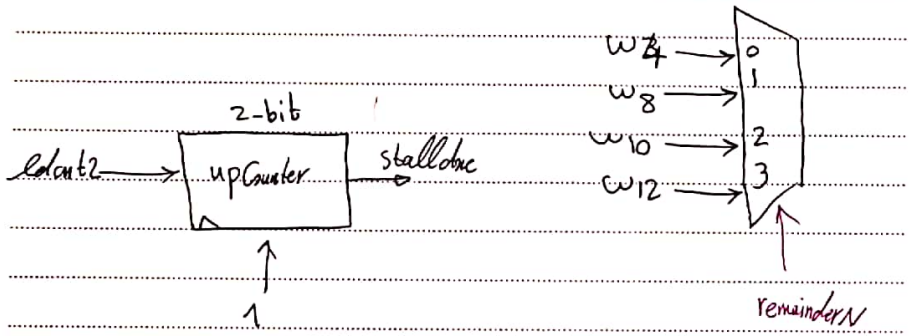
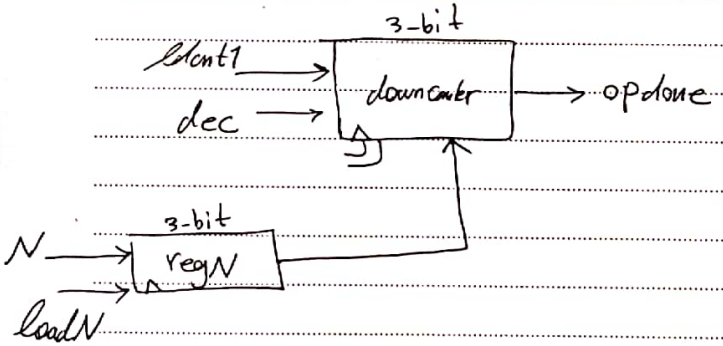
MAC Block :

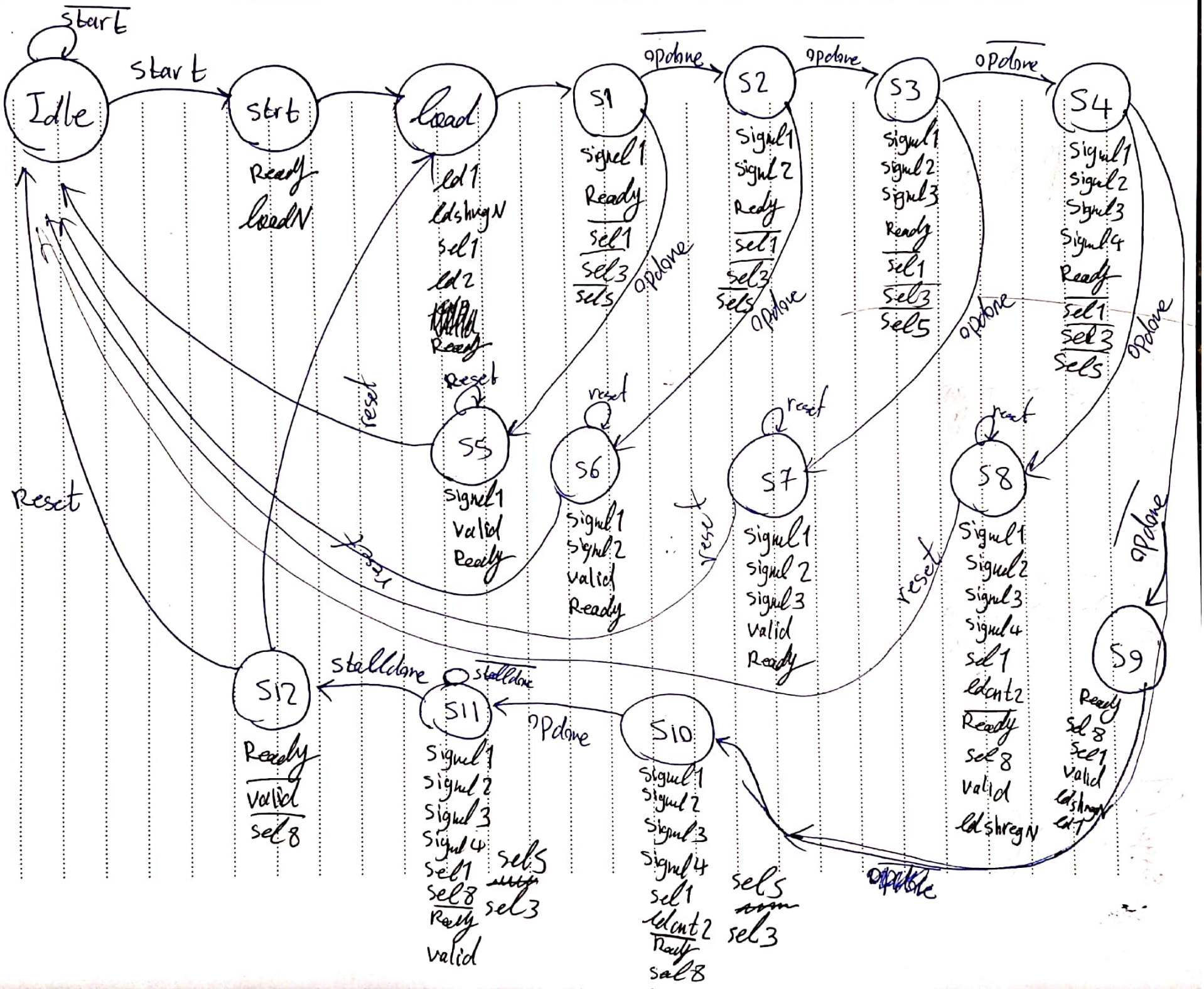

sel1
in1
in2
0
1
out1
sel1
1
in4
0
1
mode
+/-
out2
Cs1
Cs2
0
1
0
1
in3
sel2
sel1


sel1
sel2
in1
in2
in4
in3
Cs1
Cs2
MAC
out1
out2


X
ld1
regX1
outX
regX2
ldshreg
outX1
regX3
ldshreg
outX2
regX4
ldshreg
outX3
regX5
ldshreg
outX4
outX
outX4
sel1
sel1
sel2
sel3
sel4
sel5
sel6
sel7
MAC1
MAC2
MAC3
MAC4
multreg1
resreg1
multreg2
resreg2
multreg3
resreg3
multreg4
resreg4
w1
w2
w3
w4
w5
w6
w7
w8
w9
w10
w12
w13
w14
w15
w16
ld2
ld3
ld4
ld5
ld6
ld7
ld8
1
1/5
1/2
1/6
1/3
1/7
1/4
1/8


2-bit
ldcnt2
upCounter
stalldone
1
w4
w8
w10
w12
0
1
2
3
remainderN


3-bit
ldcnt1
dec
downcounter
opdone
3-bit
N
regN
loadN


start
Idle
start
strt
Ready
loadN
load
ld1
ldshregN
sel1
ld2
Ready
Reset
S1
Signal1
Ready
sel1
sel3
sel5
opdone
S2
Signal1
Signal2
Ready
sel1
sel3
sel5
S3
Signal1
Signal2
Signal3
Ready
sel1
sel3
sel5
S4
Signal1
Signal2
Signal3
Signal4
Ready
sel1
sel3
sel5
S5
Signal1
Valid
Ready
S6
Signal1
Signal2
Valid
Ready
S7
Signal1
Signal2
Signal3
Valid
Ready
S8
Signal1
Signal2
Signal3
Signal4
sel1
ldcnt2
Ready
sel8
Valid
ldshregN
S9
Ready
sel8
sel1
Valid
ldshregN
ld1
S10
Signal1
Signal2
Signal3
Signal4
sel1
ldcnt2
Ready
sel8
S11
Signal1
Signal2
Signal3
Signal4
sel1
sel8
Ready
Valid
sel5
sel3
S12
Ready
Valid
sel8
Reset
reset
stalldone
Pdone

Signal 1	Signal 2	Signal 3	Signal 4
ld2	ld4	ld6	sel6
ld3	ld5	ld7	~~sel4~~
	sel7	sel4	ld8
	~~sel3~~	~~sel5~~	ld9