Towards a Monolithic Electronic Platform in Conventional Silicon Photonics Processes

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***Abstract*—We present the design methodology to make any active silicon photonics node, a monolithic platform. The approach is based on the usage of the waveguide and complementary dopant to create MOSFETs and digital gates allowing the inclusion of basic on-chip processing and specialized analog circuitry.**

***Index Terms*—Silicon photonics, Monolithic integrated circuit, electronic-photonic co-design, CMOS integrated circuits**

I. Introduction

State-of-the art monolithic electronic-silicon photonics processes are a monumental advancement in the co-design of electronic and photonics circuits. For high speed application, sharing the same substrate has its advantages: no interconnection needed reducing the parasitic load, co-design share the same simulation environment and simpler mechanical assembly of the integrated circuit (IC) into the system. Although, even the best monolithic processes struggle to compete with recent CMOS nodes in terms of maximum frequency of operation for digital signal processing or the driving power needed for optical modulators. For lower speed application that do not need these higher speeds or driving power, monolithic nodes seems to be an enticing solution for its ease of use, embedded testing capabilities and easier physical assembly. Nevertheless, since monolithic nodes are usually build upon an existing CMOS node and modified to fit the less strainuous fabrication of the photonics[citation needed], they tend to follow and exceed the prices of CMOS processes instead of photonics'[citation needed].

Doing the opposite, as in integrating CMOS capabilities in a silicon photonics node is possible but relatively new; prior art has shown that integrating CMOS transistors into a conventionnal silicon photonics process is possible [citation needed]. It creates a new avenue to access a monolithic node for researchers and industry without the high entry price, although at the expense of poorer electrical performances and no supplied electronic libraries. In this paper, we aim to expand on the idea by proposing improvements on the transistor design, discussing the limitations and pitfalls of the implementation and tooling, and present the progress made towards a monolithic electronic platform in a conventional silicon photonics process.

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II. Fundamentals and Principle

As recent state-of-the art shows, MOSFET transistor in a conventional silicon photonics node can be useful for power reading applications and signal multiplexing[citation needed]. While the design of the basic transistor unit is a promising start, an improvement to the design opens the possibilities of integrating digital electronics. This section will present the modeling of the transistors and the effect of the proposed changes has on key parameters; the small signal gain (gm) and the cut-off frequency (F_t).

The chosen key parameters were selected for their relevance to both the analog and digital circuitry. A higher small signal gain means that analog circuitery requires less transistor for the same amplification factor, shrinking the circuits as a whole. The increase of the small signal gain also increases the current output strength of digital gates, helping in the charge and discharge of capacitive loads, such as gates or PN junctions. The other parameter, the cut-off frequency of the transistor themselves, is a measurment of how fast a single transistor can switch. Improving the cut-off frequency of the transistor opens the design area for analog and digital circuitry as it represents the upper limit at which a circuit can run in a parasitic-less environment. Both theses improvements can lead to more precision and efficiency in data collection and transport.

The small signal gain is the measurment of how much the drain current (I_D) changes in relation with the gate-to-source voltage (V_{GS}) in a specific condition of the drain-to-source voltage (v_{DS}).

$$gm = \left.\frac{\delta I_D}{\delta V_{GS}}\right|_{v_{DS}} = \mu_x C_{ox} \frac{W}{L}(V_{GS} - V_T)(1 + \lambda v_{DS}) \quad (1)$$

In 1, μ_x is the mobility of the charges, C_{ox} is the oxide capacitance per unit area, W and L are the size of the gate, V_T is the threshold voltage and λ is the channel-length modulation parameter. In conventionnal silicon photonics process, the W value is the height of the waveguide, hence the designer only has access on controlling the bias point via V_{GS}, the length L and the oxide capacitance C_{ox} up to the manufacturing limit. The C_{ox} value is also found in the formula of V_T, which influences the bias point and gm.

$$V_T = V_{fb} + 2\phi_F + \frac{\sqrt{2\epsilon_{Si} q N (2\phi_F)}}{C_{ox}} \quad (2)$$

In 2, V_{fb} is the flat band voltage, ϕ_F is fermi potential of the doped channel, ϵ_{Si} the permitivity of silicon, q the elemental charge and N the doping of the channel.

The cut-off frequency of a single transistor can be defined by the ratio of it's small-signal gain over its gate-source (C_{gs}) and gate-drain capacitance (C_{gd})

$$F_t = \frac{gm}{2\pi(C_{gs} + C_{gd})} \tag{3}$$

Developing upon 3, on can find that the cutoff frequency is function of two terms on which the designer has some control over: the threshold voltage (V_t) and the length (L) of the transistor (in saturation):

$$F_t = \frac{\mu_x(V_{gs} - V_t)}{2\pi(\frac{2}{3}L^2 + 2L_{ov}L)}, \tag{4}$$

where μ_x is the mobility of either electrons or holes, V_{gs} the gate-source voltage and L_{ov} the overlap length between the gate and the source or drain area. In this case, the minimum L value is dictaded by how close on can have two doping of the same type side by side, normally a foundry rule. If the process used has multiple levels of dopant accessible by the designer, one can circumvent the rule by overlaping different doping densities to get the desired source, channel and drain's sizes and doping densities. However, decresing the L value too much could lead to increase in the leakeage current, up to the point that the transistor is more of a doped silicon resistor instead of a MOSFET. The other value the designer has some control in order to increase the maximum frequency is the threshold voltage V_t. The V_t value is mainly linked to the dopant density in the channel (N) and the oxide capacitance by unit of surface (C_{ox}).

Having a low doping in the channel is therefore crucial to having a low V_t value. In the litterature, a V_t of around $2V$ was achieved [citation needed]. This value could be further improved by shaving away at the C_{ox}, reducing it from 200 nm to 160nm or even 140nm.

Together with the change of the L value, one could improve the maximum frequency of operation by a factor of around [citation needed]. This increase of the frequency of operation opens the door to the investigation into whether digital electronics could be done by using such a design.

III. Methods, Challenges and Implementation

A digital electronic kit from scratch was created with over 230 individual designs of logic gates and flip-flops of different kinds and strength and their description into a *Library Exchange Format* style, and construct the kit to around an automated router. In our case, the open-source automated digital flow OpenROAD [citation needed]was chosen for its easiness of usage and complete open-source stack of software of routing and placement. The GDS design themselves were made by the python-based drawing tool for photonics GDS-Factory [citation needed].

IV. Conclusion