Towards a Monolithic Electronic Platform in Conventional Silicon Photonics Processes

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***Abstract*—We present the design methodology to make any active silicon photonics node, a monolithic platform. The approach is based on the usage of the waveguide and complementary dopant to create MOSFETs and digital gates allowing the inclusion of basic on-chip processing and specialized analog circuitry.**

***Index Terms*—Silicon photonics, Monolithic integrated circuit, electronic-photonic co-design, CMOS integrated circuits**

I. Introduction

State-of-the art monolithic electronic-silicon photonics processes are a monumental advancement in the co-design of electronic and photonics circuits. For high speed application, sharing the same substrate has its advantages: no interconnection needed reducing the parasitic load, integrated simulation environment and simpler mechanical assembly of the integrated circuit (IC) into more complex systems. Although, at the moment, even the best monolithic processes struggle to compete with recent CMOS nodes in terms of maximum frequency of operation for digital signal processing or the driving power needed for optical modulators. For lower speed application that do not need these higher speeds or driving power, monolithic nodes seems to be an enticing solution for its ease of use, embedded testing capabilities and easier physical assembly. Nevertheless, since monolithic nodes are usually build upon an existing CMOS node and modified to fit the less strainuous fabrication of the photonics[citation needed], they tend to exceed the price per area of similar CMOS processes[citation needed].

Integrating CMOS capabilities in a silicon photonics node, although possible, is relatively new. It creates a new avenue to access a monolithic node for researchers and industry without the high entry price. Prior art has shown that integrating CMOS transistors into a conventionnal silicon photonics process is possible but limited [1], [2], as it shows poorer electrical performances than equivalent CMOS and has no foundry supplied electronic libraries.

In this paper, we aim to expand on the idea by proposing improvements on the transistor design, discussing the limitations and pitfalls of the implementation and tooling, and present the progress made towards a monolithic electronic platform in a conventional silicon photonics process.

II. Fundamentals and Principle

As recent state-of-the art shows, MOSFET transistor in a conventional silicon photonics node can be useful for power reading applications and signal multiplexing[citation needed]. While the design of the basic transistor unit is a promising start, improving the design opens up the possibilities of integrating digital electronics. This section will present the modeling of the transistors and the effect of the proposed changes has on key parameters; the small signal gain (gm) and the cut-off frequency (F_t).

The chosen key parameters were selected for their relevance to both the analog and digital circuitry. A higher small signal gain means that analog circuitery requires less transistor for the same amplification factor, shrinking the circuits as a whole. The increase of the small signal gain also increases the current output strength of digital gates, helping in the charge and discharge of capacitive loads, such as gates or PN junctions. The other parameter, the cut-off frequency of the transistor themselves, is a measurment of how fast a single transistor can switch. Improving the cut-off frequency of the transistor opens up the design area for analog and digital circuitry as it represents the upper limit at which a circuit can run in a parasitic-less environment. Improving both these metrics can lead to more precision and efficiency in signal collection and transport.

The saturation region small signal gain is the measurment of how much the drain current (I_D) changes in relation with the gate-to-source voltage (V_{GS}) in a specific condition of the drain-to-source voltage (v_{DS}).

$$gm = \left.\frac{\delta I_D}{\delta V_{GS}}\right|_{v_{DS}} = \mu_x C_{ox} \frac{W}{L}(V_{GS} - V_T)(1 + \lambda v_{DS}) \quad (1)$$

In 1, μ_x is the mobility of the charges, C_{ox} is the oxide capacitance per unit area, W and L are the size of the gate, V_T is the threshold voltage and λ is the channel-length modulation parameter. In conventionnal silicon photonics process, the W value is the height of the waveguide, hence the designer only has access on controlling the bias point via V_{GS} via an external application, and the length L and the oxide capacitance C_{ox} up to their respective manufacturing limit. The length of the transistor is controllable by the distance between two tubs of

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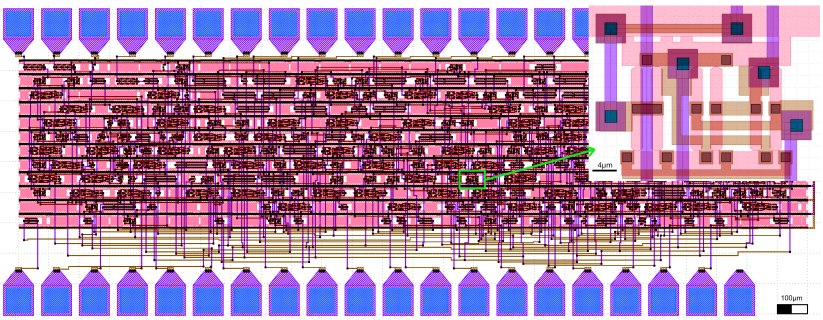

Fig. 1. A digital core made in AMF silicon photonics technology. It has two 12-bits wide pads for ADC/DAC connections.

the same type of doping and the length of the gate. As the physical limit of the gate length is the minimal width of a silicon waveguide, the limiting factor is often the minimal distance between two tubs of similar doping without causing a unwanted connection between the source and the drain. Depending on the foundry used, this distance can vary and be subject to mask alignment precision. As for the C_{ox} value, it is not only found in 1 but also in the formula of V_T, which influences the bias point and gm.

$$V_T = V_{fb} + 2\phi_F + \frac{\sqrt{2\varepsilon_{Si} q N (2\phi_F)}}{C_{ox}} \tag{2}$$

In (2), V_{fb} is the flat band voltage, ϕ_F is fermi potential of the doped channel, ε_{Si} the permitivity of silicon, q the elemental charge and N the doping of the channel. It is better to increase the C_{ox} value as much as possible, as it has the double effect of reducing the V_T in (2) and increasing the gm from (1).

The second metric, the cut-off frequency F_T, it's small-signal gain over its gate-source (C_{GS}) and gate-drain capacitance (C_{GD})

$$F_t = \frac{gm}{2\pi(C_{GS} + C_{GD})} = \frac{\mu_x (V_{GS} - V_t)}{2\pi(\frac{2}{3}L^2 + 2L_{ov}L)}, \tag{3}$$

where L_{ov} the overlap length between the gate and the source or drain area.

In the litterature, a V_t of around $2V$ was achieved using larger than minimal values of L and C_{ox} [citation needed]. This V_T value could be further improved by shaving away at the gap between the gate and the channel, reducing it from 200 nm to 160 nm or even 140 nm, increasing the C_{ox} value. Together with the diminution of the L value, one could increase the maximum frequency of operation by a factor of around 80 to 100 and the gm around [citation needed].

With the improvements made to the basic MOSFET, the next step is to create a analog and digital library of circuits enabling semi-automated designs.

III. Implementation and Challenges

A digital electronic kit was created with over 230 individual designs of logic gates and flip-flops of different kinds and strength for the AMF silicon photonics process [citation needed]. The GDS design and their *Library Exchange Format* were made by the python-based drawing tool for photonics, GDSFactory [citation needed]. Tney were then fed into an open-source automated router, OpenROAD [citation needed], along with the verilog design files and the translated technology files based on the foundry's process manual. The Linux-based tool running on a Windows-WSL machine then outputted a simple digital core made for with a serial-parrallel interface (SPI), shown in Fig. II, with the capabilities to access up to eight 12-bits DAC and ADC.

Some challenges did arise, one file we were not able to provide to the router yet is the timing library of the gates, which can either be simulated by parasitic extraction simulations or constructed via a measurment campaign. Nevertheless, not having the exact timing of the gate influences the maximum clock frequency of the circuit, not its logics, as the circuit will still be capable to compute at a lower speed than expected. Additionnaly, during our first measurment campaign of the reduced L and smaller gap transistors, a flaw in the fabrication process was discovered. Since the photonics nodes care much more about the optical properties of the waveguides, when we closed the gap between the channel and the gate,a significant amount of the transistor exhibited an unwanted electrical connection was made between the gate and the drain/source or channel, meaning that the device was unusable with the minimal distance prescribed by the foundry.

IV. Conclusion

Advancements towards a fully electronics-photonics monolithic node were demonstrated by improving of the fundamental building block, the MOSFET, permitting the building of a digital electronics library. This library was then used with open-source tooling to produce a SPI digital core

References

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