Login system

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1 explain code

1.1 Main

first, we define a key equal to the login key hash to change the password key star to log.
red LED turns on when entering the wrong password and green led for the correct password.
we are debouncing in this code with every positive edge clock to noise canceling.
for positive edge clock in key equal db, we check the password and turn on red or green led.
for positive edge clock in key hash db to change the password.
for positive edge clock in key star db to logout.
in the initial block we define a password

$$password = 123 = 10'b0001111011$$

and both led turn off.

1.2 test bench

we use the normal template of the test bench in this code.
first, we define all of the parameters equal to 0

$$keyin = 123 = 10'b0001111011$$

in line 31 changes the key equal to 1 (positive edge) and the key is equal to the password we can log in in line 33 and change the key star to 1 to log out.
in line 35 we change the password with key hash.

1.3 output

monitor function is using to print output in the console.
key in is equal to password here

```verilog
module login_system(
    input [9:0] key_in, // 10-bit input from the keyboard
    input key_equal, // input from the '=' key
    input key_hash, // input from the '#' key
    input key_star, // input from the '*' key
    output reg led_red, // output to the red LED
    output reg led_green, // output to the green LED
    input clk // clock input for debouncing
);

    reg [9:0] password; // 10-bit password
    reg logged_in; // login status

    reg key_equal_db = 0; // debounced key_equal signal
    reg key_hash_db = 0; // debounced key_hash signal
    reg key_star_db = 0; // debounced key_star signal

    always @(posedge clk) begin
        key_equal_db <= key_equal;
        key_hash_db <= key_hash;
        key_star_db <= key_star;
    end

    always @(posedge key_equal_db or posedge key_hash_db or posedge key_star_db) begin
        if (key_equal_db) begin
            if (!logged_in) begin
                if (key_in == password) begin
                    logged_in <= 1;
                    led_green <= 1;
                    led_red <= 0;
                end else begin
                    led_red <= 1;
                end
            end
        end else if (key_hash_db) begin
            if (logged_in) begin
```

Figure 1: Main .

```verilog
    always @(posedge key_equal_db or posedge key_hash_db or posedge key_star_db) begin
        if (key_equal_db) begin
            if (!logged_in) begin
                if (key_in == password) begin
                    logged_in <= 1;
                    led_green <= 1;
                    led_red <= 0;
                end else begin
                    led_red <= 1;
                end
            end
        end else if (key_hash_db) begin
            if (logged_in) begin
                password <= key_in;
            end
        end else if (key_star_db) begin
            if (logged_in) begin
                logged_in <= 0;
                led_green <= 0;
            end
        end
    end

    initial begin
        password = 10'b0001111011; // default password is '0001111011' (123 in binary)
        logged_in = 0;
        led_red = 0;
        led_green = 0;
    end

endmodule
```

Figure 2: Main .

2

```verilog
1   `timescale 1ns / 1ps
2
3   module testbench;
4       reg [9:0] key_in;
5       reg key_equal, key_hash, key_star;
6       wire led_red, led_green;
7       reg clk;
8
9       login_system u1 (
10          .key_in(key_in),
11          .key_equal(key_equal),
12          .key_hash(key_hash),
13          .key_star(key_star),
14          .led_red(led_red),
15          .led_green(led_green),
16          .clk(clk)
17      );
18
19      initial begin
20          // Monitor the signals
21          $monitor("At time %d, key_in=%b, key_equal=%b, key_hash=%b, key_star=%b, led_red=%b, led_green=%b",
22              $time, key_in, key_equal, key_hash, key_star, led_red, led_green);
23
24          // Default password is '0001111011' (123 in binary)
25          key_in = 10'b0001111011;
26          key_equal = 0;
27          key_hash = 0;
28          key_star = 0;
29          clk = 0;
```

Figure 3: test bench .

```verilog
23
24          // Default password is '0001111011' (123 in binary)
25          key_in = 10'b0001111011;
26          key_equal = 0;
27          key_hash = 0;
28          key_star = 0;
29          clk = 0;
30
31          #10 key_equal = 1; // Try to login with the correct password
32          #10 key_equal = 0;
33          #10 key_star = 1; // Logout
34          #10 key_star = 0;
35          #10 key_in = 10'b0001111100; // New password is '0001111100' (124 in binary)
36          key_hash = 1; // Change password
37          #10 key_hash = 0;
38          #10 key_equal = 1; // Try to login with the old password
39          #10 key_equal = 0;
40          #10 key_in = 10'b0001111100; // Try to login with the new password
41          key_equal = 1;
42          #10 key_equal = 0;
43          #10 key_star = 1; // Logout
44          #10 key_star = 0;
45          #10 $finish;
46      end
47
48      always #5 clk = ~clk; // Generate a clock signal with a period of 10 time units
49  endmodule
50
```

Figure 4: test bench .

```
At time          0, key_in=0001111011, key_equal=0, key_hash=0, key_star=0, led_red=0, led_green=0
At time         10, key_in=0001111011, key_equal=1, key_hash=0, key_star=0, led_red=0, led_green=0
At time         15, key_in=0001111011, key_equal=1, key_hash=0, key_star=0, led_red=0, led_green=1
At time         20, key_in=0001111011, key_equal=0, key_hash=0, key_star=0, led_red=0, led_green=1
At time         30, key_in=0001111011, key_equal=0, key_hash=0, key_star=1, led_red=0, led_green=1
At time         35, key_in=0001111011, key_equal=0, key_hash=0, key_star=0, led_red=0, led_green=0
At time         40, key_in=0001111011, key_equal=0, key_hash=0, key_star=0, led_red=0, led_green=0
At time         50, key_in=0001111100, key_equal=0, key_hash=1, key_star=0, led_red=0, led_green=0
At time         60, key_in=0001111100, key_equal=0, key_hash=0, key_star=0, led_red=0, led_green=0
At time         70, key_in=0001111100, key_equal=1, key_hash=0, key_star=0, led_red=0, led_green=0
At time         75, key_in=0001111100, key_equal=1, key_hash=0, key_star=0, led_red=1, led_green=0
At time         80, key_in=0001111100, key_equal=0, key_hash=0, key_star=0, led_red=1, led_green=0
At time         90, key_in=0001111100, key_equal=1, key_hash=0, key_star=0, led_red=1, led_green=0
At time        100, key_in=0001111100, key_equal=0, key_hash=0, key_star=0, led_red=1, led_green=0
At time        110, key_in=0001111100, key_equal=0, key_hash=0, key_star=0, led_red=1, led_green=0
At time        120, key_in=0001111100, key_equal=0, key_hash=0, key_star=0, led_red=1, led_green=0
Stopped at time : 130 ns : File "C:/Documents and Settings/Administrator/Desktop/bounes_project/testbench.v" Line 45
```

Figure 5: output .