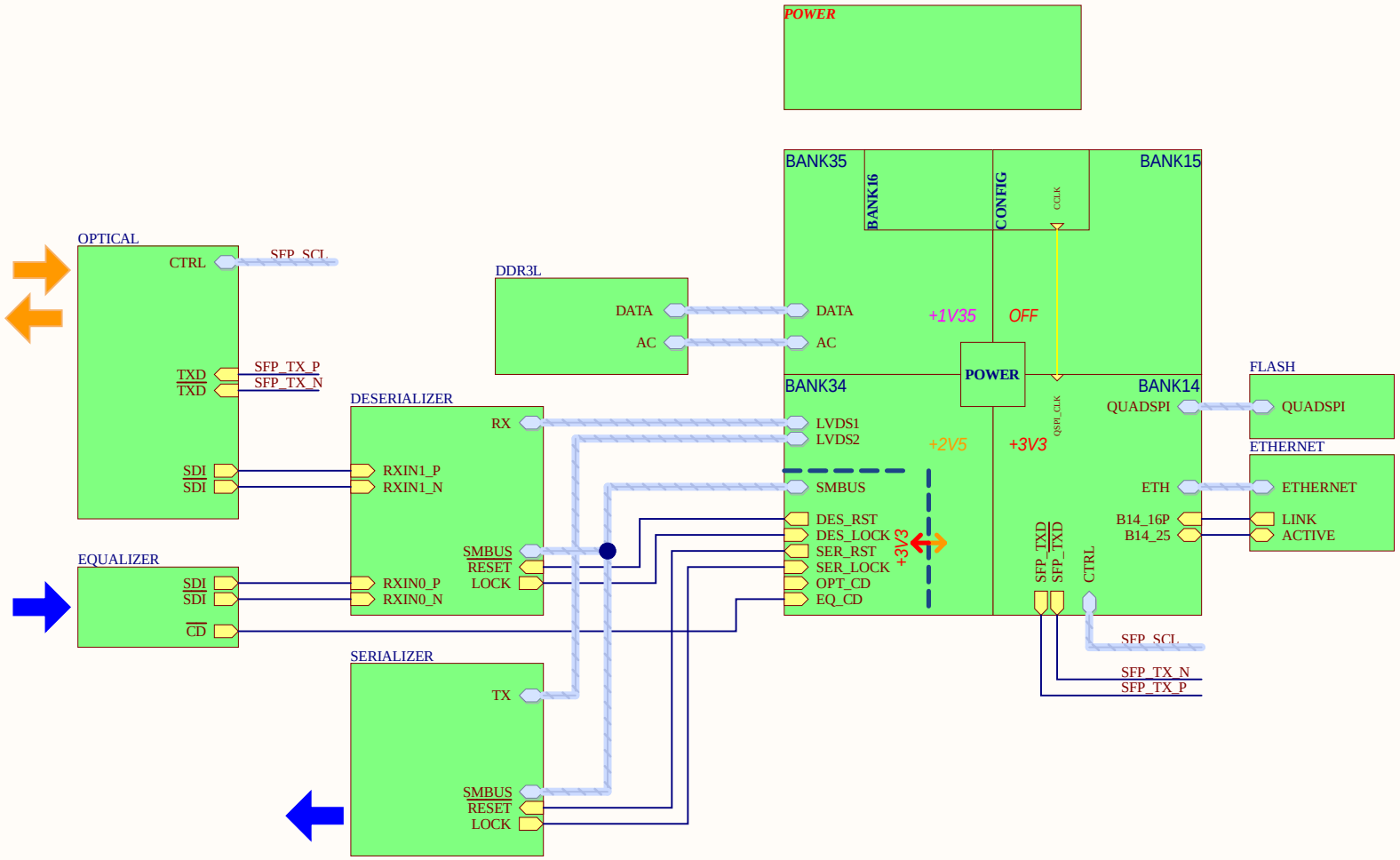
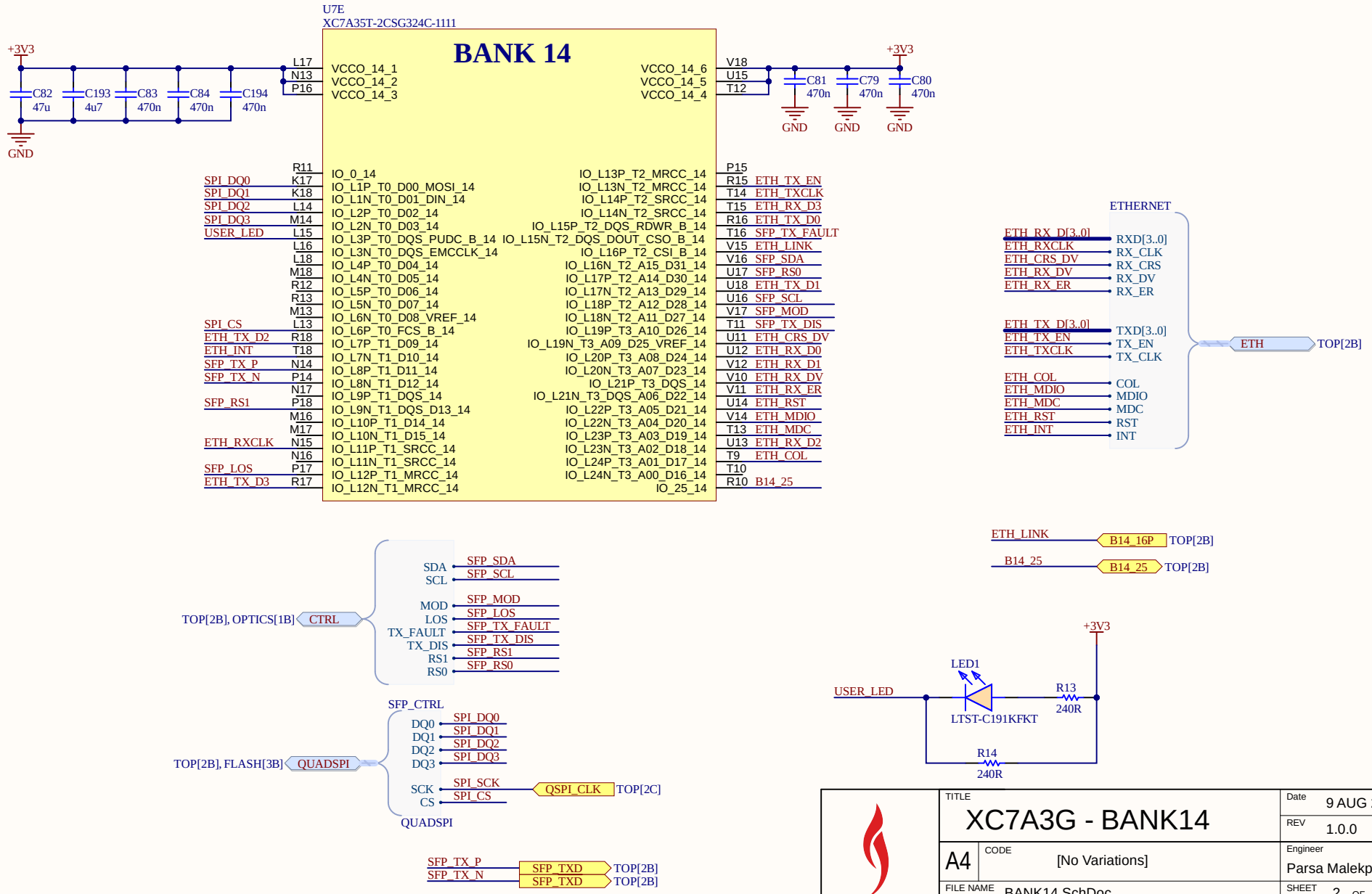


Mechanical

TITLE XC7A3G		Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
	FILE NAME TOP.SchDoc	SHEET 1 OF 18



TITLE	XC7A3G - BANK14	Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
	FILE NAME BANK14.SchDoc	SHEET 2 OF 18

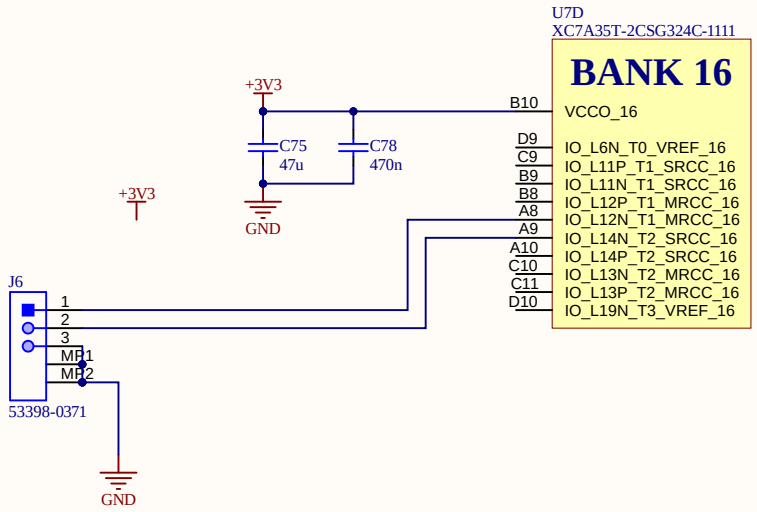
U7F

BANK 15

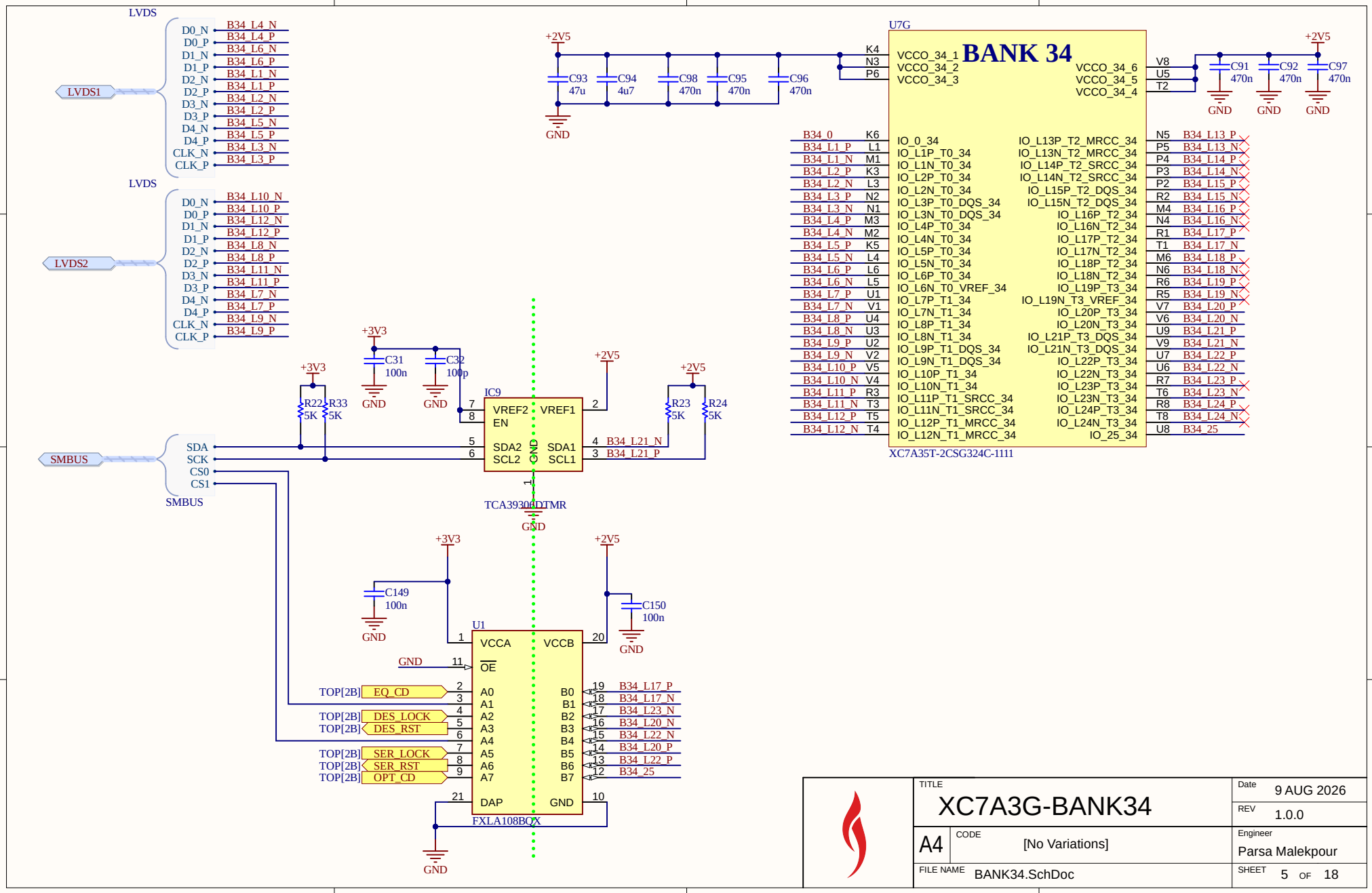
A17	VCCO_15_1		VCCO_15_6	K14	
C13	VCCO_15_2		VCCO_15_5	H18	
D16	VCCO_15_3		VCCO_15_4	G15	
B15_0	G13	IO_0_15	IO_L13P_T2_MRCC_15	H16	B15_L13_P
B15_L1_P	D14	IO_L1P_T0_AD0P_15	IO_L13N_T2_MRCC_15	G16	B15_L13_N
B15_L1_N	C14	IO_L1N_T0_AD0N_15	IO_L14P_T2_SRCC_15	F15	B15_L14_P
B15_L2_P	B13	IO_L2P_T0_AD8P_15	IO_L14N_T2_SRCC_15	F16	B15_L14_N
B15_L2_N	B14	IO_L2N_T0_AD8N_15	IO_L15P_T2_DQS_15	H14	B15_L15_P
B15_L3_P	C12	IO_L3P_T0_DQS_AD1P_15	IO_L15N_T2_DQS_ADV_B_15	G14	B15_L15_N
B15_L3_N	B12	IO_L3N_T0_DQS_AD1N_15	IO_L16P_T2_A28_15	E17	B15_L16_P
B15_L4_P	B11	IO_L4P_T0_15	IO_L16N_T2_A27_15	D17	B15_L16_N
B15_L4_N	A11	IO_L4N_T0_15	IO_L17P_T2_A26_15	K13	B15_L17_P
B15_L5_P	F13	IO_L5P_T0_AD9P_15	IO_L17N_T2_A25_15	J13	B15_L17_N
B15_L5_N	F14	IO_L5N_T0_AD9N_15	IO_L18P_T2_A24_15	H17	B15_L18_P
B15_L6_P	D12	IO_L6P_T0_15	IO_L18N_T2_A23_15	G17	B15_L18_N
B15_L6_N	D13	IO_L6N_T0_VREF_15	IO_L19P_T3_A22_15	J14	B15_L19_P
B15_L7_P	B16	IO_L7P_T1_AD2P_15	IO_L19N_T3_A21_VREF_15	H15	B15_L19_N
B15_L7_N	B17	IO_L7N_T1_AD2N_15	IO_L20P_T3_A20_15	C16	B15_L20_P
B15_L8_P	A15	IO_L8P_T1_AD10P_15	IO_L20N_T3_A19_15	C17	B15_L20_N
B15_L8_N	A16	IO_L8N_T1_AD10N_15	IO_L21P_T3_DQS_15	E18	B15_L21_P
B15_L9_P	A13	IO_L9P_T1_DQS_AD3P_15	IO_L21N_T3_DQS_A18_15	D18	B15_L21_N
B15_L9_N	A14	IO_L9N_T1_DQS_AD3N_15	IO_L22P_T3_A17_15	G18	B15_L22_P
B15_L10_P	B18	IO_L10P_T1_AD11P_15	IO_L22N_T3_A16_15	F18	B15_L22_N
B15_L10_N	A18	IO_L10N_T1_AD11N_15	IO_L23P_T3_FOE_B_15	J17	B15_L23_P
B15_L11_P	E15	IO_L11P_T1_SRCC_15	IO_L23N_T3_FWE_B_15	J18	B15_L23_N
B15_L11_N	E16	IO_L11N_T1_SRCC_15	IO_L24P_T3_RS1_15	K15	B15_L24_P
B15_L12_P	D15	IO_L12P_T1_MRCC_15	IO_L24N_T3_RS0_15	J15	B15_L24_N
B15_L12_N	C15	IO_L12N_T1_MRCC_15	IO_25_15	K16	B15_25

XC7A35T-2CSG324C-1111

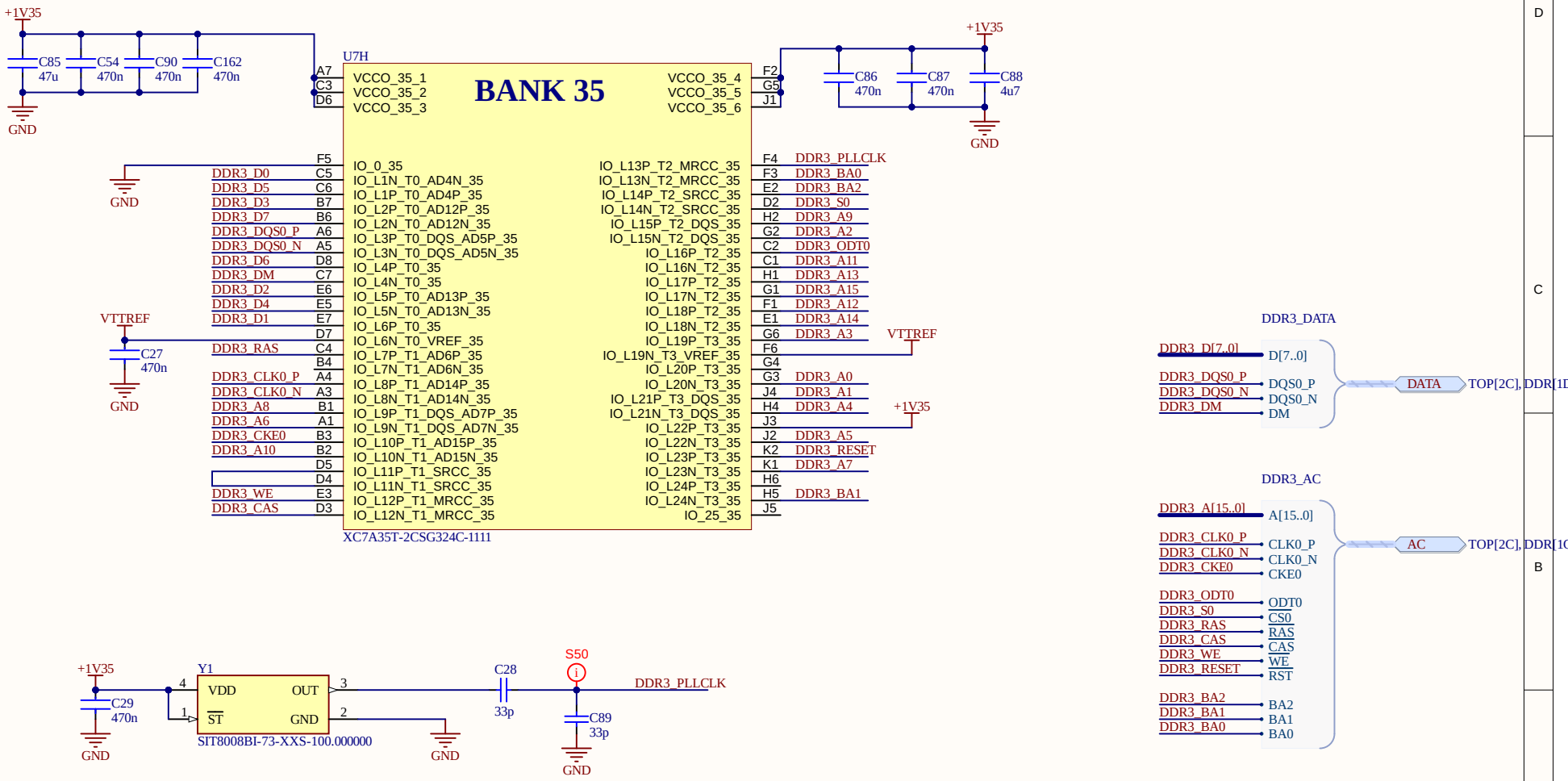
TITLE	XC7A3G-BANK15	Date	9 AUG 2026
		REV	1.0.0
A4	CODE [No Variations]	Engineer	Parsa Malekpour
FILE NAME	BANK15.SchDoc	SHEET	3 OF 18



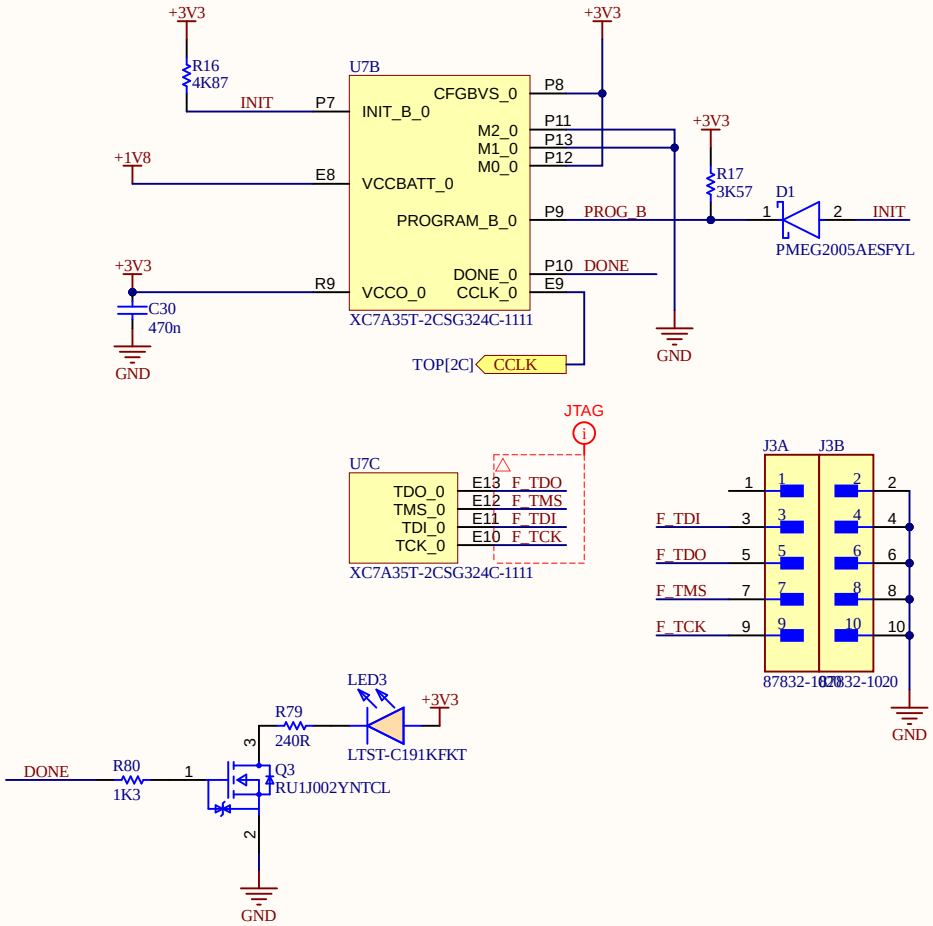
TITLE	XC7A3G-BANK16	Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
FILE NAME	BANK16.SchDoc	SHEET 4 OF 18



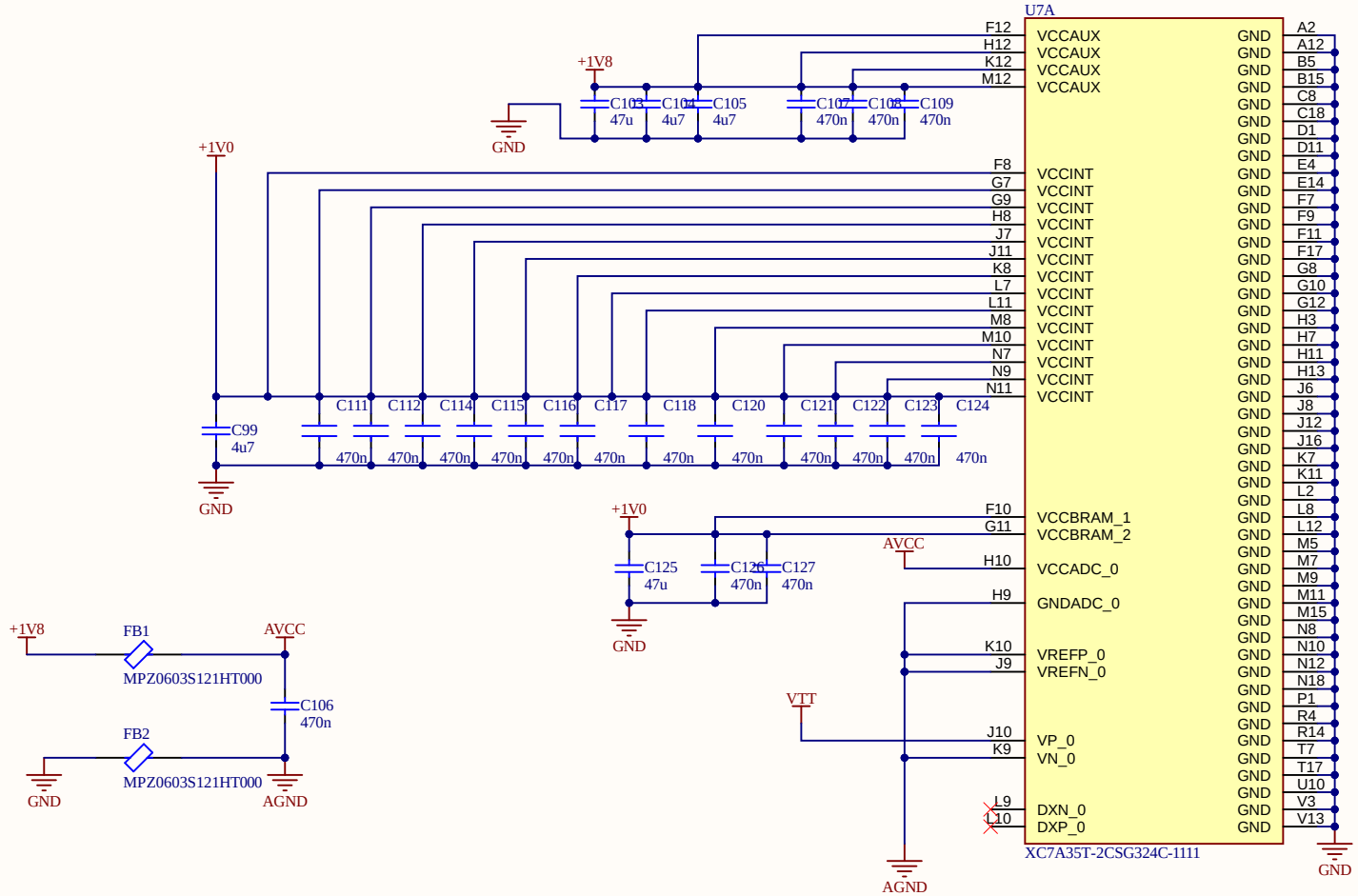
TITLE	XC7A3G-BANK34	Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
	FILE NAME BANK34.SchDoc	SHEET 5 OF 18



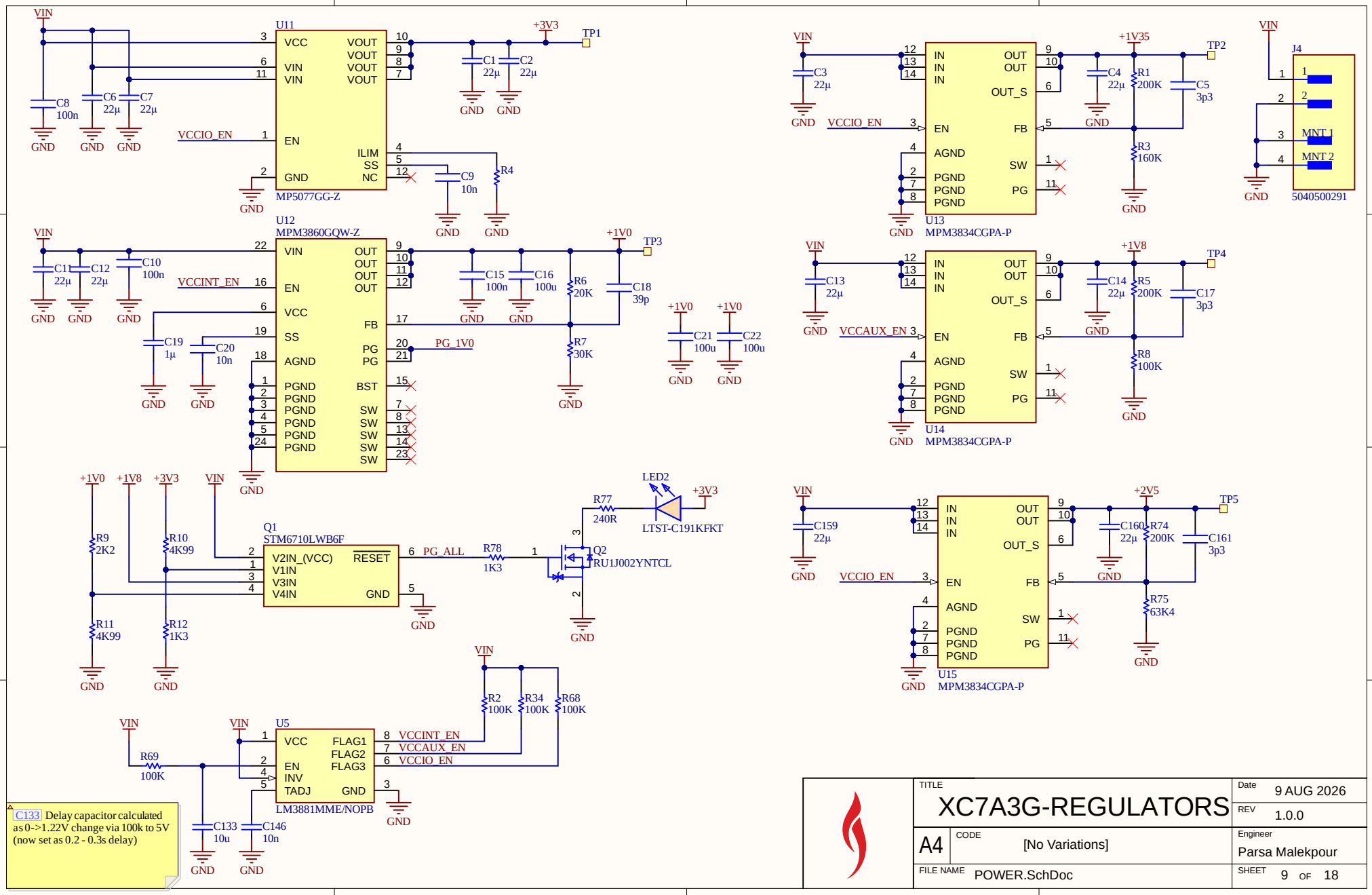
TITLE	XC7A3G-BANK35	Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
	FILE NAME BANK35.SchDoc	SHEET 6 OF 18

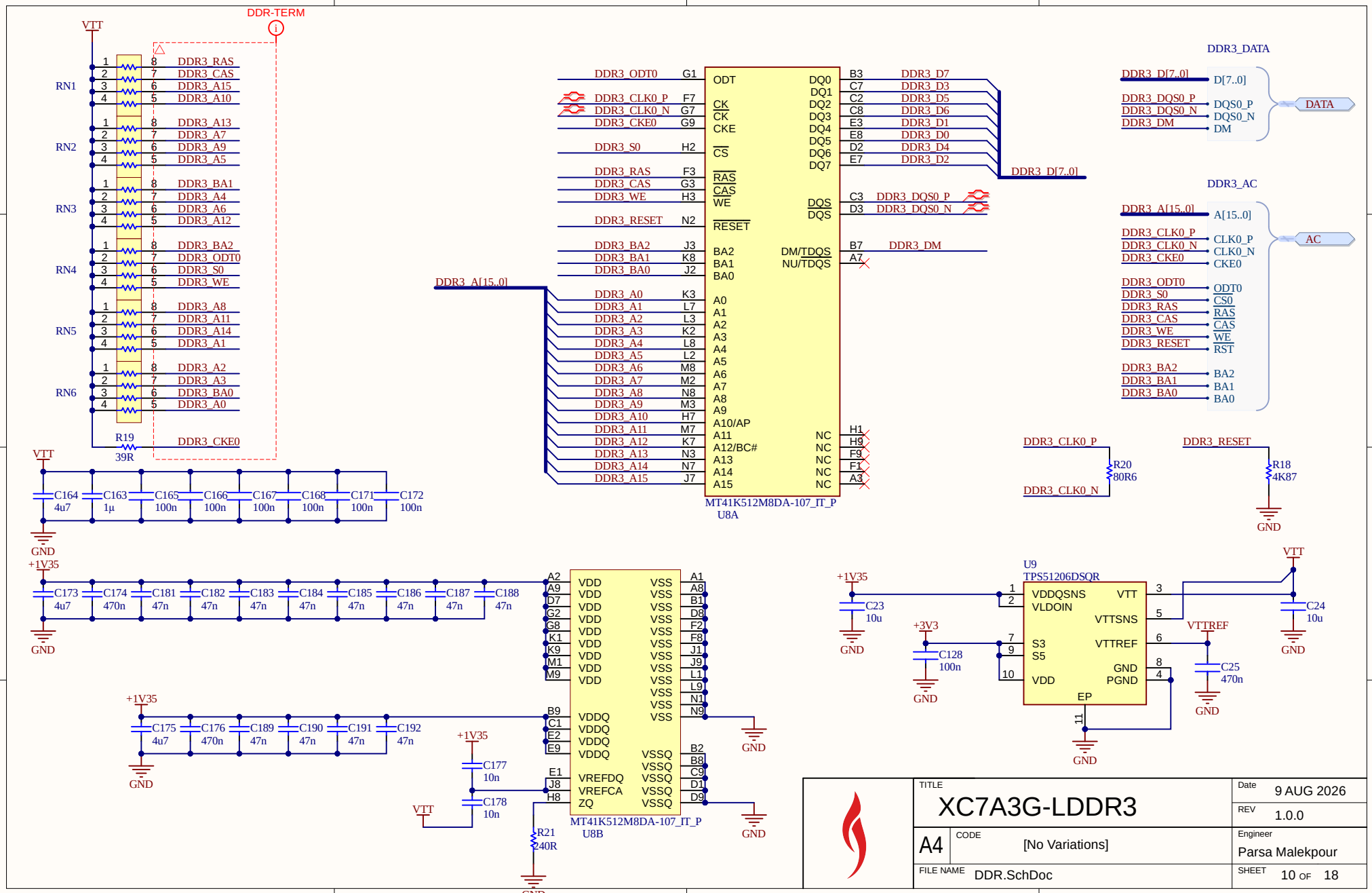


TITLE	XC7A3G-JTAG	Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
	FILE NAME FPGA CONFIG.SchDoc	SHEET 7 OF 18

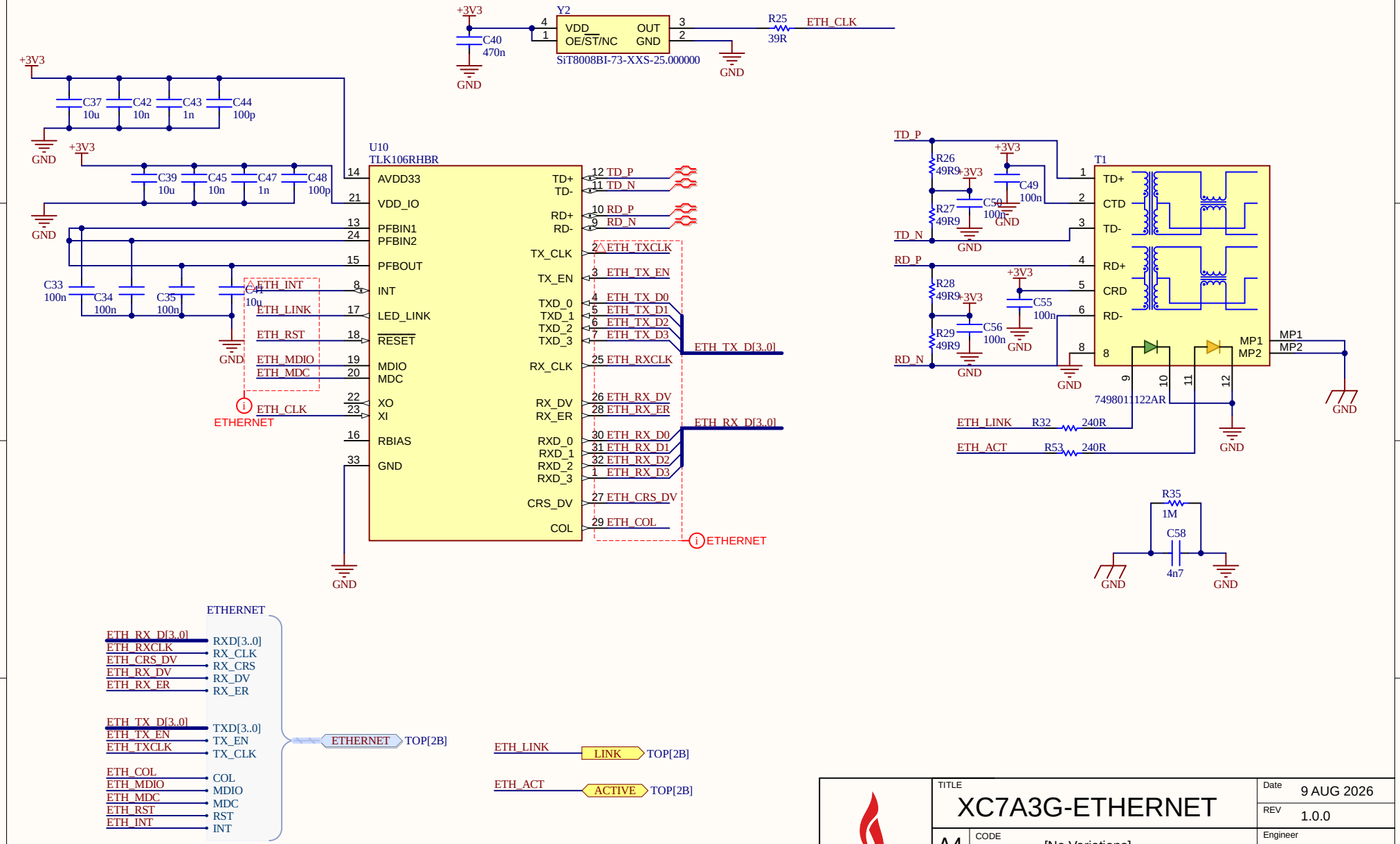


TITLE	XC7A3G-POWER	Date	9 AUG 2026
		REV	1.0.0
A4	CODE [No Variations]	Engineer	Parsa Malekpour
FILE NAME	FPGA PWR.SchDoc	SHEET	8 OF 18

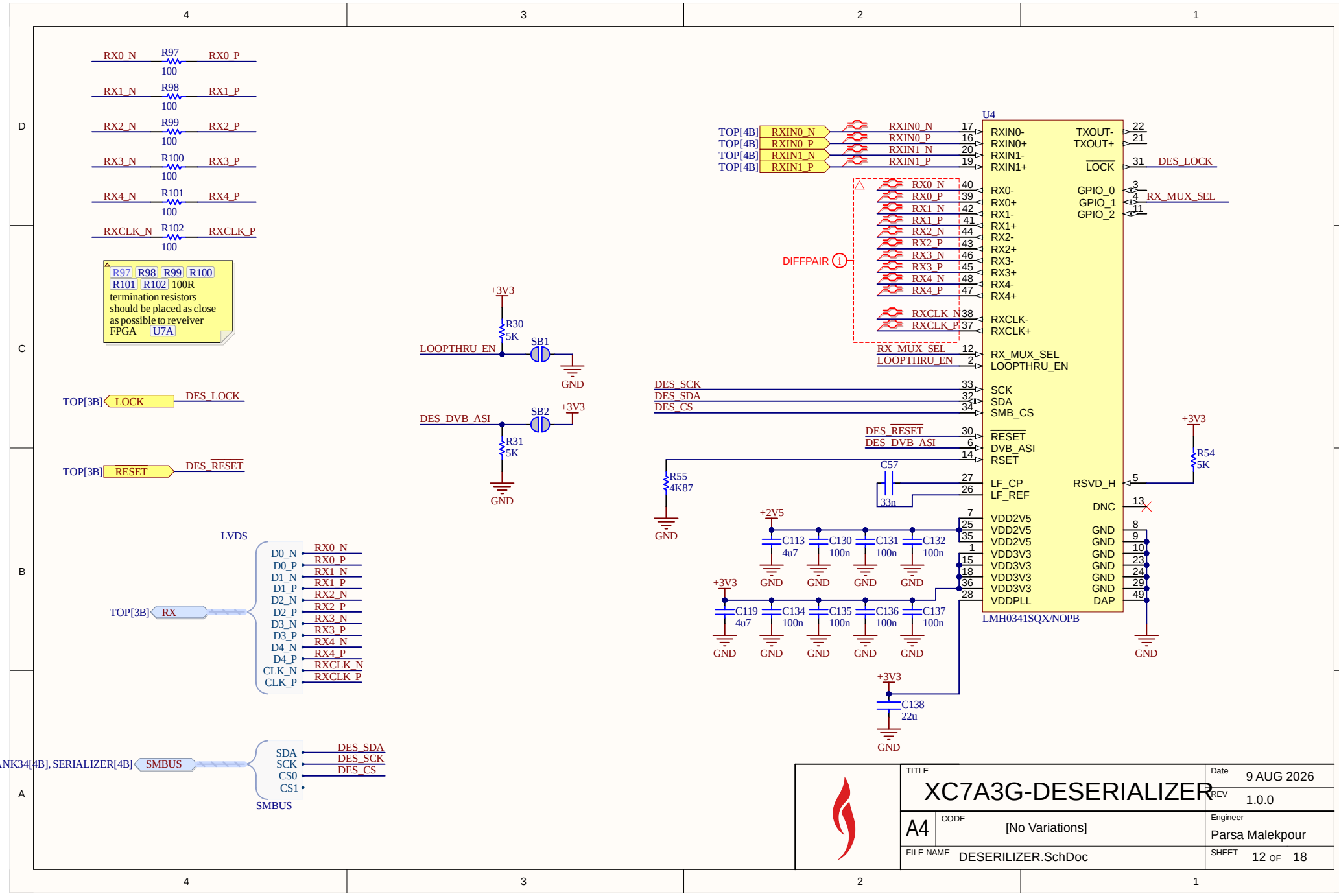

U11
MP5077GG-Z
VCC
VIN
VIN
EN
GND
VOUT
VOUT
VOUT
VOUT
ILIM
SS
NC
VCCIO_EN
+3V3
TP1
C1 22µ
C2 22µ
C8 100n
C6 22µ
C7 22µ
C9 10n
R4
U12
MPM3860GQW-Z
VIN
EN
VCC
SS
AGND
PGND
OUT
FB
PG
BST
SW
VCCINT_EN
PG_1V0
+1V0
TP3
C10 100n
C11 22µ
C12 22µ
C15 100n
C16 100u
R6 20K
C18 39p
R7 30K
C19 1µ
C20 10n
C21 100u
C22 100u
U13
MPM3834CGPA-P
IN
OUT_S
EN
AGND
PGND
OUT
FB
SW
PG
VCCIO_EN
+1V35
TP2
C3 22µ
C4 22µ
R1 200K
R3 160K
C5 3p3
J4
5040500291
MNT 1
MNT 2
U14
MPM3834CGPA-P
VCCAUX_EN
+1V8
TP4
C13 22µ
C14 22µ
R5 200K
R8 100K
C17 3p3
U15
MPM3834CGPA-P
VCCIO_EN
+2V5
TP5
C159 22µ
C160 22µ
R74 200K
R75 63K4
C161 3p3
Q1
STM6710LWB6F
V2IN_(VCC)
V1IN
V3IN
V4IN
RESET
GND
PG_ALL
R78 1K3
Q2
RU1J002YNTCL
R77 240R
LED2
LTST-C191KFKT
+3V3
R9 2K2
R10 4K99
R11 4K99
R12 1K3
U5
LM3881MME/NOPB
VCC
EN
INV
TADJ
FLAG1
FLAG2
FLAG3
GND
VCCINT_EN
VCCAUX_EN
VCCIO_EN
R2 100K
R34 100K
R68 100K
R69 100K
C133 10u
C146 10n
C133 Delay capacitor calculated as 0->1.22V change via 100k to 5V (now set as 0.2 - 0.3s delay)
TITLE
XC7A3G-REGULATORS
Date
9 AUG 2026
REV
1.0.0
A4
CODE
[No Variations]
Engineer
Parsa Malekpour
FILE NAME
POWER.SchDoc
SHEET
9 OF 18

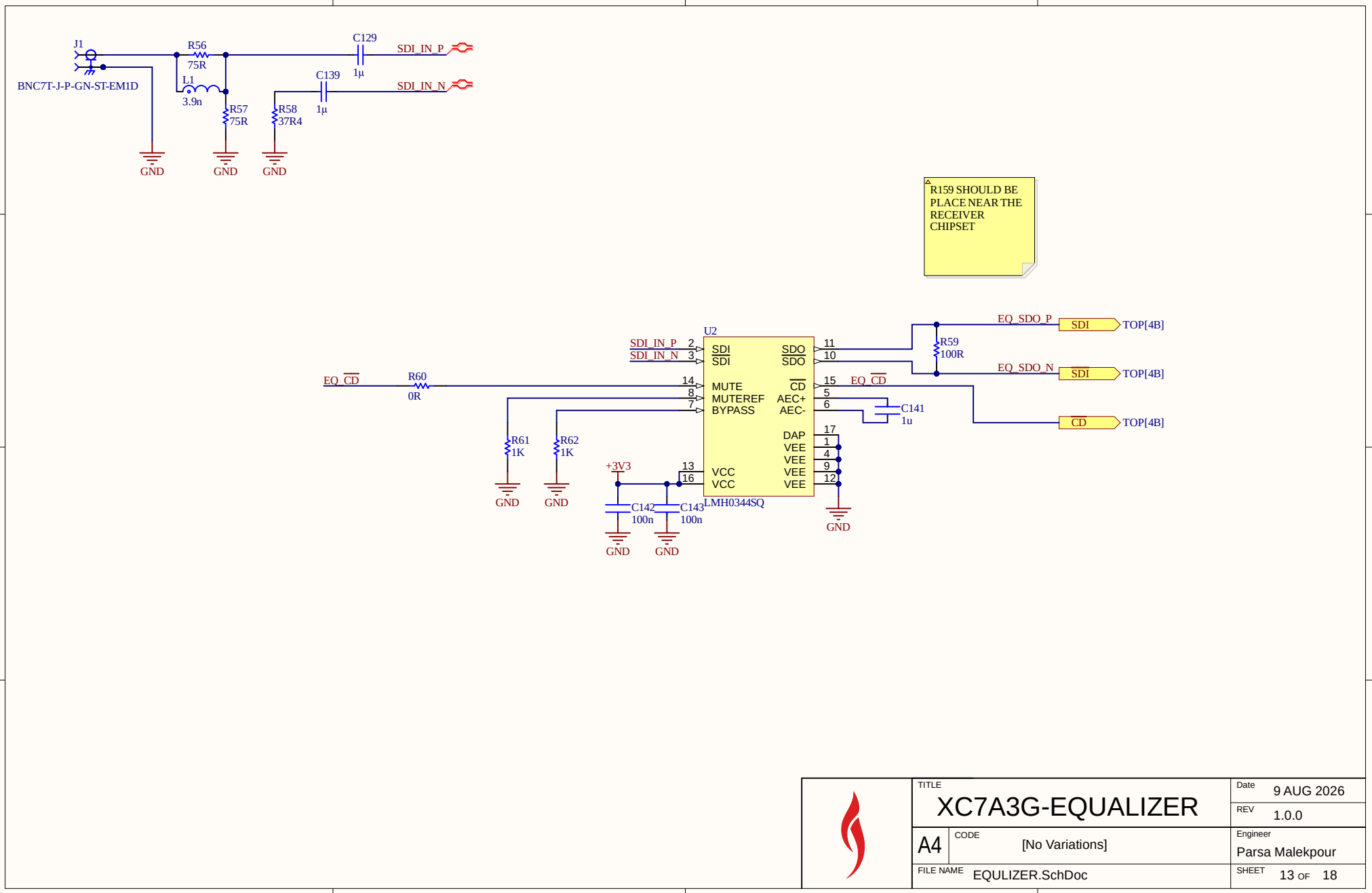


TITLE	XC7A3G-LDDR3	Date	9 AUG 2026
		REV	1.0.0
A4	CODE [No Variations]	Engineer	Parsa Malekpour
FILE NAME	DDR.SchDoc	SHEET	10 OF 18

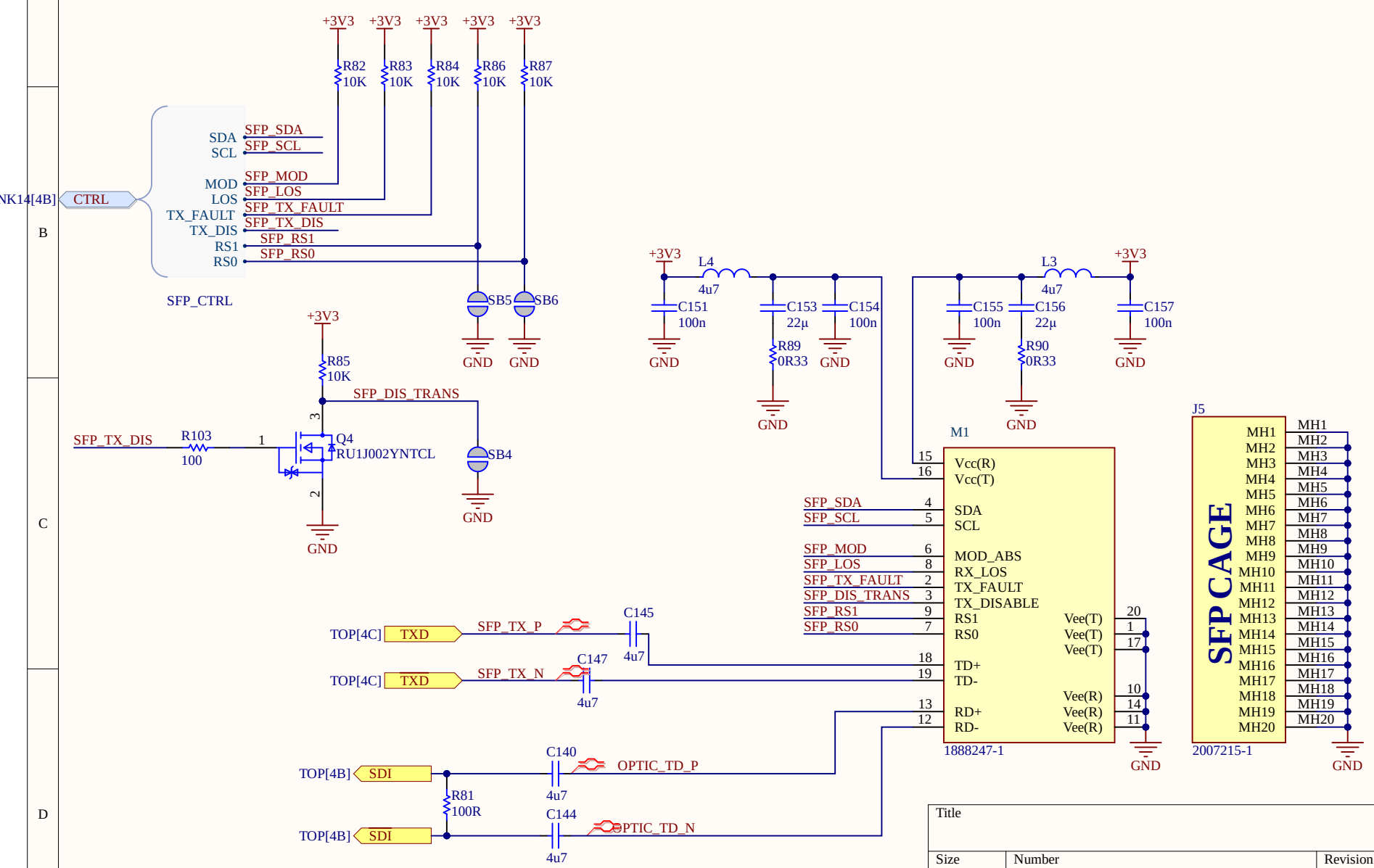


TITLE	XC7A3G-ETHERNET	Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
	FILE NAME ETHERNET.SchDoc	SHEET 11 OF 18

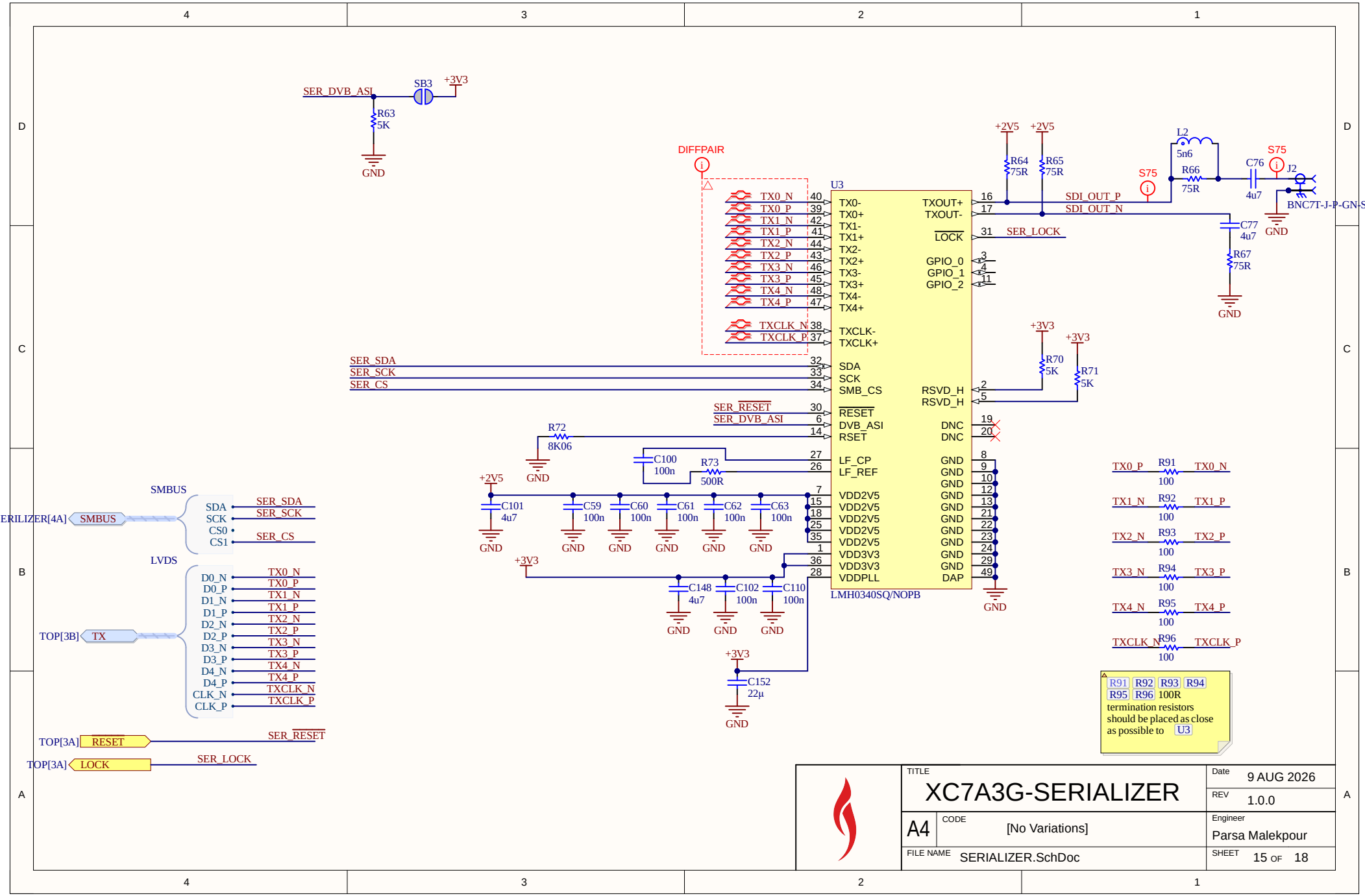

RX0_N R97 100 RX0_P
RX1_N R98 100 RX1_P
RX2_N R99 100 RX2_P
RX3_N R100 100 RX3_P
RX4_N R101 100 RX4_P
RXCLK_N R102 100 RXCLK_P
R97 R98 R99 R100 R101 R102 100R termination resistors should be placed as close as possible to reveiver FPGA U7A
TOP[3B] LOCK DES_LOCK
TOP[3B] RESET DES_RESET
TOP[3B] RX
LVDS
D0_N RX0_N
D0_P RX0_P
D1_N RX1_N
D1_P RX1_P
D2_N RX2_N
D2_P RX2_P
D3_N RX3_N
D3_P RX3_P
D4_N RX4_N
D4_P RX4_P
CLK_N RXCLK_N
CLK_P RXCLK_P
ANK34[4B], SERIALIZER[4B] SMBUS
SDA DES_SDA
SCK DES_SCK
CS0 DES_CS
CS1
SMBUS
+3V3 R30 5K LOOPTHRU_EN SB1 GND
DES_DVB_ASI SB2 +3V3 R31 5K GND
TOP[4B] RXIN0_N RXIN0_P RXIN1_N RXIN1_P
DIFFPAIR
U4
RX0_N RX0_P RX1_N RX1_P RX2_N RX2_P RX3_N RX3_P RX4_N RX4_P RXCLK_N RXCLK_P
RX_MUS_SEL LOOPTHRU_EN
DES_SCK DES_SDA DES_CS
DES_RESET DES_DVB_ASI
R55 4K87 GND
C57 33n
+2V5 C113 4u7 C130 100n C131 100n C132 100n
+3V3 C119 4u7 C134 100n C135 100n C136 100n C137 100n
+3V3 C138 22u GND
RXIN0- RXIN0+ RXIN1- RXIN1+ RX0- RX0+ RX1- RX1+ RX2- RX2+ RX3- RX3+ RX4- RX4+ RXCLK- RXCLK+ RX_MUX_SEL LOOPTHRU_EN SCK SDA SMB_CS RESET DVB_ASI RSET LF_CP LF_REF VDD2V5 VDD2V5 VDD2V5 VDD3V3 VDD3V3 VDD3V3 VDDPLL
TXOUT- TXOUT+ LOCK GPIO_0 GPIO_1 GPIO_2 RSVD_H DNC GND GND GND GND GND GND GND DAP
DES_LOCK RX_MUX_SEL
+3V3 R54 5K
LMH0341SQX/NOPB
TITLE XC7A3G-DESERIALIZER
Date 9 AUG 2026
REV 1.0.0
A4
CODE [No Variations]
Engineer Parsa Malekpour
FILE NAME DESERILIZER.SchDoc
SHEET 12 OF 18



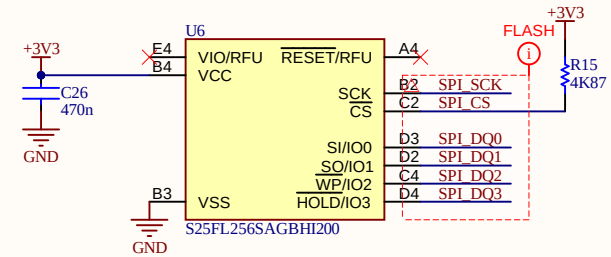
	TITLE XC7A3G-EQUALIZER	Date 9 AUG 2026	
		REV 1.0.0	
A4	CODE [No Variations]	Engineer Parsa Malekpour	
	FILE NAME EQULIZER.SchDoc	SHEET 13 OF 18	

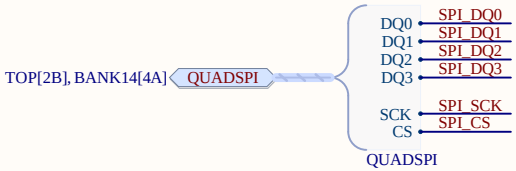


Title		
Size A	Number	Revision
Date: 8/09/2026		Sheet of
File: C:\Users\..\OPTICS.SchDoc		Drawn By:



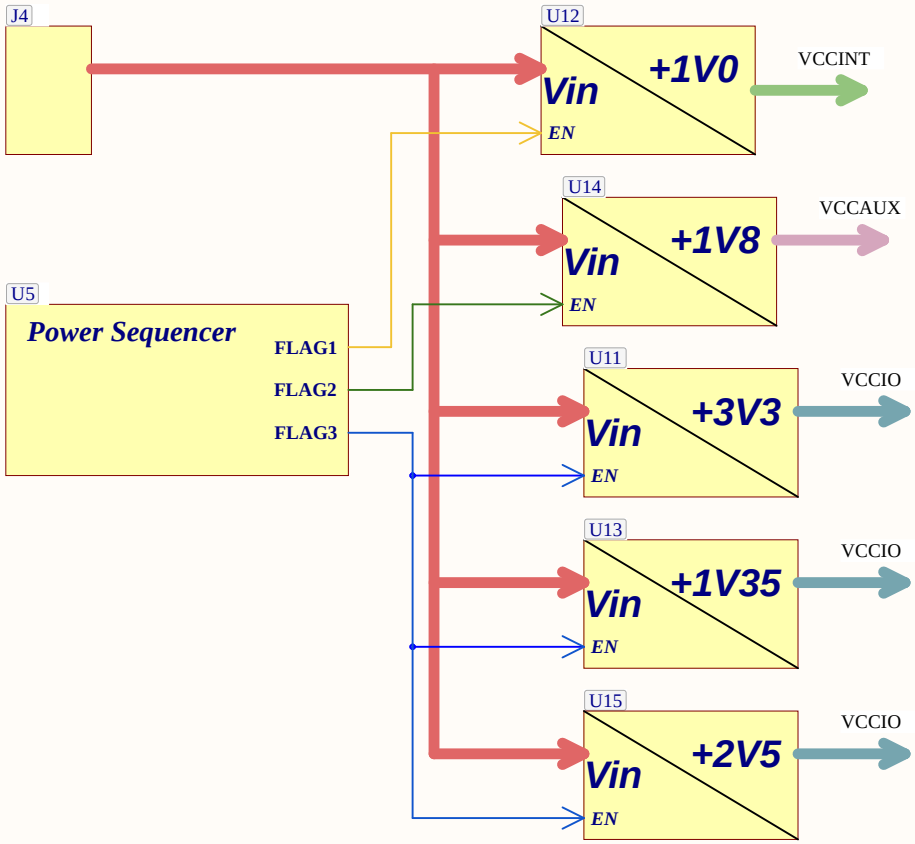
TITLE	XC7A3G-SERIALIZER	Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
	FILE NAME SERIALIZER.SchDoc	SHEET 15 OF 18



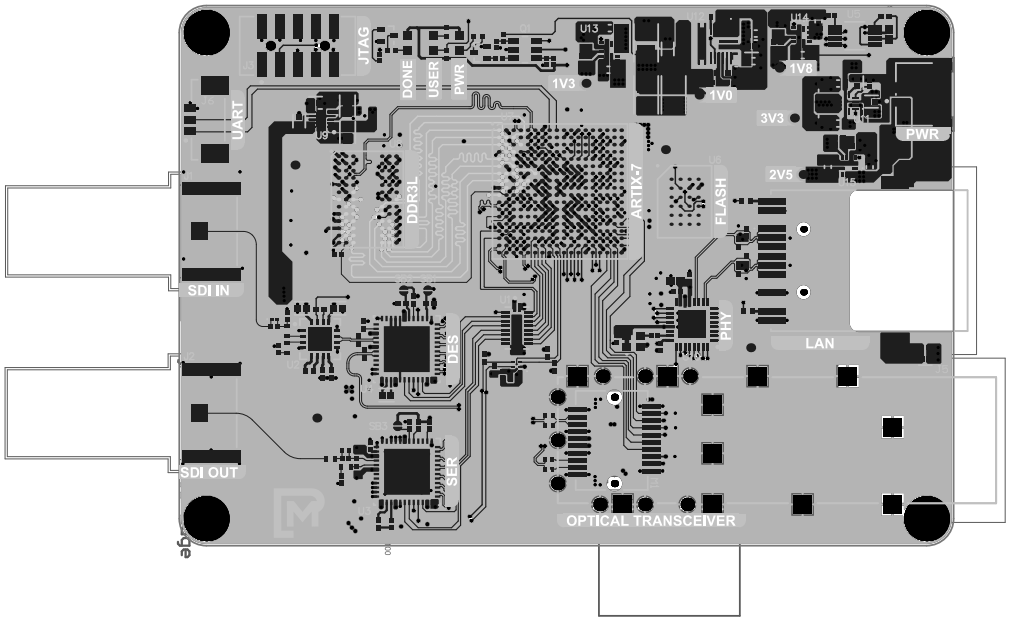


TITLE XC7A3G-FLASH		Date 9 AUG 2026
		REV 1.0.0
A4	CODE [No Variations]	Engineer Parsa Malekpour
	FILE NAME FLASH.SchDoc	SHEET 16 OF 18

Title		
Size A	Number	Revision
Date: 8/09/2026		Sheet of
File: C:\Users\..\Mechanical.SchDoc		Drawn By:



Title		
Size A	Number	Revision
Date: 8/09/2026		Sheet of
File: C:\Users\..\Power Diagram.SchDoc		Drawn By:



JLCPCB Code: JLC10121H-2116					
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.60mil	3.8	
1	L1 (SIG)	CF-004	1.38mil		
	Dielectric 1	NP-155F	3.91mil	4.1	
2	L2 (GND)	CF-004	0.60mil		
	Dielectric 2	NP-155F	7.87mil	4.36	
3	L3 (SIG)	CF-004	0.60mil		
	Dielectric 3	NP-155F	4.58mil	4.16	
4	L4 (GND)	CF-004	0.60mil		
	Dielectric 4	NP-155F	7.87mil	4.36	
5	L5 (PWR)	CF-004	0.60mil		
	Dielectric 5	NP-155F	4.58mil	4.16	
6	L6 (SIG)	CF-004	0.60mil		
	Dielectric 6	NP-155F	7.87mil	4.36	
7	L7 (GND)	CF-004	0.60mil		
	Dielectric 7	NP-155F	3.91mil	4.1	
8	L8 (SIG)	CF-004	1.38mil		
	Bottom Solder	Solder Resist	0.60mil	3.8	
	Bottom Overlay				
Total board thickness:			48.16mil		