## ASSIGNMENT 2:

## TITLE: Study of the design of combinational and sequential circuit using Proteus.

PRN**:** 22510064

DATE: 9/9/2023

AIM: a) Implement half adder and full adder circuit. Verify the truth table.

b) Implement circuit using basic gates for following flip flops: SR, JK, D, T. Verify the truth table.

c) Implement 2x1 and 4x2 multiplexer using basic gates. Derive output equation using K Map. Verify the truth table.

HARDWARE USED: No

SOFTWARE USED: Proteus 8 Professional

PROCEDURE:

* Open Proteus and create a new project.
* Select the Digital library and **add desired gates to the workspace / add the multiplexer IC to use.**
* Connect the **gates together using wires** / **multiplexer to circuit**.
* **Add input and output signals to the circuit / set the values of selector inputs.**
* Simulate he circuit by clicking play button.
* Observe the output for different combinations of input signals.

Results:

a)Adders:

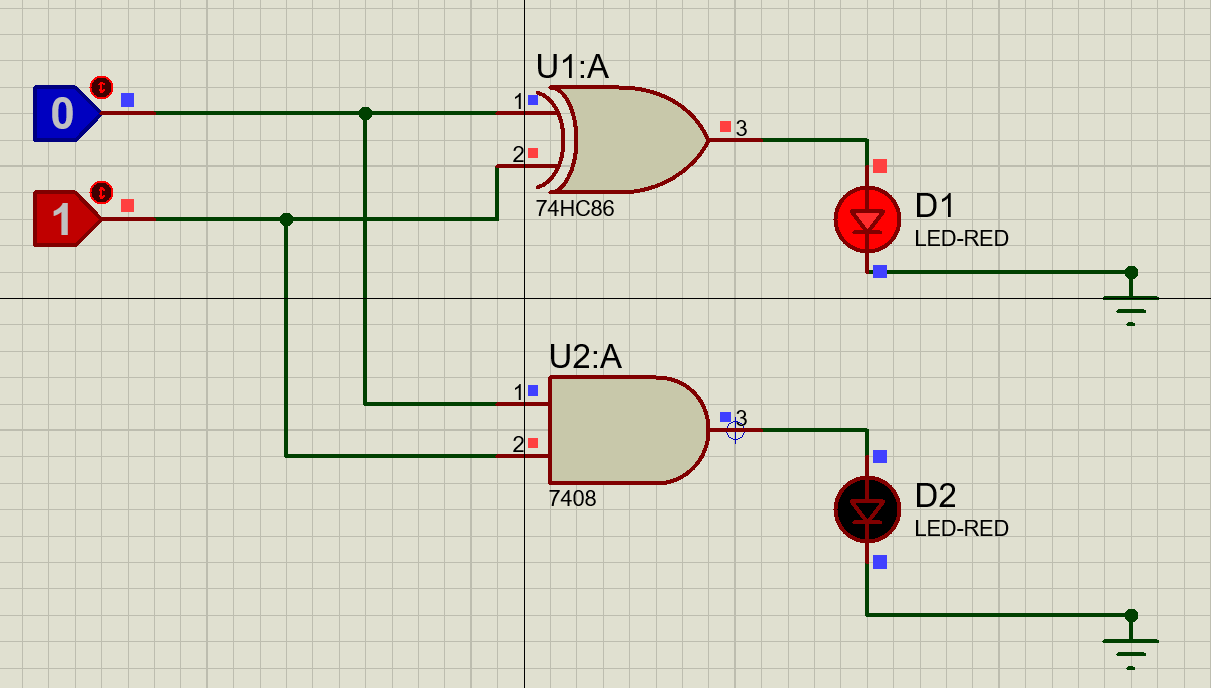
Half Adder:

Boolean Expression:  
S= A Ex-Or B

C=A.B

TRUTH TABLE:

|  |  |  |  |
| --- | --- | --- | --- |
| INPUTS | | OUTPUTS | |
| A | B | S | C |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |



Full Adder:

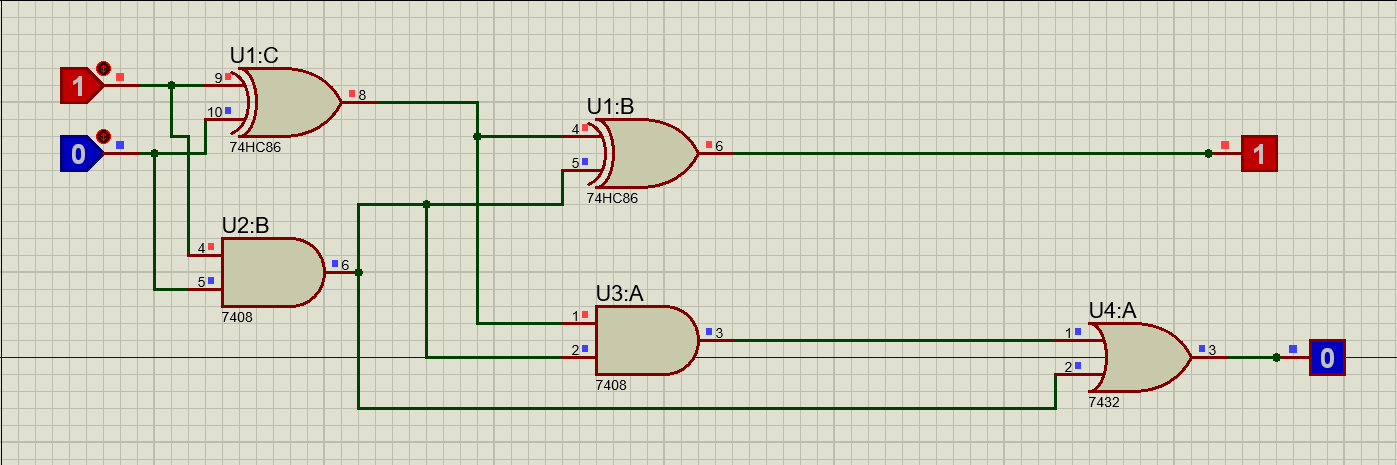
Boolean Expression:

S=A Ex-Or B Ex-Or C

C=A.B+B.Cin+A.Cin

TRUTH TABLE:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| INPUTS | | | OUTPUT | |
| A | B | Cin | S | C |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

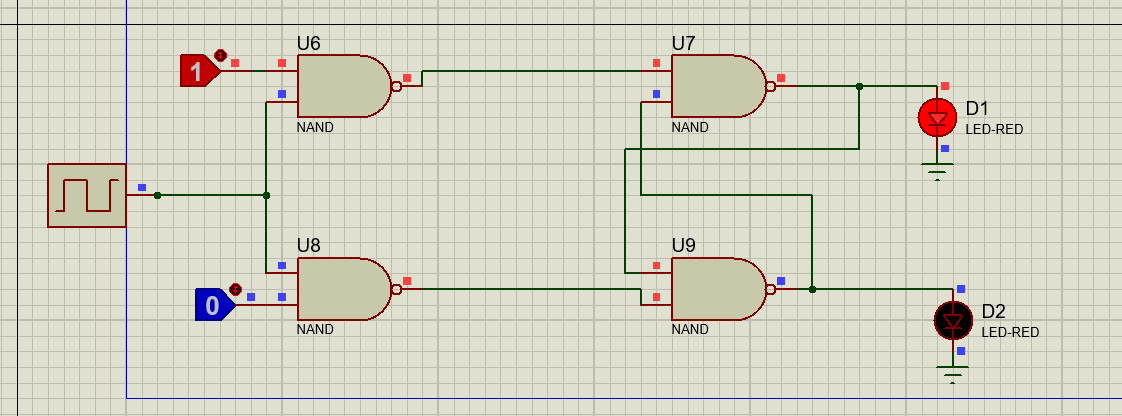


b) SR-FLIP FLOP:

TRUTH TABLE:

|  |  |  |
| --- | --- | --- |
| S | R | Qn+1 |
| 0 | 0 | Invalid |
| 0 | 1 | 1 |
| 1 | 0 | 01 |
| 1 | 1 | Hold |

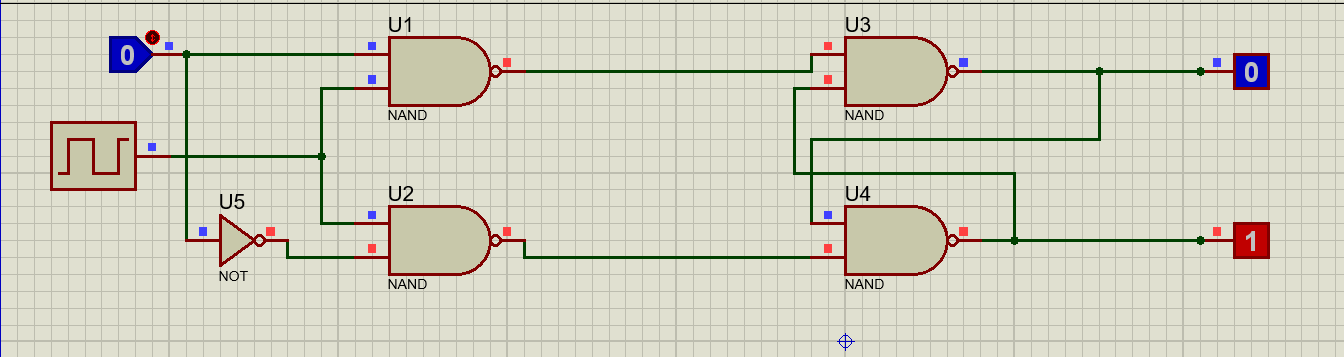
Logic Diagram:



D-Flip Flop

TRUTH TABLE:

|  |  |  |
| --- | --- | --- |
| Qn | Qn+1 | D |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

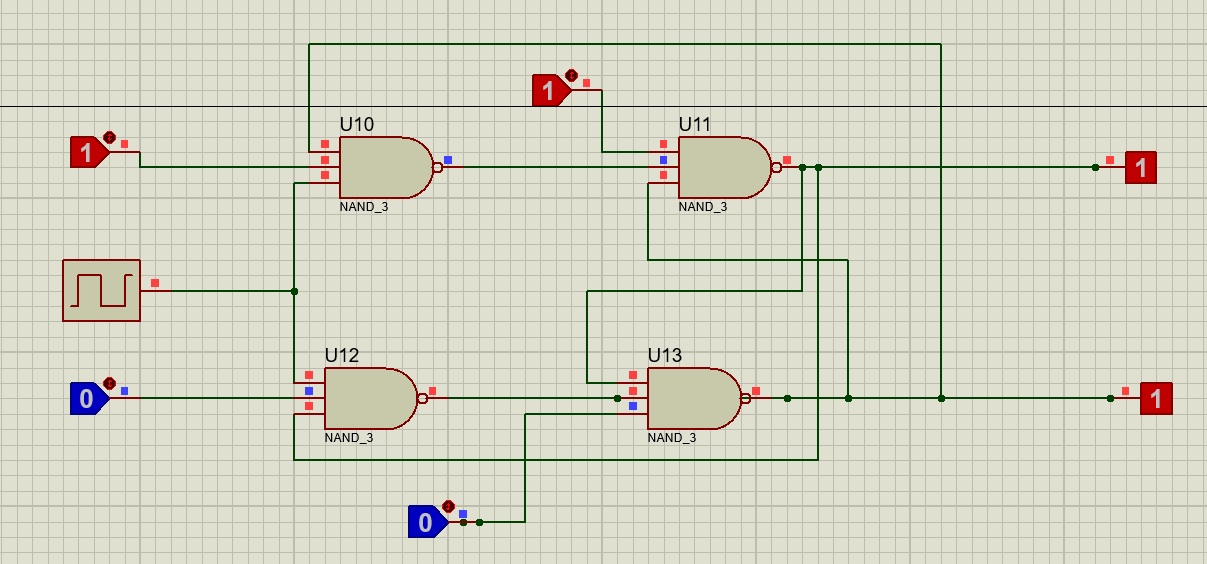
Logic Diagram:  


J-K FLIP FLOP:

TRUTH TABLE:

|  |  |  |
| --- | --- | --- |
| J | K | Qn+! |
| 0 | 0 | Hold |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Invalid |

Logic Diagram:

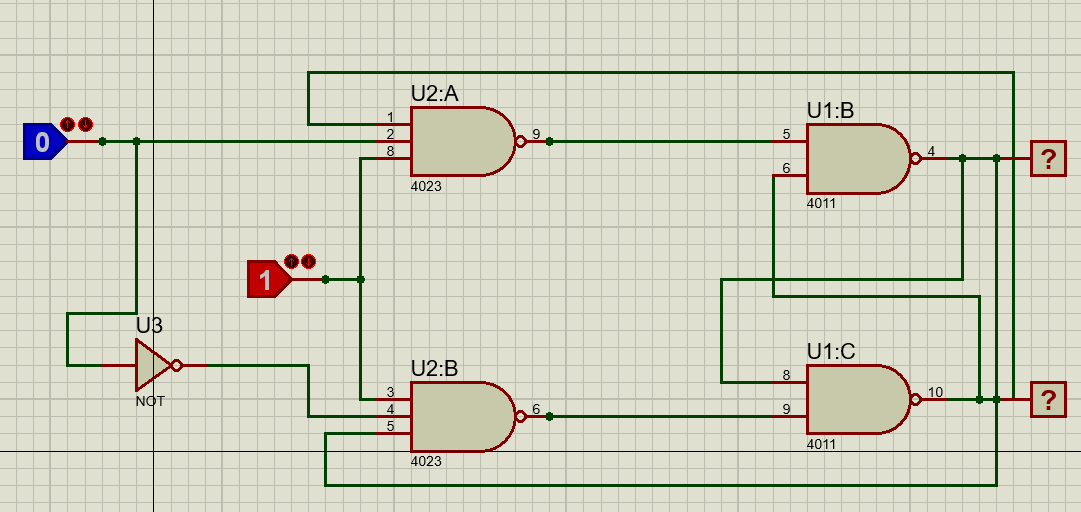


T Flip Flop:

Truth Table:

|  |  |  |
| --- | --- | --- |
| T |  |  |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

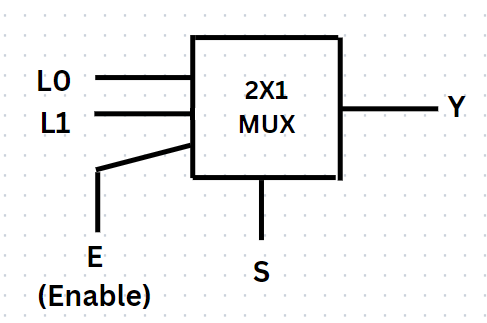
Logic Diagram:



c)Multiplexers

2X1:

Prototype:



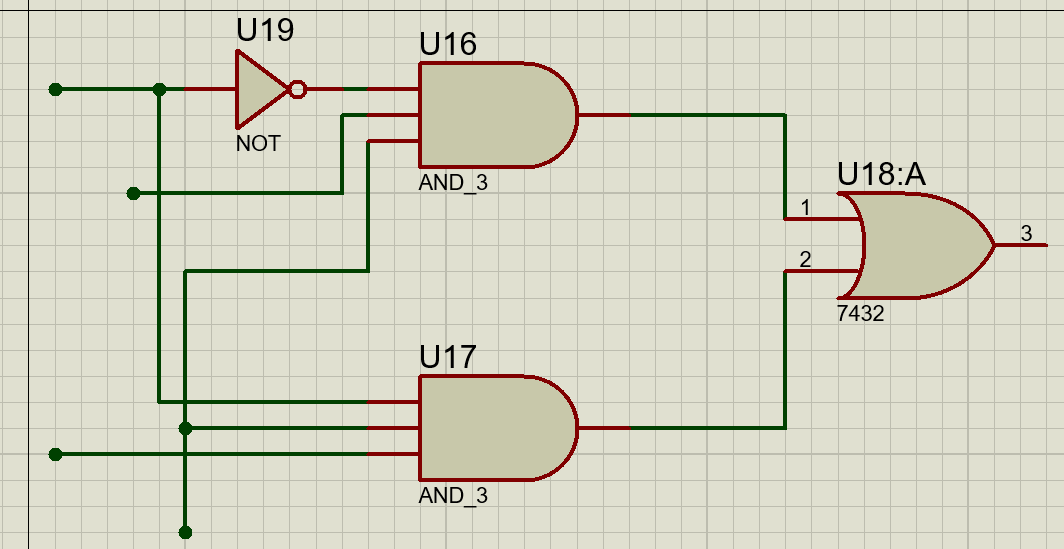
TRUTH TABLE:

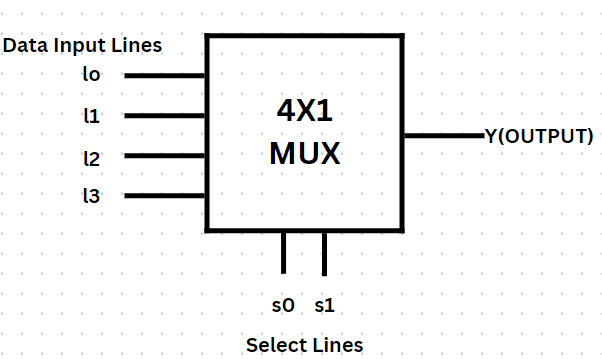
|  |  |  |
| --- | --- | --- |
| E | S | Y |
| 0 | - | 0 |
| 1 | 0 | L0 |
| 1 | 1 | L1 |

LOGIC EQUATION:

Y=EL0+ESL1=E(L0+SL1)

CIRCUIT:



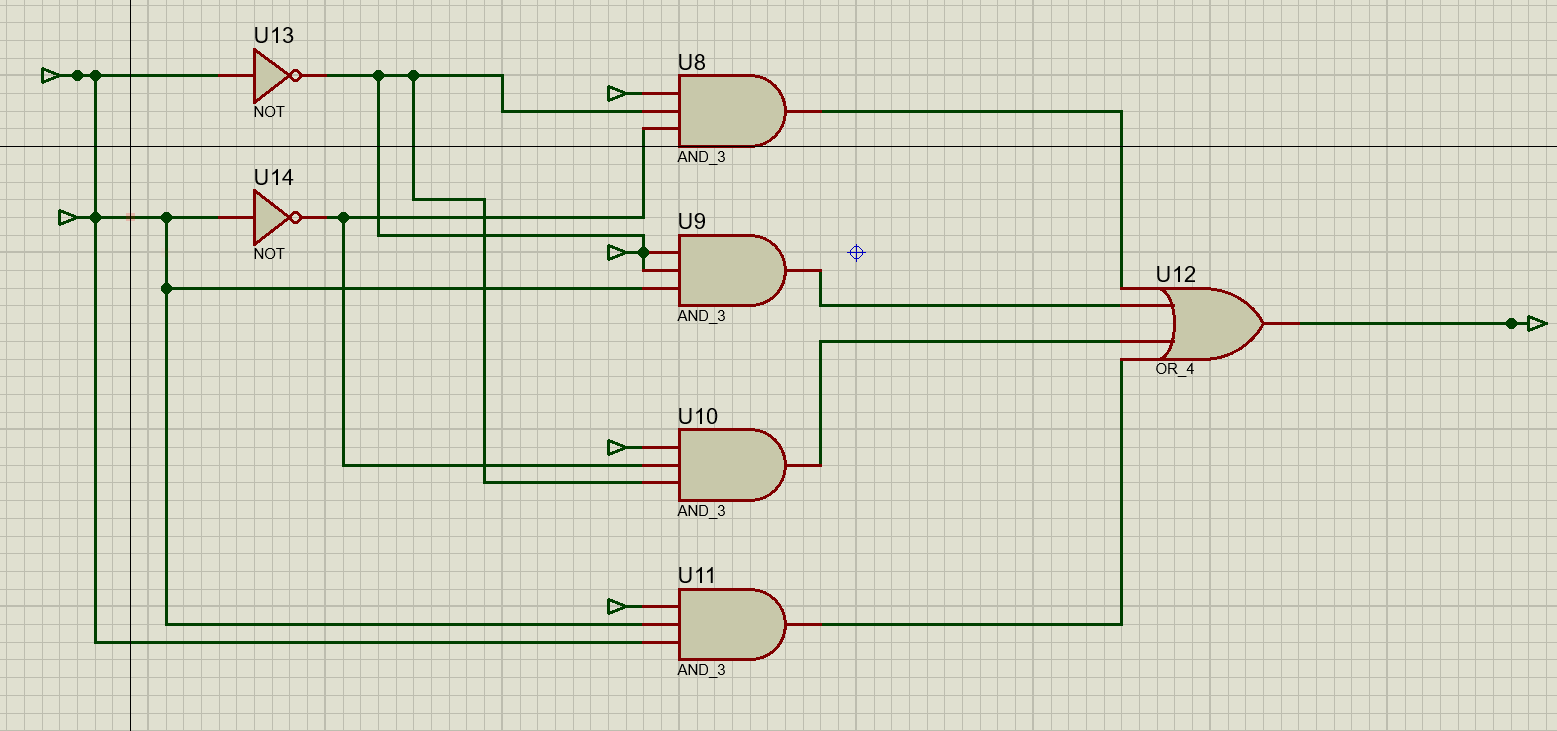
4x1:  
  
Prototype:  


TRUTH TABLE:

|  |  |  |
| --- | --- | --- |
| S1 | S0 | Y |
|  |  |  |
| 0 | 0 | L0 |
| 0 | 1 | L1 |
| 1 | 0 | L2 |
| 1 | 1 | L3 |

LOGIC EQUATION:

Y=L0+S0L1+S1L2+S1S0L3

Circuit:  


RESULTS:

* Optimization of circuit for speed can be done.
* Circuits can be tested for different input values.
* To compare different circuits.

CONCLUSION:

* Arithmetic circuits such as adders, subtractors, and multiplexers.
* Logic circuits such as multiplexers.