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DIGITAL CIRCUITS

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ABOUT SUBJECT

- Subject code : SSCA1020
- Semester : 1
- Web Reference :

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REFERENCE BOOKS

Title	Author/s	Publication
Computer System Architecture	M. Morris Mano	Pearson
Computer Architecture and Organization	Ghoshal, Subrata	Pearson
Computer Architecture &Organization	M. Murdocca & V. Heuring	WILEY

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LOGIC GATES

- Logic Gate act according to logic/programme given by us.
- Logic gates are made up of diodes and transistors.
- Logic gate is used to allow and denied a digital circuit.

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LOGIC GATES

- Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output.
- The relationship between the input and the output is based on a **certain logic**.
- Digital electronic circuits operate with voltages of two logic levels namely Logic Low and Logic High. The range of voltages corresponding to Logic Low is represented with '0'. Similarly, the range of voltages corresponding to Logic High is represented with '1'.

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LOGIC GATES CLASSIFICATION

- Basic gates
- Universal gates
- Special gates

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BASIC GATES

- We learnt that the Boolean functions can be represented either in sum of products form or in product of sums form based on the requirement.
- So, we can implement these Boolean functions by using basic gates. The basic gates are AND, OR & NOT gates.

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NOT GATE

- A NOT gate is a digital circuit that has single input and single output.
- The output of NOT gate is the logical inversion of input. Hence, the NOT gate is also called as inverter.

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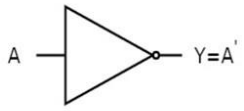
NOT GATE

- The following table shows the truth table of NOT gate.

A	Y = A'
0	1
1	0



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NOT GATE

- Here A and Y are the input and output of NOT gate respectively. If the input, A is '0', then the output, Y is '1'. Similarly, if the input, A is '1', then the output, Y is '0'.

- The following figure shows the symbol of NOT gate, which is having one input, A and one output, Y.

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AND GATE

- An AND gate is a digital circuit that has two or more inputs and produces an output, which is the logical AND of all those inputs. It is optional to represent the Logical AND with the symbol '.'.
- The following table shows the truth table of 2-input AND gate.

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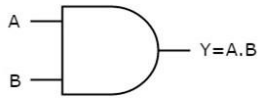
AND GATE

The following table shows the truth table of 2-input AND gate.

A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1



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AND GATE

- Here A, B are the inputs and Y is the output of two input AND gate. If both inputs are '1', then only the output, Y is '1'. For remaining combinations of inputs, the output, Y is '0'.

- The following figure shows the symbol of an AND gate, which is having two inputs A, B and one output, Y.

- This AND gate produces an output (Y), which is the logical AND of two inputs A, B. Similarly, if there are 'n' inputs, then the AND gate produces an output, which is the logical AND of all those inputs. That means, the output of AND gate will be '1', when all the inputs are '1'.

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OR GATE

- An OR gate is a digital circuit that has two or more inputs and produces an output, which is the logical OR of all those inputs.

- This logical OR is represented with the symbol '+'.

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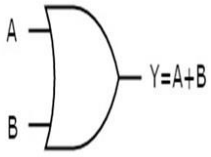
OR GATE

The following table shows the truth table of 2-input OR gate.

A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1



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OR GATE

- Here A, B are the inputs and Y is the output of two input OR gate. If both inputs are '0', then only the output, Y is '0'. For remaining combinations of inputs, the output, Y is '1'.

- This OR gate produces an output (Y), which is the logical OR of two inputs A, B. Similarly, if there are 'n' inputs, then the OR gate produces an output, which is the logical OR of all those inputs. That means, the output of an OR gate will be '1', when at least one of those inputs is '1'.

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UNIVERSAL GATE

- NAND & NOR gates are called as universal gates. Because we can implement any Boolean function, which is in sum of products form by using NAND gates alone.
- Similarly, we can implement any Boolean function, which is in product of sums form by using NOR gates alone.
- **So It is possible to implements all the other gates using NAND and NOR so is called Universal gates.**

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NAND GATE

- NAND = AND +NOT
- NAND gate is a digital circuit that has two or more inputs and produces an output, which is the inversion of logical AND of all those inputs.

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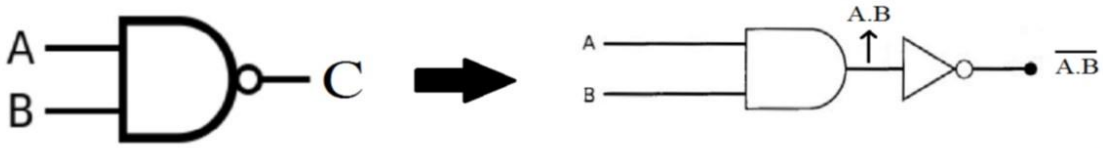
NAND GATE

- The following table shows the truth table of 2-input NAND gate.

A	B	Y = (A.B)'
0	0	1
0	1	1
1	0	1
1	1	0



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NAND GATE

- Here A, B are the inputs and Y is the output of two input NAND gate. When both inputs are '1', the output, Y is '0'. If at least one of the input is zero, then the output, Y is '1'. This is just opposite to that of two input AND gate operation.

- NAND gate operation is same as that of AND gate followed by an inverter. That's why the NAND gate symbol is represented like that.

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NOR GATE

- NOR gate is a digital circuit that has two or more inputs and produces an output, which is the inversion of logical OR of all those inputs.

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NOR GATE

The following table shows the truth table of 2-input NOR gate.

A	B	Y = (A+B)'
0	0	1
0	1	0
1	0	0
1	1	0

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NOR GATE

- Here A, B are the inputs and Y is the output. If both inputs are '0', then the output, Y is '1'. If at least one of the input is '1', then the output, Y is '0'.
- This is just opposite to that of two input OR gate operation.
- Here A, B are the inputs and Y is the output. If both inputs are '0', then the output, Y is '1'. If at least one of the input is '1', then the output, Y is '0'. This is just opposite to that of two input OR gate operation.

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SPECIAL GATE

- Ex-OR & Ex-NOR gates are called as special gates.
- Because, these two gates are special cases of OR & NOR gates.

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EX-OR GATE

- The full form of Ex-OR gate is Exclusive-OR gate.
- Its function is same as that of OR gate except for some cases, when the inputs having even number of ones.

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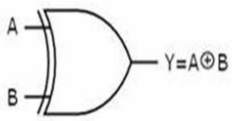
EX-OR GATE

The following table shows the truth table of 2-input Ex-OR gate.

A	B	Y = A⊕B
0	0	0
0	1	1
1	0	1
1	1	0



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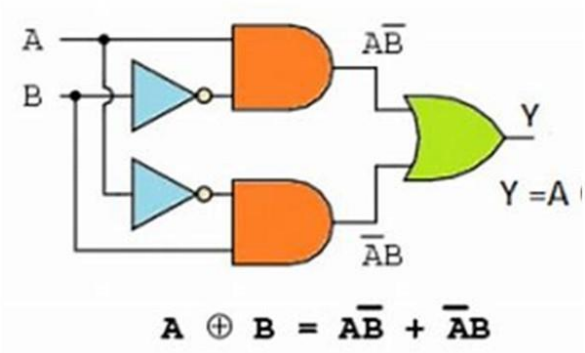
EX-OR GATE



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EX-OR GATE

- Here A, B are the inputs and Y is the output of two input Ex-OR gate. The truth table of Ex-OR gate is same as that of OR gate for first three rows. The only modification is in the fourth row. That means, the output (Y) is zero instead of one, when both the inputs are one, since the inputs having even number of ones.

- Therefore, the output of Ex-OR gate is '1', when only one of the two inputs is '1'. And it is zero, when both inputs are same.

- Ex-OR gate operation is similar to that of OR gate, except for few combination(s) of inputs. That's why the Ex-OR gate symbol is represented like that. The output of Ex-OR gate is '1', when odd number of ones present at the inputs. Hence, the output of Ex-OR gate is also called as an odd function.

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EX-NOR GATE

- The full form of Ex-NOR gate is Exclusive-NOR gate.
- Its function is same as that of NOR gate except for some cases, when the inputs having even number of ones.

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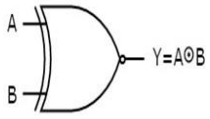
EX-NOR GATE

The following table shows the truth table of 2-input Ex-NOR gate.

A	B	Y = A⊙B
0	0	1
0	1	0
1	0	0
1	1	1



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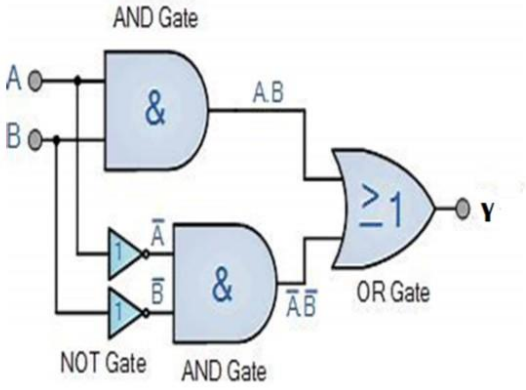
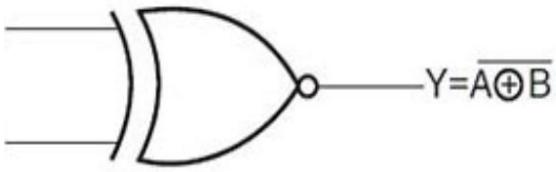
EX-NOR GATE





$$Y = (\overline{A \oplus B}) = (A.B + \overline{A}.\overline{B})$$

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FLIP FLOPS

- A circuit that has two stable states is treated as a flip flop. These stable states are used to store binary data that can be changed by applying varying inputs.
- **The flip flops are the fundamental building blocks of the digital system.** Flip flops and latches are examples of data storage elements.
- In the sequential logical circuit, **the flip flop is the basic storage element that maintains the state until directed by input to change the state.**

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FLIP FLOPS

- Flip-flops are formed from pairs of logic gates where the gate outputs are fed into one, of the inputs of the other gate in the pair.
- This results in a regenerative circuit 'having two stable output states (binary one and zero). Frequently additional gates are added for control of the circuit.
- While some flip-flops are operated " as yet chrohously (without timing pulses), most are ,operated 'Linier clock control in a synchronous system

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TYPES OF FLIP FLOPS

- SR Flip-Flop
- D Flip-Flop
- JK Flip-Flop
- T Flip-Flop

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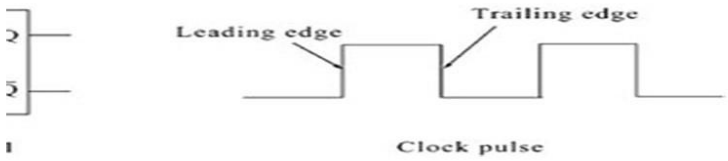
CLOCK PULSE

Clock pulse referred to as CP, the clock pulse is the **vibration of a quartz crystal** located inside a computer for synchronizing the timing of hardware components.

The speed of the computer's processor, measured in MHz or GHz, refers to its number of clock pulse cycles per second. CPU terms, GHz, MHz.



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TYPES OF FLIP FLOPS

- SR flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, SR latch operates with enable signal.

- This circuit has two inputs S & R and two outputs Q & Q'. The operation of SR flip-flop is similar to SR Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable.

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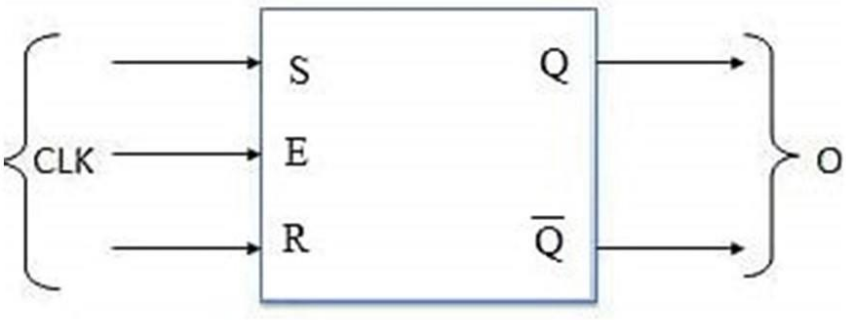
SR FLIP-FLOP

Block Diagram



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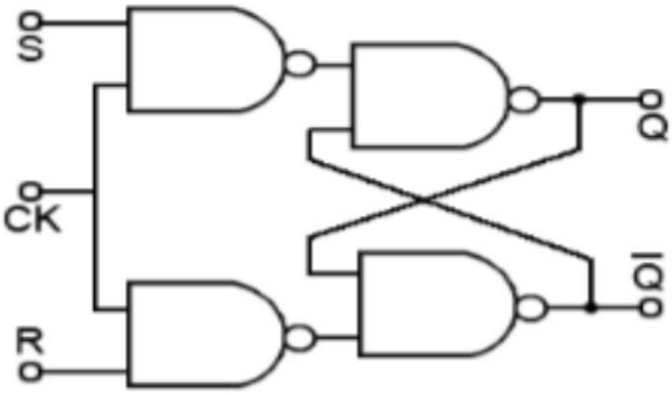
SR FLIP-FLOP

Circuit Diagram of SR Flip-flop



Truth table of SR Flip-flop

INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

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SR FLIP-FLOP

- Here, present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive transition of clock signal is applied.

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D FLIPFLOP

- D(data) flip-flop operates with only positive clock transitions or negative clock transitions.

- Whereas, D latch operates with enable signal. That means, the output of D flip-flop is insensitive to the changes in the input, D except for active transition of the clock signal.

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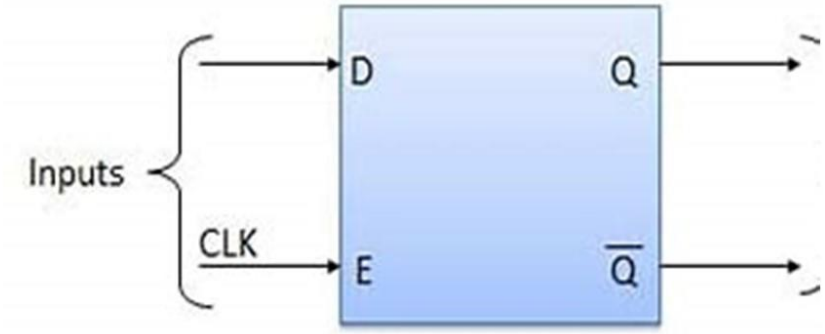
D FLIPFLOP

Block Diagram



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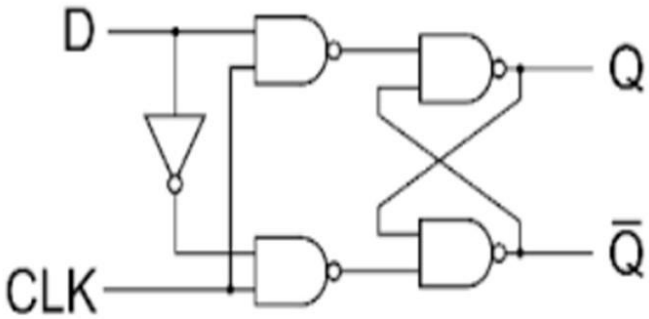
D FLIPFLOP

Circuit Diagram of D Flip-flop



Truth table of D Flip-flop

CLOCK	D	Q_{+1}	State
1	0	0	RESET
1	1	1	SET
0	x	Q_n	NO CHANGE

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D FLIPFLOP

- This circuit has single input D. The operation of D flip-flop is similar to D Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable.
- Therefore, D flip-flop always Hold the information, which is available on data input, D of earlier positive transition of clock signal.
- Next state of **D flip-flop is always equal to data input**, D for every positive transition of the clock signal. Hence, D flip-flops can be used in registers, shift registers and some of the counters.

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JK FLIPFLOP

- **JK flip-flop is the modified version of SR flip-flop.**
- It operates with only positive clock transitions or negative clock transitions.
- JK flip-flop can be used for one of these four functions such as Hold, Reset, Set & Complement of present state based on the input conditions, when positive transition of clock signal is applied.

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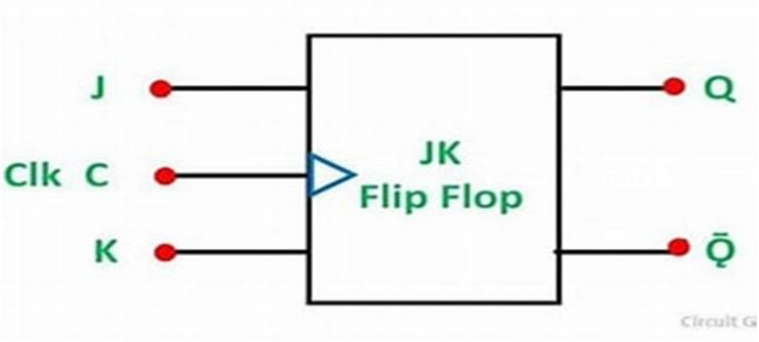
J-K FLIPFLOP

Block Diagram



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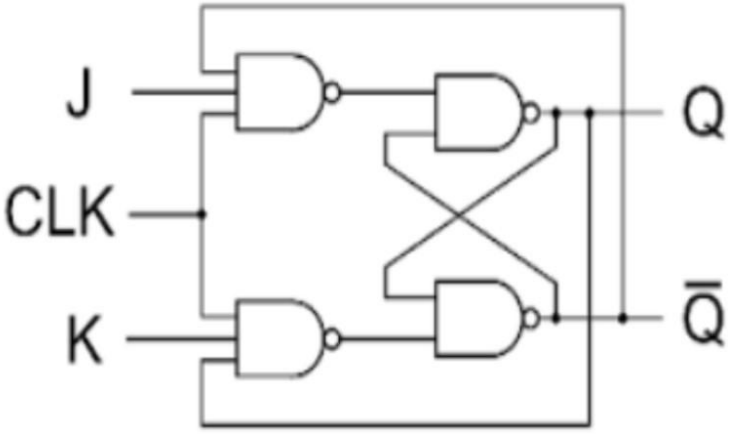
J-K FLIPFLOP

Circuit Diagram of JK Flip-flop



Truth table of JK Flip-flop

Clk	J	K	Q	Q'	State
1	0	0	Q	Q'	No change in state
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles Q̄

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T FLIPFLOP

- **T (Toggle)flip-flop is the simplified version of JK flip-flop.**
- It is obtained by connecting the same input 'T' to both inputs of JK flip-flop.
- It operates with only positive clock transitions or negative clock transitions.

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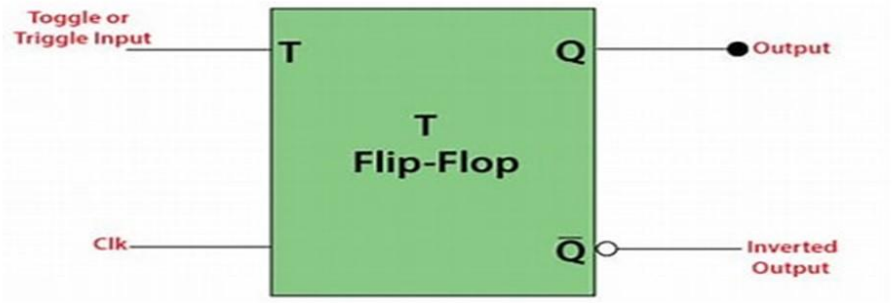
T FLIPFLOP

Block Diagram



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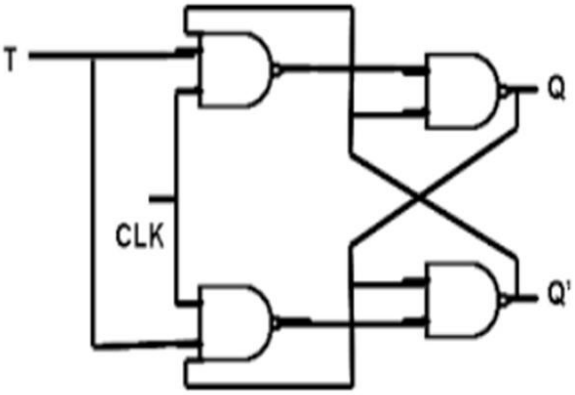
T FLIPFLOP

Circuit Diagram of T Flip-flop



Truth table of T Flip-flop

CP	T	Q_{n+1}	State
1	0	Q_n	NO CHANGE
1	1	$\overline{Q}_n$	TOGGLES

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