RISHIK SAHA-2022CS11932| PARTH VERMA-2022CS11936

COL215-HARDWARE_3

REPORT

PART-1

AIM

To Design and test compute unit, implementation of MAC unit (simple or optimized) for image filtering operation.

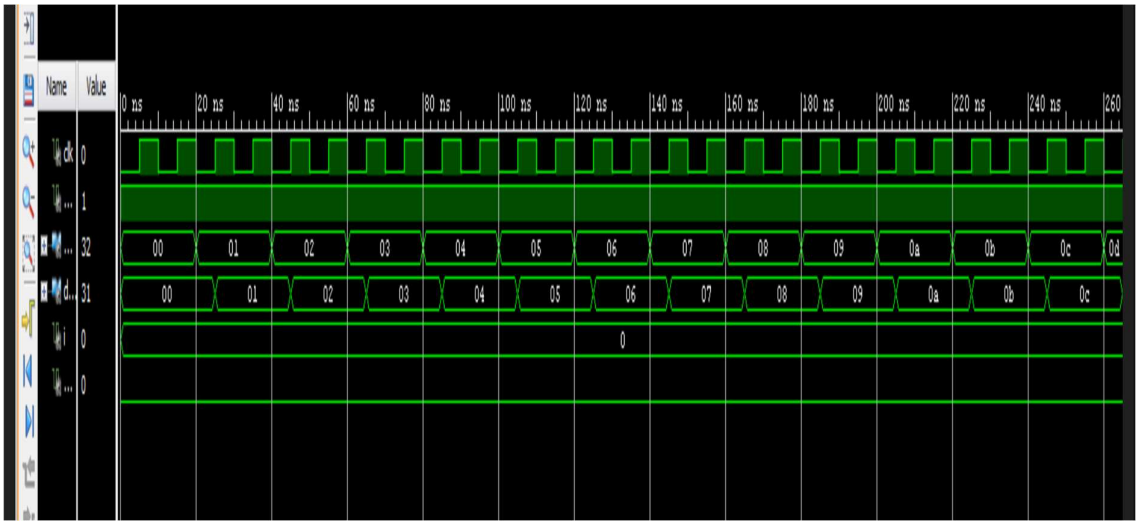
APPROACH

- First of all, all the basic sub components required for the hardware design were identified and created.
- The sub components included MAC, Comparators (max and min) and Registers.
- These modules were carefully designed and were tested using test benches for each of them.

FUNCTIONALITY OF SUB MODULES

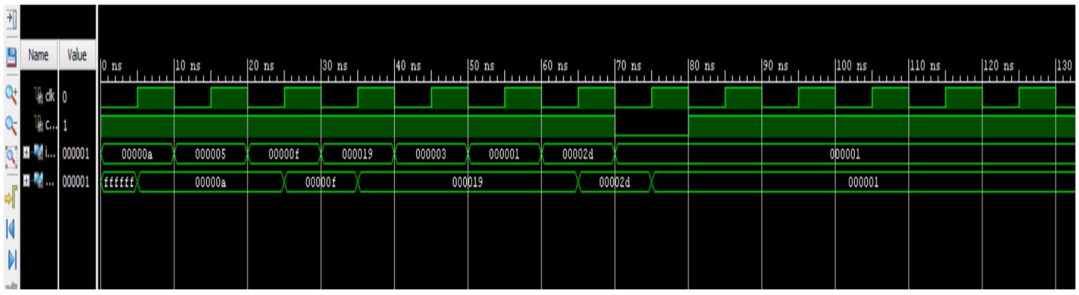
Registers

- Registers as an entity have 3 input ports (clock, write enable, data in) and 1 output port (data out).
- These are used to locally store the data and are essential in data transfer.



Comparator (Max)

- The comparator (max) is used to extract the maximum out of the data stream.
- The comparators are useful in the process of normalization of the output pixels.



Comparator (Min)

- The comparator (min) is used to extract the minimum out of the data stream.
- The comparators are useful in the process of normalization of the output pixels.

MAC (Multiplicative Accumulator)

- The MAC is responsible for evaluating output pixels by pre decided operations on the input pixels with the data of kernel.
- MAC consists of 4 input signals “clock, input1, intput2, and a control signal”. While it gives a single output signal.
- FSM is responsible for proper accumulation of multiplicative products in the MAC to produce the desired output pixel. This is done via “control signal” which is received by MAC as an input signal.