RISHIK SAHA-2022CS11932| PARTH VERMA-2022CS11936

COL215-HARDWARE_3

REPORT

PART-1

AIM

To Design and test compute unit, implementation of MAC unit (simple or optimized) for image filtering operation.

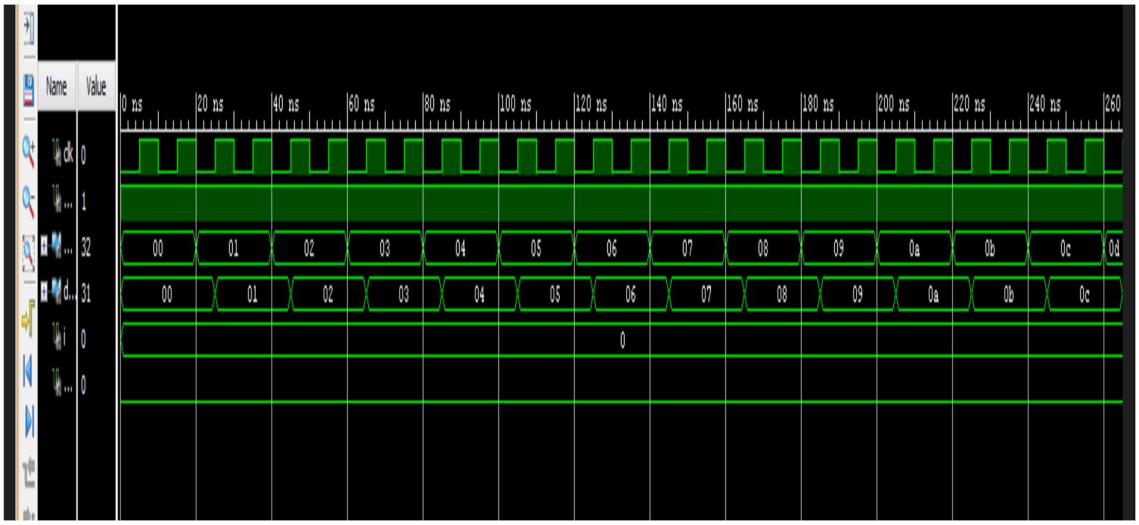
APPROACH

- First of all, all the basic sub components required for the hardware design were identified and created.
- The sub components included MAC, Comparators (max and min) and Registers.
- These modules were carefully designed and were tested using test benches for each of them.

FUNCTIONALITY OF SUB MODULES

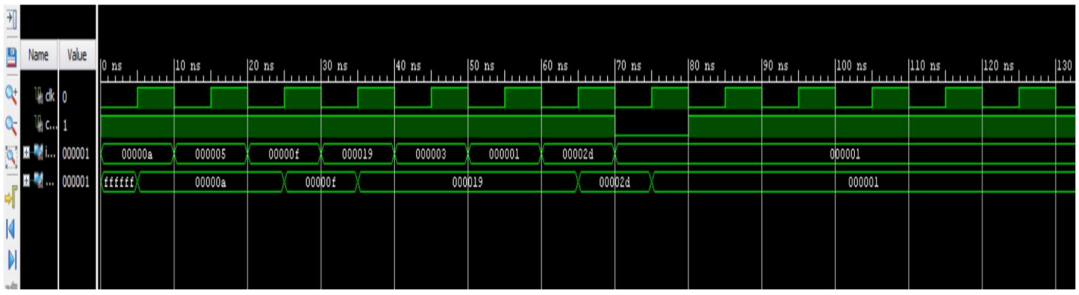
Registers

- Registers as an entity have 3 input ports (clock, write enable, data in) and 1 output port (data out).
- These are used to locally store the data and are essential in data transfer.



Comparator (Max)

- The comparator (max) is used to extract the maximum out of the data stream.
- The comparators are useful in the process of normalization of the output pixels.

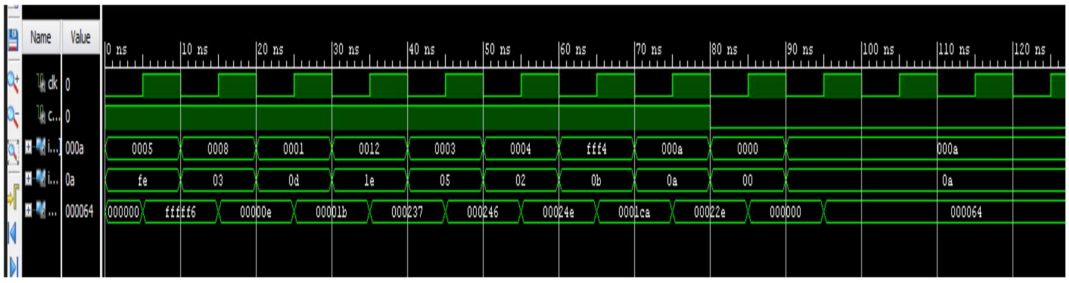


Comparator (Min)

- The comparator (min) is used to extract the minimum out of the data stream.
- The comparators are useful in the process of normalization of the output pixels.

MAC (Multiplicative Accumulator)

- The MAC is responsible for evaluating output pixels by pre decided operations on the input pixels with the data of kernel.
- MAC consists of 4 input signals “clock, input1, intput2, and a control signal”. While it gives a single output signal.
- FSM is responsible for proper accumulation of multiplicative products in the MAC to produce the desired output pixel. This is done via “control signal” which is received by MAC as an input signal.



PART2

- Part 2 of this assignment mainly consisted of forming FSM, The FSM here is responsible for joining all the sub components developed in part 1.
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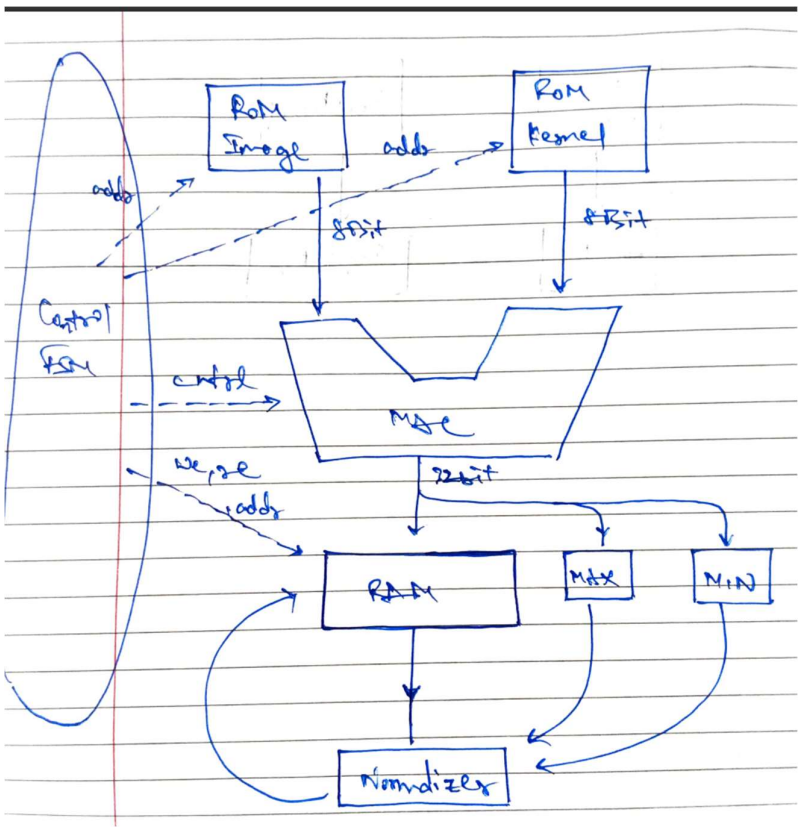

- The FSM was developed ensuring it satisfies the above control path.
- Majorly it consisted of compute unit and display unit.
- In the compute unit the input pixels from ROM and filter values from kernel were read and were given to the mac.

- The logic for this was carefully developed and was named as “CONV” state of the FSM.
- “max” and “min” comparators were installed at the output signal of the MAC to extract the minimum and maximum of the output signals of resultant pixels.
- The max and min output pixels were later utilized for normalization.
- Once the output pixels were formed this was given to the display controller developed in the previous assignment.
- The final output image was developed.

The State Diagram for the above model is shown as below: