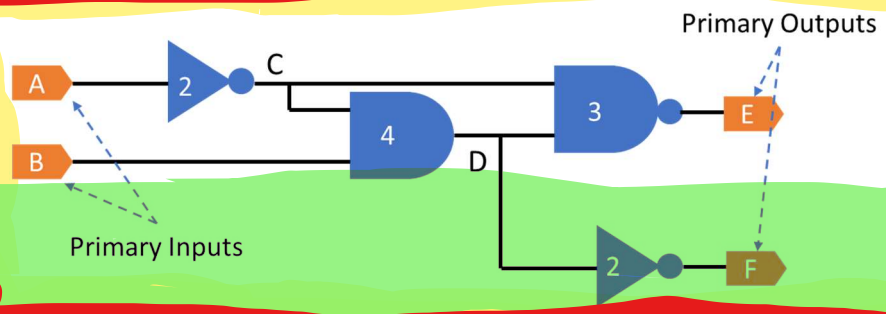
COL215: Digital Logic and System Design
Software Assignment 1
Submission Deadline: 20 August 2023, 11:55 PM

Consider the following diagram representing a combinational digital circuit – each gate implements a Boolean function of its inputs and there are no cycles in the circuit. The numbers annotated on the gates represent the delay *d* through the gate, in nanoseconds. If the inputs of a gate are ready at time *t*, then the output is ready at time *t+d*.



(a) How much time does such a circuit take to compute its primary outputs? For the example above, the maximum delay *for E is 2+4+3=9, and for F is 2+4+2=8*. Write a program to compute the **delay** of every primary output in a combinational circuit (defined as the earliest time when the output is ready), given the circuit representation and delay information of the individual gates.
Input: Circuit file (see example file *circuit.txt* for diagram above)
Input: Gate Delay file (see example file *gate_delays.txt* for diagram above)
Output: Output Delay file (see example file *output_delays.txt* for diagram above)

(b) Extend your program to answer the converse question: suppose we require the output to be ready at a specific time. When do we require each input to be ready so that the output timing requirement is met?
Input: Circuit file (see example file *circuit.txt* for diagram above)
Input: Required Output Delay file (see example file *required_delays.txt* for diagram above)
Output: Input Delay file (see example file *input_delays.txt* for the diagram and *required_delays.txt* file above)

Use Python or C/C++ for implementation. Submit the following:

(a) A short document with the following details:
   a. Your algorithm.
   b. Explain the time complexity of your algorithm.
   c. Your *testing strategy*. What test cases did you write to check your implementation? Why? Make sure that the test cases validate the features of your algorithm.

(b) Your implementation.
   a. Code
   b. Test cases