Rishik Saha- 2022CS11932 | Parth Verma-2022CS11936

COL215 – Hardware Assingment_1

4- Digit 7-Segement Display

Part1: 7 Segment Decoder

Approach:

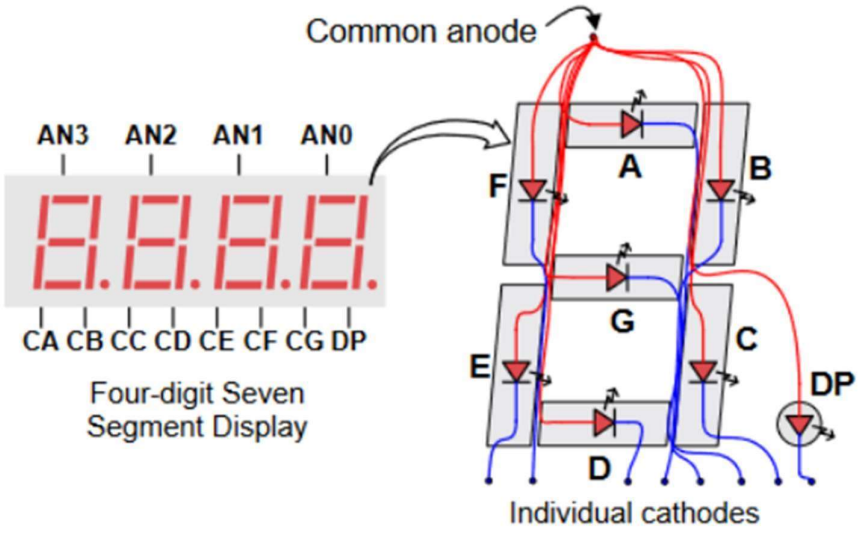
The 7-segment decoder takes a 4-bit input and outputs a 7-bit vector which guides the LEDs to turn on in seven segment Display. (Here we have represented hexadecimal values,

(A, b, C, d, E, F)).

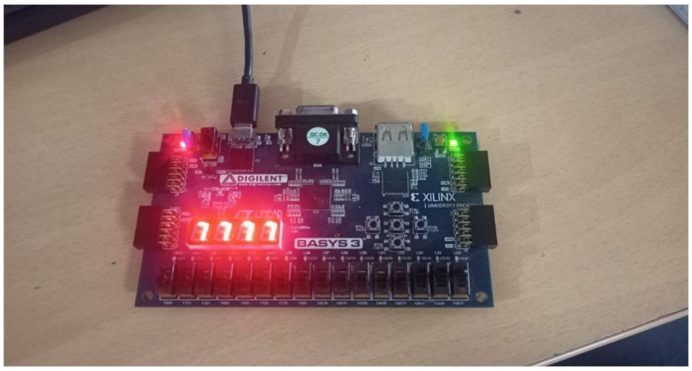
Lab Work:

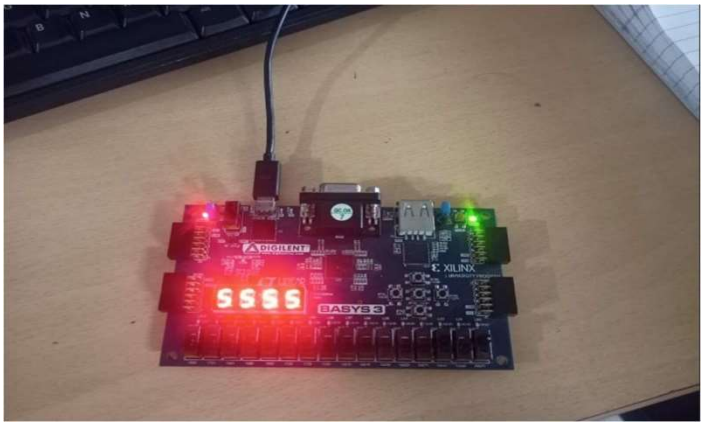
We developed the minimal combinatorial logic formula on of each individual cathodes on the basis of 4-bit input.

The decoder module was implemented with input as a 4-bit number and output as 7-bit cathode signals. (By default, we made all the four anodes ON)



Some of the outputs:





Part2: Driving all 4 LED's Display

Approach

Seven Segment Decoder:

We use the same 7 segment decoder as developed above.

Timing Circuit:

This module uses the inbuilt clock on Basys3 FGPA Board, (100 MHz) and contains a counter which sets the frequency to 1Khz. This gives input to the 4:1 Multiplexer to select the correct signal. It also drives the anode signal.

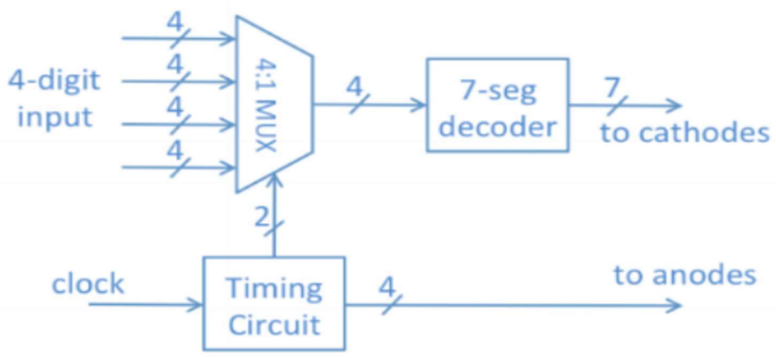
4:1 Multiplexer:

The module receives 4 (4 -Bit signals), input from the timing circuit. This then selects one signal and outputs to the
seven-segment display.

Lab Work:

All the above modules were implemented in VHDL, and then properly connected. To give the desired output.

Block Diagram:



Synthesis Report:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	11	0	0	20800	0.05
LUT as Logic	11	0	0	20800	0.05
LUT as Memory	0	0	0	9600	0.00
Slice Registers	20	0	0	41600	0.05
Register as Flip Flop	20	0	0	41600	0.05
Register as Latch	0	0	0	41600	0.00
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

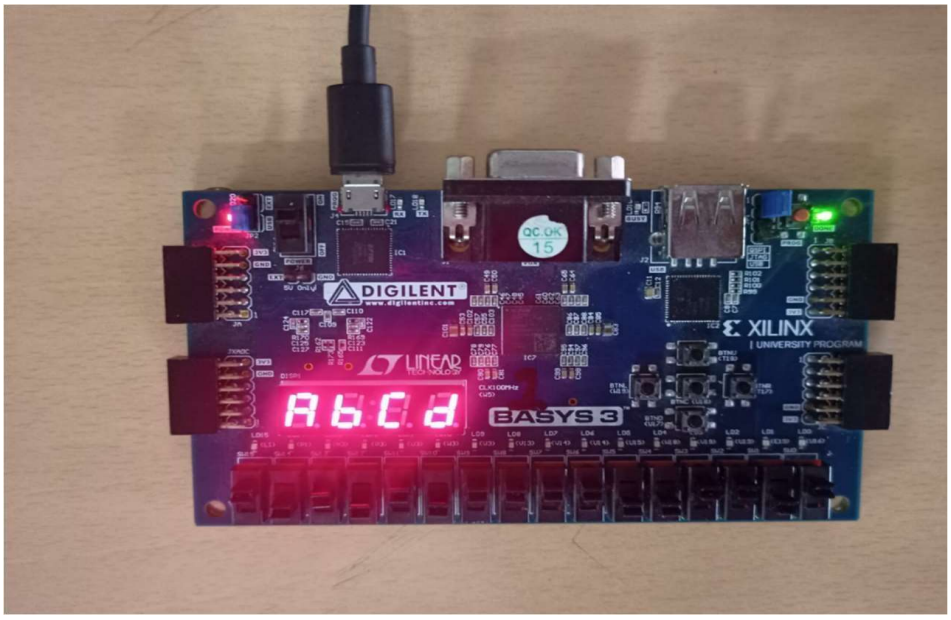
3. DSP

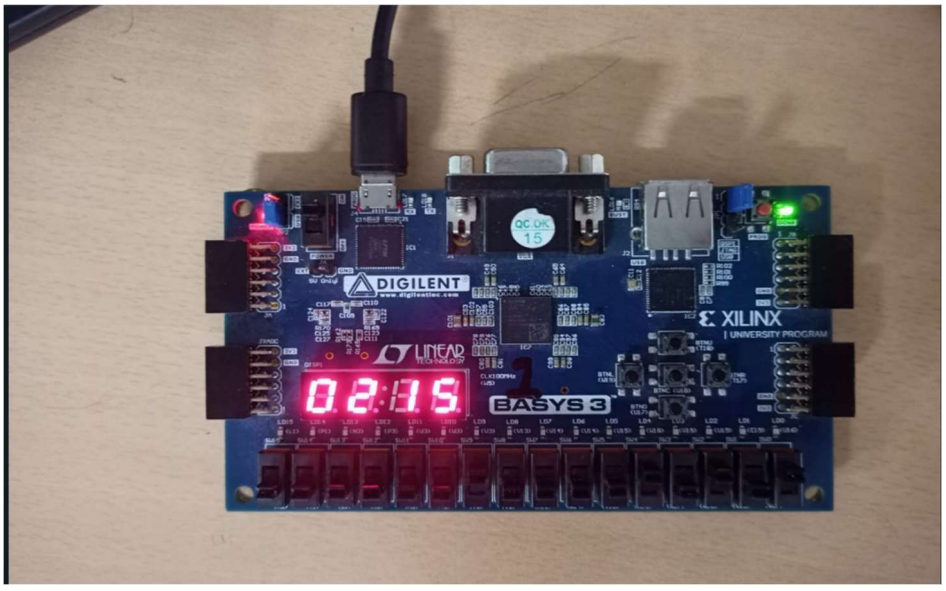
Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	90	0.00

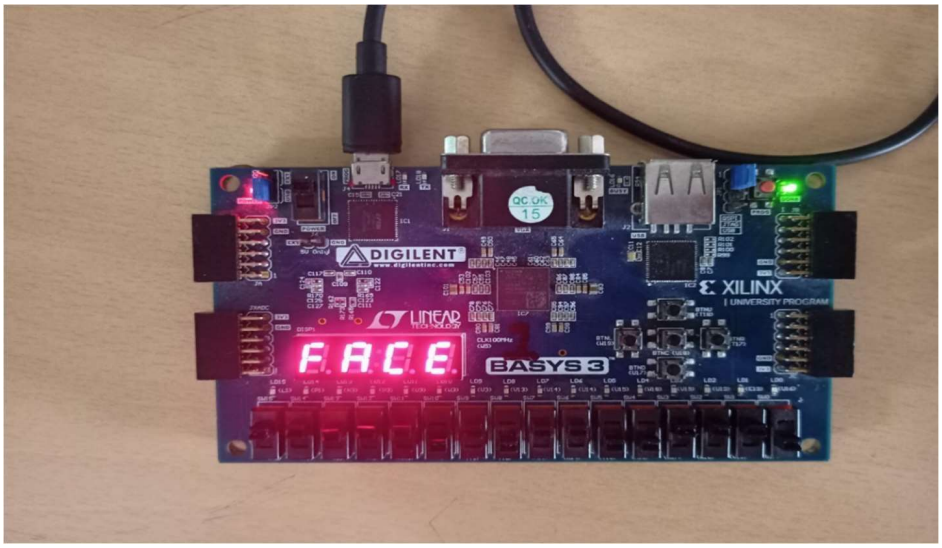
7. Primitives

Ref Name	Used	Functional Category
FDRE	20	Flop & Latch
IBUF	17	IO
OBUF	11	IO
LUT4	7	LUT
CARRY4	5	CarryLogic
LUT6	4	LUT
LUT2	4	LUT
LUT1	1	LUT
BUFG	1	Clock

Some of the outputs:



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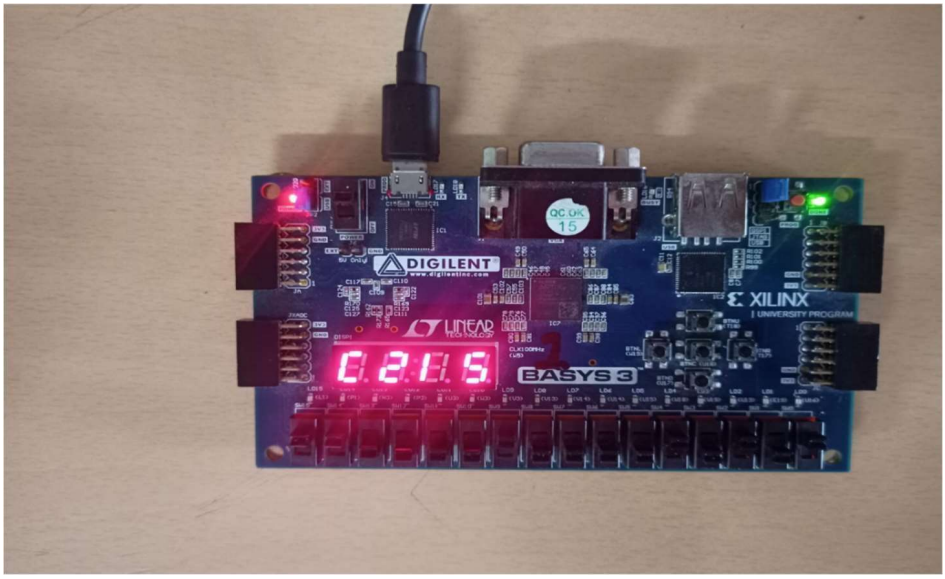
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