COL216

BUILD THE PROCESSOR(4)

PROCESSOR

Department of Computer Science and Engineering

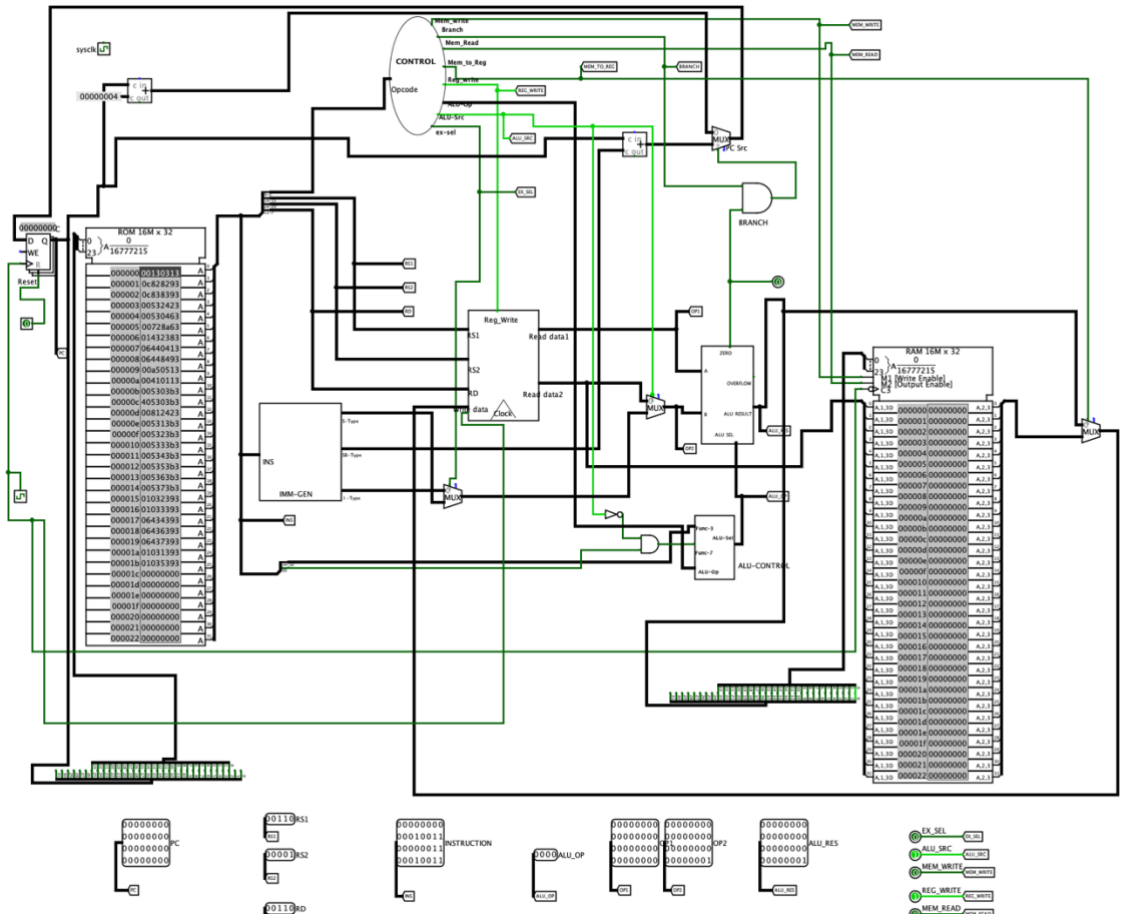
IIT Delhi

Parth Verma -2022CS11936

Umang Tripathi – 2022CS51134

Circuit Design :-

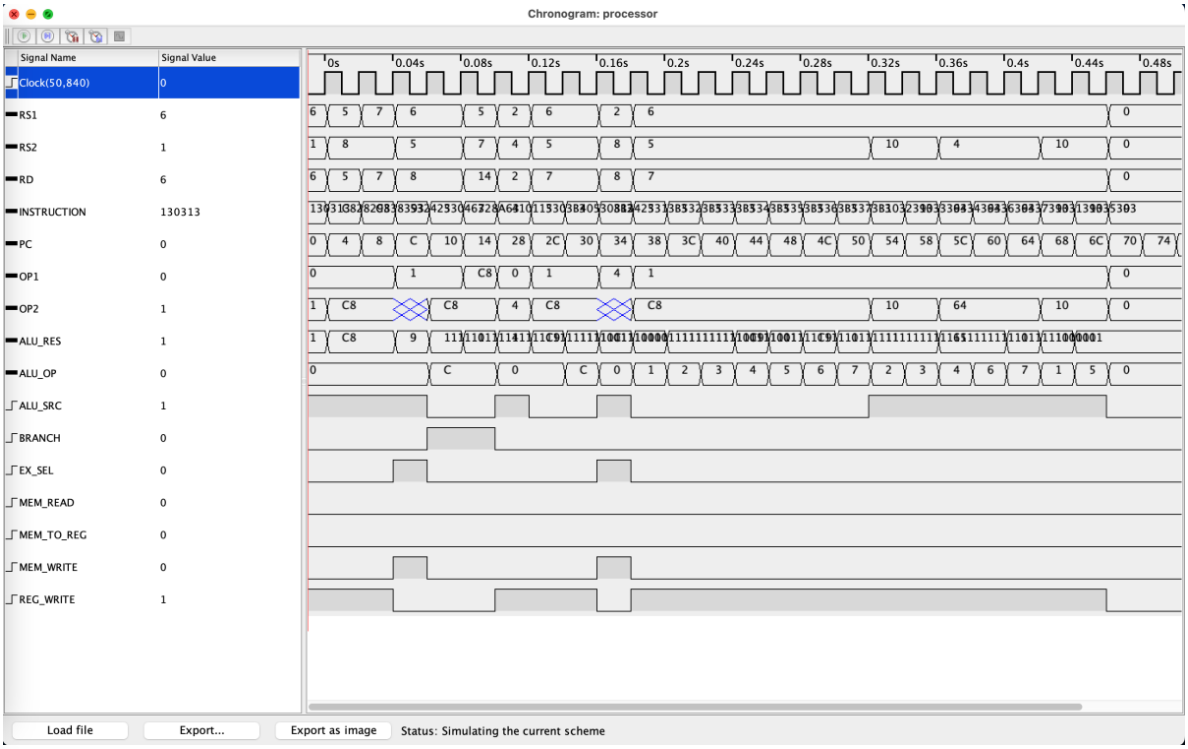
PROCSESSOR

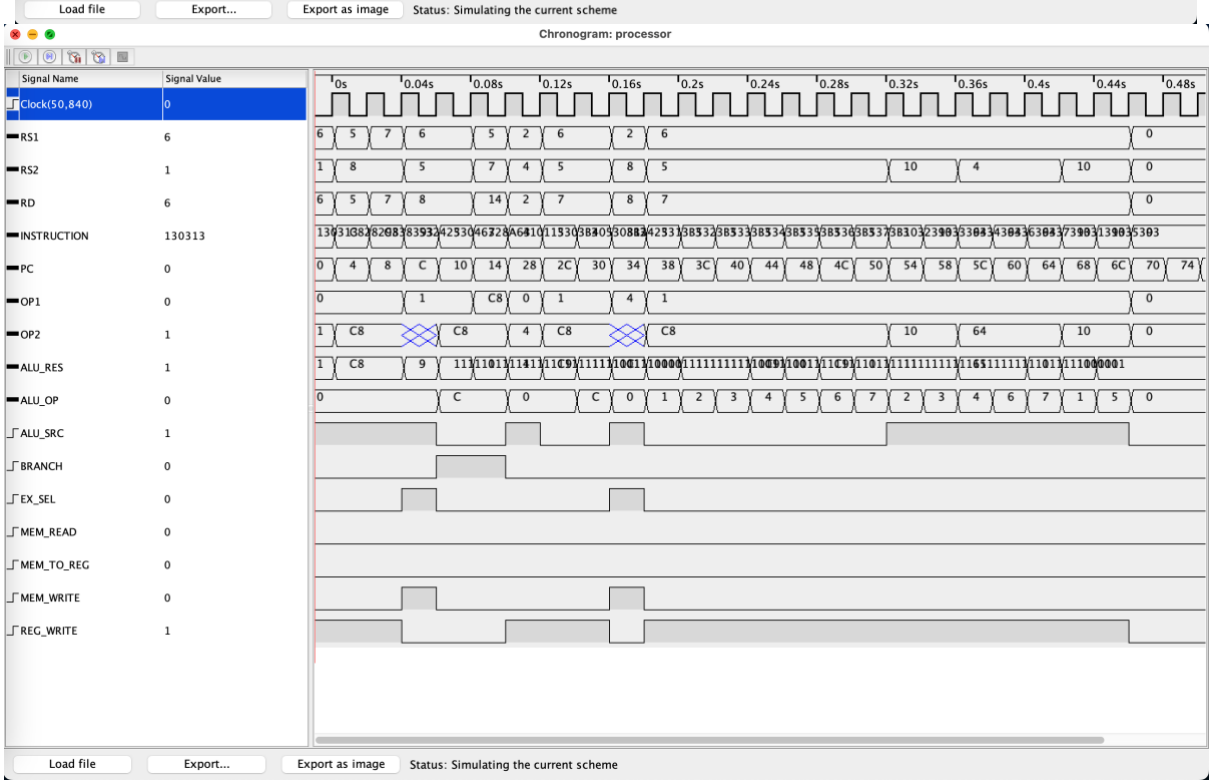


INSTRUCTION CODE

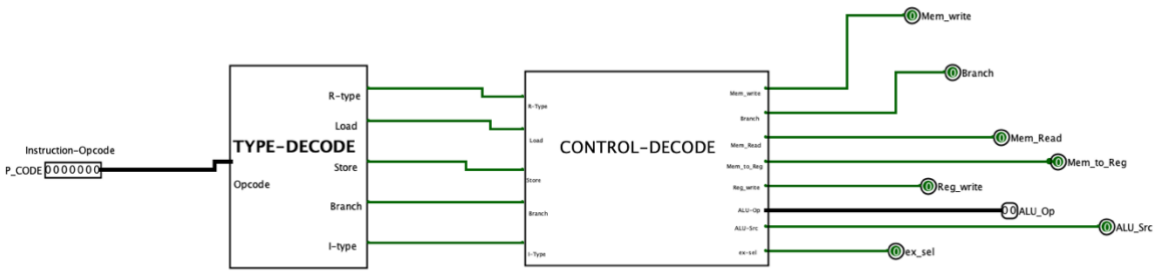
Logisim-evolution: Hex Editor

```
000000 00130313 0c828293 0c838393 00532423 00530463 00728a63 01432383 06440413 06448493 00a50513 00410113 005303b3 405303b3 00812423 005313b3 005323b3
000010 005333b3 005343b3 005353b3 005363b3 005373b3 01032393 01033393 06434393 06436393 06437393 01031393 01035393 00000000 00000000 00000000 00000000
000020 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000030 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000040 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000050 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000060 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000070 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000080 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000090 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000a0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000b0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000c0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000d0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000e0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
0000f0 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000100 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000110 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000120 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000130 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000140 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000150 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000160 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
000170 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
```


Chronogram: processor
Signal Name
Signal Value
Clock(50,840)
RS1
RS2
RD
INSTRUCTION
PC
OP1
OP2
ALU_RES
ALU_OP
ALU_SRC
BRANCH
EX_SEL
MEM_READ
MEM_TO_REG
MEM_WRITE
REG_WRITE
Load file
Export...
Export as image
Status: Simulating the current scheme


Chronogram: processor
Signal Name
Signal Value
Clock(50,840)
RS1
RS2
RD
INSTRUCTION
PC
OP1
OP2
ALU_RES
ALU_OP
ALU_SRC
BRANCH
EX_SEL
MEM_READ
MEM_TO_REG
MEM_WRITE
REG_WRITE
Load file
Export...
Export as image
Status: Simulating the current scheme

CONTROL

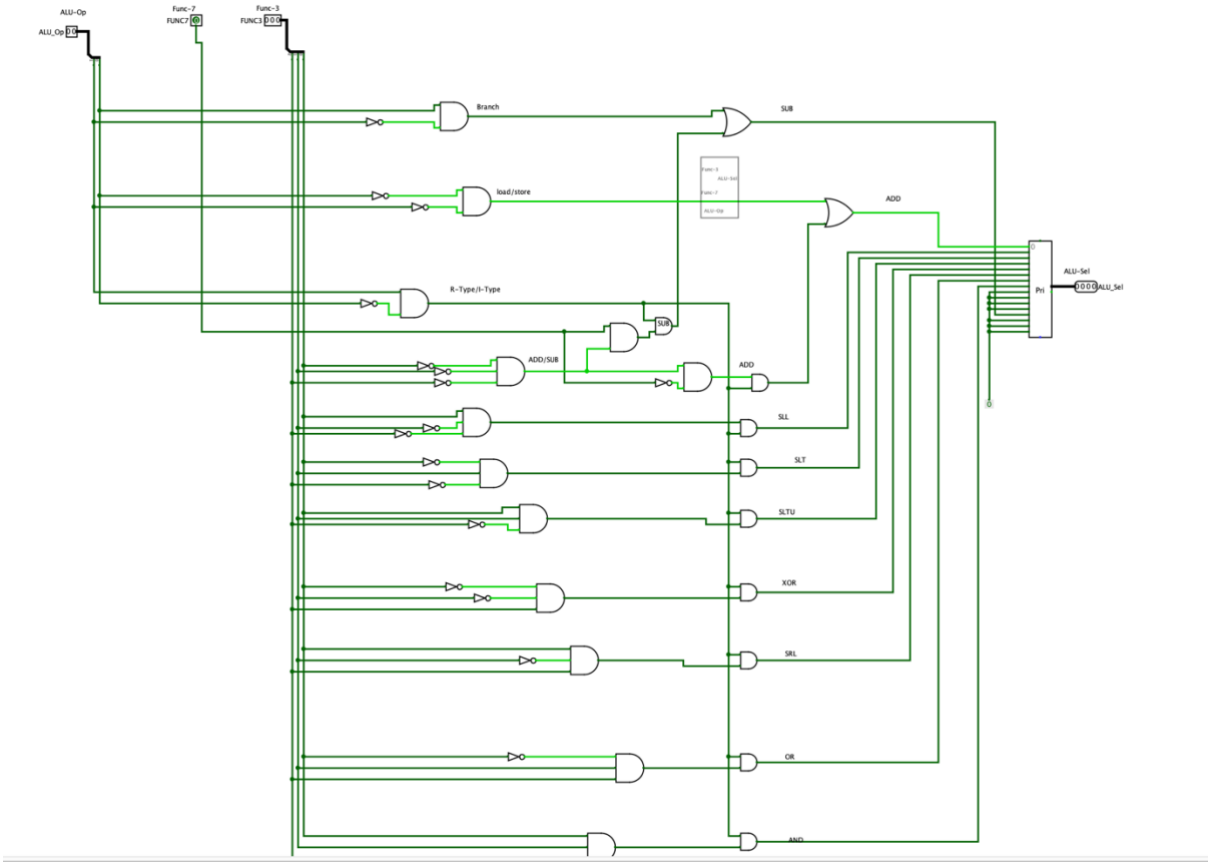


TESTING IMAGE

Passed: 5 Failed: 0

status	OP_CODE	Mem_write	Branch	Mem_Read	Mem_to_Reg	Reg_write	ALU_Op	ALU_Src	ex_sel
pass	011 0011	0	0	0	0	1	10	0	0
pass	000 0011	0	0	1	1	1	00	1	0
pass	010 0011	1	0	0	0	0	00	1	1
pass	110 0011	0	1	0	0	0	01	0	0
pass	001 0011	0	0	0	0	1	10	1	0

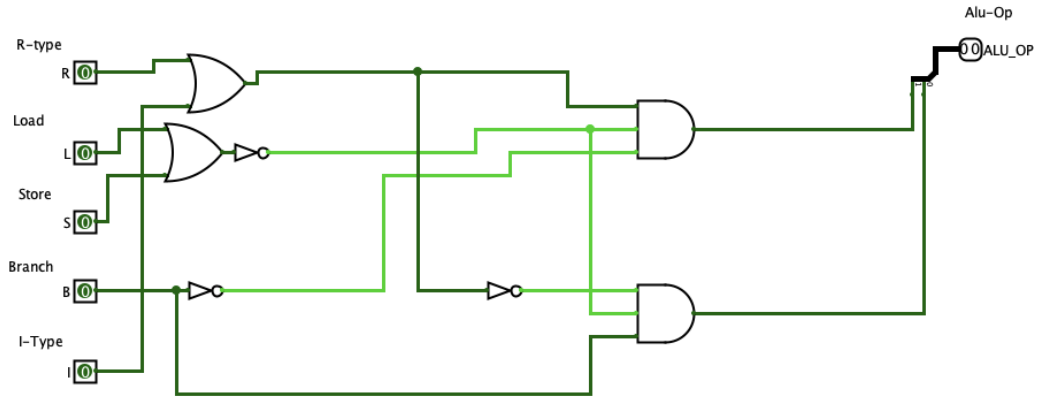
ALU CONTROL



Passed: 31 Failed: 0

status	ALU_Op	FUNC7	FUNC3	ALU_Sel
pass	10	0	000	0000
pass	10	1	000	1100
pass	10	0	001	0001
pass	10	0	010	0010
pass	10	0	011	0011
pass	10	0	100	0100
pass	10	0	101	0101
pass	10	0	110	0110
pass	10	0	111	0111
pass	10	0	000	0000
pass	10	1	000	1100
pass	10	0	010	0010
pass	10	1	010	0010
pass	10	1	011	0011
pass	10	0	011	0011
pass	10	1	100	0100
pass	10	0	100	0100
pass	10	1	110	0110
pass	10	0	110	0110
pass	10	1	111	0111
pass	10	0	111	0111
pass	10	1	001	0001
pass	10	0	001	0001
pass	10	1	101	0101
pass	10	0	101	0101
pass	10	1	010	0010
pass	10	0	010	0010
pass	00	1	010	0000
pass	00	0	010	0000
pass	01	1	000	1100
pass	01	0	000	1100

ALU_OP

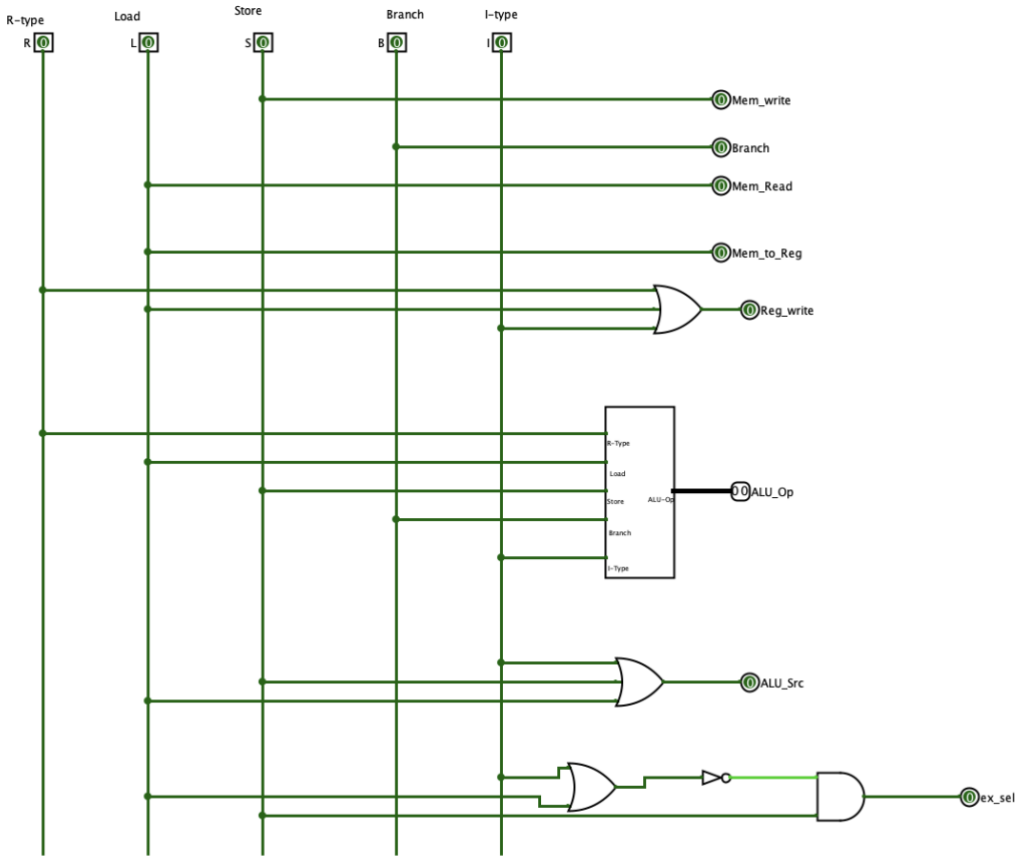


TESTING IMAGE

Passed: 6 Failed: 0

status	R	L	S	B	I	ALU_OP
pass	0	0	0	0	0	00
pass	1	0	0	0	0	10
pass	0	1	0	0	0	00
pass	0	0	1	0	0	00
pass	0	0	0	1	0	01
pass	0	0	0	0	1	10

CONTROL DECODE



TESTING IMAGE

Passed: 5 Failed: 0

status	R	L	S	B	I	Mem_write	Branch	Mem_Read	Mem_to_Reg	Reg_write	ALU_Op	ALU_Src	ex_sel
pass	1	0	0	0	0	0	0	0	0	1	10	0	0
pass	0	1	0	0	0	0	0	1	1	1	00	1	0
pass	0	0	1	0	0	1	0	0	0	0	00	1	1
pass	0	0	0	1	0	0	1	0	0	0	01	0	0
pass	0	0	0	0	1	0	0	0	0	1	10	1	0