A Lab Report on Implementation of 4x1 multiplexer and 1x4 demultiplexer using logic gates

Digital Electronics Lab EC 212

Gauray Saha

Scholar ID: 1914092

4th Semester, Bachelor of Technology Electronics and Communication Engineering National Institute of Technology, Silchar Aim of the Experiment: To analyse the truth table and working of 1×4 de-multiplexer and 4×1 multiplexer by using 3-input NAND, and 1-input NOT logic gates ICs, and using 3-input NAND, 3-input OR, and 1-input NOT logic gates ICs.

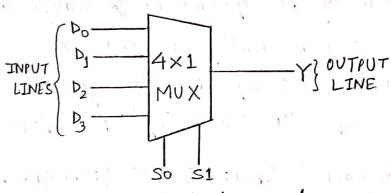
Components Used: IC 7404 [NOT Gate], IC 7411[NAND Gate],

IC 4072B [OR Gate], Oligital Lab Freiner Kit

— in VLabs software

Bruef Theory: of multiplexer is a digital criaid which has n input lines and one output line, along with select lines. The select lines determine the input line that is connected to the output line. For any particular combination of the select lines, a particular input line gets connected to the output line. It decides the data that is being transmitted incoming from the input lines. It has its application in time division multiplexing where the select lines keep on changing their combinations, so that data coming from multiple lines of input are transmitted through the same output line within a given time freid. It is also known. as a data selector. A multiplexer with n input lines is shown as nx1 multiplier. Mainly, it is classified into four types: 2×1 multiplexer (1 select line) 4x1 multiplexer (2 select line) 8x 1 multiplexer (3 select line) 16 x 1 mulliplemen (4 select line)

The 4x1 MUX wicuit has 4 input lines Do, D1, D2, and B, and one output line Y with two select lines So and S1. Based on the different combinations of So, S1, different input lines are



▲ Fig 6.1 Block diagram of 4x1 multiplener

connected to Y and the corresponding data is transmitted. Its truth table is shown as follows:

So	S ₁	Y
0	0	D _o
0	1	D_1
1	. 0	D ₂
1	1	D ₃

▲ Sable 6.1 South table of 4×1 MUX

A demultiplencer on the other hand has one input line and 'm' output lines, along with select lines. For any given combination of select lines, the input line is connected to the corresponding outfut line and the incoming data gets bransmitted along with it. In a multiplexed input, where the incoming data actually consists of multiple messages, the combinations of the select wires keep on changing continuously and the required data is transmitted along the couresponding output line. This demultiplener is

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represented in the form 1 x m be classified into four types: de-multiplexer-It can also 1×2 demultiplexer (1 select line) 1×4 demultiplener (2 select lines)

1 × 8 demultiplexer (3 select line)

1×16 demultiplexer (4 select lines)

In the 1×4 DEMUX rincuit, There is input D, and output lines Yo, Y1, Y2, and Y3, which also has two select lines So and S1. Based on the different combinations of So, S1; the input line gets transmitted to a particular output.

		Y
(A) ATAD	1×4	
, \	DEMUX	Y
INPUT		12 V2
,		13
\leq	50 51	in the
	1 3 4 1 1 5 1 1 T	

So	Sı	Yo	41	Y2	Y3	1
0	100	P	0	0	0	
0	1	0	MAD	10	001	
1	10 01	0	1,00	, D	0.	
1	1	0	O S	0	4	

▲ Fig. 6.2 Block diagram

Fig. 6.2 Block diagram

of 1×4 demultiplexer

Procedure: Multiplexer: 1) +5V supply is connected the region

- 2) 'ADD' button is frist faced pressed to add basic state of output in the given lable.
- 3) 'So' and 'Ss' are present to select the desired input line.
- 4) Any one button of Do/D1/D2 and D3 foressed to add inputs.
- 5) 'ADD' button is used to add the inputs and author outputs in the given table.
- 6) Steps 3, 4 and 5 are repeated for next state of influts and

their corresponding outputs.

- 7) 'PRINT' button is pressed after completion of semulation to get the results.
- De-Muttiplexer: 1)+5V supply is connected to the circuit: 2) 'ADD' button is first placessed to add basic state of
 - output in the given table.
 - 3) DATA (D) button is pressed for input.
 - 4) 'So' and 'S1' are pressed to select the desired output line.
 - 5) 'ADD' button is used to add the inputs and outputs in the gaven lable.
 - 6) Steps 4 and 5 are repeated for next state of inputs and their corresponding outputs.
- 7) 'PRINT' button is pressed after completion of simulation to get the results.

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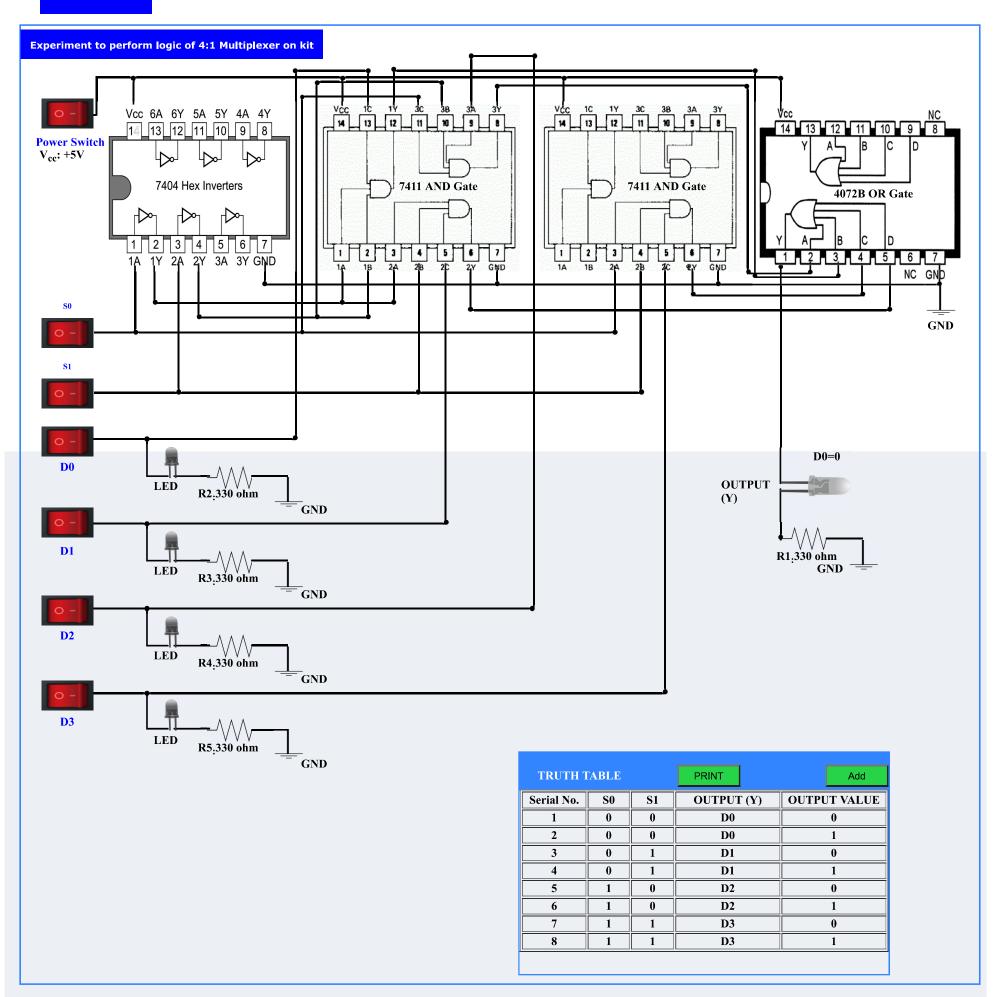
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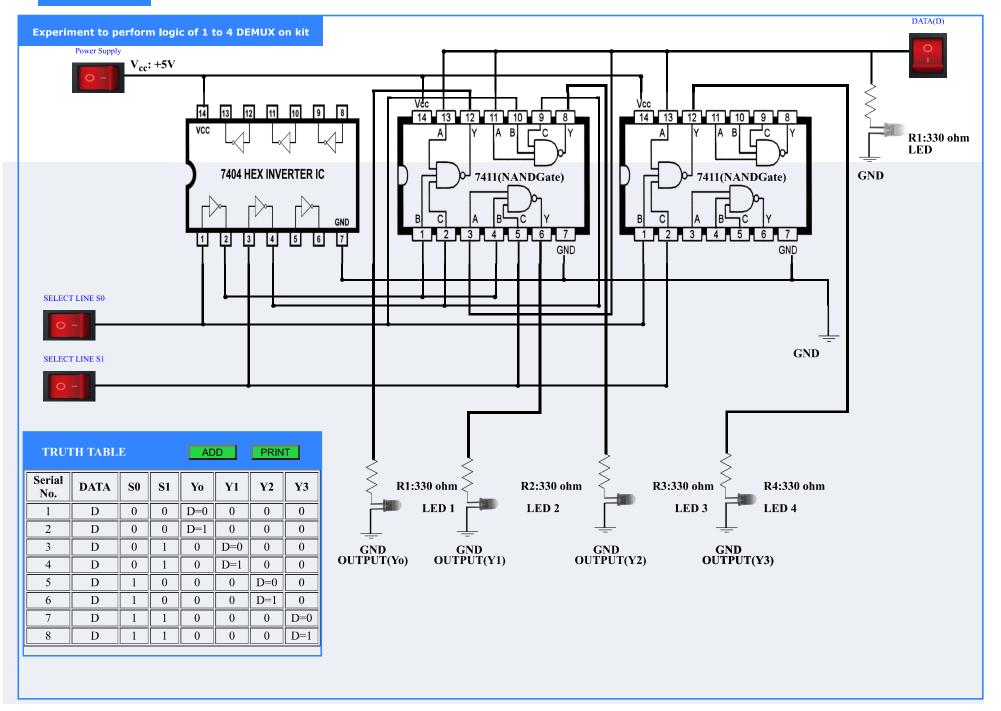
3/24/2021 4:1 Multiplexer

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Conclusion: Both the digital coicuits of multipleners and demultipleners, their mode of working, and their applications have been studied. The working has been discussed in details using the 4×1 multiplener and 1×4 de-multiplener along with their touth tables for different combinations of select lines. In the simulators, both the cricuits have been realised using logic gates, and these cricuits have been run and verified.

Thus, the implementation and analysis of multiplexers and de-multiplexers has been carried out successfully.