

COMPAL CONFIDENTIAL


MODEL NAME : Goliad MLK 12 UMA  
PCB NO : LA-A971P  
BOM P/N : 4319RJ31LXX  
GPIO MAP: 3.3b

Goliad MLK 12" UMA  
Broadwell U Processor

2013-12-23  
REV : 0.3 (X01)

- @ : Nopop Component
- EMC@ : EMI, ESD and RF Component
- @EMC@ : EMI, ESD and RF Nopop Component
- CXDP@ : XDP Component
- CONN@ : Connector Component
- VPRO@ : Vpro Component
- NVPRO@ : Non-Vpro Component

Layout Dell logo




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REV: X01  
PWB: 89XM3  
DATE: 1351-05

MB PCB	
Part Number	Description
DAA00083000	PCB 14A LA-A971P REV0 MB WITH DOCKING 2

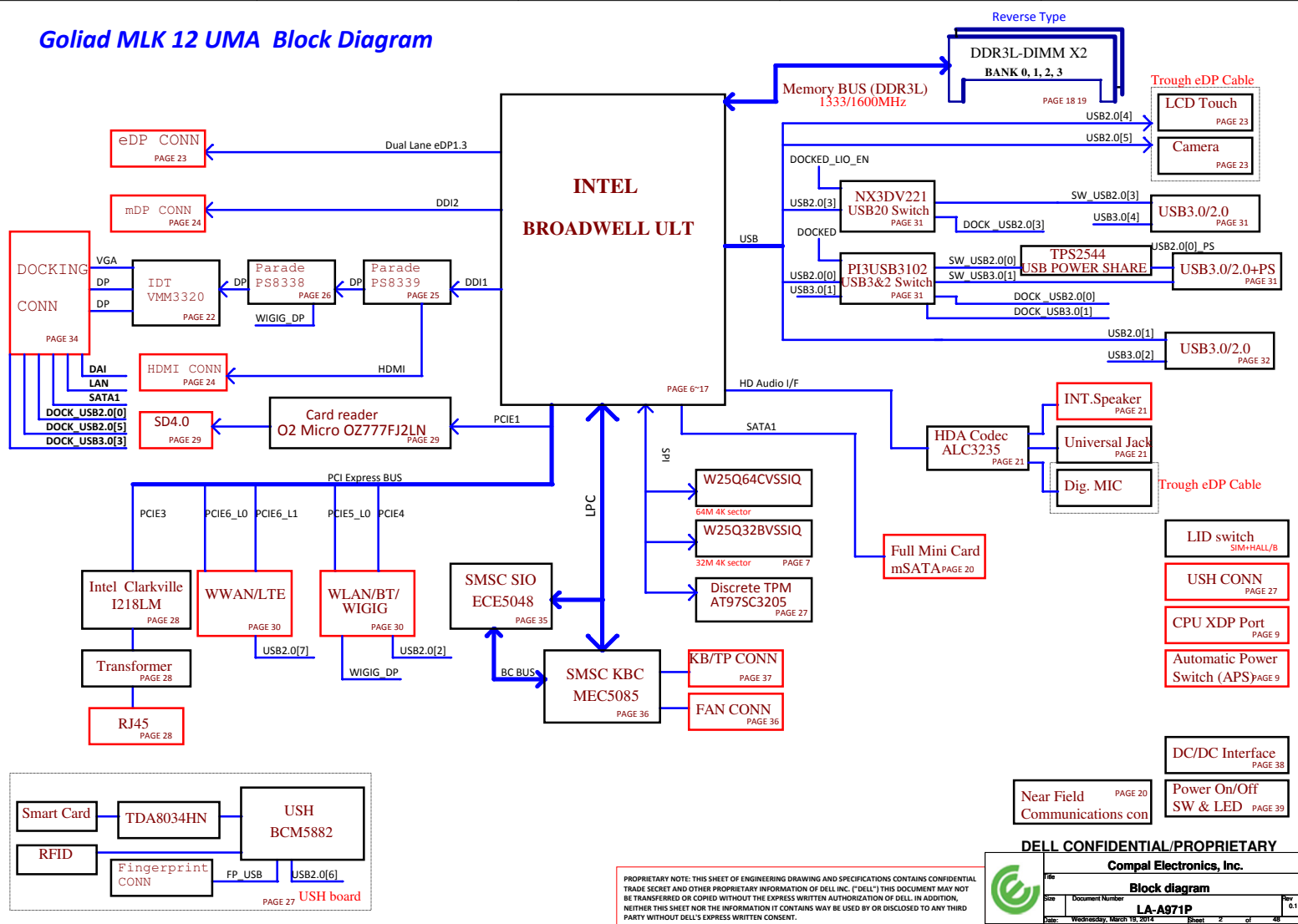
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Cover Sheet		
Size	Document Number	Rev
	LA-A971P	0.1
Date	Wednesday, March 19, 2014	Sheet 1 of 45

### ***Goliad MLK 12 UMA Block Diagram***



## POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6		SATA 3	HCA & SATA Cache - JNGFF2
		SATA 2	SATA Cache - JNGFF2
		SATA 1	JMINI3
		SATA 0	JDOCK1

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1 or DOCK1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2 or DOCK2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

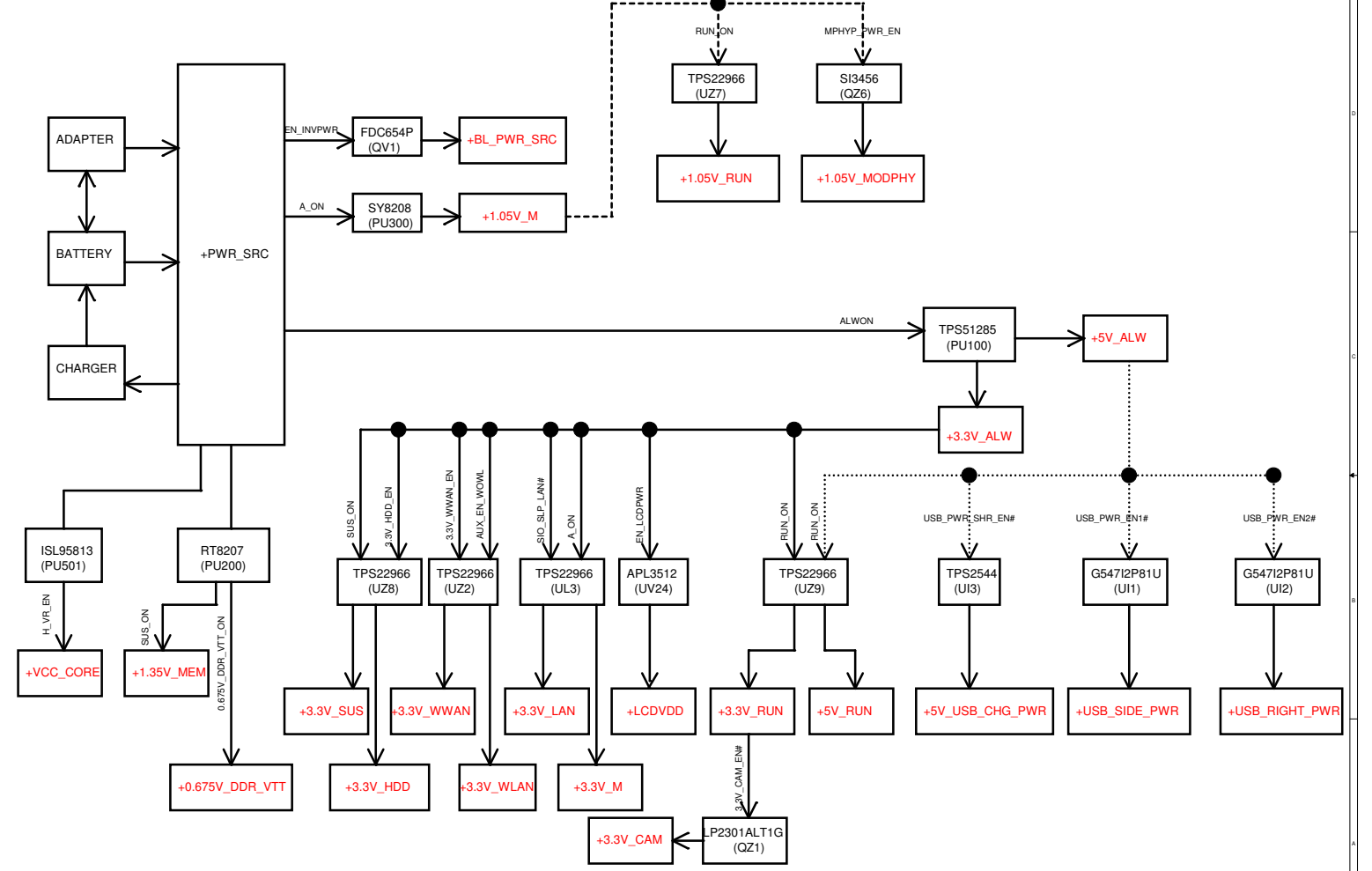
USH	0	BIO
	1	NA

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File	Port assignment
Size	Document Number
	LA-A971P
Date	Wednesday, March 19, 2014
Sheet	3 of 40

Rev 0.1

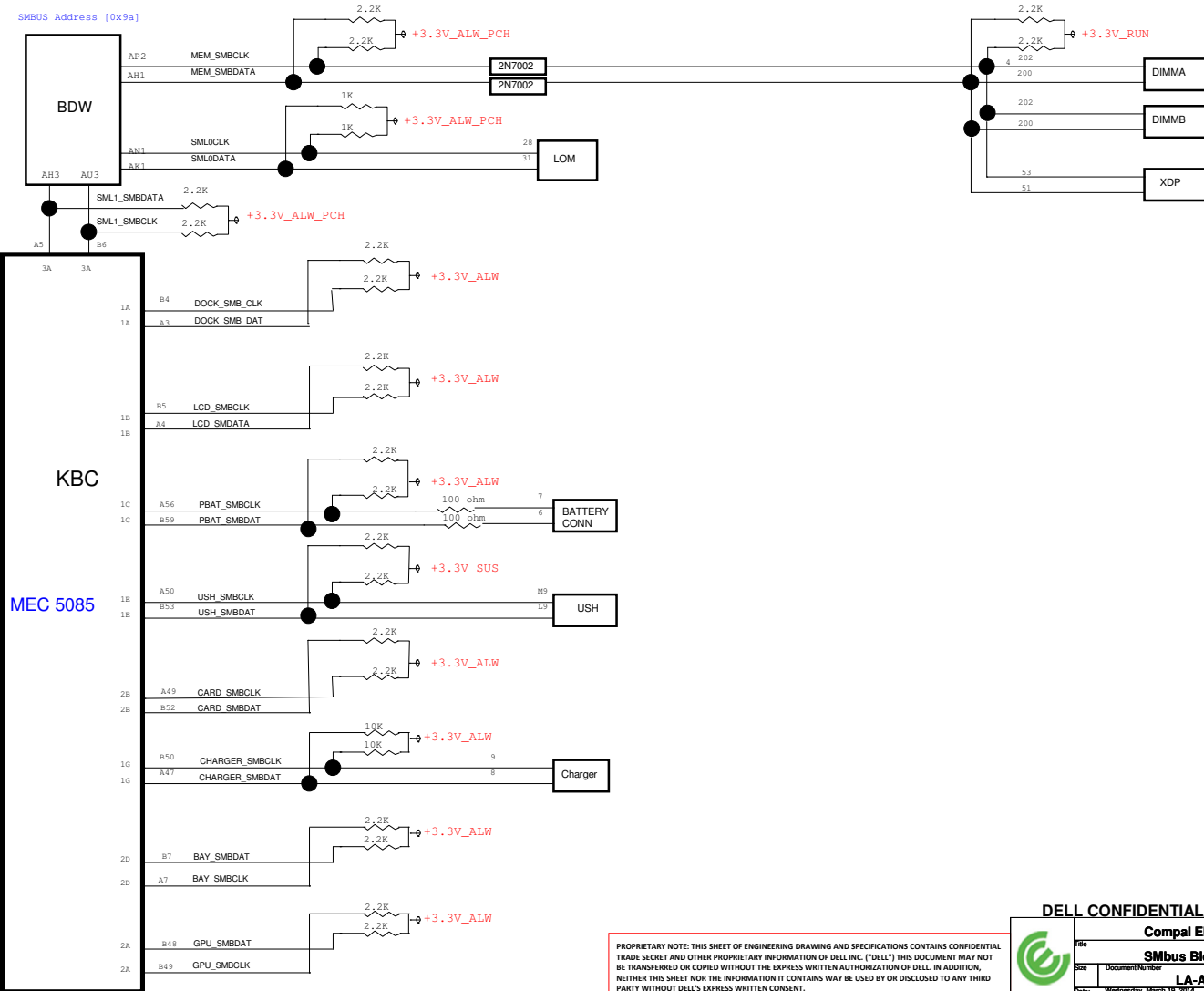


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File		Power rails	
Size	Document Number	Rev	
	LA-A971P	6.1	
Date	Wednesday, March 19, 2014	Sheet	4 of 40



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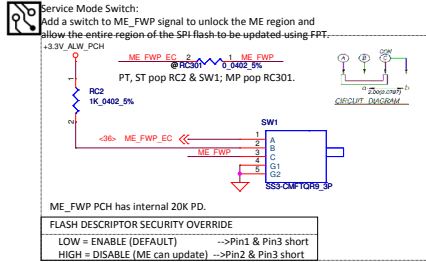
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### SMbus Block diagram

LA-A971P

Date: Wednesday, March 19, 2014 Sheet 5 of 40

# UMA SATA port



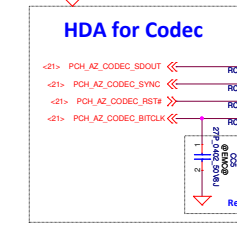
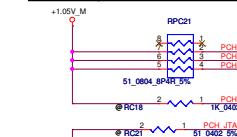
INTVRMEN - INTEGRATED SUS 1.05V VRM  
ENABLE  
High - Enable Internal VRs  
Low - Enable External VRs

ME\_CLR1  
Shunt  
Open  
Keep ME RTC Registers

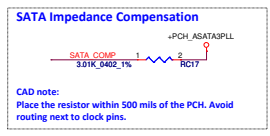
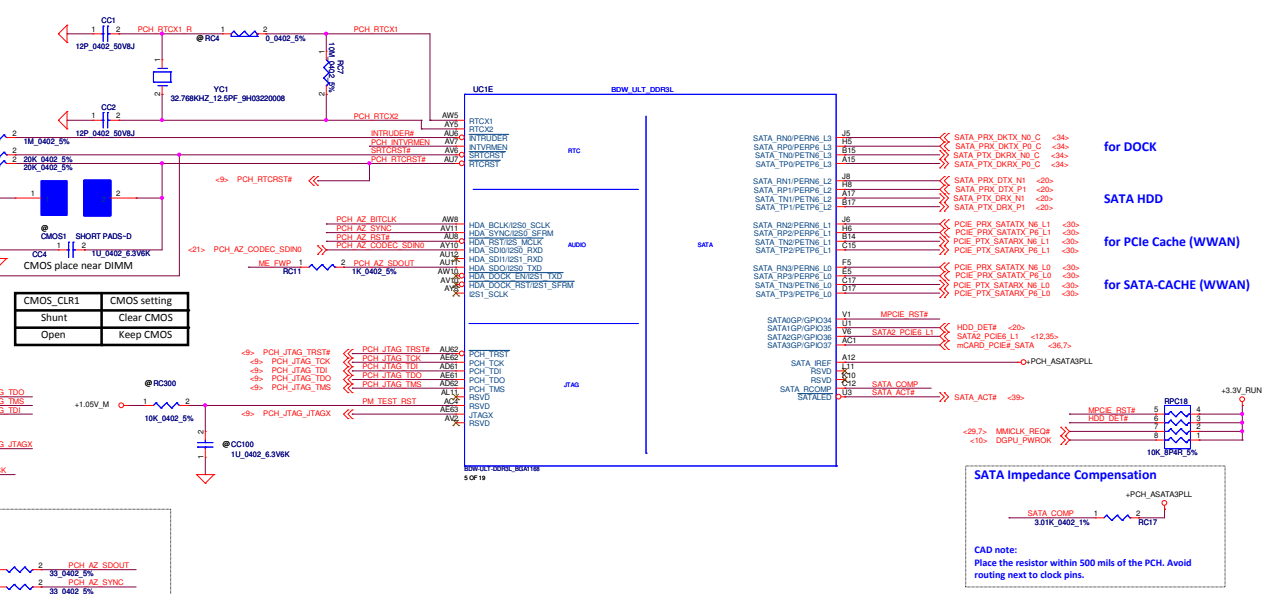
TPM setting  
Clear ME RTC Registers  
Keep ME RTC Registers

CMOS\_CLR1  
Shunt  
Open  
Clear CMOS

CMOS setting  
Clear CMOS  
Keep CMOS



SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0	
E-Dock	mSATA	G12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G12 Entry	NA	NA	
E-Dock	mSATA	G14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	G14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	G14U_En	NA	NA	



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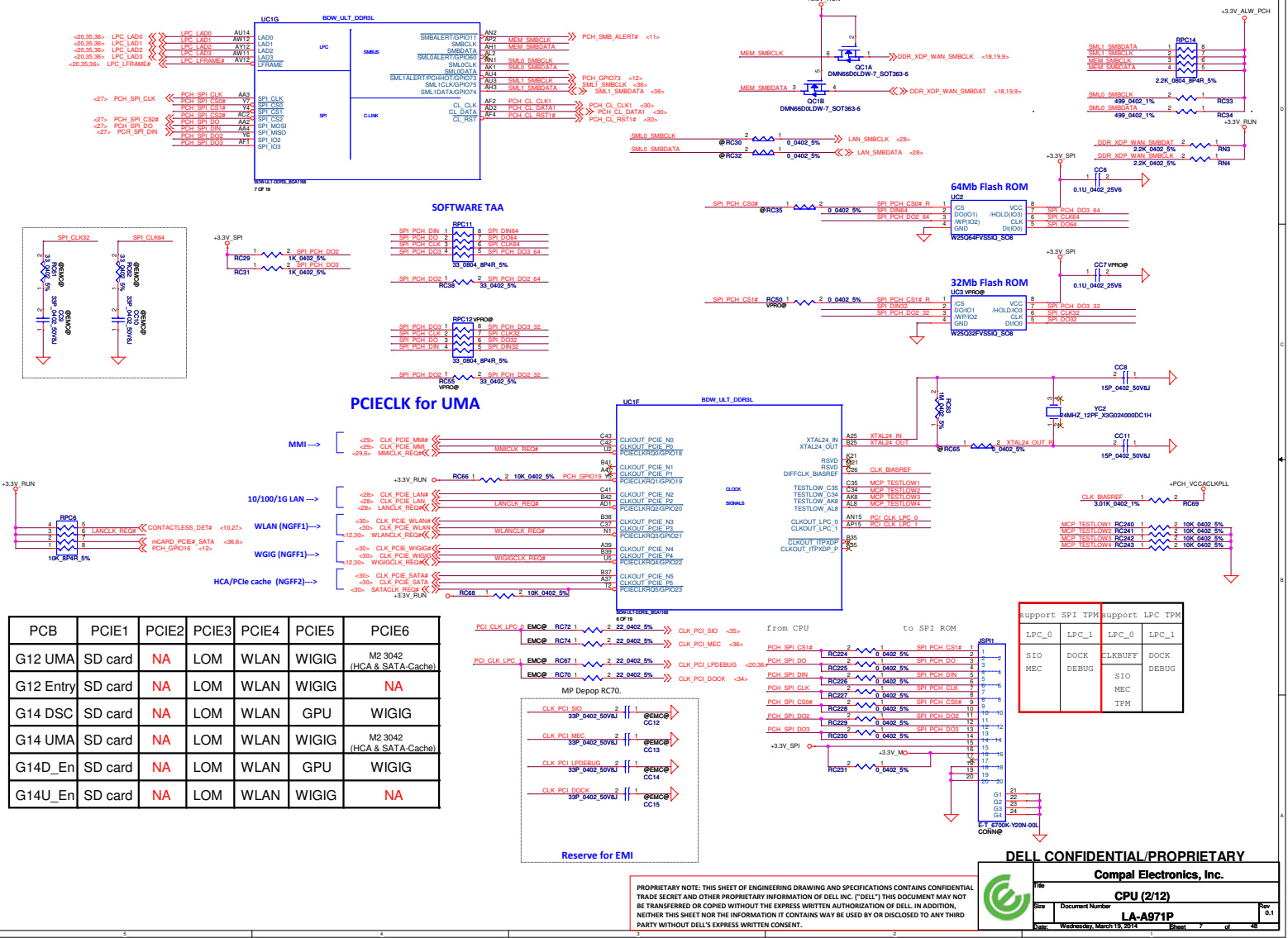
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CPU (1/12)

LA-A971P

Wednesday, March 19, 2014

Sheet 5 of 45



PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA

support SPI TPM		support LPC TPM	
LPC_0	LPC_1	LPC_0	LPC_1
SIO	DOCK	CLKBUFF	DOCK
MEC	DEBUG		DEBUG
		SIO	
		MEC	
		TPM	

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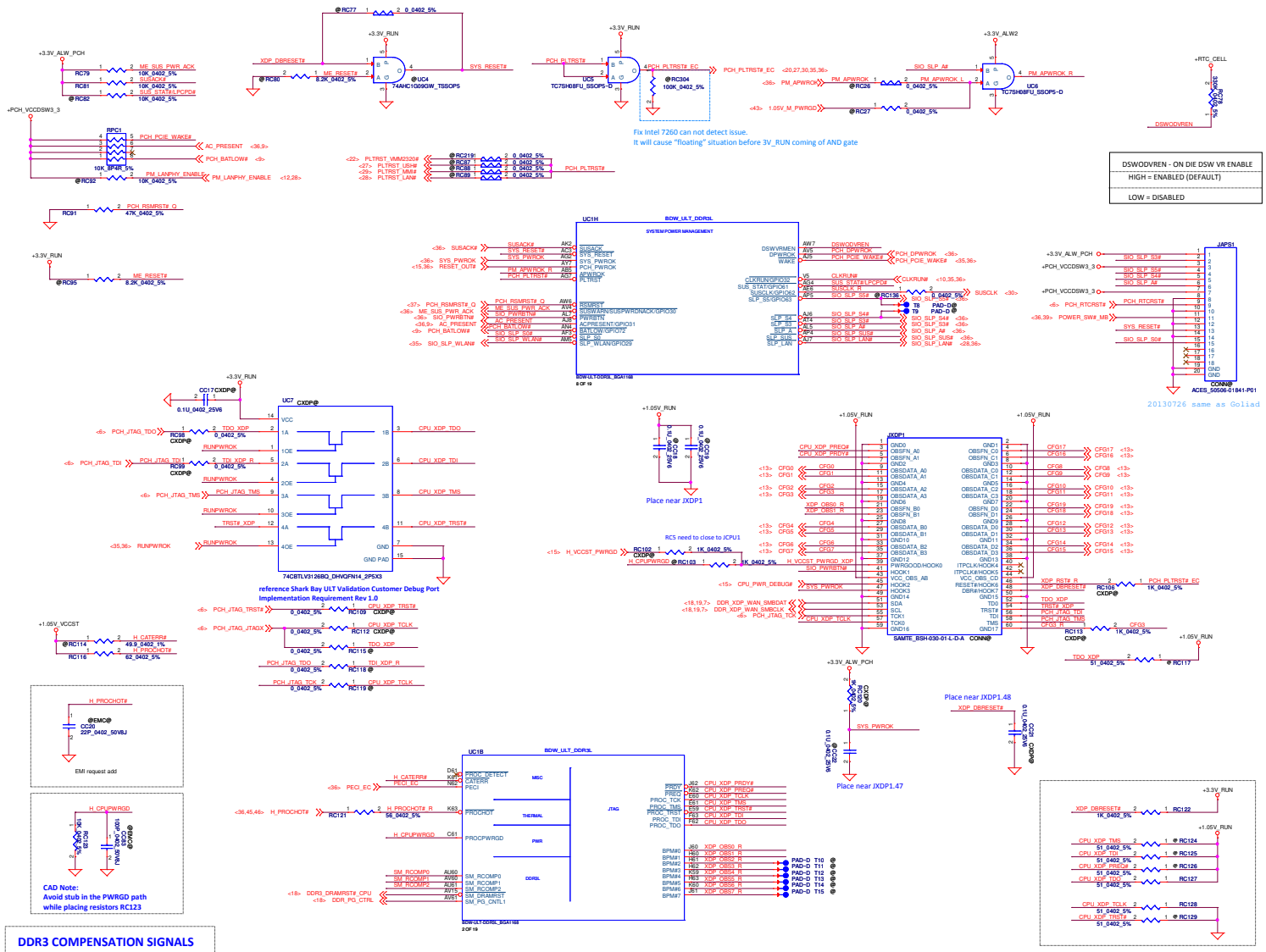
File: **CPU (2/12)**

Doc: **LA-A971P**

Date: Wednesday, March 15, 2014 Sheet: 7 of 48







DSW00VREN - ON the DSW VR ENABLE  
HIGH = ENABLED (DEFAULT)  
LOW = DISABLED

Pin 7260 can not detect issue.  
It will cause "floating" situation before 3V\_RUN coming of AND gate

20130726 same as Goldil

**DDR3 COMPENSATION SIGNALS**

25M 0.402 1% 2 1 RC138 SM RC00M3  
125M 0.402 1% 2 1 RC139 SM RC00M3  
125M 0.402 1% 2 1 RC138 SM RC00M3

CAD Note:  
Trace width=12-15 mil, Spacing=20 mils  
Max trace length= 500 mil

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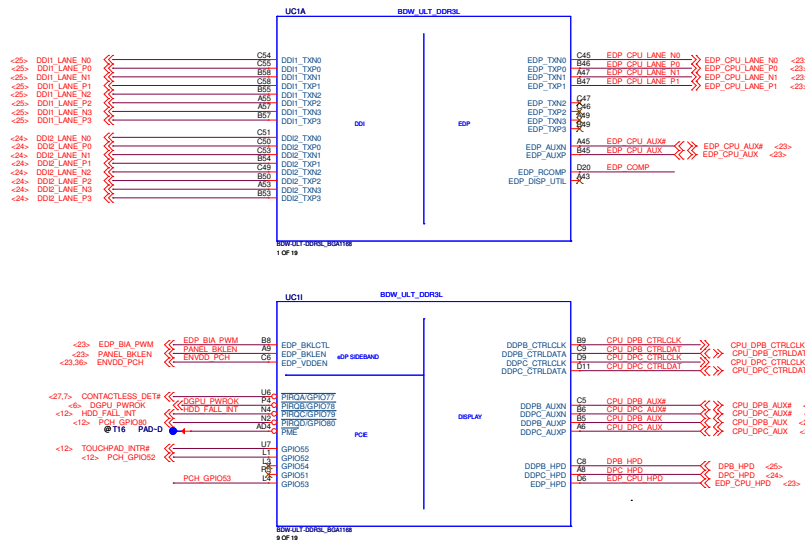
**CPU (4/12)**

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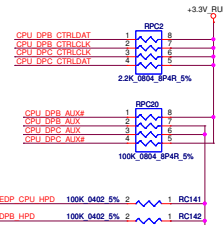
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Sheet: 9 of 40



**COMPENSATION PU FOR eDP**

CAD Note: Trace width=20 mils, Spacing=25mil, Max length=100 mils.

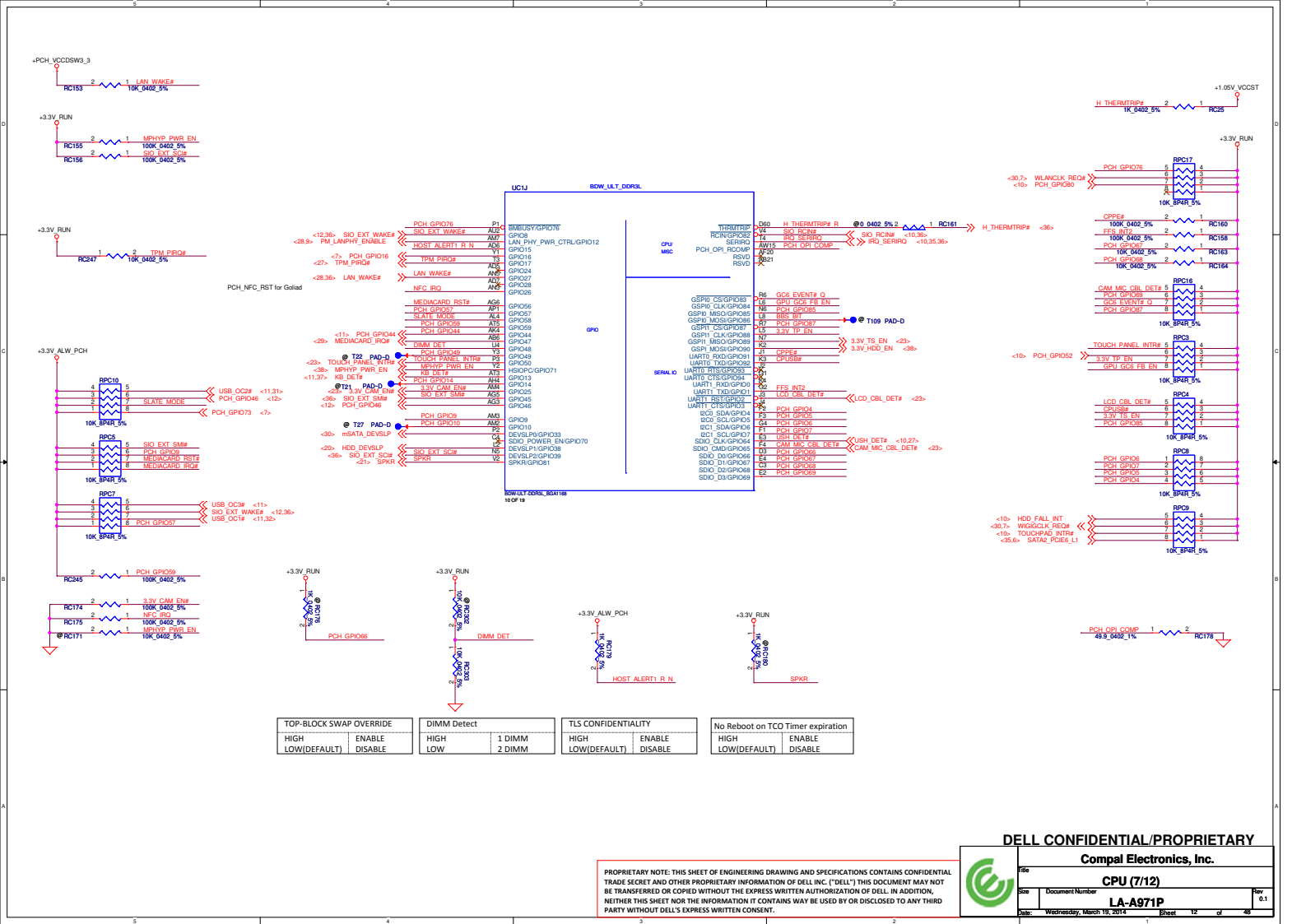


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CPU (5/12)	
LA-A971P	Rev 6.1
Date: Wednesday, March 19, 2014	Sheet 10 of 45





TOP-BLOCK SWAP OVERRIDE		DIMM Detect		TLS CONFIDENTIALITY		No Reboot on TCO Timer expiration	
HIGH	ENABLE	HIGH	1 DIMM	HIGH	ENABLE	HIGH	ENABLE
LOW(DEFAULT)	DISABLE	LOW	2 DIMM	LOW(DEFAULT)	DISABLE	LOW(DEFAULT)	DISABLE

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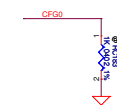
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CPU (7/12)

LA-A971P

Wednesday, March 19, 2014

Sheet 12 of 48



	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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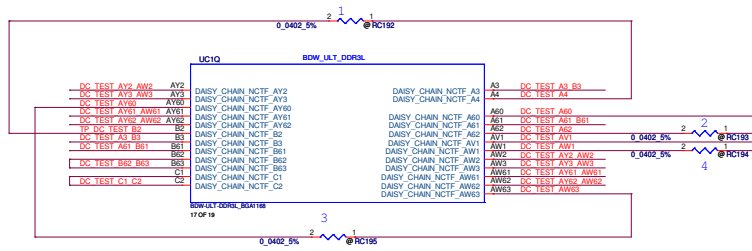
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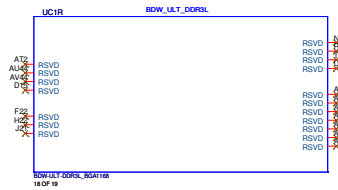
**CPU (8/12)**

LA-A971P

Date: Wednesday, March 19, 2014 Sheet 13 of 48



- Package Daisy Chain:
- 1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
  - 2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
  - 3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
  - 4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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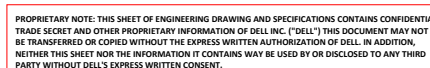
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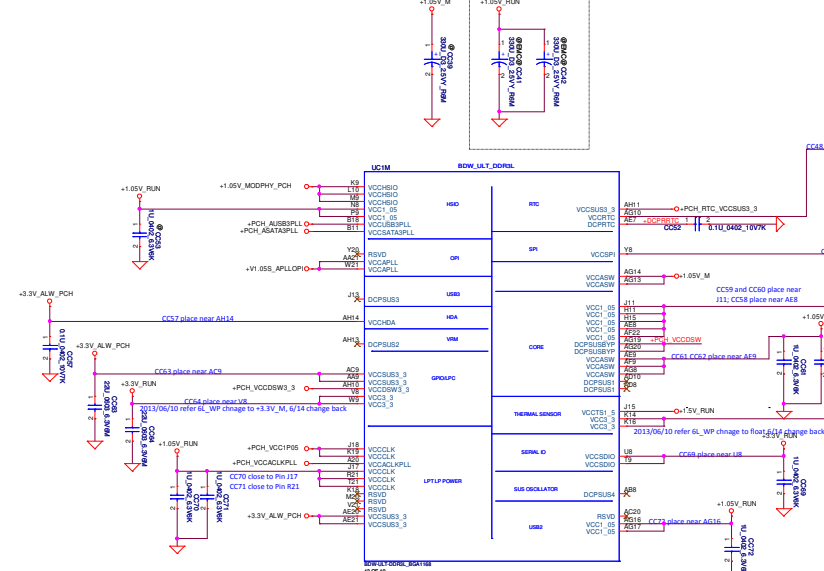
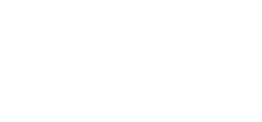
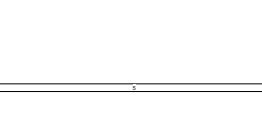
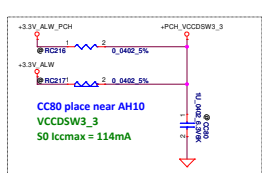
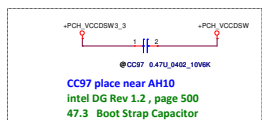
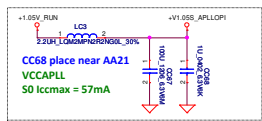
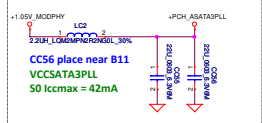
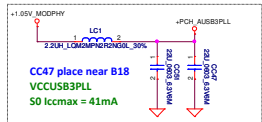
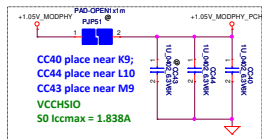
CPU (9/12)

LA-A971P

Date: Wednesday, March 19, 2014 Sheet 14 of 45

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Voltage Rail	Voltage (V)	S0 Iccmax Current (A) <sup>1</sup>	Sx Iccmax Current (A) <sup>2</sup>	Deep Sx Iccmax (A) <sup>3</sup>	G3
VCC1_05 (Internal Suspend VR mode using HTRVMM)	1.05	1.741	0	0	0
VCC1_05 (Internal Suspend VR mode using HTRVMM)	1.05	1.632	0	0	0
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCC1_15	1.5	0.003	0	0	0
VCC1_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSP1	3.3	0.018	0	0	0
VCC1_05	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using HTRVMM)	3.3	0.063	0.024	0	0
VCCSUS3_3 (Internal Suspend VR mode using HTRVMM)	3.3	0.062	0.005	0	0
DpSux1 <sup>4</sup>	1.05	0.109	0.014	0	0
DpSux2 <sup>4</sup>	1.05	0.025	0.001	0	0
DpSux3 <sup>4</sup>	1.05	0.010	0.001	0	0
DpSux4 <sup>4</sup>	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	See notes 1, 2



Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

#### Power Rail Isolation

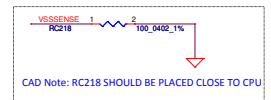
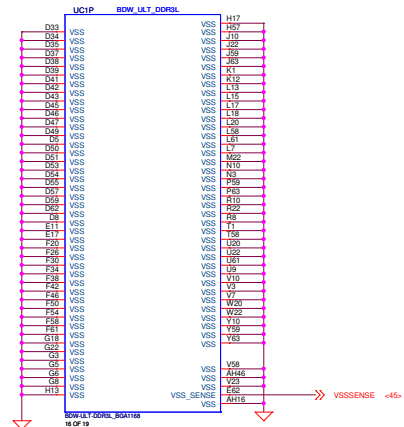
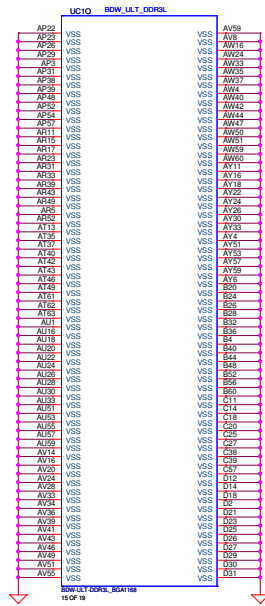
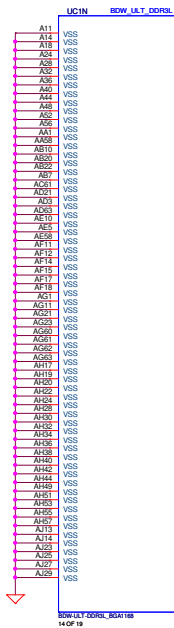
Voltage Supply	Interface (power rail isolation required)	PCB Pin sharing power rail
V1.05s	Core DPE HSD0 USB2 CLKAPLL CLK(A) CLK(B) CLK(C)	J11, H11, H15, A8B, AF22 HAC1, H21 K9, L10, NL, P9, B18, B11, M9 AG16, AG17 A20 J21, J21 J28, K19 J17
V3.3s	LPD0 RTC HDA	AC5, A8B, AE20, AE21 AH11
V3.3s	LPD0 RTC HDA	V8, W9 UL, T9 K14, K15

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CPU (11/12)			
File	Document Number	LA-A971P	
Date	Wednesday, March 19, 2014	Sheet	16 of 48

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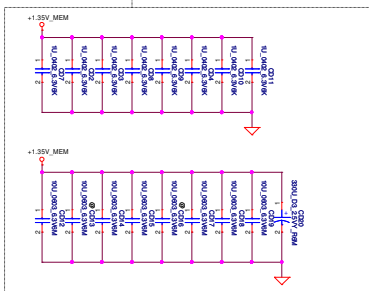


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Date		Wednesday, March 19, 2014
Sheet		17 of 48

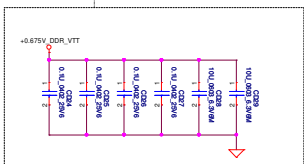
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<-> DDR\_A\_DQS[0..7] <->  
 <-> DDR\_A\_DQ[0..63] <->  
 <-> DDR\_A\_DQS[0..7] <->  
 <-> DDR\_A\_M[0..15] <->

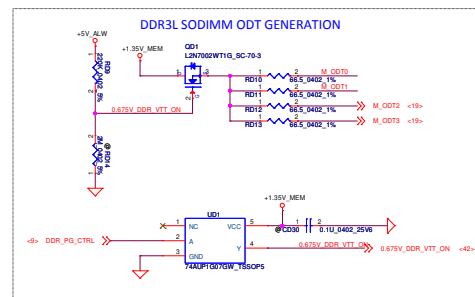
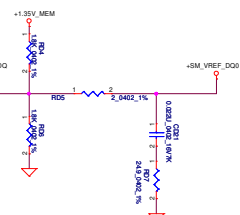
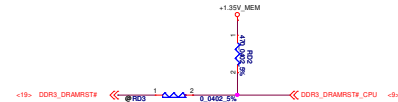
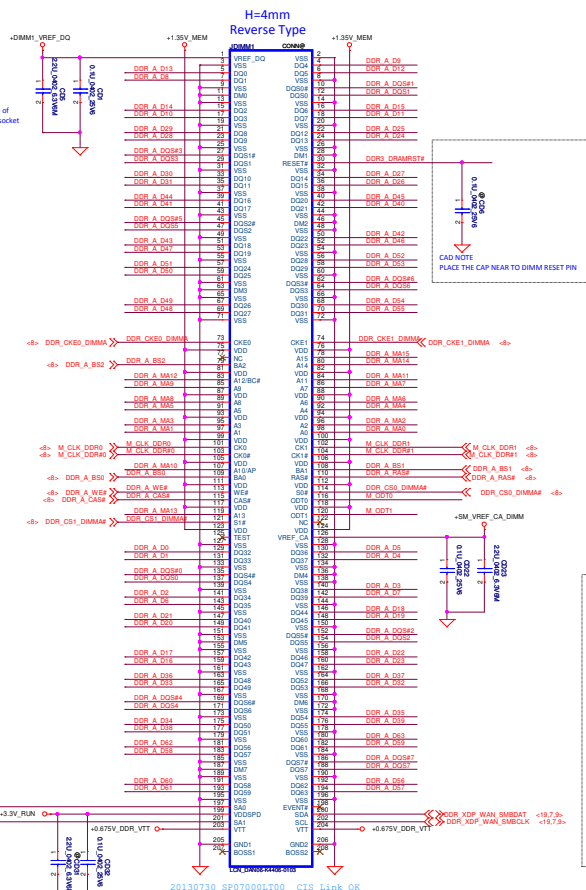
Layout Note:  
Place near JDIMM1



Layout Note:  
Place near JDIMM1.203,204



Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



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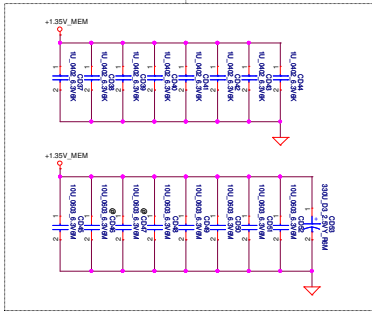
Part Number: LA-A971P  
 Date: Wednesday, March 19, 2014  
 Sheet: 18 of 48

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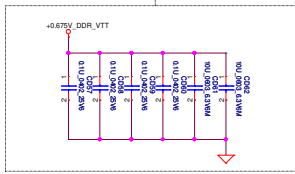
# H=4mm Reverse Type

DDR\_B\_D0[4:7] <<>  
DDR\_B\_D0[4:7] <<>  
DDR\_B\_D0[4:7] <<>  
DDR\_B\_Map[1:1] <<>

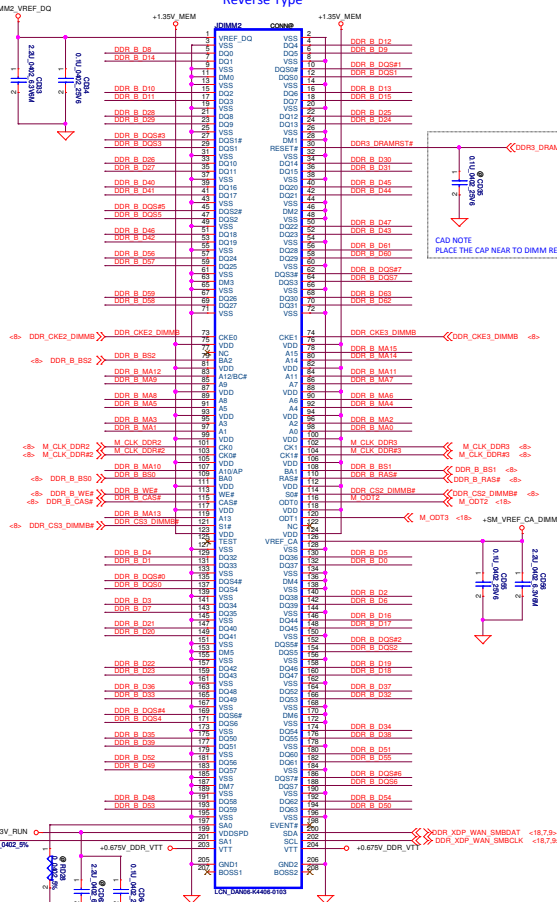
Layout Note:  
Place near JDIMM2



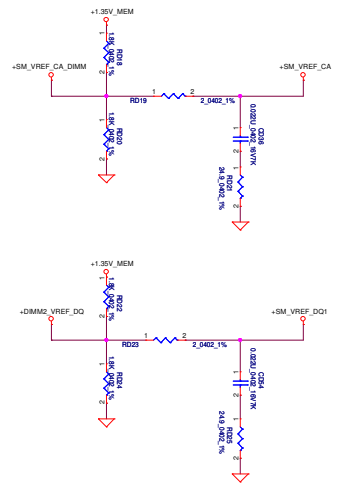
Layout Note:  
Place near JDIMM2.203,204



Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket



20130730 SP07000L700 CIS Link OK

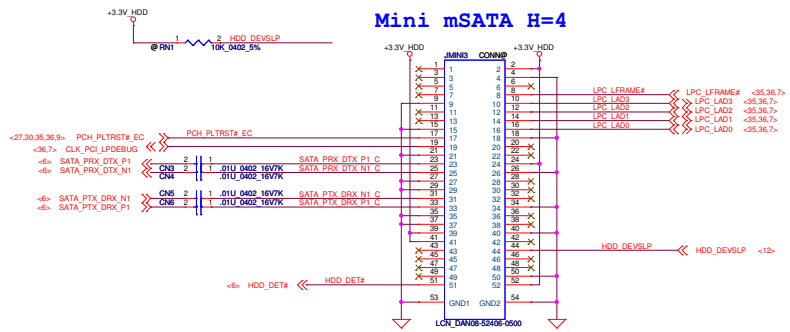


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DDR3L			
Size	Document Number	LA-A971P	Rev
Rev	Workorder	March 14, 2014	Page 15 of 46

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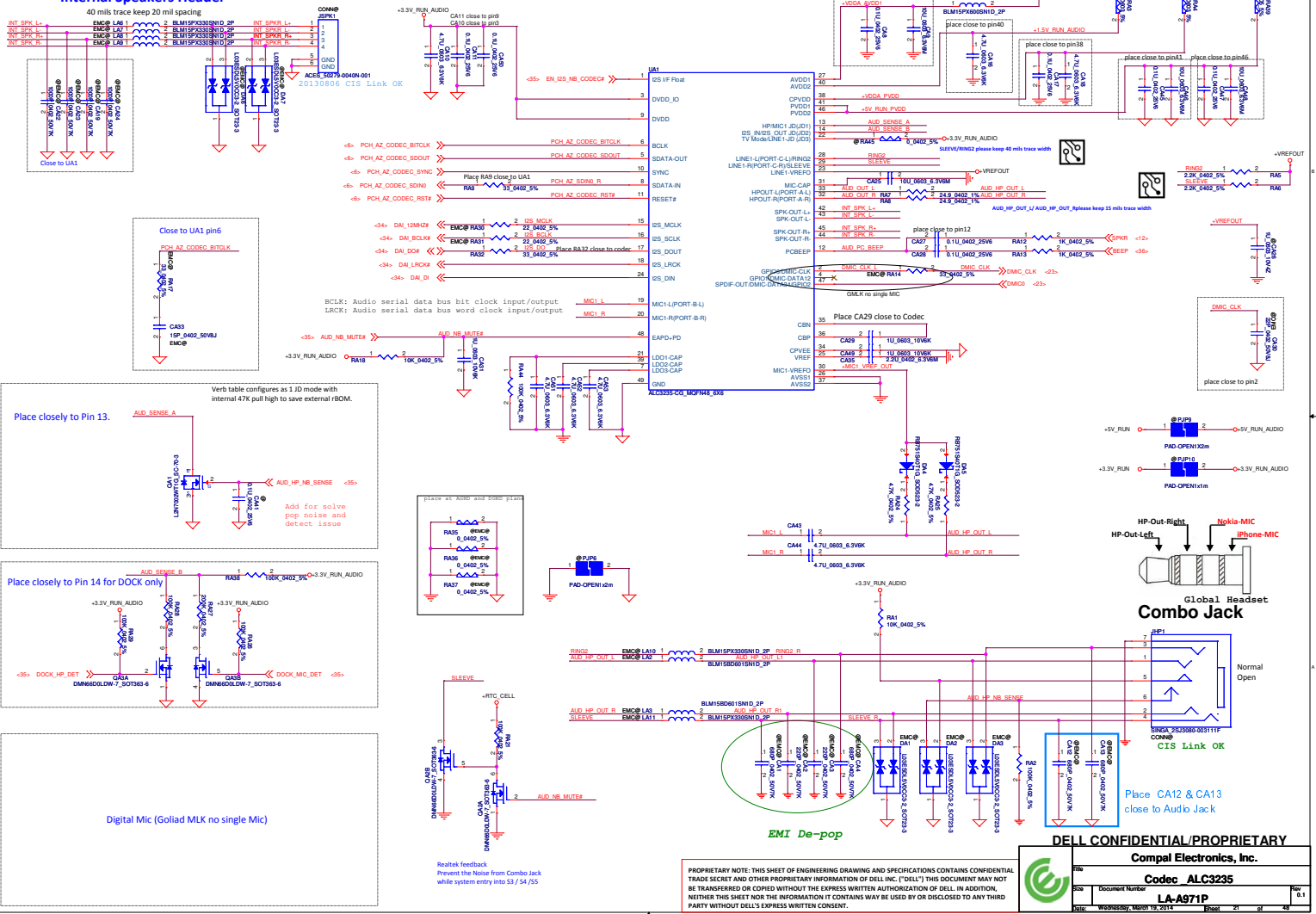
Compal Electronics, Inc.

HDD CONN		
Size	Document Number	Rev
	LA-A971P	0.1
Date	Wednesday, March 19, 2014	Sheet 20 of 25

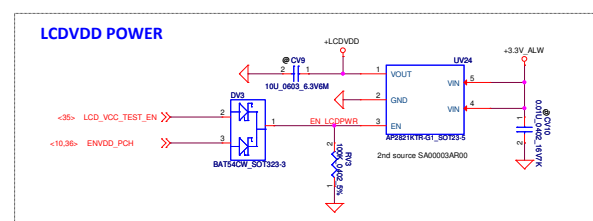
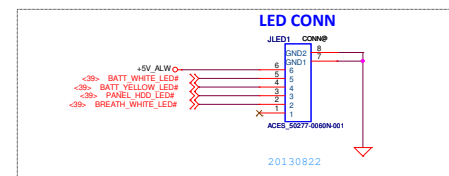
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40 mils trace keep 20 mil spacing

40 mils trace keep 20 mil spacing



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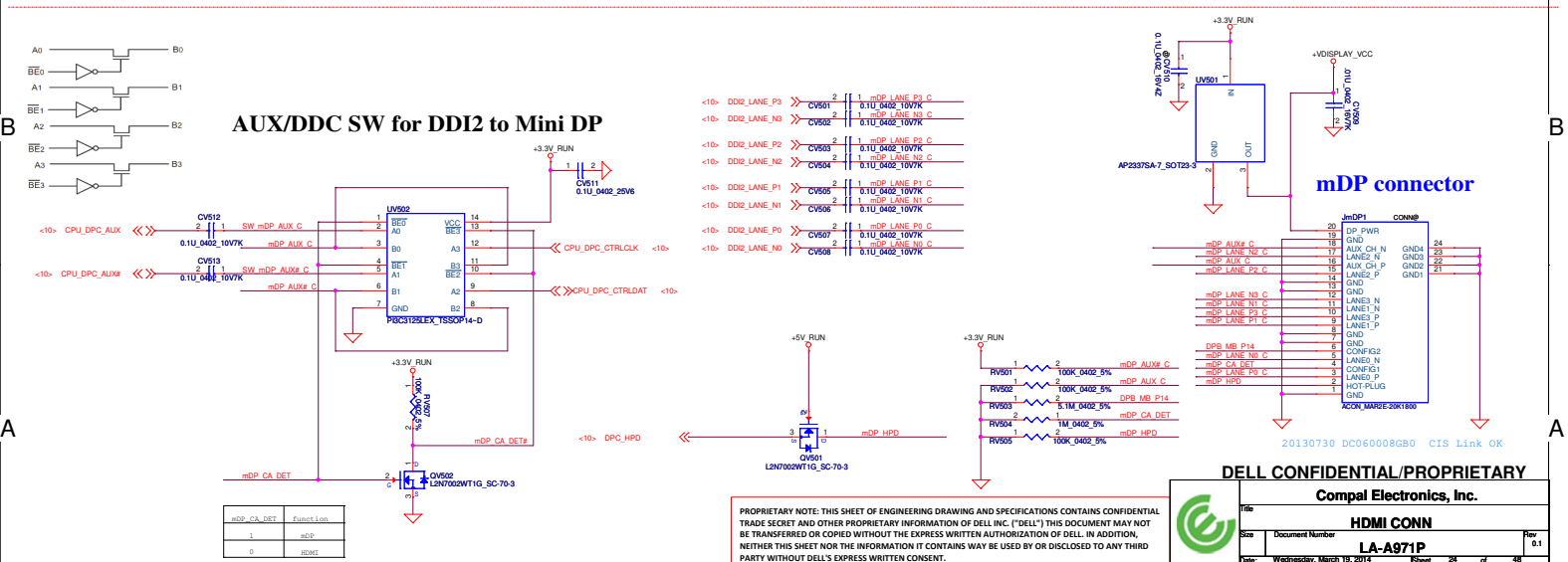
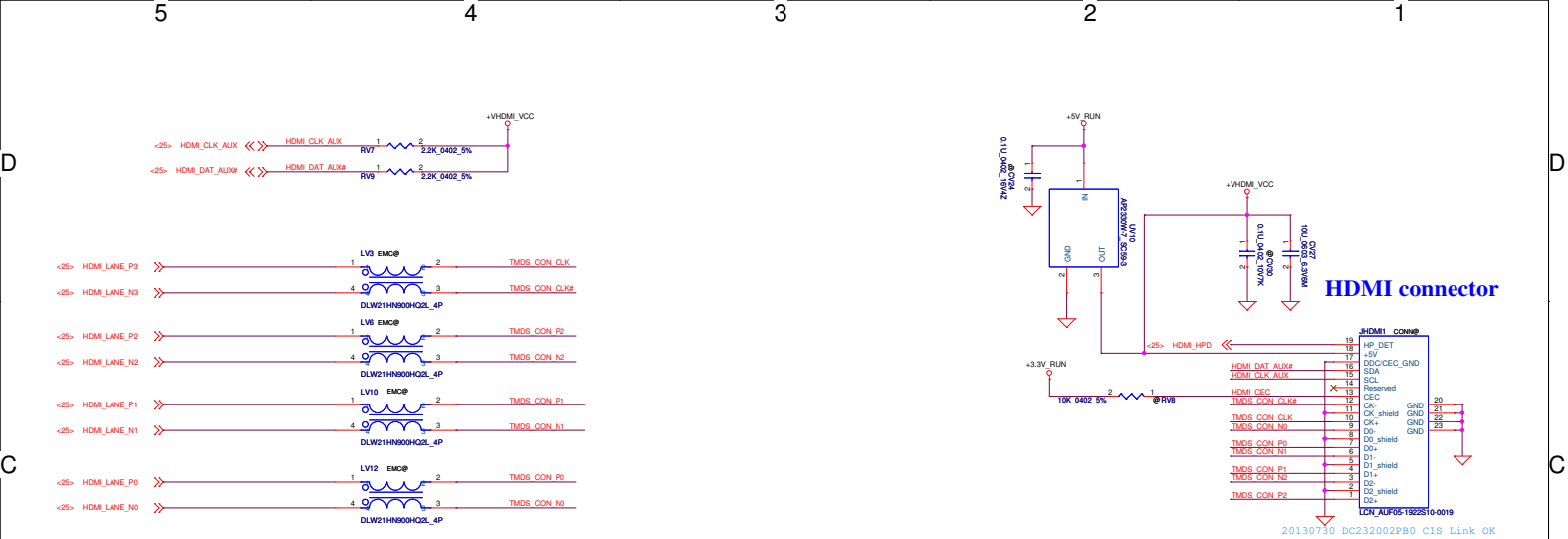
**Compal Electronics, Inc.**

**eDP CONN & Touch screen**

LA-A971B

LA-A971P

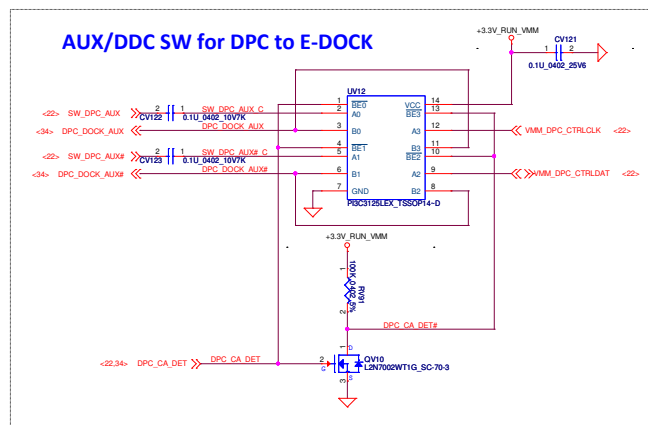
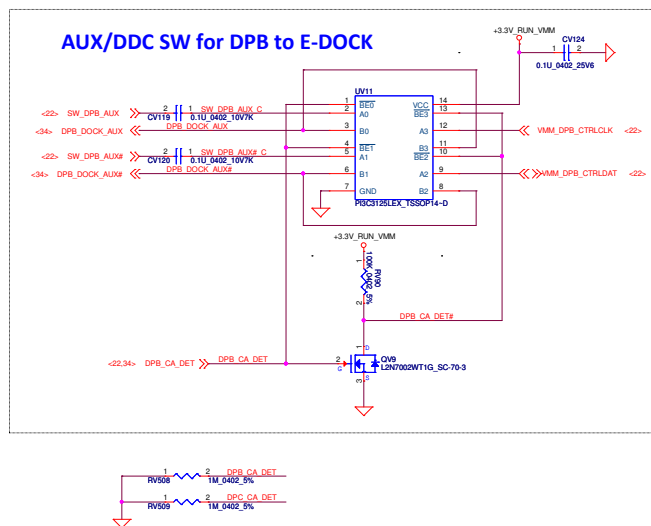
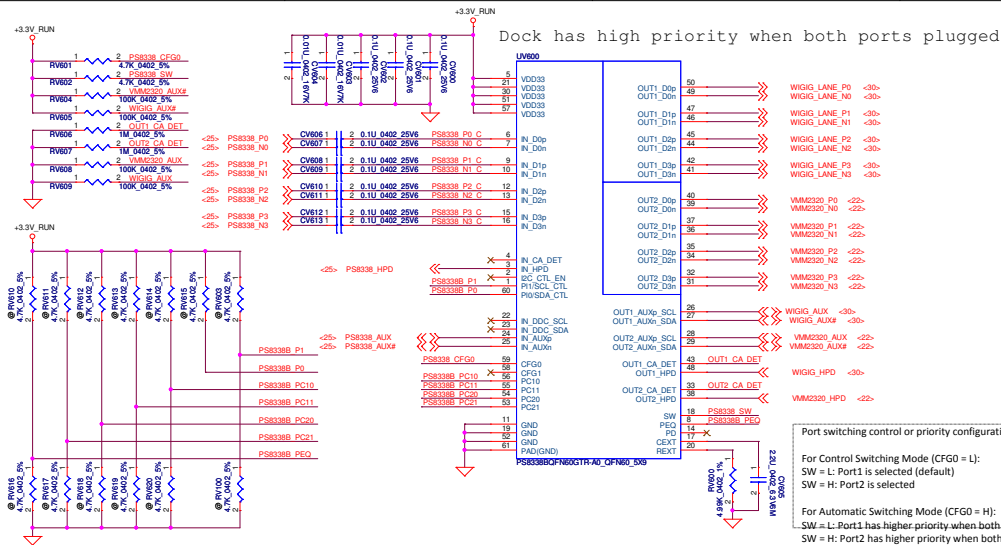
Date: Wednesday, March 19, 2014 Sheet 23 of 48







PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339



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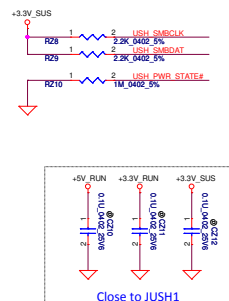
**Compal Electronics, Inc.**

DP SW

**LA-A971B**

LA-A971P  
Date: Wednesday, March 19, 2014 Sheet 25 of 49

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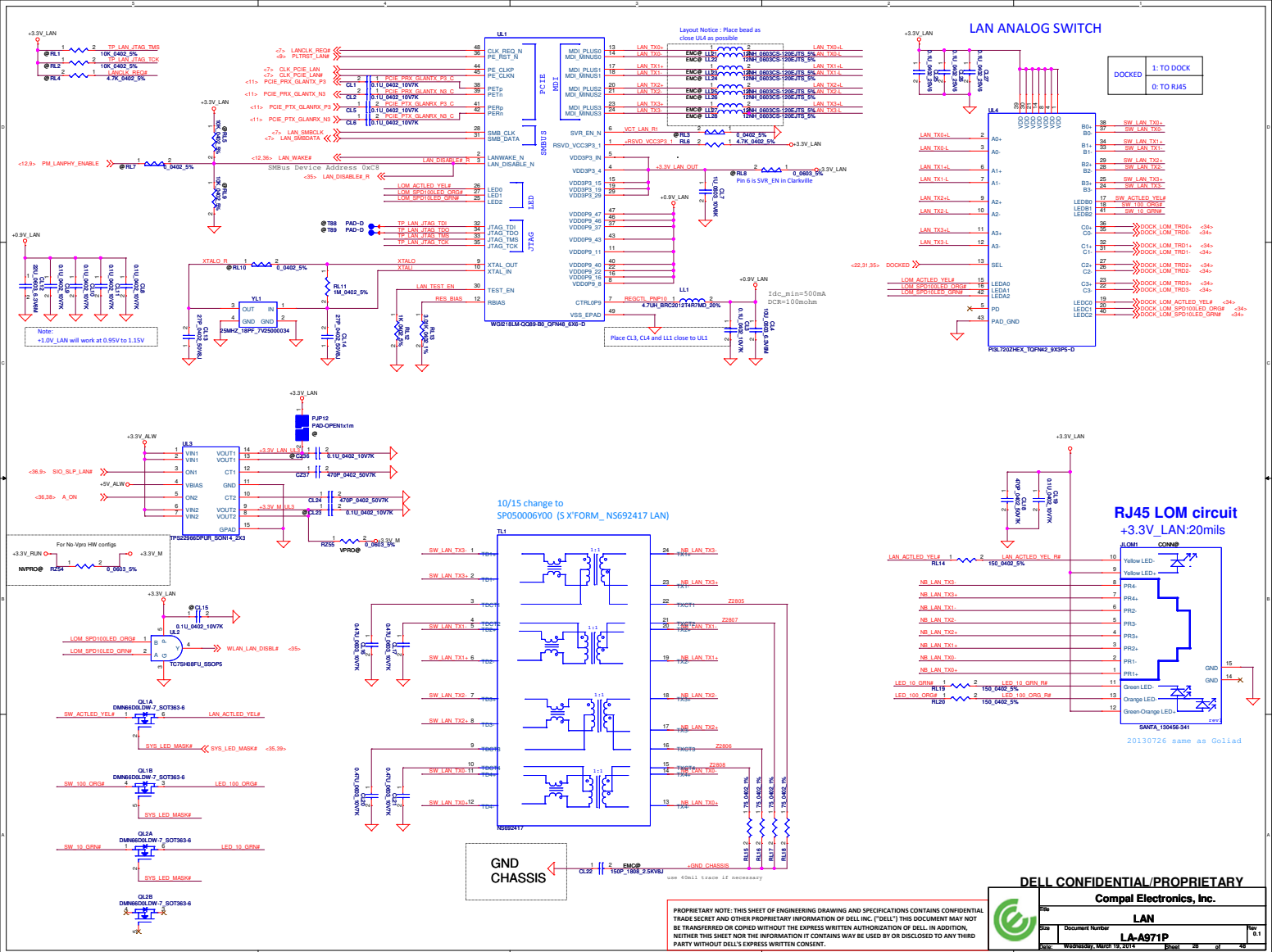
**Compal Electronics, Inc.**

## USH & TPM

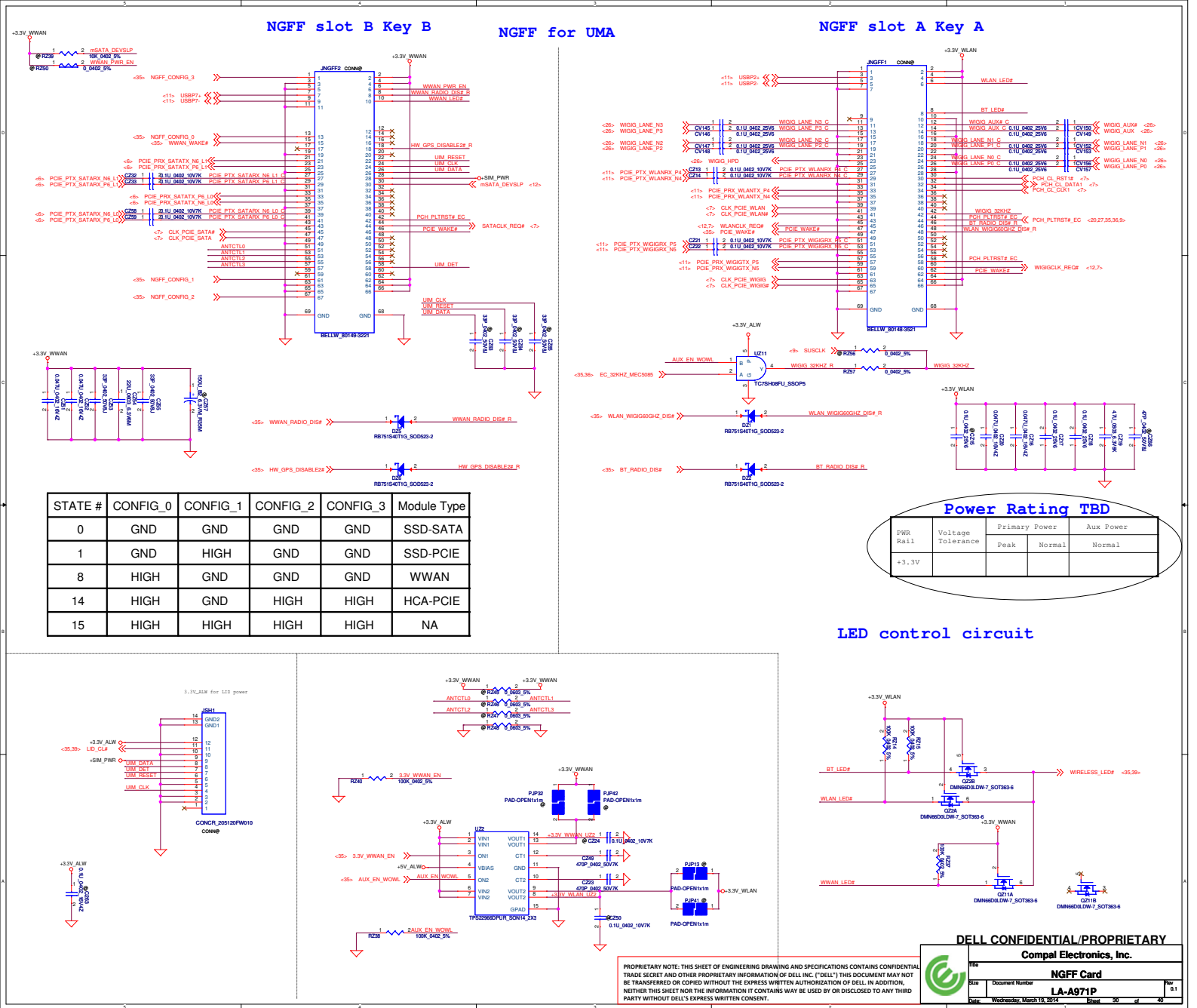
LA-A971P

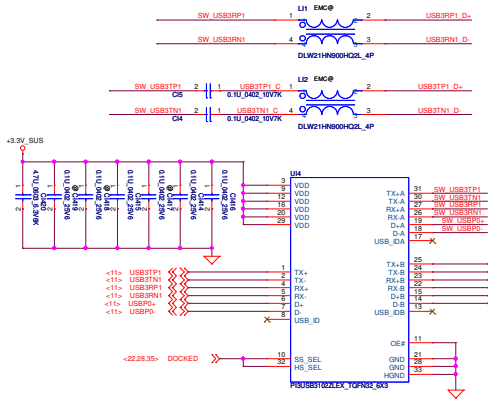
Date: Wednesday, March 19, 2014 Sheet 27 of 48

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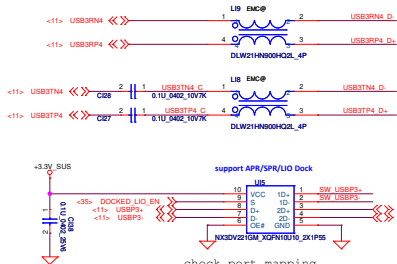






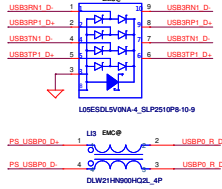
check port mapping

DOCKED	function
1	Dock
0	N/S

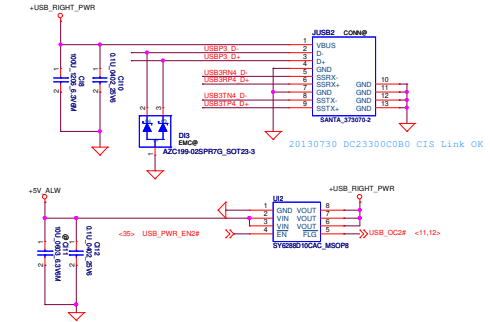
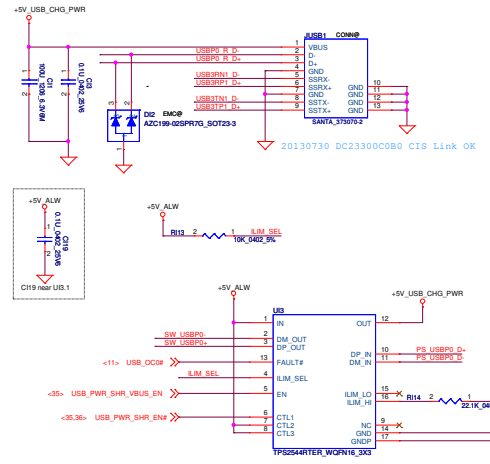
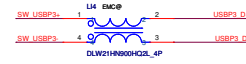
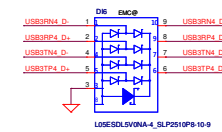


check port mapping

DOCKED_L10_EN	Function
1	Dock
0	N/S



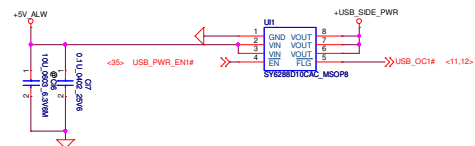
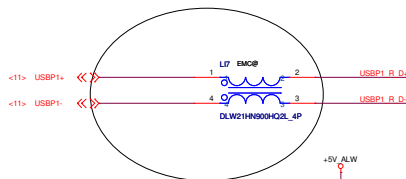
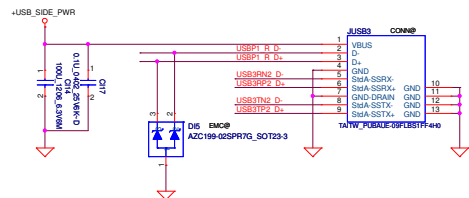
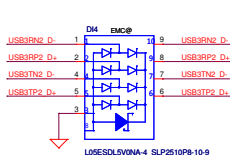
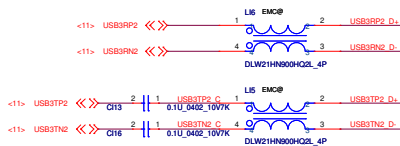
PCB	USB2 0	USB2 3
G12 UMA	USB3102	NX3DV221
G12 Entry	NA	NA
G14 DSC	USB3102	NX3DV221
G14 UMA	USB3102	NX3DV221
G14D_En	NA	NA
G14U_En	NA	NA



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USB3.0			
Rev	Document Number	Rev	
1	LA-A971P	1	1
Rev	Workorder	Rev	1



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USB SW

LA-A971P

Date: Wednesday, March 19, 2014 Sheet 32 of 45

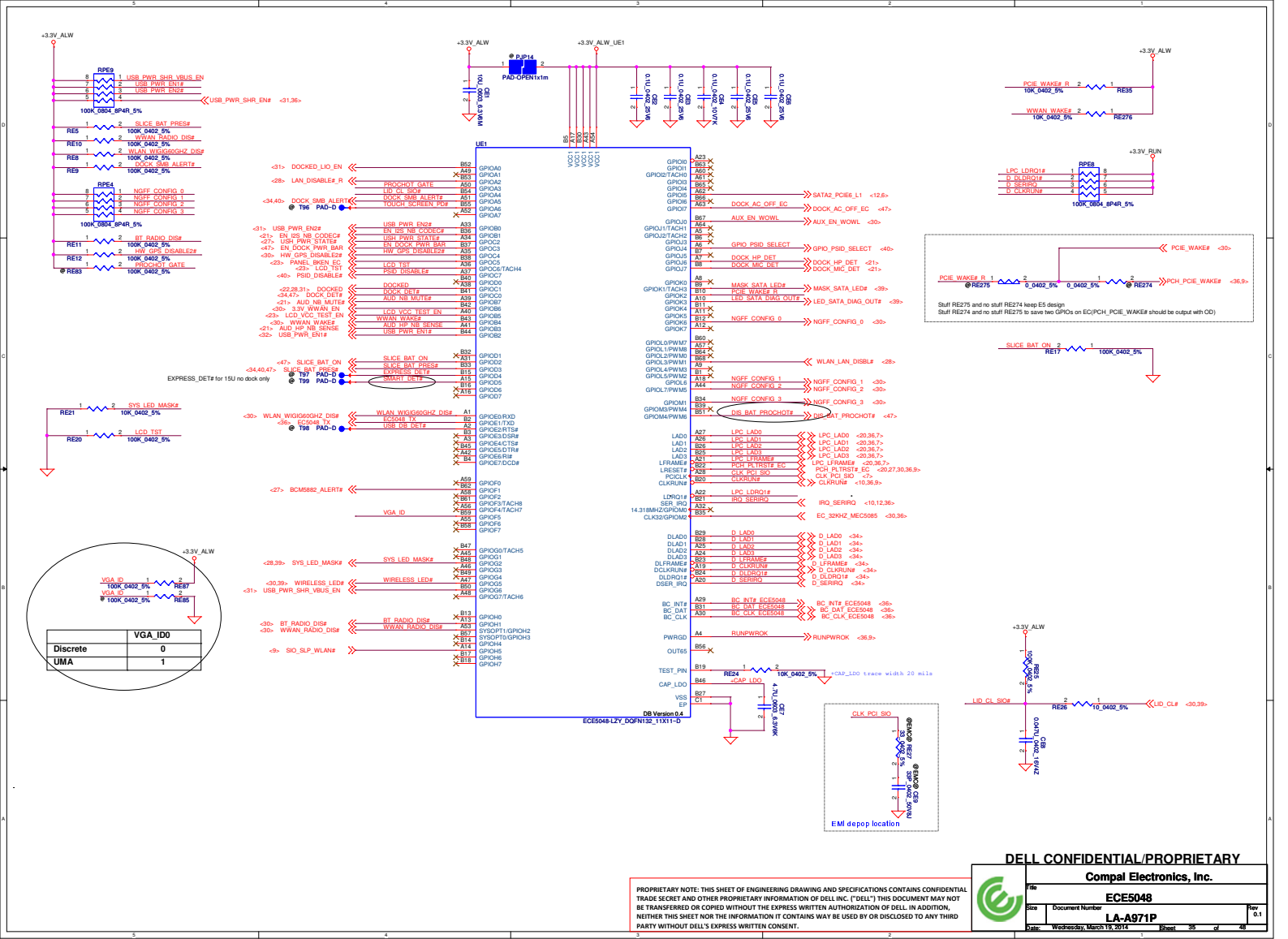


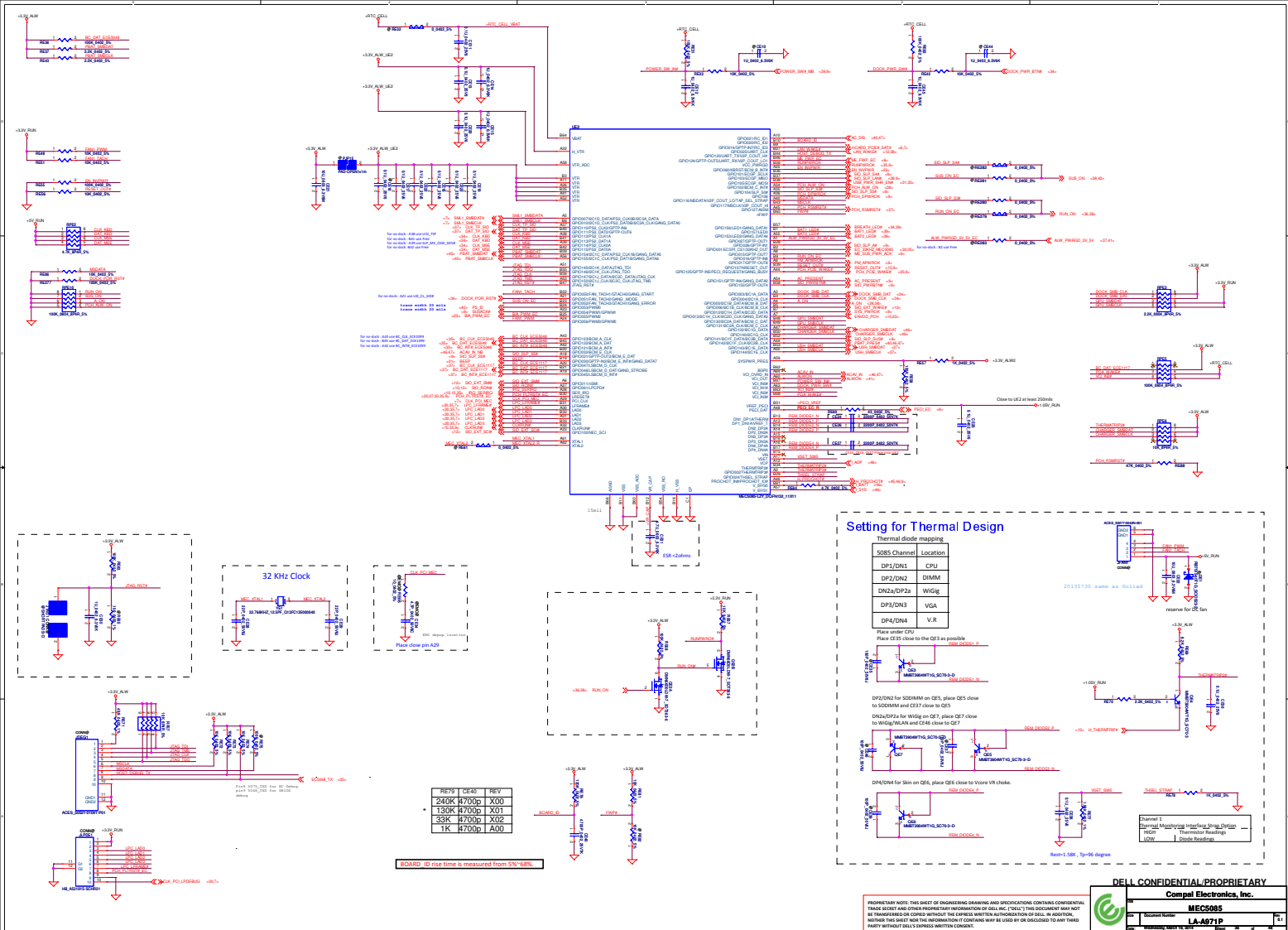
# NFC on USH/B

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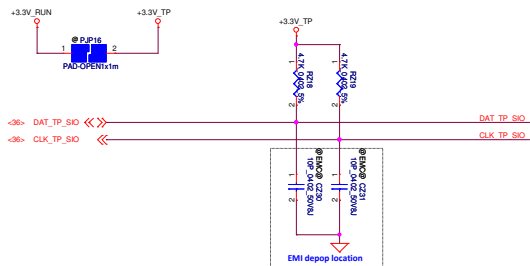
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Compal Electronics, Inc.			
NFC			
Size	Document Number		Rev
	LA-A971P		0.1
Date	Wednesday, March 19, 2014		Sheet 33 of 45

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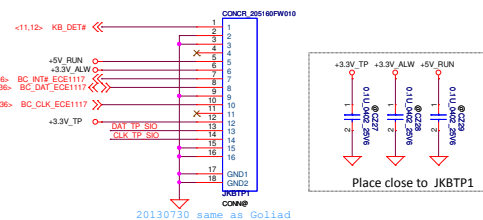




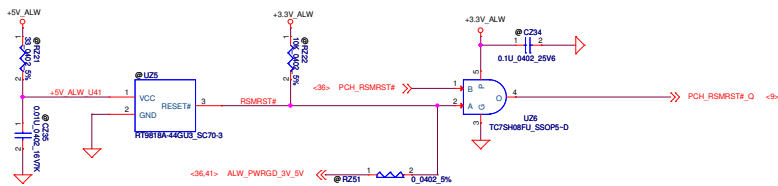
## Touch Pad



## Keyboard



## RSMRST circuit



### @IO FFC

Part Number	Description
DA300000200	FFC 0VW 1P-5551P MEVO W/B-10/B

### @HDP TS Cable

Part Number	Description
DC02C004000	R-COMM SET 0VW MB-LCD-LED-CAM-TS

### @HDP Cable

Part Number	Description
DC02C004000	R-COMM SET 0VW MB-LCD-LED-CAM

### @SATA Cable

Part Number	Description
DC02C004000	R-COMM SET 0VW MB-HDD

### @DC-IN Cable

Part Number	Description
DC30100M000	CONN SET 0VW DC3AC-MB 20W1003-038110P

### @RTC BATT

Part Number	Description
DC30100M000	CONN SET 0VW DC3AC-MB 20W1003-038110P

### @FAN

Part Number	Description
DC28A000000	FAN SET DAQ20 DC5V AB740500B-WB3 A20A

### @MEDIA Board FFC

Part Number	Description
NBK0001C000	FFC 6P G PG.5 PAD0.3 50MM MB-MEDIA/B 0VW

### @KBTP FFC

Part Number	Description
NBK0001C000	FFC 15P G P.5 PAD.3 50MM MB-KBTP N000 0VW

### @NFC Board FFC

Part Number	Description
NBK0001C000	FFC 15P G P.5 PAD.3 50MM MB-NFC N000 0VW

### @USH Board FFC

Part Number	Description
NBK0001C000	FFC 20P G PG.5 PAD0.3 75MM MB-USR/B 0VW

### @FP FFC

Part Number	Description
NBK0001D100	FFC 6P G PG.5 PAD0.3 75MM USR/B-PP 0VW

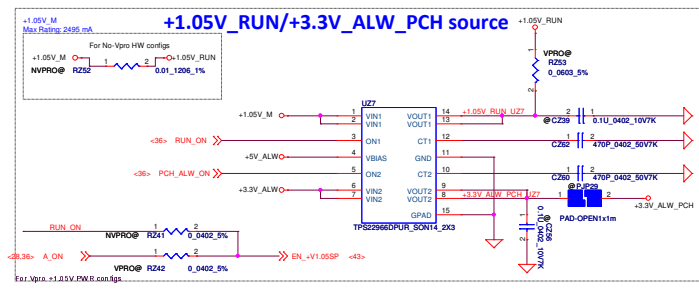
### @Speaker

Part Number	Description
PX230003000	SPK PACK 2.5W 2.0W 4 OHM PD

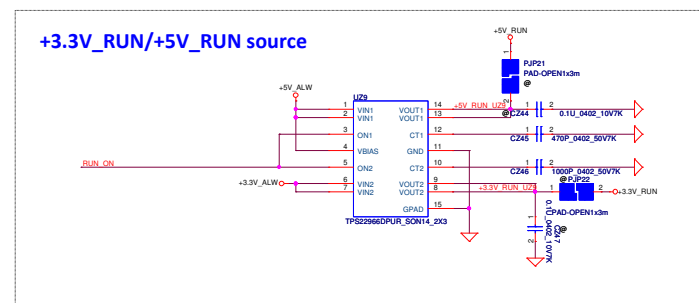
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Keyboard	
Size	Document Number
	LA-A971P
Date	Sheet
Wednesday, March 19, 2014	37 of 46

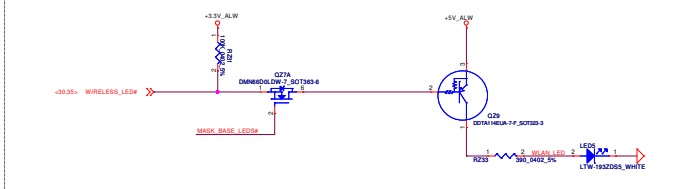


Timing diagram showing the relationship between HSIOPC, VCOSEL, and VCOSELPU signals. The diagram includes a 100ns scale bar and labels for the signals: HSIOPC, VCOSEL, VCOSELPU, and VCOSELPU. The VCOSEL signal is labeled with a slope of 10 pV/us, and the VCOSELPU signal is labeled with a slope of < 0.1 pV/us.

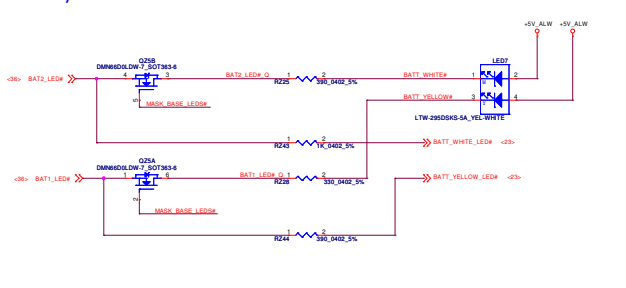


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<b>Compaq Electronics, Inc.</b>			
<b>Power control</b>			
<b>LA-A971P</b>		<b>Rev 0.1</b>	
Size	Document Number		
Date	Wednesday, March 19, 2014	Sheet	38 of 48

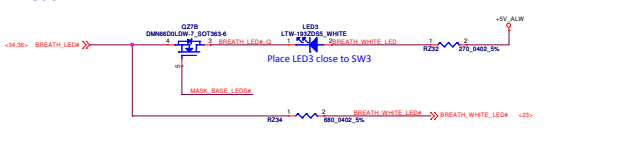
## WLAN LED solution for White LED



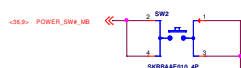
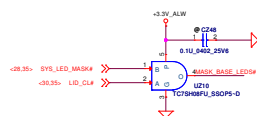
## Breath LED



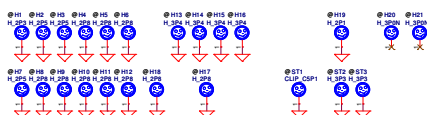
## Breath LED



## POWER & INSTANT ON SWITCH



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



**Fiducial Mark**

FD1  
FIDUCIAL MARK-D

FD2  
FIDUCIAL MARK-D

FD3  
FIDUCIAL MARK-D

FD4  
FIDUCIAL MARK-D

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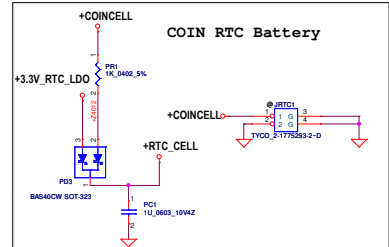
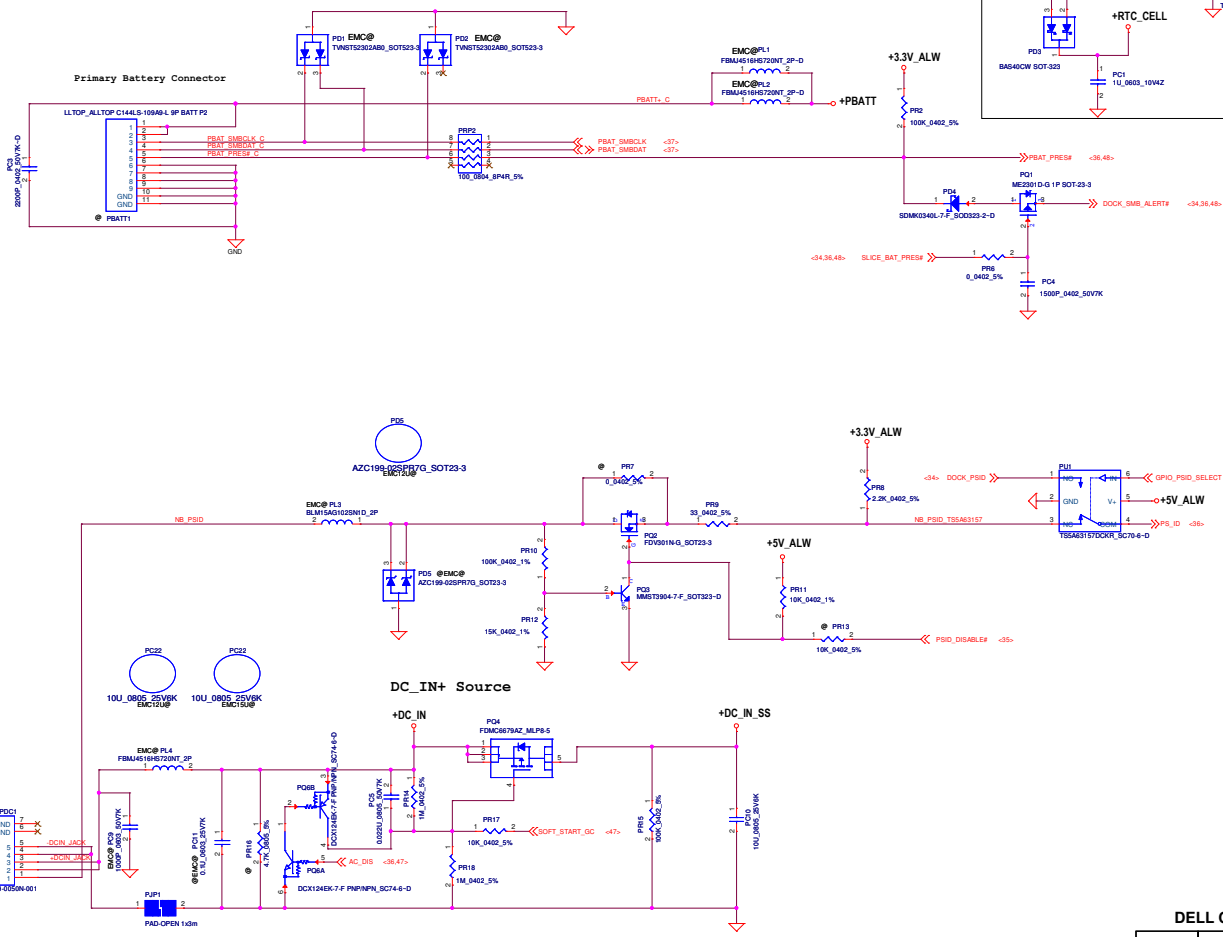
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**PAD, LED**

Size	Document Number	Rev
	<b>LA-A971P</b>	0

Size	Document Number	Rev
	<b>LA-A971P</b>	0

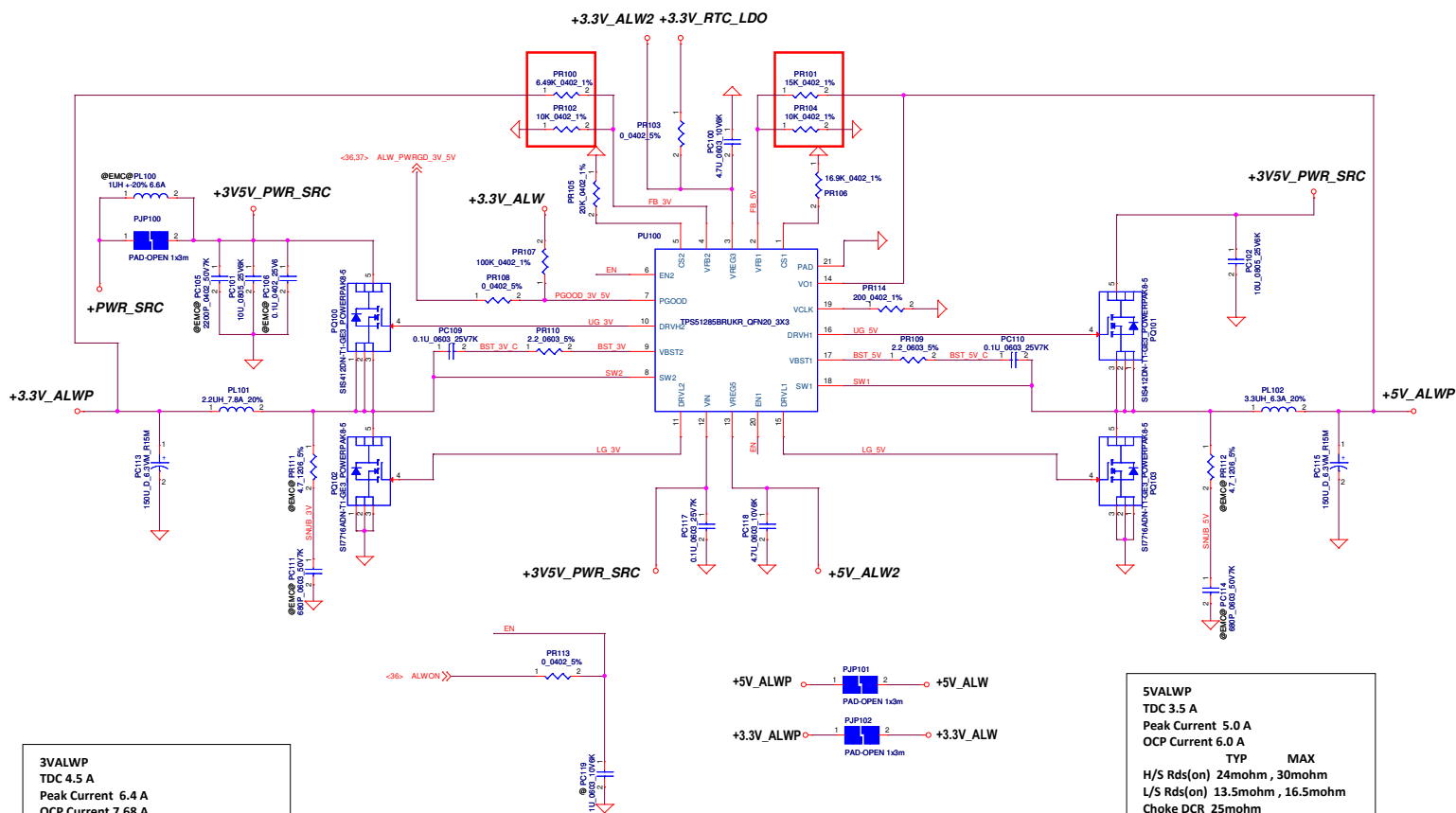


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Compal Electronics, Inc.			
+DCIN			
Doc	Document Number	LA-A901P	
Rev	Revision	Rev	0.3

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3VALWP  
TDC 4.5 A  
Peak Current 6.4 A  
OCP Current 7.68 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	15.5mohm	
CAP ESR	18mohm	

5VALWP  
TDC 3.5 A  
Peak Current 5.0 A  
OCP Current 6.0 A

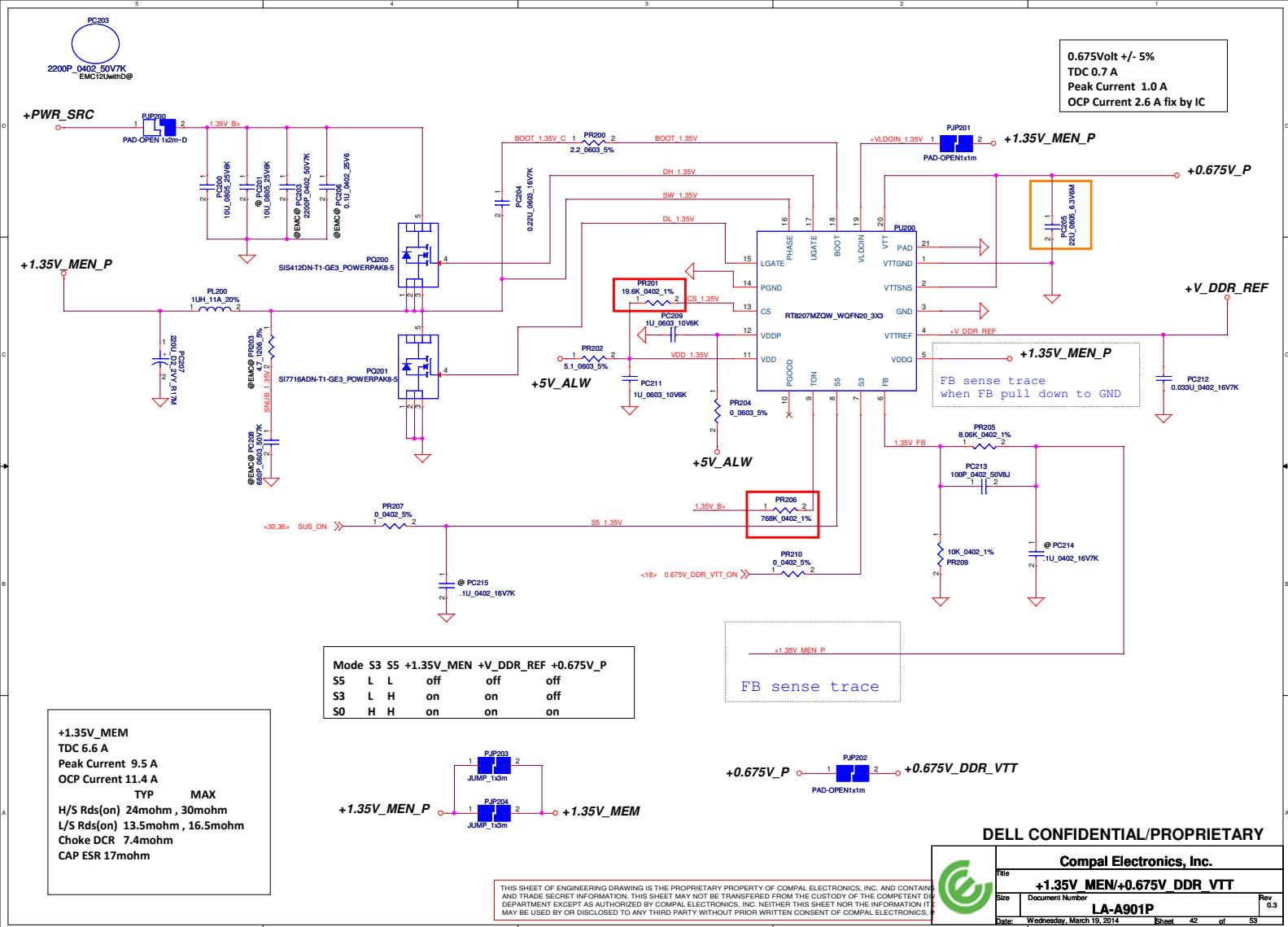
	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	25mohm	
CAP ESR	18mohm	

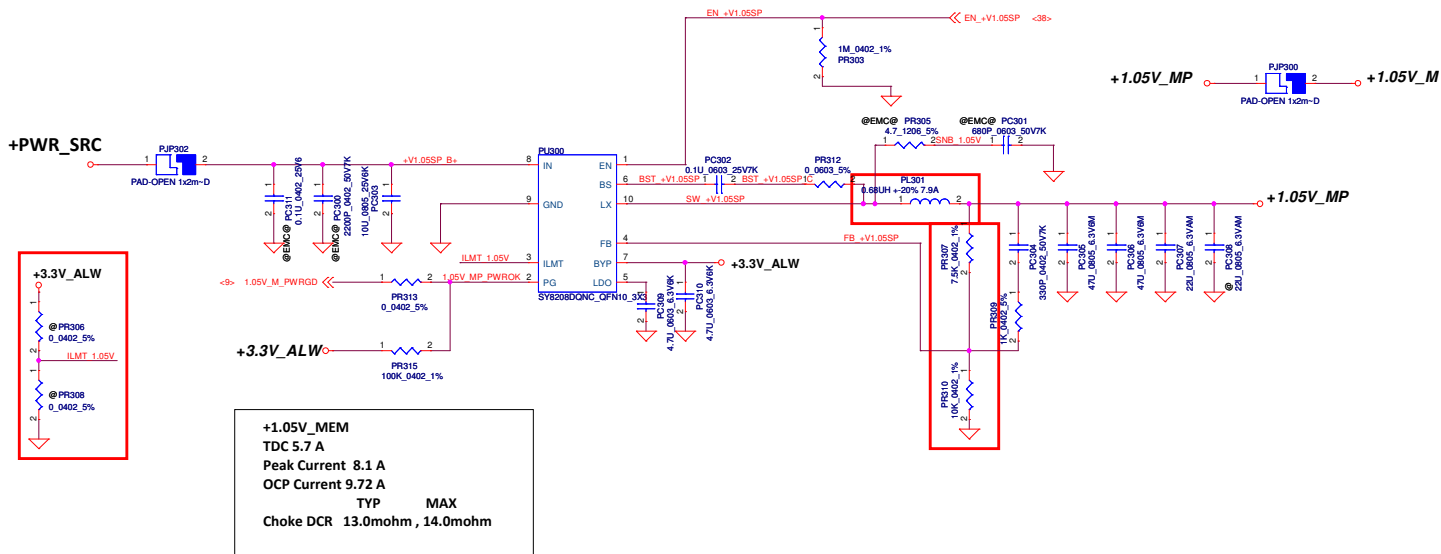
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<b>Compal Electronics, Inc.</b>			
Title <b>+5V_ALW/3.3V_ALW</b>			
Size	Document Number <b>LA-A901P</b>		Rev <b>0.3</b>
Date: <b>Wednesday, March 19, 2014</b>	Sheet <b>41</b>	of <b>53</b>	

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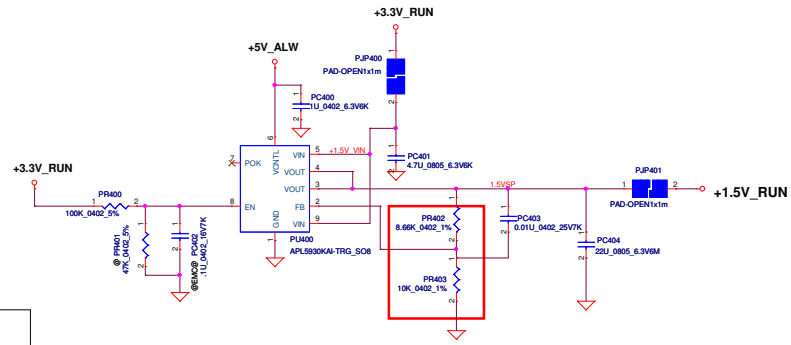
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Title			
<b>+1.05V M</b>			
Size	Document Number		Rev
	<b>LA-A901P</b>		<b>0.3</b>
Date:	Wednesday, March 19, 2014	Sheet 43 of	53

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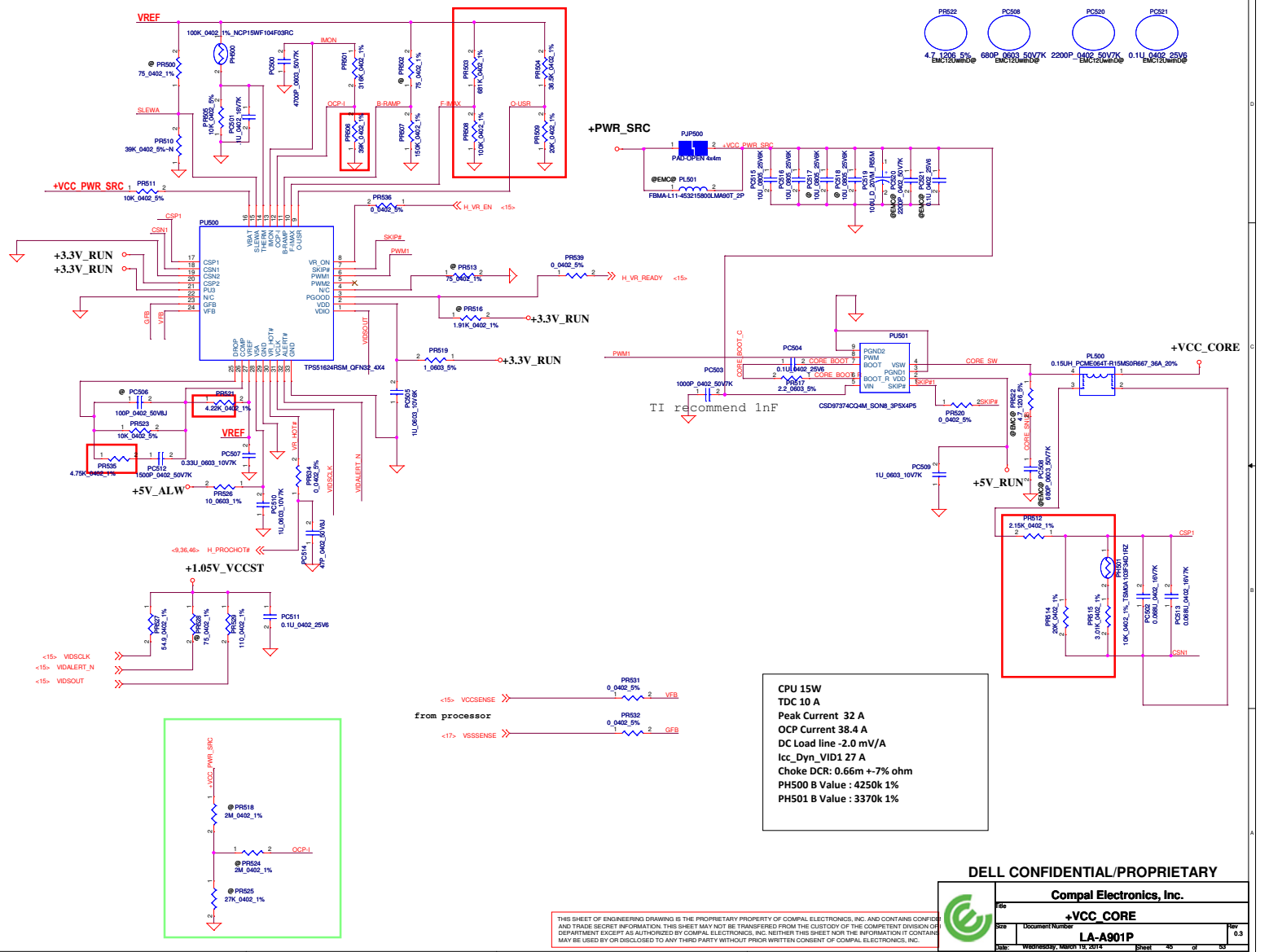
+1.5V\_RUN  
TDC 0.47 A  
Peak Current 0.67 A

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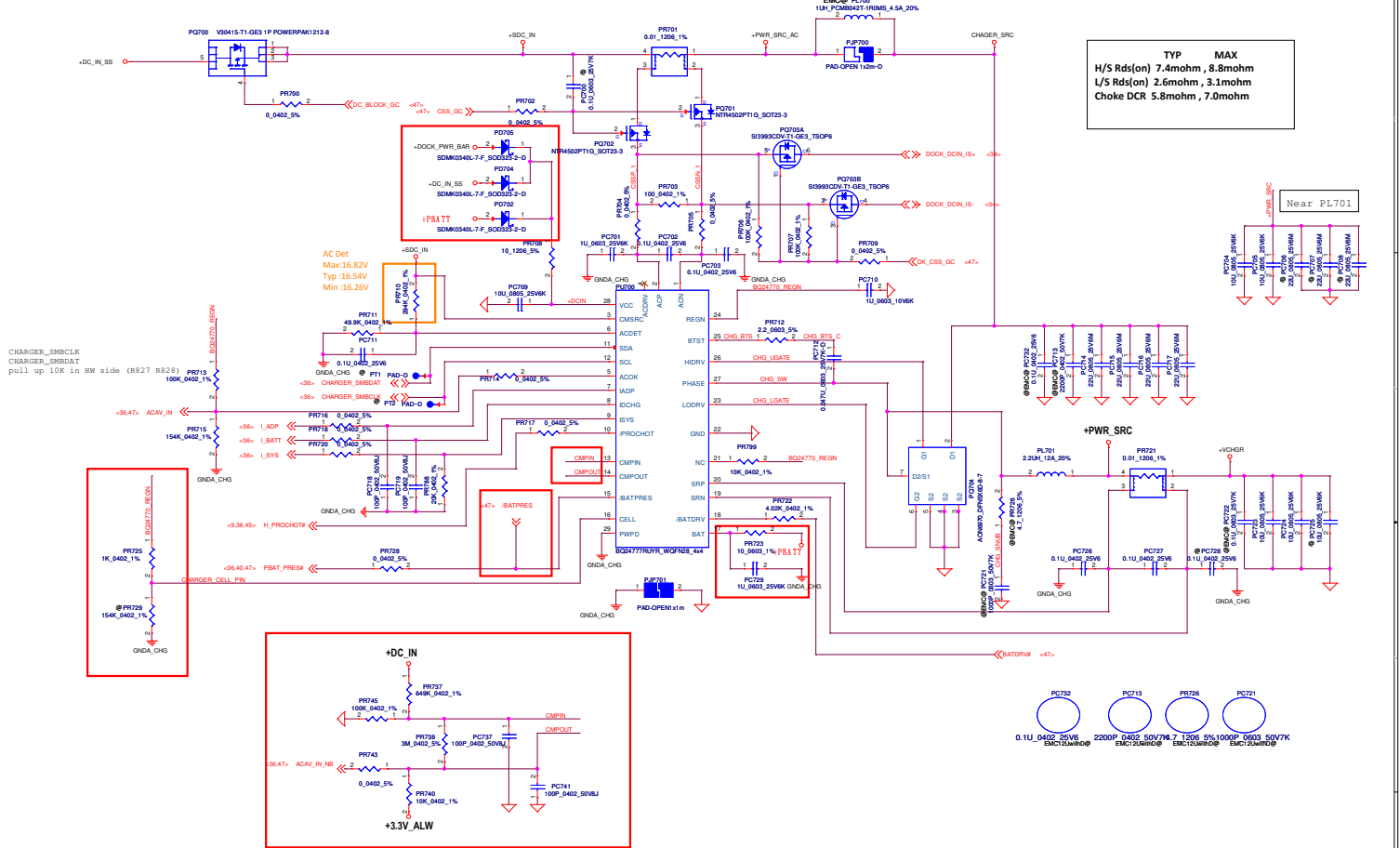


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+1.5V_RUN			
Size	Document Number	Rev	
	LA-A901P	0.3	
Date	Wednesday, March 19, 2014	Sheet	44 of 53

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+VCC CORE			
Doc	Document Number	LA-A901P	
Rev		0.3	
Date	Wednesday, March 15, 2017	Sheet	46 of 50

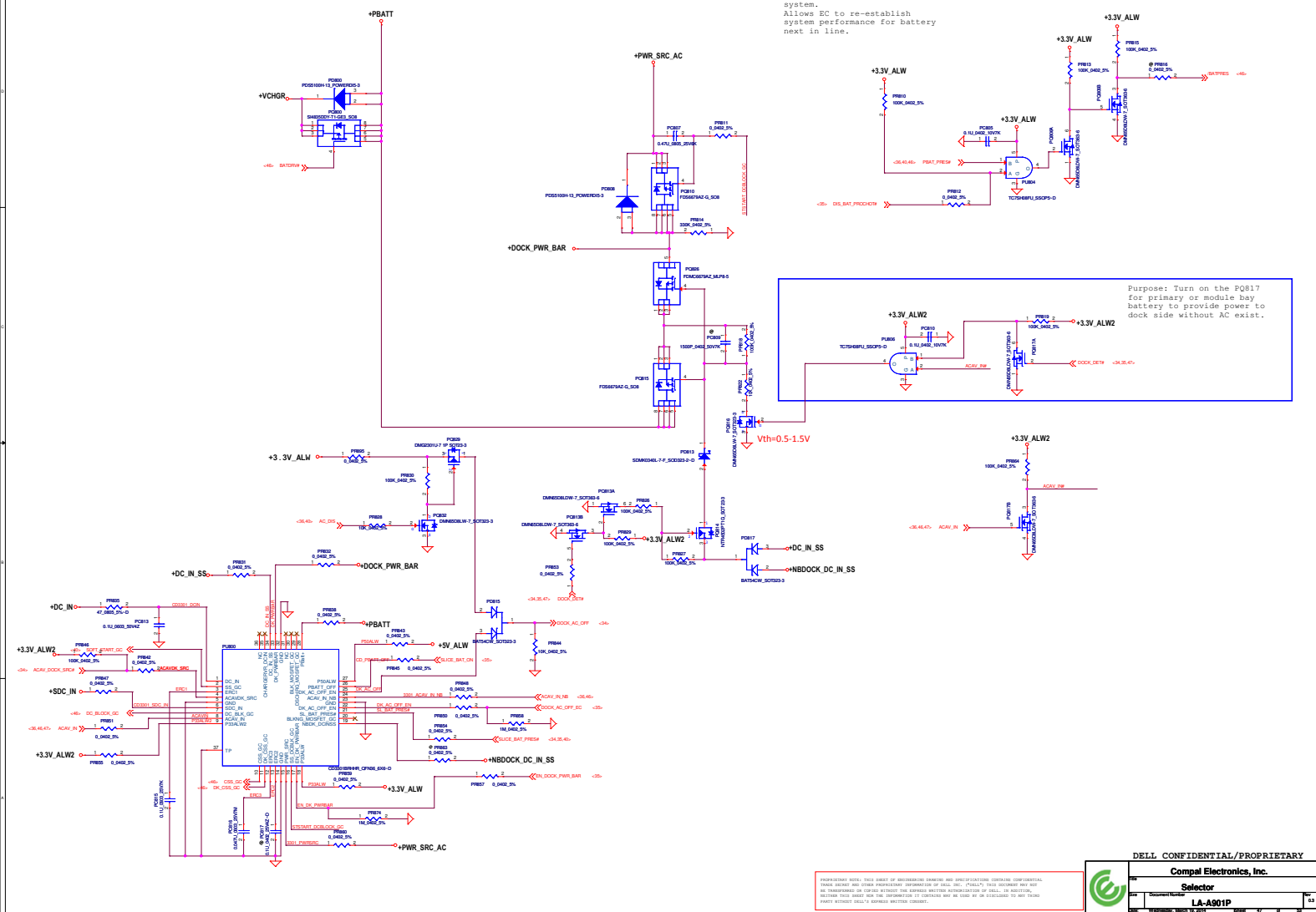


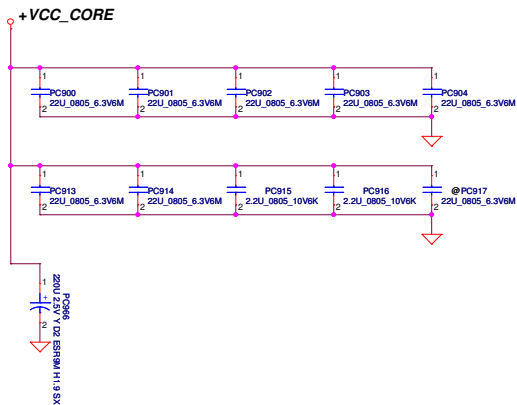
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Charger			
Rev	Document Number	LA-A901P	Rev
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Date: Wednesday, March 15, 2017	Sheet	48	of 53

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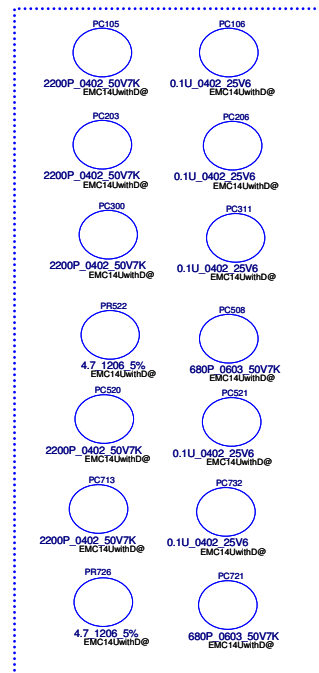
Purpose: Trigger PROCHOT# when active battery is removed from system.  
Allows EC to re-establish system performance for battery next in line.





961

Based on \_RF Cheng. Hill  
鄭智仁 (11257) for PT 20131107



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File		PROCESSOR DECOUPLING	
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		LA-A901P	
Date		Wednesday, March 19, 2014	
		Sheet 48 of 53	
		Rev 0.3	



*Version Change List (P. I. R. List)*

<i>Item</i>	<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
B 1	47	Selector	10/8	Compal	Remove slice battery support circuit	Remove PC808, PC811, PC812 , PC814, PD806, PD807, PD811, PD814, PD819, PD821, PQ801, PQ807, PQ809, PQ811, PQ812, PQ818, PQ821, PQ828, PQ830, PQ831, PR802, PR804, PR808, PR813, PR815, PR816, PR817, PR821, PR823, PR825, PR834, PR836, PR837, PR839, PR849, PR852, PR861, PU805, PU807, PU808	X01
2	45	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
3	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
4	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR713, PR725 to 100k Change PR715, PR729 to 154k	X01
C 5	41, 43, 44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
6	46	Charger	10/25	Compal	Change /BATPRES pin control net from /BATPRES to PBAT_PRES#	Pop PR728 Depop PR816	X01
7	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
8	ALL	ALL	10/31	Compal	RF request	Add PC521, PC206, PC106, PC311, PC732 ( 0.1uF )	X01
9	ALL	ALL	10/31	Compal	RF request	Pop PR111, PC111, PR112, PC114, PR203, PC208, PR305, PC301, PR522, PC508, (4.7ohm, 680pF)	X01
D 10	46	Charger	10/31	Compal	To prevent VCP trigger PROCHOT#	PR703 change to 100ohm	X01
A							

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Title: PWR P.I.R (1/1)  
 Doc No: LA-A901P  
 Date: Wednesday, March 19, 2014      Sheet: 48 of 53

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2 (X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2 (X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2 (X01)
4	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. UV8 pin B5, B6 change to +3.3V_RUN_VMM 7. LP_CTL reserved RV516, 2.2K resistor PU to +3.3V_RUN_VMM 8. Depop RV73	0.2 (X01)
5	24	HW	2013/10/9	COMPAL	correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2 (X01)
6	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_ CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_ MURATA DLW21HN900HQ2L)	0.2 (X01)
7	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, reserved RC27.	0.2 (X01)
8	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2 (X01)
9	24	HW	2013/10/9	COMPAL	SATA ciruit issue	Swap mSATA P & N	0.2 (X01)
10	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2 (X01)
11	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2 (X01)
12	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2 (X01)
13	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2 (X01)
14	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	QL1 Pin2,5 & QL2 Pin2 change from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2 (X01)

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EE P.I.R (1/3)

LA-A971P

Wednesday, March 19, 2014


Sheet 60 of 70

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	UZ8 Pin2 change from +3.3V_ALW to 3.3V_RUN	0.2 (X01)
16	28, 36, 38	HW	2013/10/17	COMPAL	follow Dell requirement.	Add back SUS_ON, change control pin from SUS_ON to SIO_SLP_S4# 1. UZ8.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 -- SUS_ON_EC , RPE10.2 -- SUS_ON 3. add RE282, RE281, RE280, RE279 4. UE2.B9 -- RUN_ON_EC	0.2 (X01)
17	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4? to replace PCH_GPIO48 , Reserve RC302 &RC303	0.2 (X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2 (X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2 (X01)
20	6, 7, 22, 28	HW	2013/10/23	COMPAL	follow xtal vender suggest	1 CC1 &CC2 change from 18PF to 3PF 2 CC8 & CC11 change from 18PF to 15PF 3 CL13 & CL14 change from 33PF to 27PF 4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF	0.2 (X01)
21	23	HW	2013/10/29	COMPAL	it's designed for E5 Goliad, E6 GMLK doesn't need.	remove RZ1	0.2 (X01)
22	30	HW	2013/10/29	COMPAL	To solve WWAN can not detec issue.	Add RZ50, 100k pull up for WWAN_PWR_EN	0.2 (X01)
23	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up ( RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2 (X01)
24	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop Q26, QZ10, RZ16, RZ5, CZ25, CZ38	0.2 (X01)
25	7	HW	2013/11/2	COMPAL	SMBUS Pull High	Add RN3&RN4 pull high to +3.3V_RUN for DDR_XDP_WAN_SMBDAT/SMBCLK	0.2 (X01)
26	21	HW	2013/11/2	COMPAL	EMC request.	Add RA42, RA43.	0.2 (X01)
27	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2 (X01)
28	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2 (X01)
39	21	HW	2013/12/17	COMPAL	follow vender suggest to solve "Bo" noise	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.3 (X01)
40	22	HW	2013/12/17	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10k 2.UC1.F2 &RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 &RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 &RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 &RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM 9.Depop RV516, CV116, CV117	0.3 (X01)

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EE P.I.R (2/3)

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Wednesday, March 19, 2014

Sheet 81 of 70

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