

ECEN 5623

Bus 10

Be Boulder.
 University of Colorado **Boulder**

VITA VME/VXS/VXI vs. PCI / PCIe

VITA VME (VESA Module Expansion)

Asynchronous 20 MHz
A32, A24, A16 Addr Bus
D32, D24, D16 Data Bus
Word or Block Transfer
Daisy-Chained Prio Interrupts
Interrupt Data Cycle

Device Designed in MMIO
Custom Bus Integration on 6U
3U/6U D-shell form factor
VME, VXS Bus, VXI Bus

PCI 2.1, 2.2, 2.3 (Peripheral Component Interconnect)

Synch Clock 33/66 MHz
Muxed 32/64 bit A/D Bus

Burst Transfer Always
Int A-D Routed to APIC, MSI added
Map onto IRQ 0...15
Built-in Hidden Arbiter
Plug 'n' Play Configuration Space
PCI-to-PCI Bridge Scalability
CPCI, PMC, PC/104+, PCI-X
PCI-Express

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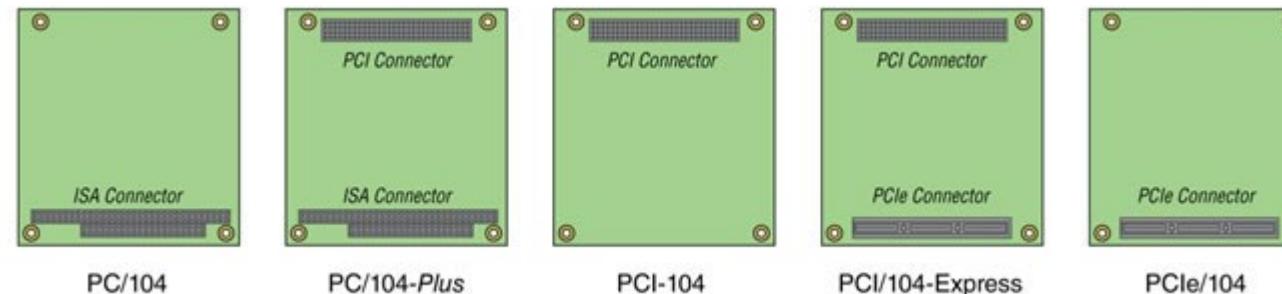
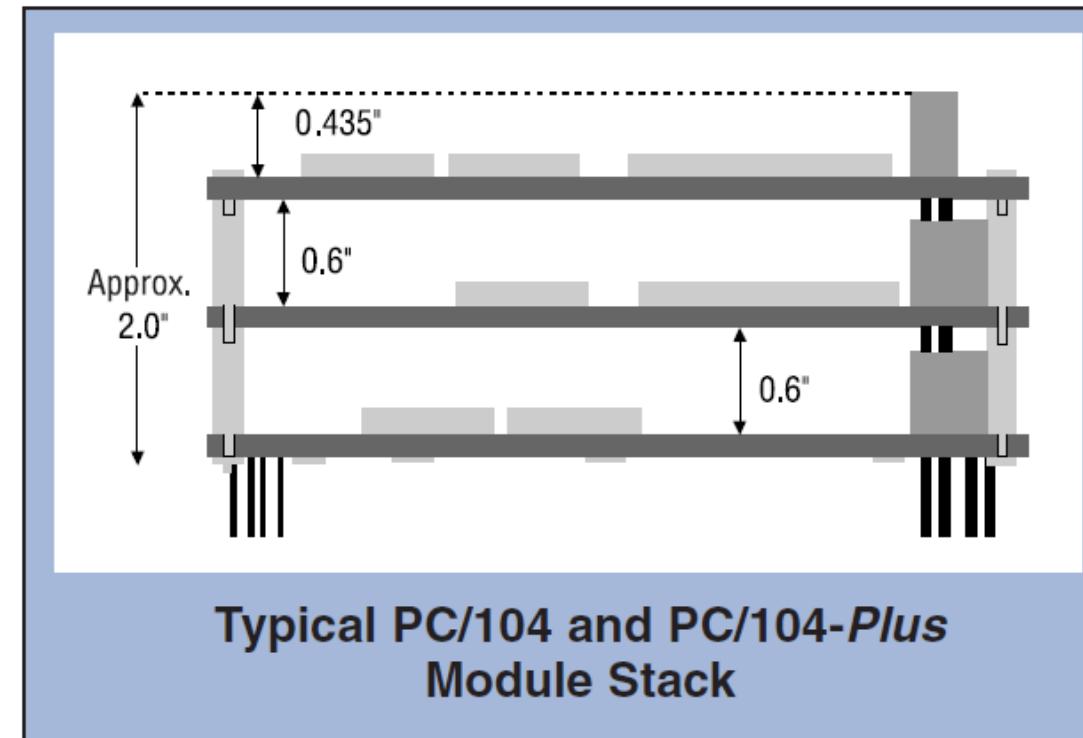


Backplane Buses

Bus	Description
ISA	The first PC expansion card bus; 16 bits at 8 MHz
PCI	The next PC expansion card bus; 32 then 64 bits at 33 then 66 MHz
PC104	ISA bus for industrial or ruggedized use, 3.55" x 3.75" stackable bus
PC104+, PCI104	PC104 with PCI bus added, or just PCI bus
EPIC	Embedded Platform for Industrial Computing – 4.5" x 6.5"platform for PC104 stack
CPCI	Compact PCI; Used for Telecom racks and networking switches in the 90's, 6U or 3U form factor
PCIe	The latest PC expansion bus; Serial differential lanes
VME	Motorola parallel bus for large rugged card cage. Military and Avionics use, 320 MB/s BW
VPX	VME with additional SERDES backplane signals – increases BW to 30 GB/s
ATCA	Advance Telecom. Computing Architecture. Supplanted CPCI. Spawns MicroTCA
PICMG	PCI Industrial Computer Manufacturers Group (PICMG) is a consortium of over 227 companies



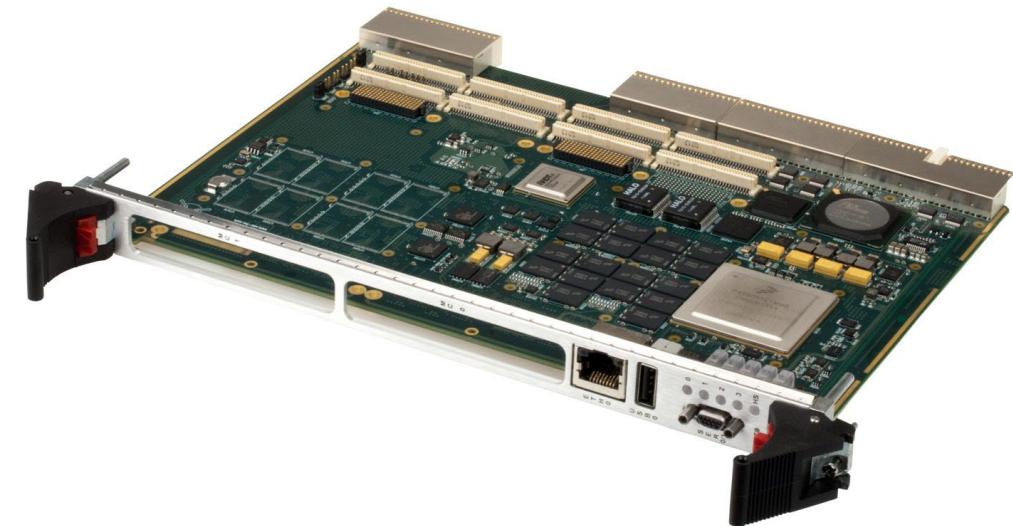
PC104 Connector Backplane



VPX Chassis

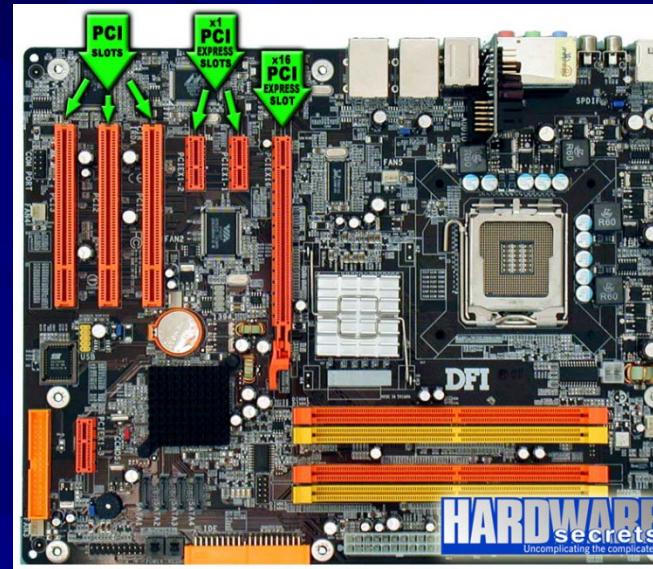
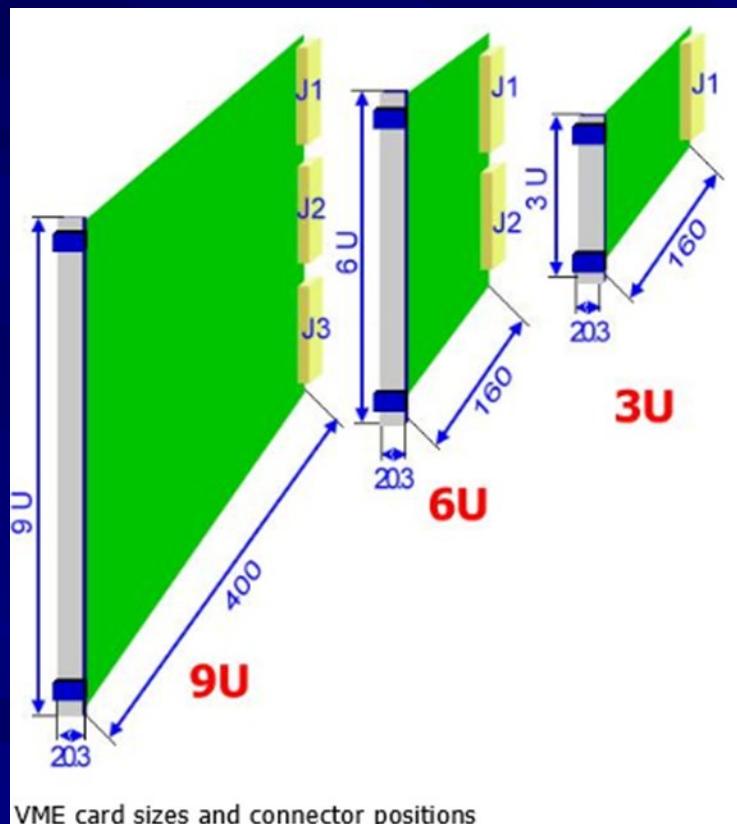


CPCI Chassis



Card / Backplane I/O Expansion

- Scalable Embedded Systems
- DoD, Commercial Aviation, etc.



PCI Revisions Compared

Bus	Frequency	Potential Bandwidth	Number of Devices
PCI 2.x 32-bit	33 Mhz	133 Mbytes/sec	4-5
PCI 2.x 32-bit	66 Mhz	266 Mbytes/sec	1-2
PCI-X 1.0a	133 Mhz	533 Mbytes/sec	1-2
PCI-X 2.0	266 Mhz	1066 Mbytes/sec	1 Point-to-Point Bus
PCI-E x8 bi-directional	2.5 Ghz	4 GBytes/sec	Switched Scalable Differential Serial Byte Lanes

Bus I/O Understanding

- Parallel Buses Have Been Overtaken by Serial for High Bandwidth Because [choose best]:
 - A. Serial is an Inherently Simpler Bus Interface
 - B. Signal Integrity Issues Such as Crosstalk for Many Parallel Traces
 - C. Required for Plug and Play
 - D. Serializer/Deserializer (SERDES) and Encoding Technology (e.g. 8b/10b) With Byte Lanes (Parallel Serial) Enable Superior Performance and Scaling
 - E. Parallel Signal Skew Makes PCB Layout Too Hard

- Bus Physical Form Factors Matter Because [choose best]:
 - A. Changes the Signal and Logical Protocol of the Bus
 - B. Requires Software Device Interfaces to Be Re-Written
 - C. Slows Down Data Transfer
 - D. Ruggedized for Embedded Environment (Vibration, EMI/EMC, Thermal, Insertions, Size)
 - E. None of the above

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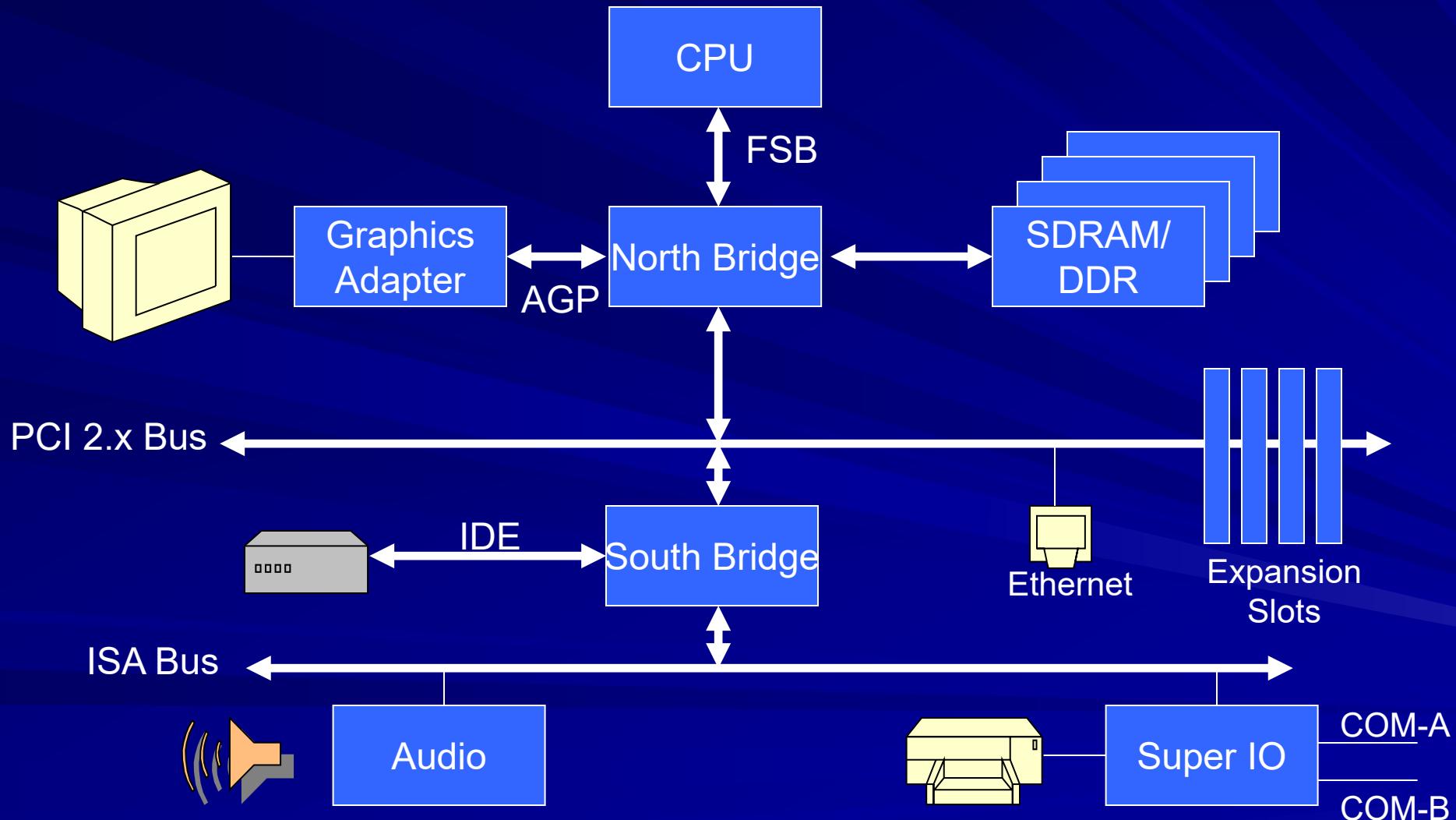
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Original PCI System



PCI Key Concepts

- PCI SIG Industry Consortium for Standard
 - PCI 2.1, 2.2, 2.3
 - PCI-X 1.0a/b, PCI-X 2.0
 - PCI-Express
- North Bridge: CPU, Memory, AGP, PCI Bus
- South Bridge: PCI Bus, APIC, ISA Bus
 - Legacy I/F for x86 IRQs and SuperIO ISA Chipsets
 - Not Required, but PCI NB/SB Often on a Single Chip
- PCI-to-PCI Bus Bridges for Scalability
 - Type 0 Configuration Transaction for Bus 0
 - Type 1 Configuration Transaction for Bridged Bus

PCI Key Concepts

- Plug 'n' Play (Resource Config Space)
 - OS and/or BIOS can probe configuration space registers at well known port address
 - For Each Bus (256), Probe to Find all Devices (32)
 - Vendor ID and Device ID
 - Setup Each Device Function (8)
 - Setup Interrupts A-D for Each Function
 - Program Command Register for MMIO, IO, and Mastering
 - Program BAR 0-5 for MMIO or IO
 - Program Int A-D if Applicable
 - Hidden Arbitration
 - Req/Gnt During Master to Target Bursts
 - Master Latency Timer is Minimum Burst

PCI Form Factors

- PC Edge Connected 32 bit and 64 bit slots
- CPCI Backplane Pin Connectors
- PC/104+ PCI and ISA Stackable
- PMC PCI Mezzanine Cards
- PCI-Express Scalable Differential Serial
 - PCI Compatible Message Transport Protocol
 - x1 to x32 PCI Express Byte Lanes (8 to 256 bits)
 - Root Complex (Replaces North Bridge)
 - Byte Lanes are 2.5 Gb/s/direction Differential Serial 8b/10b Encoded
 - Switched Architecture
 - Slots, Embedded, Cables
- MiniPCI

Bus I/O Understanding

- A Bus is a Shared Interconnection Between Devices
 - A. TRUE
 - B. FALSE
- Bus Transactions Require an Initiator (Master) and a Target Device
 - A. TRUE
 - B. FALSE
- It is Most Efficient to Address Each and Every Data Transfer
 - A. TRUE
 - B. FALSE

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A Bus is a Shared Interconnection Between Devices

True

False

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PCI-Express

■ Design Goals:

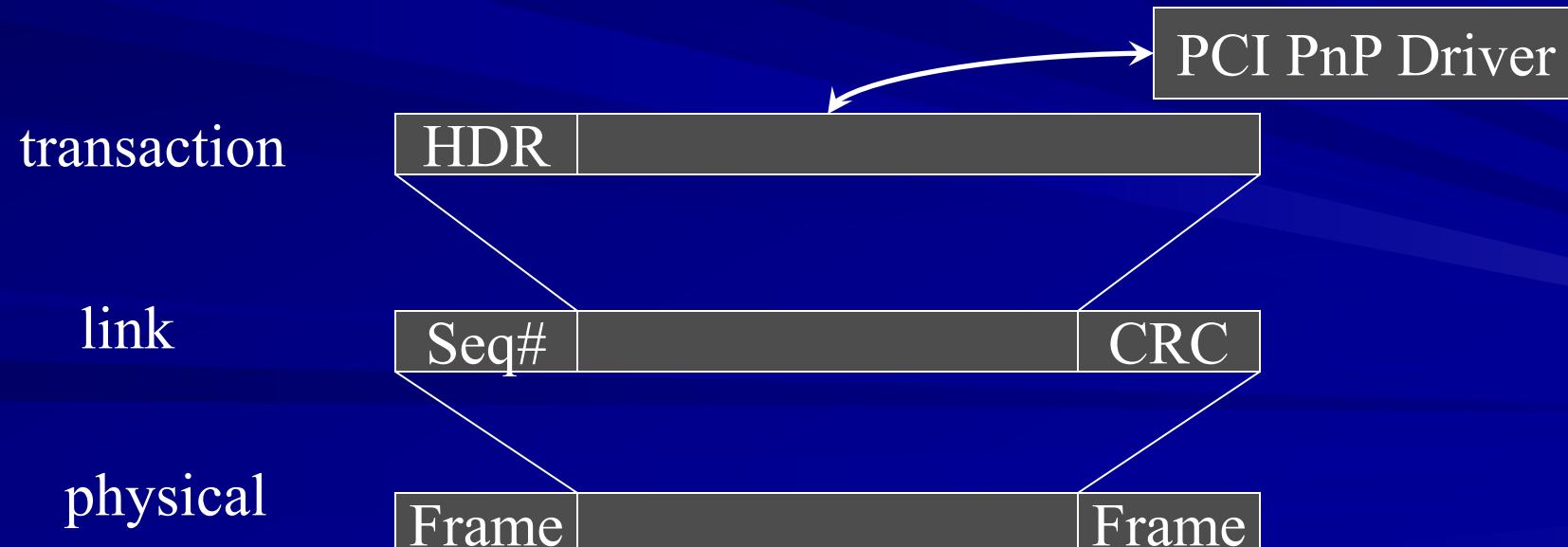
- Highest Bandwidth / pin (2.5 Gb/sec/direction)
 - PCI-Express
$$[(2.5 \text{ Gb/s/dir} \times 8\text{b/dir}) \times (1\text{B}/8\text{b})]/40 \text{ pins} = 100 \text{ MB/s/pin}$$
 - PCI
$$[(32\text{b} \times 33 \text{ MHz}) \times (1\text{B}/8\text{b})]/84 \text{ pins} = 1.58 \text{ MB/s/pin}$$
 - PCI-X 2.0 (DDR)
$$[(64\text{b} \times 266 \text{ MHz}) \times (1\text{B}/8\text{b})]/150 \text{ pins} = 7.09 \text{ MB/s/pin}$$
- De-couple Physical Signaling from Protocol
- Switched Architecture
- Message Protocol with Minimized Side-Band Signals
 - MSI and MSI-X Message-Based Interrupts
 - Data Transport
 - Management
 - Power Management Side-Band Signals
- Compatible with PCI-2.x, PCI-X 1.0a/b, PCI-X 2.0
 - PCI buses Bridged with PCI-Express Switches on I/O Bridge
 - North Bridge Becomes Root Complex
 - Memory Bridge
 - I/O Bridge

PCI-Express

Version	Intro-d uced	Line code	Transfer rate ^{[1][2][3]}	Throughput ^{[1][2][3]}				
				×1	×2	×4	×8	×16
1.0	2003	<u>8b/10b</u>	2.5 GT/s	0.250 GB/s	0.500 GB/s	1.000 GB/ s	2.000 GB/s	4.000 GB/s
2.0	2007	8b/10b	5.0 GT/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s	8.000 GB/s
3.0	2010	<u>128b/130b</u>	8.0 GT/s	0.985 GB/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s
4.0	2017	128b/130b	16.0 GT/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s
5.0	2019	128b/130b	32.0 GT/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s	63.015 GB/s
6.0	2022	1b/1bFLIT+ PA <u>M-4</u> + ECC	64.0 GT/s	7.563 GB/s	15.125 GB/s	30.25 GB/s	60.50 GB/s	121.00 GB/s
7.0	2025 (Planned)	1b/1b FLIT + <u>PAM-4</u> + FEC	128.0 G/s	15.125 GB/s	30.25 GB/s	60.5 GB/s	121.0 GB/s	242.0 GB/s

PCI-Express

- Each Tx/Rx Differential Pair (HSOp,n and HSIn,n) forms a Byte Lane
 - Byte Lanes Ganged x1, x2, x4, x8, x12, x16, x32
 - Serializer/Deserializer on Each Byte Lane
 - Driver, Buffering, and PLL on Each Byte Lane
 - Lane-to-Lane Deskewing Done in Phy
- Data Tx/Rx with Packet Protocol



Bus I/O Understanding

- The PCI bus is a Standard for Both Parallel and Serial Component Interconnect such that [choose best]:
 - A. Plug and Play is Supported and Device Interface Software is Provided a Standard Interface for Addressing, Interrupts, and Data Transfer
 - B. All Systems that Integrate PCI must Use Optical Transport
 - C. All Systems that Integrate PCI must Use Parallel Copper Physical Layer
 - D. Data Transfers Require Programmed I/O
 - E. Scaling is Limited to One Bus Master and a Few Bus Targets

- The VME Bus is [choose best]:
 - A. An Adaptation of a General Purpose Computing Bus to Embedded that was Originally an Asynchronous Bus
 - B. No Longer Used at All
 - C. Multi-plexes Address and Data Lines
 - D. Has Just Two Interrupt Levels
 - E. None of the above

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I/O Trends

- High Speed Differential Serial Overtaking Parallel Buses?
 - USB 2.x, 3.x
 - PCI-Express
 - 1/10G Ethernet (1G Cat-5 UTP Copper, 10G Fiber)
 - SAS
- Parallel Buses Hit Signal Integrity Limits (Skew, Crosstalk)
 - DDR (266, 400 Mhz)
 - PCI-X 2.0
 - Quad-Rate

Bus I/O Understanding

- Block and DMA (Direct Memory Access) Typically Address a Base and Initiate a Transfer of Many Bytes with Auto-increment
 - A. TRUE
 - B. FALSE
- Plug and Play Requires a Well-Known Configuration Space and Allows a Bus Master to Negotiate MMIO, Interrupts and General Resources Used for Each Device
 - A. TRUE
 - B. FALSE
- All Bus Transactions Require the Bus to Be HELD Until Data Transfers are Complete on the PCI Express Bus
 - A. TRUE
 - B. FALSE

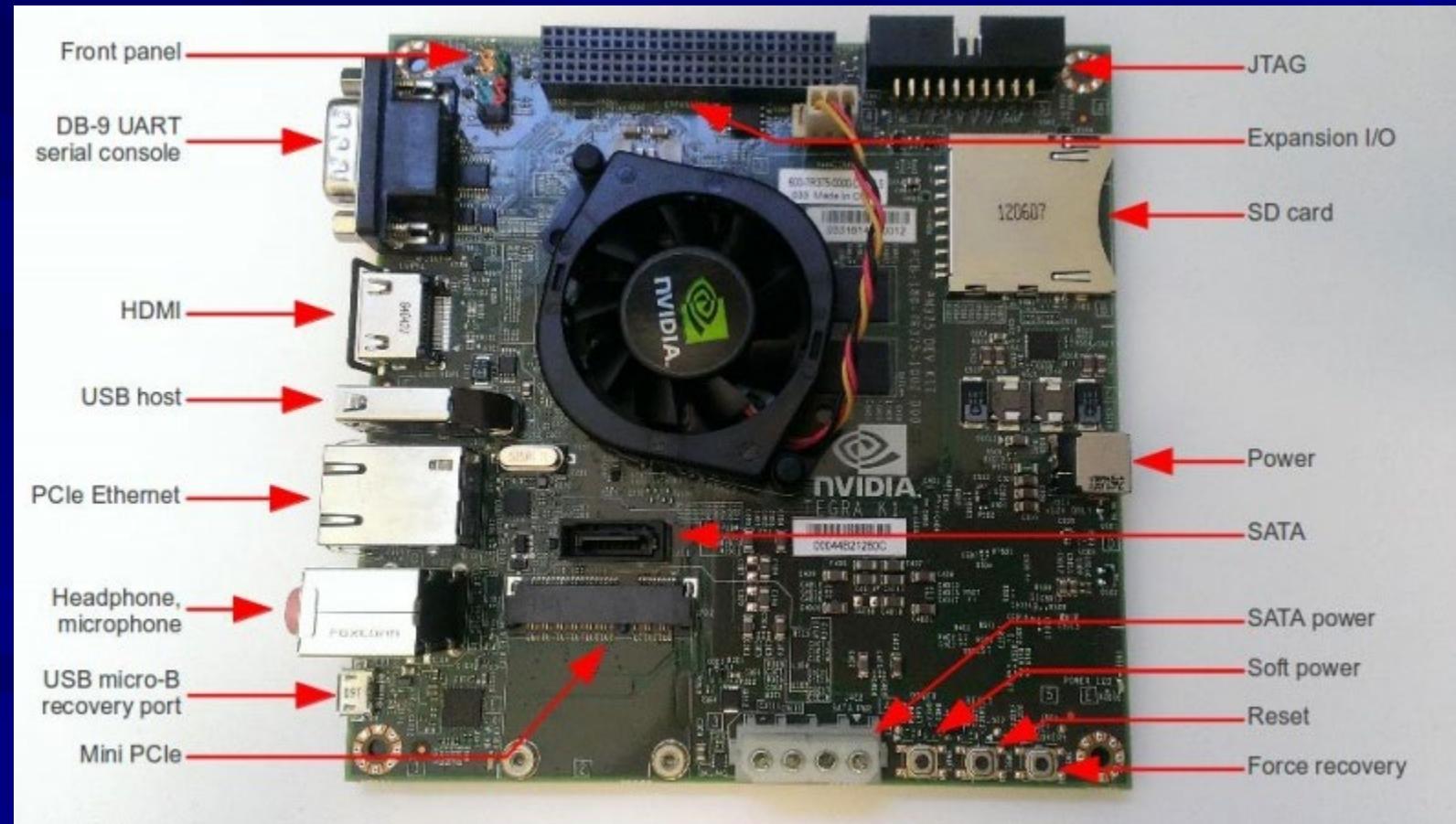
Single Board Computer SoCs

- SBC = Single Board Computer (Instead of Backplane)
- For RT Systems 4 Boards are Use for High Rate I/O (with Co-Processing)
 - Jetson TK-1 – Multi-Core CPU + GPU Co-Processor
 - Jetson Nano - Multi-Core CPU + GPU Co-Processor
 - DE1-SoC – Multi-Core CPU + FPGA Co-Processor
 - Raspberry Pi 3 or 4 with Multi-Core CPU + GPU Co-Processor
- For Low Rate, Texas Instruments Tiva TM4C is also an Option
- SBCs are Less Scalable than a CPCI or VXS/VXI Backplane, But SoC Packs Multiple Cores and I/O onto a Single Chip!

Embedded SBC I/O Devices - Jetson TK1

■ CPU+GPU

- NVIDIA "4-Plus-1" 2.32GHz ARM quad-core Cortex-A15
- NVIDIA Kepler "GK20a" GPU with 192 SM3.2 CUDA cores (upto 326 GFLOPS)



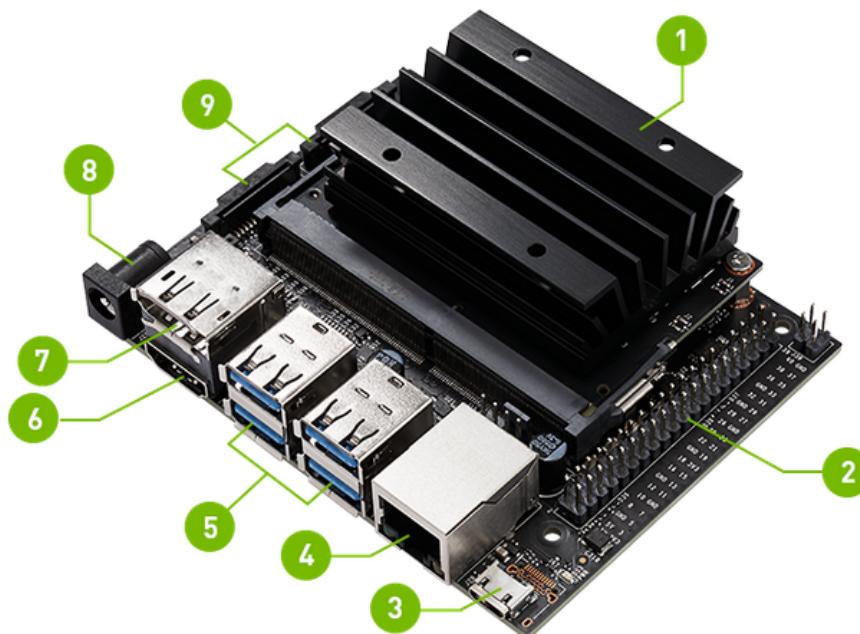
Embedded SBC I/O Devices - Jetson Nano

■ CPU+GPU

- NVIDIA 1.43 GHz ARM quad-core Cortex-A57
- NVIDIA Maxwell GPU with 128 CUDA cores (upto 326 GFLOPS)

The Jetson Nano Developer Kit includes an expansive variety of ports and connectors, making it the ideal way to get started with your AI journey.

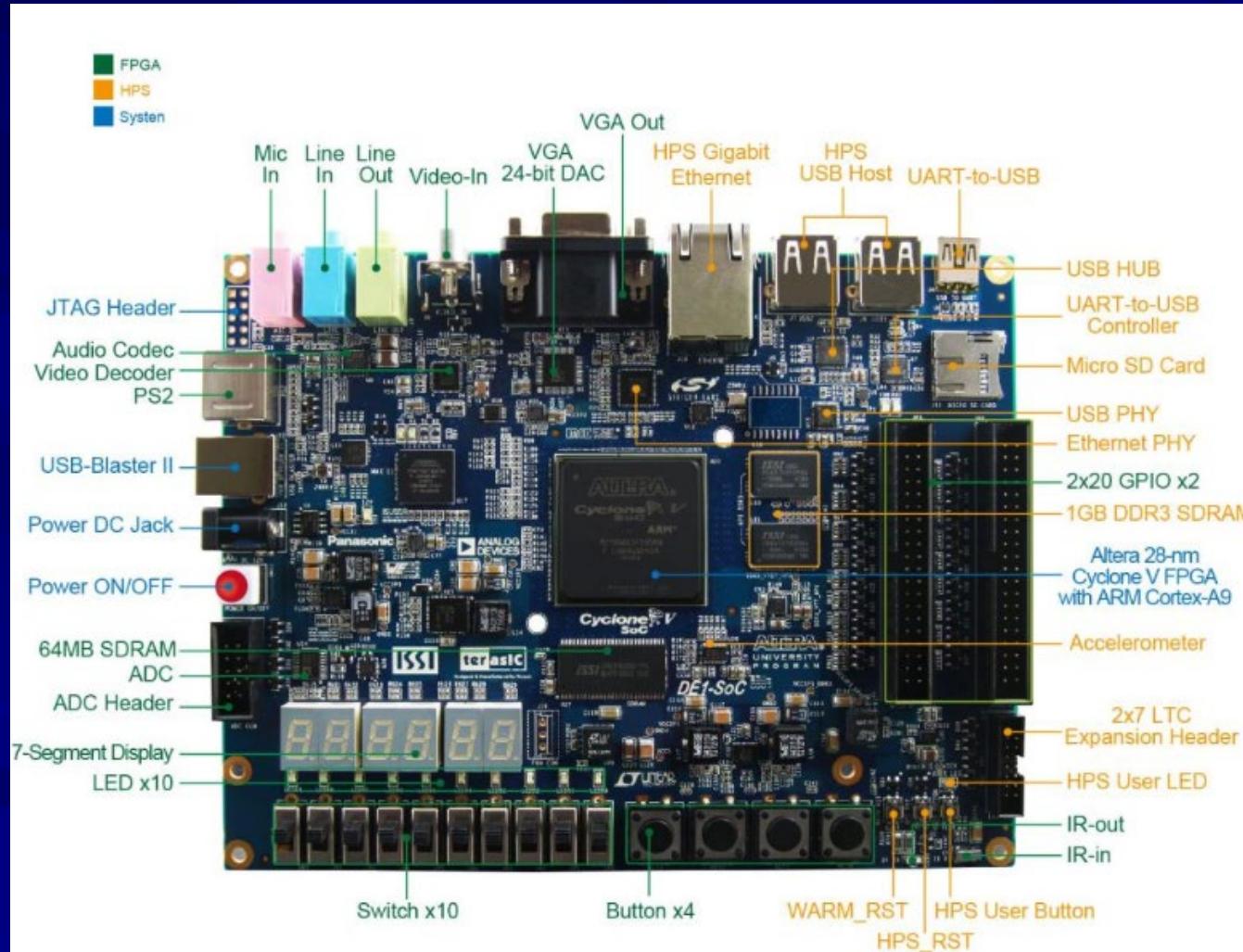
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- ① microSD card slot for main storage
- ② 40-pin expansion header
- ③ Micro-USB port for 5V power input or for data
- ④ Gigabit Ethernet port
- ⑤ USB 3.0 ports (x4)
- ⑥ HDMI output port
- ⑦ DisplayPort connector
- ⑧ DC Barrel jack for 5V power input
- ⑨ MIPI CSI camera connector (x2)

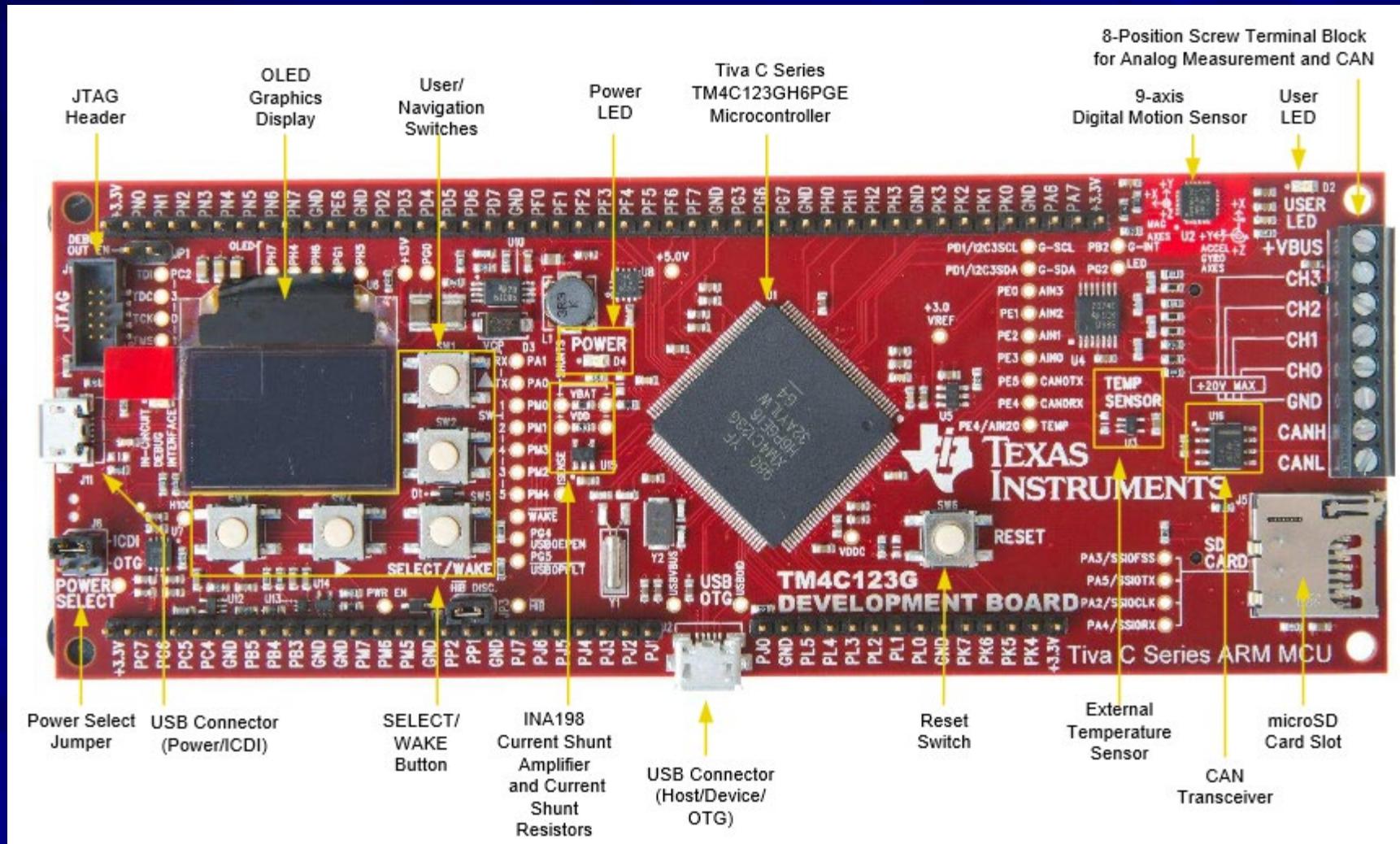
Embedded SBC I/O Devices – DE1-SoC

- Reconfigurable SoC with FPGA Co-processing
- Dual-Core ARM Cortex A9, Linux or FreeRTOS



Embedded SBC I/O Devices – TM4C123G

- ARM Cortex M4 Microcontroller, IAR IDE, Cyclic Executive or FreeRTOS



Processor Trends

- Yesterday's Board, Today's Chipset, Tomorrow's ASIC
- System on a Chip - SoC
 - Core(s) + IO (PowerPC 8xx, 82xx)
 - Reconfigurable (Virtex II)
 - Configurable (Tensilica)
 - IP Modules (CPU Cores, Memory Controller, Local Bus)
- Offloading to HW (Today's SW is Tomorrow's HW)
- Multi-Core SoCs
 - Cache Coherency – e.g. MOESI
 - Messaging
 - Shared Memory
 - Asymmetric MP
 - SMP
 - NUMA
 - DPDR (Dual-Ported RAM)

Open Discussion

- Thoughts on I/O Trends?
- Thoughts on Processors and SoC?
- Thoughts on Impact to RT Embedded Systems!