

ECEN 5623

Harmonic LCM Cheddar

What is the LCM of 2, 10, 15?

- A. 300
- B. 150
- C. 10
- D. 15
- E. 30

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Text **TIMSCHERR391** to **37607** once to join

What is the LCM of 2, 10, 15?

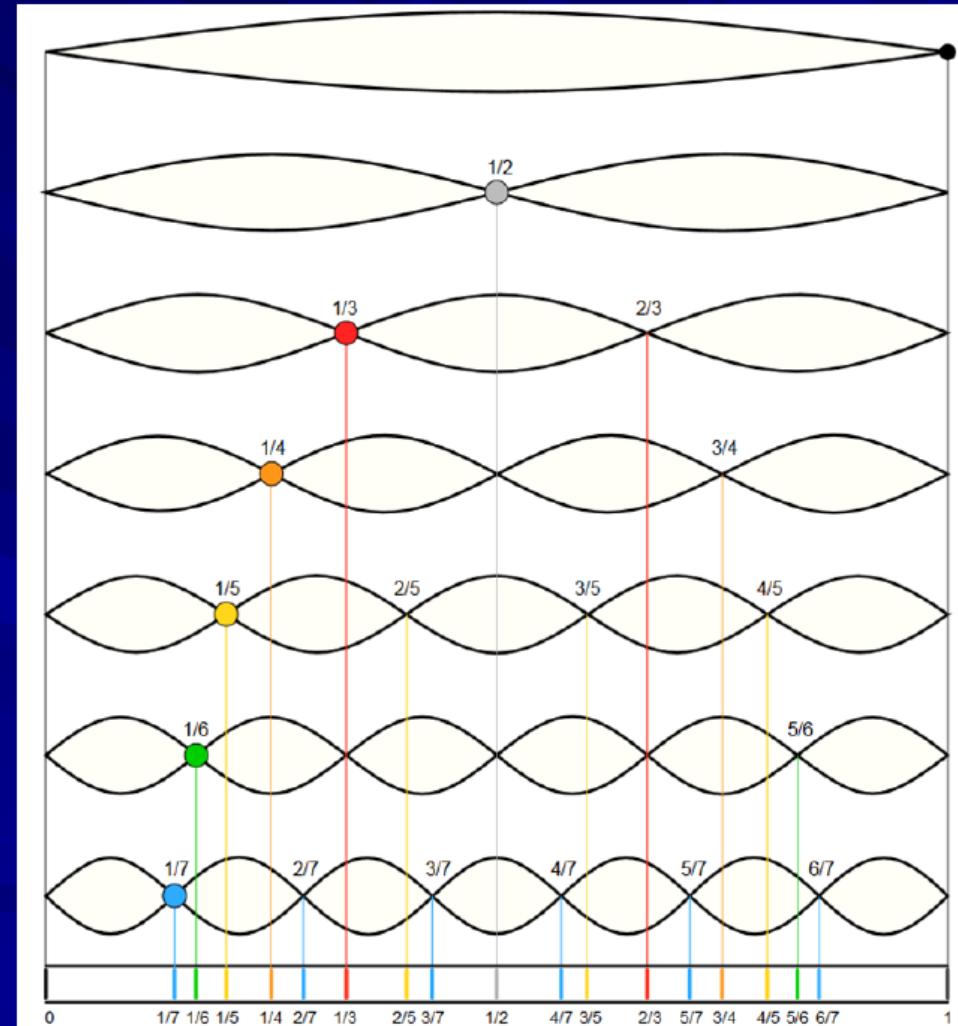
- A 300
- B 150
- C 10
- D 15
- E 30

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Harmonics

- Smallest f is largest T
- All other f 's (T 's) must be such that they are a multiple of the smallest f , f_0
- f_0 = fundamental
 - 1st harmonic is $1 \times f_0$
 - 2nd harmonic is $2 \times f_0$
 - Nth harmonic is $N \times f_0$
- Add f_0 to get any next harmonic



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<https://en.wikipedia.org/wiki/Harmonic>

4

Question

- If Services are Harmonic, then does this mean that $\text{LCM}(T_1 \dots T_n) = \text{Longest}(T_1 \dots T_n)$?
- Harmonic Services mean that all $f_n (1/T_n), f_1 \dots f_n$ are multiples of f_0 (fundamental), smallest f
 - Common mistake – T's that are multiples of smallest T are not always harmonic
 - Check T's by converting to f, determine if all f are $\sum f_0$, not just any multiple, but a whole multiple

Example 9		harmonic f ₀ multiple								LCM/T
f ₃	0.166667	4	T ₁	6	C ₁	1	U ₁	0.166667	LCM = 24	4
f ₂	0.125	3	T ₂	8	C ₂	2	U ₂	0.25		3
f ₁	0.083333	2	T ₃	12	C ₃	4	U ₃	0.333333		2
f ₀	0.041667	1	T ₄	24	C ₄	6	U ₄	0.25	U _{tot} = 1	1

Example 9		harmonic f ₀ multiple								LCM/T
f ₃	0.133333	4	T ₁	7.5	C ₁	1	U ₁	0.133333	LCM = 210	28
f ₂	0.1	3	T ₂	10	C ₂	2	U ₂	0.2		21
f ₁	0.066667	2	T ₃	15	C ₃	4	U ₃	0.266667		14
f ₀	0.033333	1	T ₄	30	C ₄	6	U ₄	0.2	U _{tot} = 0.8	7

Example 9		harmonic f ₀ multiple								LCM/T
f ₃	0.111111	4	T ₁	9	C ₁	1	U ₁	0.111111	LCM = 36	4
f ₂	0.083333	3	T ₂	12	C ₂	2	U ₂	0.166667		3
f ₁	0.055556	2	T ₃	18	C ₃	4	U ₃	0.222222		2
f ₀	0.027778	1	T ₄	36	C ₄	6	U ₄	0.166667	U _{tot} = 0.666667	1

So, Two Simple Examples

■ Harmonic Services S_1, S_2, S_3 with

$T_1=3, f_1=1/3 = 5 \times f_3$ (f_3 is the fundamental a.k.a f_0)

$T_2=5, f_2=1/5 = 3 \times f_3$

$T_3=15, f_3=1/15 = f_3$ is the smallest (lowest frequency)

■ NOT Harmonic

$T_1=4, f_1=1/4 = 5 \times f_3$ (f_3 is the fundamental here)

$T_2=8, f_2=1/8 = 2/3 \times f_3$

$T_3=12, f_3=1/12 = f_3$ is the smallest (lowest frequency)

■ Check with S are harmonic by comparing all f

- Multiples of smallest T , not a good check [common mistake]
- LCM / T should reveal harmonics, factors of largest T
- Or $T_n/2, T_n/3, T_n/4, \dots$



Using Cheddar

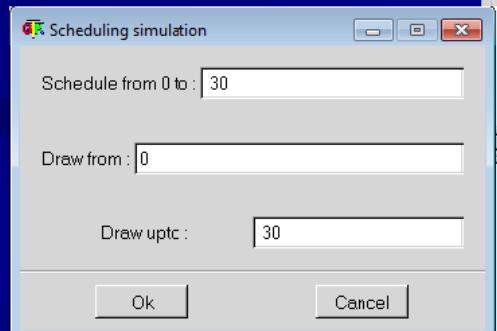
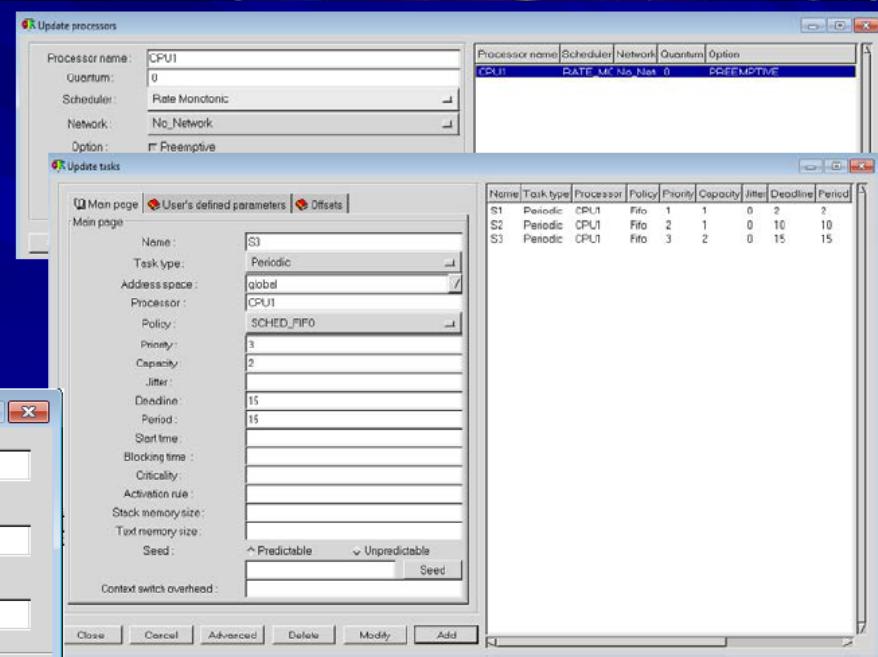
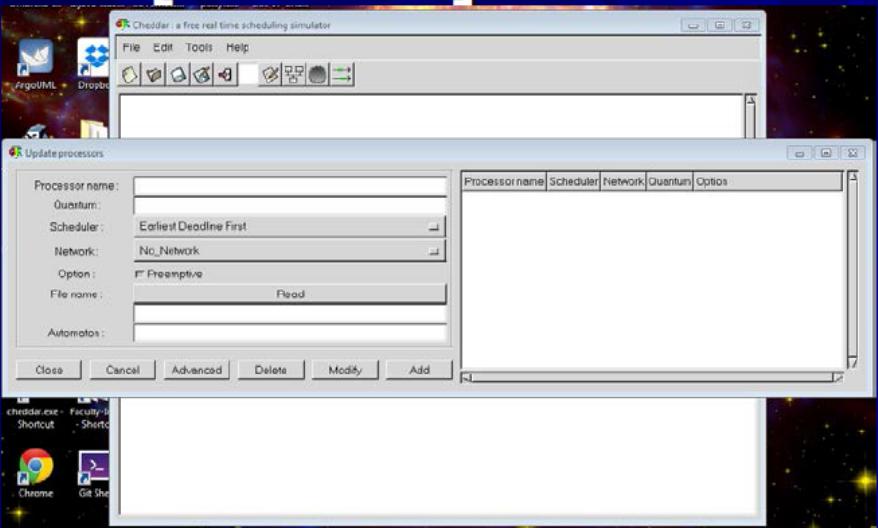


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Using Cheddar [Basics]

- Download for Windows
[\[here\]](#)
- Use “Edit” to Start
- Start with Update Processors
- Add it
- Update Address Spaces,
Add it
- Update Tasks, Add $S_1 \dots S_n$
- Note Cheddar Runs over
LCM





Versions of the Tool

Cheddar 2.0 for Windows

Cheddar 2.1 for Windows (tested for these slides)

Cheddar 3.0 for Windows

Cheddar 3.0 for Linux (Bugs reported by students)

Cheddar 3.1 for Windows (new! Untested)

Cheddar 3.1 for Linux (new! Untested)

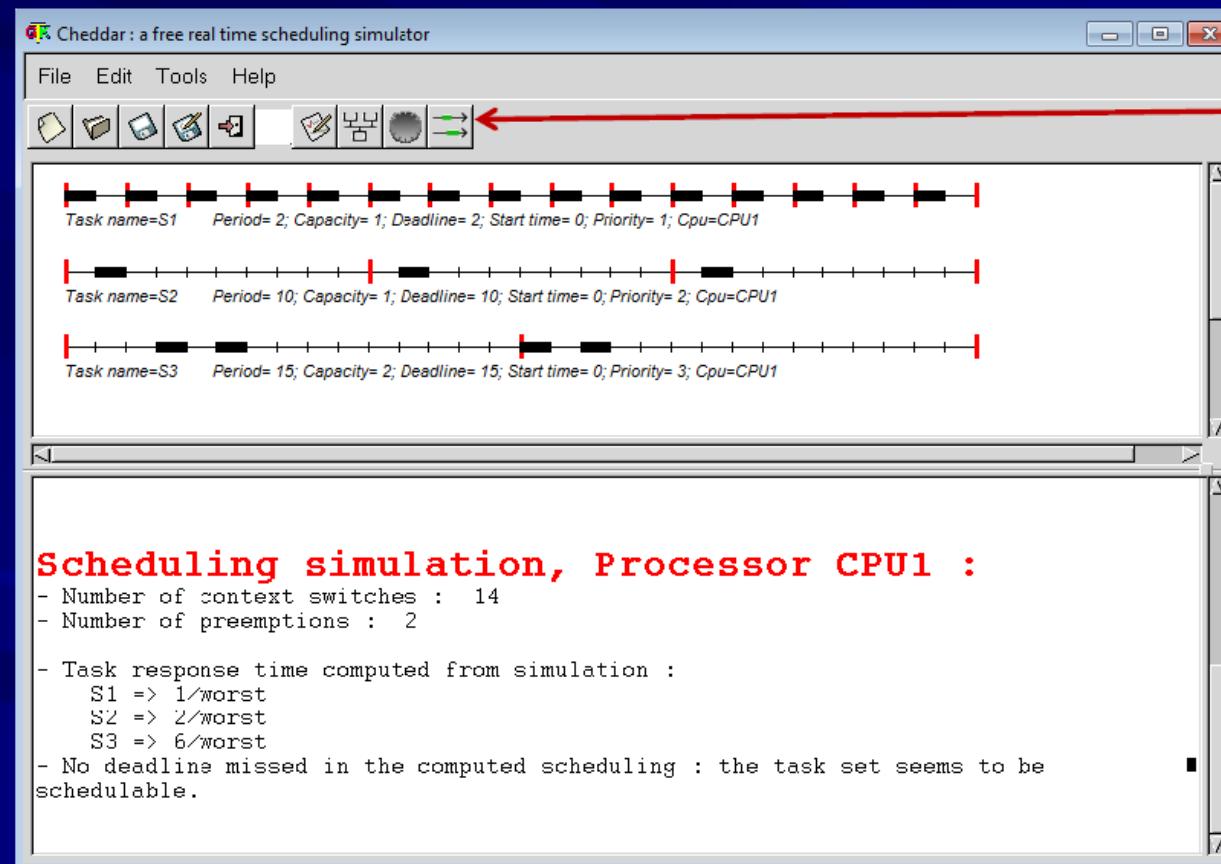
<http://beru.univ-brest.fr/cheddar/> ,

<http://beru.univ-brest.fr/svn/CEDDAR/trunk/releases/>



Simulation

- Hit Simulation button to Start
- Calculates LCM, Runs, Produces Timing Diagram and Summary



Simulation Button

Timing Diagram

Summary – Note the conclusion “seems”

Feasibility Test

- Hit Feasibility button to Test
- For RM Policy, Cheddar Uses the RM LUB
- For All Policies, Cheddar Provides Worst-Case Analysis

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

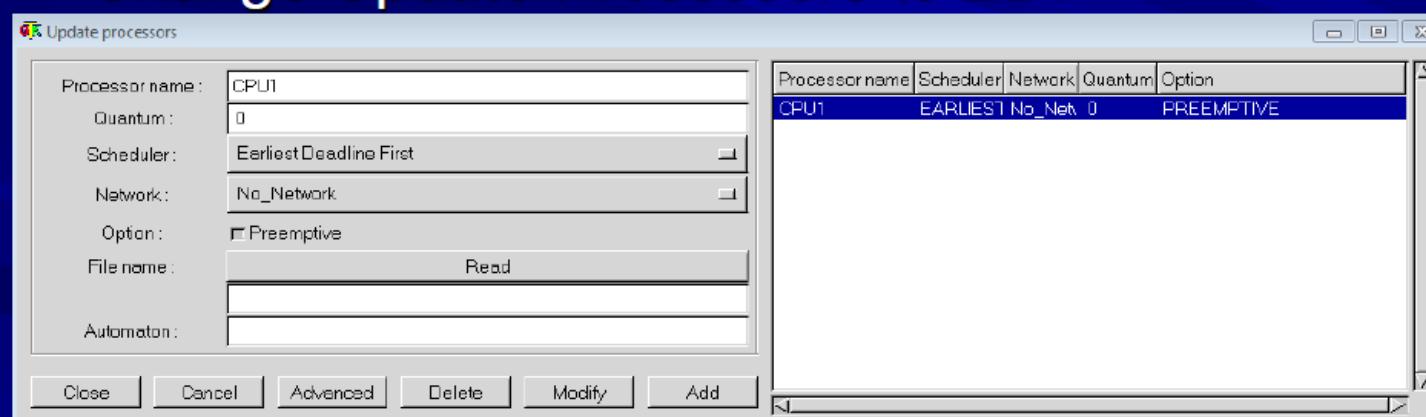
- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with RM, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 0.77976 (see [1], page 16, theorem 8).

RM Policy Example

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
S3 => 6
S2 => 2
S1 => 1
- All task deadlines will be met : the task set is schedulable.

- Change Update Processors to EDF



Run Again with EDF to Compare

- Priorities are Dynamic, So Just Change Processor Scheduler Policy, Re-Run Simulation and Feasibility

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
 - S1 => 1
 - S2 => 8
 - S3 => 13
- All task deadlines will be met : the task set is schedulable.

Note EDF

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 1.00000 (see [7]).

2) Feasibility test based on worst case task response time :

- Bound on task response time :
 - S1 => 1
 - S2 => 8
 - S3 => 13
- All task deadlines will be met : the task set is schedulable.

Note LLF

Example-0 Timing Diagram

- RM, EDF, LLF Succeed, 73.33% CPU Utilization

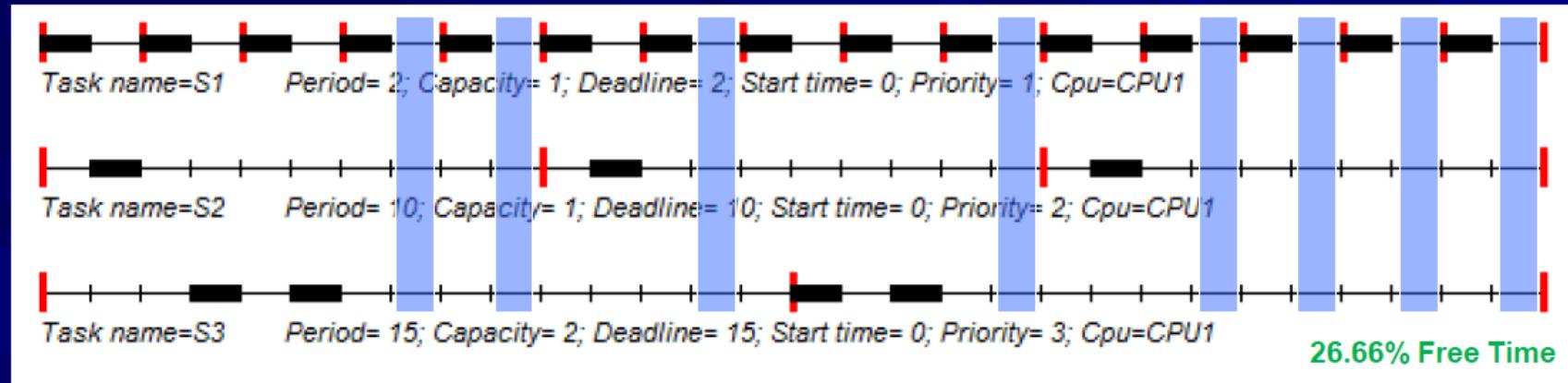
Example 0	T1	2	C1	1	U1	0.5	LCM =	30
	T2	10	C2	1	U2	0.1		
	T3	15	C3	2	U3	0.133	Utot =	0.733
RM Schedule	1	2	3	4	5	6	7	8
S1								
S2								
S3								
EDF Schedule								
S1								
S2								
S3								
TTD								
S1	2	X	2	X	2	X	2	X
S2	10	9	X	X	X	X	X	X
S3	15	14	13	12	11	10	X	X

Scheduling simulation, Processor CPU1 :

- Number of context switches : 14
 - Number of preemptions : 2
 - Task response time computed from simulation :
 - S1 => 1/worst
 - S2 => 2/worst
 - S3 => 6/worst
 - No deadline missed in the computed scheduling : the task set seems to be schedulable.

Example-0 Cheddar RTSS

■ Download Cheddar RT Analyzer, Example-0 XML



Scheduling feasibility, Processor CPU1 :

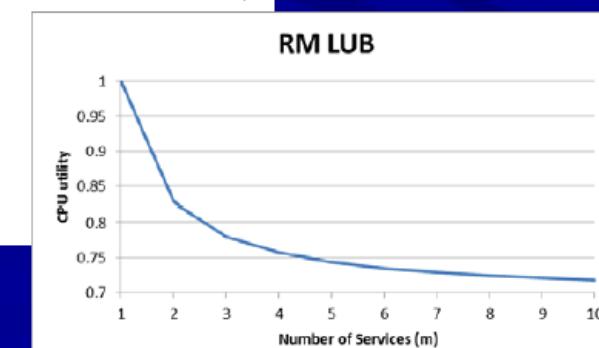
1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with RM, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 0.77976 (see [1], page 16, theorem 8).

$$U = \sum_{i=1}^m (C_i / T_i) \leq m(2^{\frac{1}{m}} - 1)$$

2) Feasibility test based on worst case task response time :

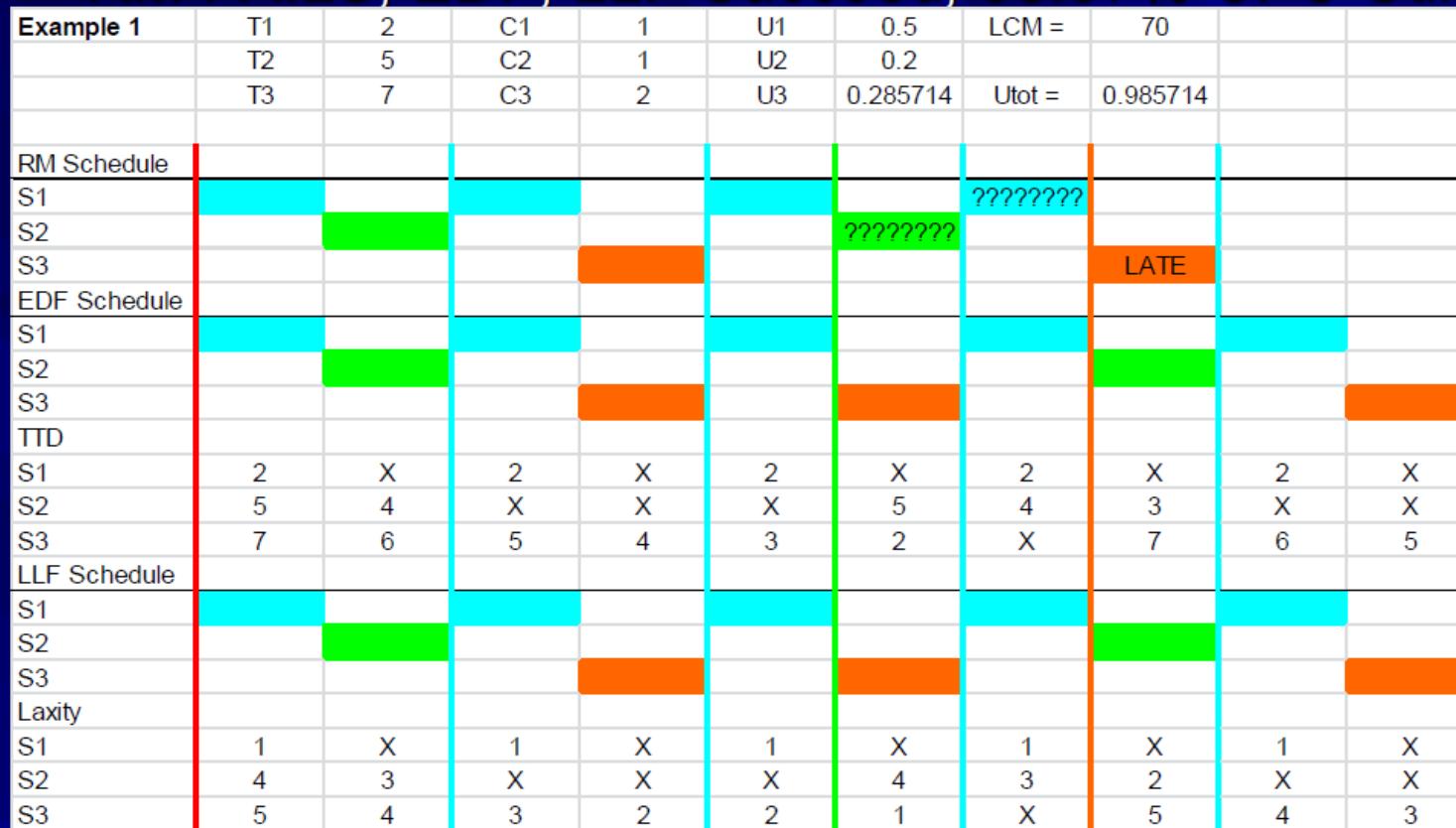
- Bound on task response time : (see [2], page 3, equation 4).
 - S3 => 6
 - S2 => 2
 - S1 => 1
- All task deadlines will be met : the task set is schedulable.



Cheddar Simulates over LCM (Hyperperiod)

Example-1 Timing Diagram

■ RM FAILS, EDF, LLF Succeed, 98.57% CPU Utilization



Scheduling simulation, Processor CPU1 :

- Number of context switches : 68
- Number of preemptions : 10
- Task response time computed from simulation :
 - S1 => 1/worst
 - S2 => 2/worst
 - S3 => 8/worst , missed its deadline (deadline = 7 ; completion time = 8)
- Some task deadlines will be missed : the task set is not schedulable.

Example-1 Cheddar RTSS

■ RM Not Feasible by LUB or by Inspection over LCM

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 70 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.98571 (see [1], page 6).
- Processor utilization factor with period is 0.98571 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable is more than 0.77976 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
 $S_3 \Rightarrow 8$, missed its deadline (deadline = 7)
 $S_2 \Rightarrow 2$
 $S_1 \Rightarrow 1$
- Some task deadlines will be missed : the task set is not schedulable.

■ EDF?

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

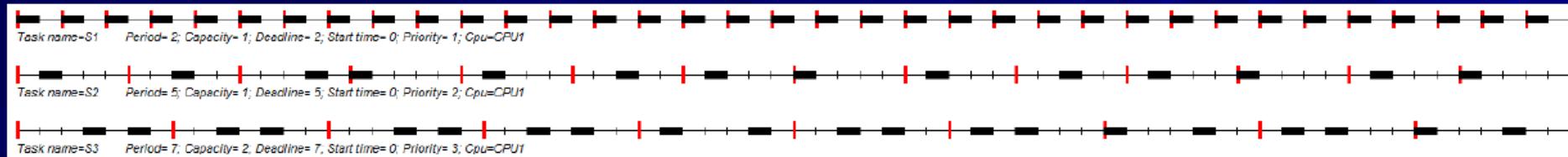
- The base period is 70 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.98571 (see [1], page 6).
- Processor utilization factor with period is 0.98571 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.98571 is equal or less 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

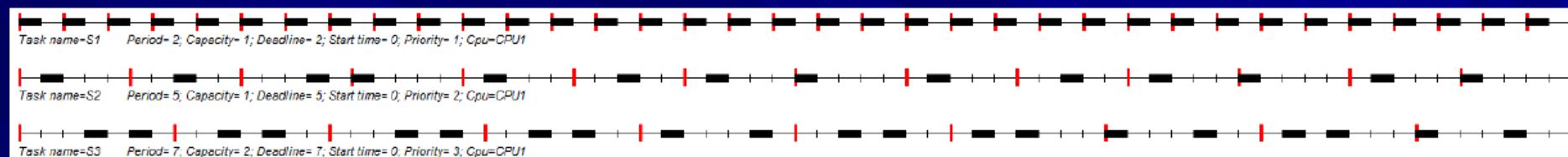
- Bound on task response time :
 $S_1 \Rightarrow 1$
 $S_2 \Rightarrow 4$
 $S_3 \Rightarrow 6$
- All task deadlines will be met : the task set is schedulable.

Example-1 Cheddar RTSS

■ EDF Simulation over LCM of 70



■ LLF Simulation over LCM of 70

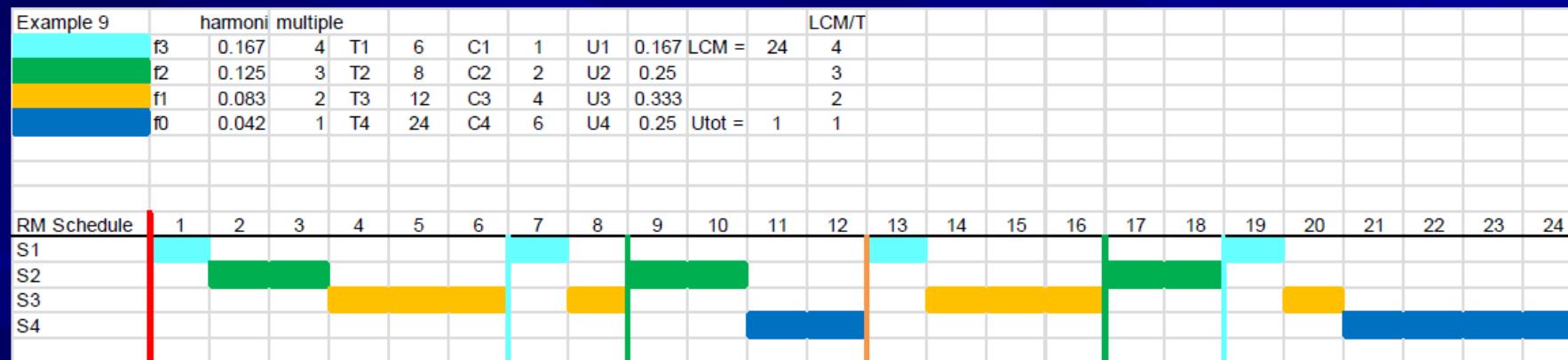


■ Worst Case Feasibility Test

- Fixed Priority (RM Policy) FAILS LUB and WC Feasibility Test (Scheduling Point or Completion Test)
- Dynamic Priority Succeeds by Two Methods

Example 9 – RM Policy

- Harmonic Services with 100% CPU Utilization
- Preemptions – 3 in Total:
 - @6 S1 preempts S3
 - @12 S1 preempts S4
 - @16 S2 preempts S3



Example 9 – Cheddar RM WC Analysis and Simulation

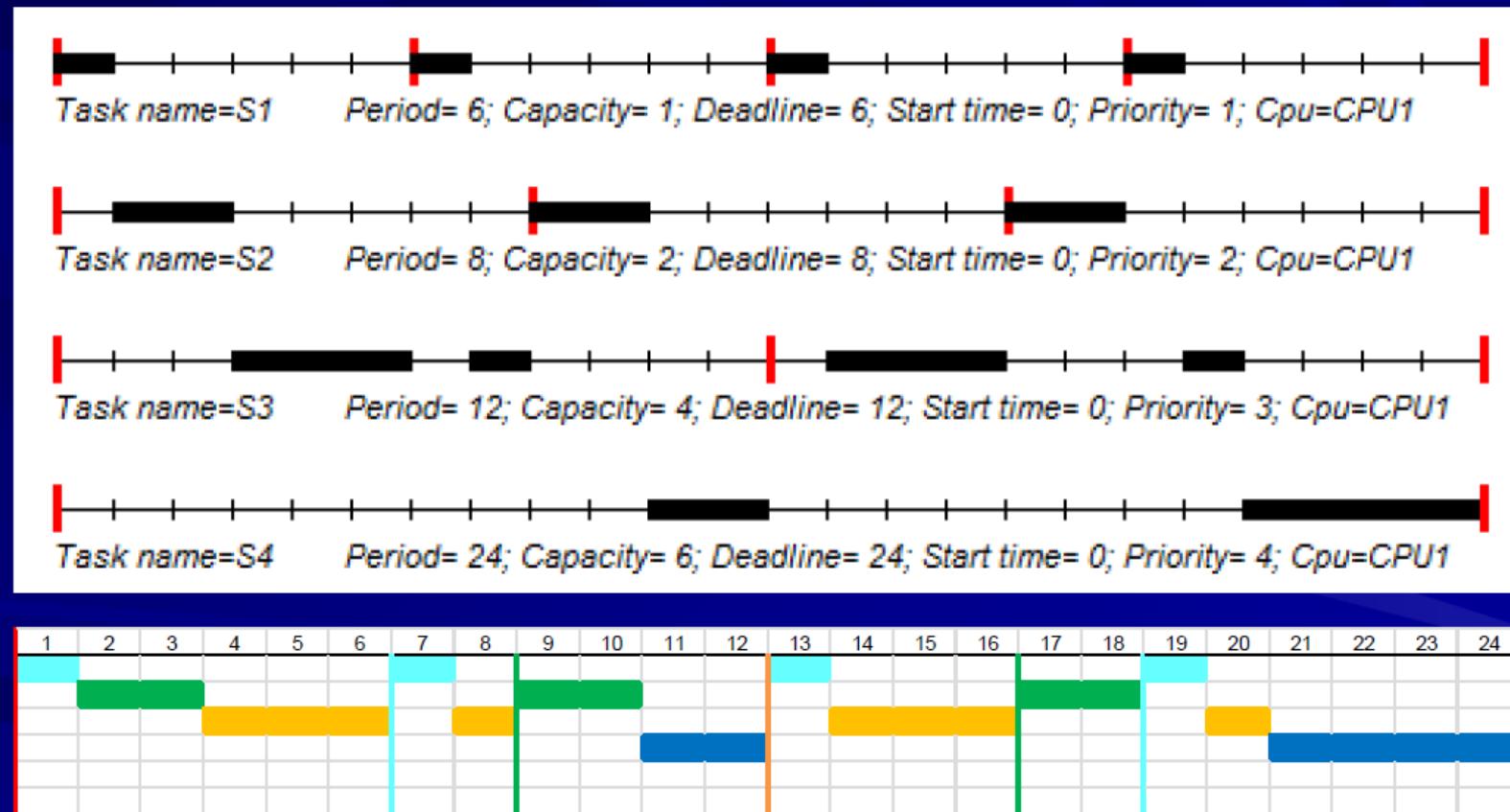


- Run WC analysis
- Run Simulation to Graph over Longest T or LCM



Example 9 – RM Simulation

- Automates Hand Simulation
- Simpler Modification for Multiple CPUs, Policies, etc.



Example 9 – EDF Simulation

- No Difference from RM in Simulation
- Ties Could Be Broken Randomly [Most Often Favor Highest Frequency – Same as RM]
- Worst-Case Analysis However Shows “task set is schedulable”

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 24 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

- Bound on task response time :

S1 => 6
 S2 => 8
 S3 => 12
 S4 => 24

- All task deadlines will be met : the task set is schedulable.

TTD metric for dispatch results in “ties”, noted in red

EDF Schedule																									
		S1	S2	S3	S4																				
TTD		6	X	X	X	X	X	6	X	X	X	X	6	X	X	X	X	6	X	X	X	X	X	X	X
		8	7	6	9	8	7	6	5	8	7	10	9	12	11	10	9	8	7	6	5	4	3	2	1
		12	11	10	9	8	7	6	5	10	9	8	7	12	11	10	9	8	7	6	5	4	3	2	1
		24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Feasibility Test Methods and Tools

I. Hand-drawn System Timing Diagrams

Works for all Scheduling Policies, Proves Feasibility over LCM

Can be done in Excel to help with calculations and make neat

II. Cheddar

Fastest way to Create Diagrams and run Feasibility Tests

III. Custom Code

RM – RM Lub, Scheduling Point test and Completion test as given in the example code

EDF & LLF – Feasible if Utility ≤ 1.0 , or if no deadlines missed over LCM (actually over longest service period)

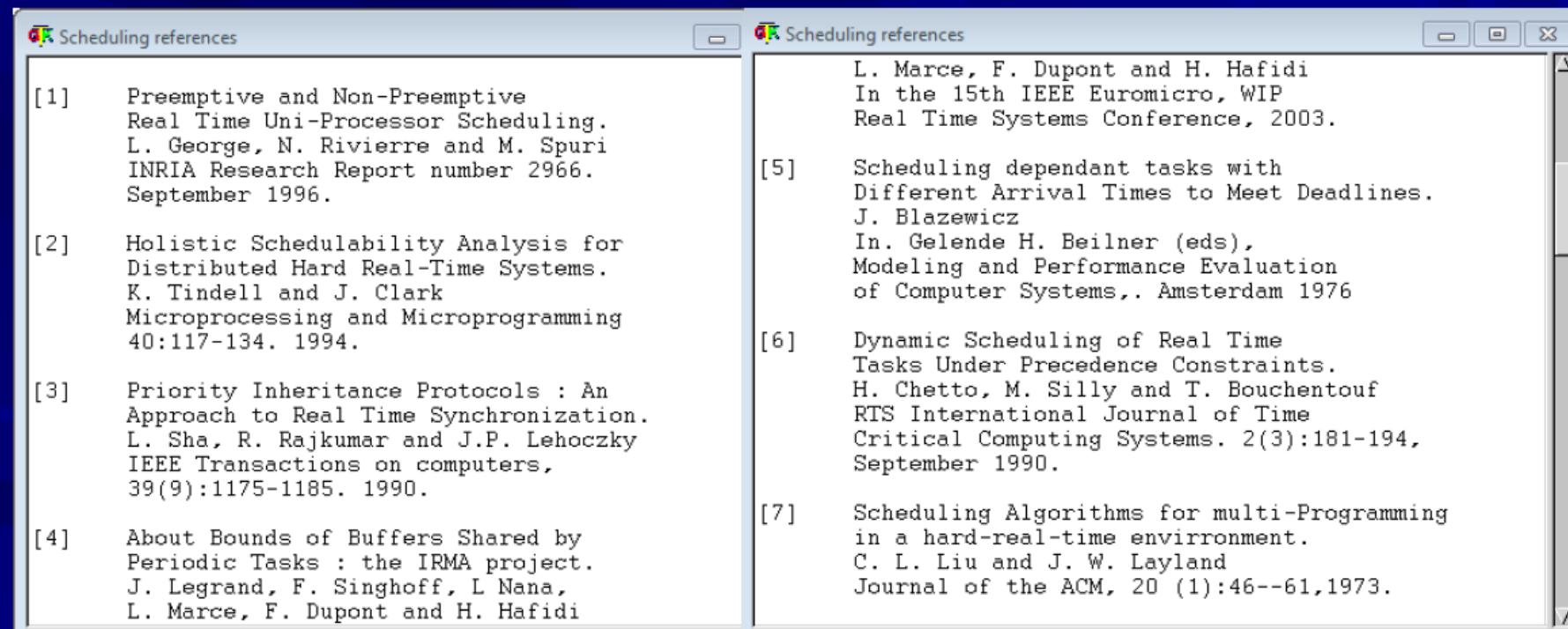
DM – Burns-Audsley Test or if no deadlines missed over LCM

Review Remaining Examples

- [http://mercury.pr.erau.edu/~siewerts/cec450/documents/Timing Diagrams Updated 2020/](http://mercury.pr.erau.edu/~siewerts/cec450/documents/Timing%20Diagrams%20Updated%202020/)
- As noted in Liu and Layland, Static Priority Policy may not be feasible in cases where Dynamic Priority Policy is
 - Are Feasibility and Safety Synonymous?
 - Is it wise to have Zero Margin?
 - Have we accounted for Context Switch Overhead and ISR Latency?

Cheddar References

- Help, Scheduling References
- References Used to Build Cheddar – [Here](#)
- General References - [Here](#)





Scheduling References

- [1] Preemptive and Non-Preemptive Real Time Uni-Processor Scheduling. L. George, N. Rivierre and M. Spuri. INRIA Research Report number 2966. September 1996.
- [2] Holistic Schedulability Analysis for Distributed Hard Real-Time Systems. K. Tindell and J. Clark. Microprocessing and Microprogramming 40:117-134. 1994.
- [3] Priority Inheritance Protocols : An Approach to Real Time Synchronization. L. Sha, R. Rajkumar and J.P. Lehoczky. IEEE Transactions on computers, 39(9):1175-1185. 1990.
- [4] About Bounds of Buffers Shared by Periodic Tasks : the IRMA project. J. Legrand, F. Singhoff, L Nana, L. Marce, F. Dupont and H. Hafidi. In the 15th IEEE Euromicro, WIP Real Time Systems Conference, 2003.
- [5] Scheduling dependant tasks with Different Arrival Times to Meet Deadlines J. Blazewicz. In. Gelende H. Beilner (eds), Modeling and Performance Evaluation of Computer Systems. Amsterdam 1976
- [6] Dynamic Scheduling of Real Time Tasks Under Precedence Constraints. H. Chetto, M. Silly and T. Bouchentouf. RTS International Journal of Time Critical Computing Systems. 2(3):181-194, September 1990.
- [7] Scheduling Algorithms for multi-Programming in a hard-real-time environment. C. L. Liu and J. W. Layland. Journal of the ACM, 20 (1):46--61,1973.
- [8] On non preemptive Scheduling of periodic and Sporadic Tasks K. Jeffay, D. Stanat, C. Martel. in Proc. Of IEEE Real Time Systems Symposium San Antonio, Texas, December 1991
- [9] Assigning Real-Time Tasks to Homogeneous Multiprocessor Systems . A. Burchard, Y. Oh. Liebeherr, and S. H. Son Technical Report CS-94-01, University of Virginia, 1994, Department of Computer Science.
- [10] Tight Performance Bounds of Heuristics for a Real-Time Scheduling Problem. Y. Oh and S. H. Son. Technical Report CS93-24, University of Virginia, 1993, Department of Computer Science.
- [11] Performance Analysis of Buffers Shared by Independent Periodic Tasks. J. Legrand, F. Singhoff, L Nana and L. Marce LISyC Technical report number legrand-02-2004 University of Brest, 2005, Department of Computer Science.
- [12] Queueing systems. Volume I : Theory L. Kleinrock. A Wiley interscience publication.
- [13] Analyse de tampons partages par des taches periodiques et independantes. J. Legrand, F. Singhoff, L Nana and L. Marce. LISyC Technical report number legrand-01-2005 University of Brest, 2005, Department of Computer Science.
- [14] Extending Rate Monotonic Analysis when Tasks Share Buffers. F. Singhoff, J. Legrand, L Nana and L. Marce. In the DAta Systems in Aerospace conference (DASIA'2004), ESA Publication Division - Nice (France), 2004.
- [15] Cheddar : a Flexible Real Time Scheduling Framework. F. Singhoff, J. Legrand, L Nana and L. Marce

