

# 6EDL7141



## Datasheet

### Product Feature Summary

- **3 phase smart gate driver**
  - 5.5 V to 60 V operating supply voltage (recommended operating condition)
  - 1.5 A sink/ 1.5 A source peak gate driver currents
  - Programmable driving voltage (7 V, 10 V, 12 V, 15 V)
  - Independently programmable high side/low side slew rate control
  - Independently programmable dead time for turn on/off switching
  - Control using 3PWM or 6PWM inputs up to 200 kHz
  - Built-in commutation tables for using 1PWM with or without Hall sensors
- **Integrated power supplies**
  - High efficiency synchronous buck converter with programmable switching frequency. Supplies gate driver charge pumps, DVDD linear regulator and both internal and external components
  - Linear regulator with 300 mA current capability for MCU and other components supply (DVDD)
  - Dual charge pump for supplying gate driver even at low supply voltage
- **Three integrated current sense amplifiers**
  - Adjustable gain and offset
  - Configurable low side  $R_{DSON}$  sensing
- Three integrated Hall sensor comparators
- Integrated ADC for signal monitoring
- Locked rotor detection
- 3.3 V/5 V compatible digital interface
- Programmable SPI digital interface
- **Protection features:**
  - External brake with programmable braking response
  - Over-Current Protection (OCP) on current sense amplifiers (programmable)
  - Over-Current Protection (OCP) for buck converter and DVDD linear regulator (programmable)
  - Under-Voltage Lockouts (UVLO) for internal and external supplies
  - Over-Voltage Fault (OVLO) reporting for buck converter and DVDD linear regulator
  - Over-Temperature warning and shutdown (OTW, OTS)
  - Programmable watchdog timer
  - Reporting through nFAULT and SPI registers
- Thermally enhanced 48pin VQFN package

## Potential Applications

- Power tools
- Gardening tools
- 3 Phase BLDC and PMSM motors
- E-bikes
- Robotics, RC toys, consumer drones and multi-copters
- Pumps and fans

## Product Description

6EDL7141 is a gate driver IC for 3 phase BLDC or PMSM motor drive applications. It provides three half-bridge drivers, each capable of driving a high side and low side N-type MOSFET.

The gate driver is also provided with programmable dead time delays for preventing current shoot-through between HS and LS switches in normal operation.

Separate charge pumps for low and high side gate drivers support 100% duty cycle and low voltage supply operation. Supplies for the gate drivers are programmable to one of the following levels: 7 V, 10 V, 12 V or 15 V. Additionally, the slew rate of the driving signal can be programmed with fine granularity to reduce EMI emissions.

An integrated synchronous buck converter provides an efficient supply of current to the rest of the system. However, power tool systems require high precision current measurements, involving a very precise ADC reference voltage. For that purpose, **6EDL7141 uses a linear voltage regulator** (up to 300mA), powered by the buck converter to supply the MCU and other sensitive components in the system. With this advanced power supply architecture, not only the best possible signal quality is achieved, but also the power efficiency is optimized at any input and output condition.

6EDL7141 includes three current sense amplifiers for accurate current measurements that support bi-directional low side current sensing with programmable gain.  $R_{DSON}$  sensing is supported through internal connection of the phase nodes to the current sense amplifiers inputs. Temperature compensation if needed shall be provided by the user application. Outputs of current sense amplifiers support both 3.3V and 5V allowing most commercial controllers to be compatible. Low noise, low settling times and high accuracy are the main features of the integrated operational amplifiers. An internal buffer can be used to offset the sense amplifier outputs for optimizing the dynamic range.

The device provides numerous protection features for improving application robustness during adverse conditions like monitoring of power supply voltages as well as system parameters. The failure behavior, threshold voltages and filter times of the supervisions of the device are adjustable via SPI. Monitored aspects include inverter currents, gate drive voltages and currents, device temperature, and rotor locked. When a fault occurs, the device stops driving and pulls nFAULT pin low, in order to prevent system damage or other possible malfunction. This signal can be connected to a microcontroller to inform the processor that a fault has happened. The microcontroller can request more information on the fault via SPI commands.

The integrated SPI interface can be used to configure 6EDL7141 for the application. The SPI provides both detailed fault reporting and flexible parameter settings such as gain of the current sense amplifiers, slew rate control of the gate drivers, various protection features or gate driver voltage.

## System Block Diagram

Figure 1 shows a simplified system block diagram where 6EDL7141 is used as a 3-phase gate-driver in a µC-based Hall-sensored BLDC motor control system. The integrated buck regulator provides the power supply for both the microcontroller unit (MCU) and the Hall sensors in the BLDC motor.

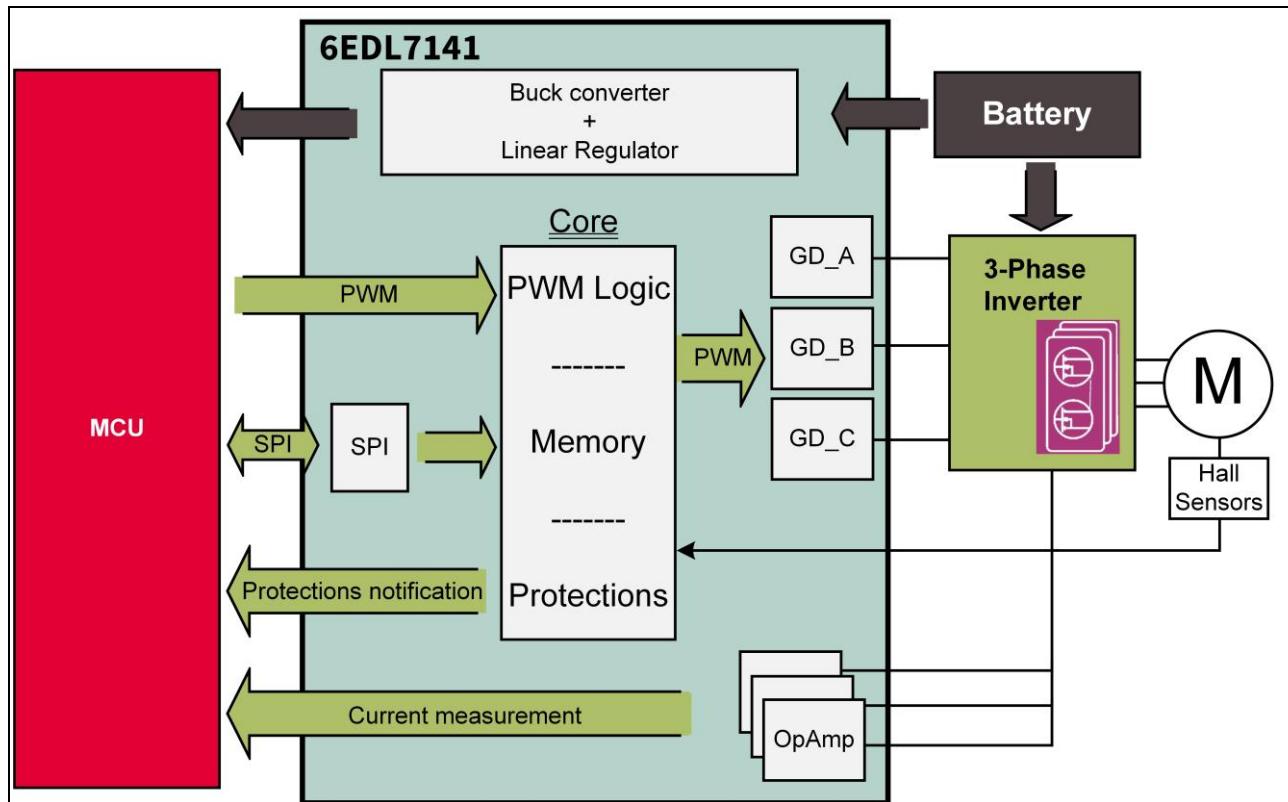


Figure 1 Simplified System Block Diagram

## Package Description

6EDL7141 is integrated in a VQFN48 7mm x 7mm package with an exposed pad. The device and package information is shown in Table 1.

Table 1 Device and package information

Part Number	Package	Body Size	Lead Pitch
6EDL7141	PG-VQFN-48-78	7.0 mm × 7.0 mm	0.5 mm

**Table of contents**

<b>Product Feature Summary .....</b>	<b>1</b>
<b>Potential Applications .....</b>	<b>2</b>
<b>Product Description .....</b>	<b>2</b>
<b>System Block Diagram .....</b>	<b>3</b>
<b>Package Description .....</b>	<b>3</b>
<b>1 Pin Configuration.....</b>	<b>7</b>
1.1 Pin Assignment.....	7
1.2 Pin Definitions and Functions.....	8
<b>2 General Product Characteristics .....</b>	<b>11</b>
2.1 Absolute Maximum Ratings .....	11
2.2 Recommended Operating Conditions.....	13
2.3 ESD Robustness.....	14
2.4 Thermal Resistance.....	14
2.5 Electrical Characteristics.....	14
2.6 Electrical Characteristic Graphs .....	25
<b>3 Product Features .....</b>	<b>32</b>
3.1 Functional Block Diagram.....	32
3.2 PWM Modes.....	33
3.2.1 PWM with 6 Independent Inputs – 6PWM.....	33
3.2.2 PWM with 3 Independent Inputs – 3PWM.....	34
3.2.3 PWM with 1 Input and Commutation Pattern – 1PWM .....	35
3.2.4 PWM with 1 Input and Commutation with Hall Sensor Inputs – 1PWM with Hall Sensors.....	38
3.2.5 PWM with 1 Input and Commutation with Hall Sensor Inputs and Alternating Recirculation – 1PWM with Hall Sensors and Alternating Recirculation .....	40
3.2.6 PWM Braking Modes.....	42
3.2.7 Dead Time Insertion.....	44
3.3 Integrated Three Phase Gate Driver .....	45
3.3.1 Gate Driver Architecture .....	45
3.3.2 Slew Rate Control.....	46
3.3.3 Gate Driver Voltage Programmability .....	50
3.4 Charge Pump Configuration .....	51
3.4.1 Charge Pump Clock Frequency Selection .....	51
3.4.2 Charge Pump Clock Spread Spectrum Feature .....	51
3.4.3 Charge Pump Pre-Charge for VCCLS .....	52
3.4.4 Charge Pump Tuning .....	52
3.4.5 Gate Driver and Charge Pumps Protections.....	52
3.5 Power Supply System .....	55
3.5.1 Synchronous Buck Converter Description .....	55
3.5.2 DVDD Linear Regulator.....	57
3.6 Current Sense Amplifiers.....	59
3.6.1 R <sub>DSON</sub> Sensing Mode vs Leg Shunt Mode.....	60
3.6.2 Current Shunt Amplifier Timing Mode.....	61
3.6.3 Current Shunt Amplifier Blanking Time .....	63
3.6.4 Current Sense Amplifier Offset Generation: Internal or External (VREF pin) .....	65
3.6.5 Overcurrent Comparators and DAC for Current Sense Amplifiers .....	65
3.6.6 Current Sense Amplifier Gain Selection .....	68
3.6.7 Current Sense Amplifier DC Calibration .....	69
3.6.8 Auto-Zero Compensation of Current Sense Amplifier .....	69

3.7	Hall Comparators .....	71
3.8	Watchdog Timers.....	71
3.8.1	Buck converter watchdog.....	72
3.8.2	General Purpose Watchdog .....	72
3.8.3	Locked-Rotor Protection Watchdog Timer .....	73
3.9	Multi-Function Pins .....	74
3.9.1	EN_DRV Pin.....	74
3.9.2	VSENSE/nBRAKE Pin .....	75
3.9.3	CS_GAIN/AZ Pin .....	75
3.10	ADC Module-Analog to Digital Converter .....	76
3.10.1	ADC Measurement Sequencing and On Demand Conversion .....	77
3.10.2	Die Temperature Sensor .....	78
<b>4</b>	<b>Device Start-Up .....</b>	<b>79</b>
4.1	Power Supply Start-Up.....	79
4.2	Gate Driver and CSAMP Start-up.....	79
<b>5</b>	<b>Device Functional States .....</b>	<b>82</b>
<b>6</b>	<b>Protections and Faults Handling.....</b>	<b>84</b>
<b>7</b>	<b>Device Programming-OTP and SPI interface .....</b>	<b>88</b>
7.1.1	OTP User Programming Procedure: Loading Custom Default Values .....	88
7.1.2	SPI Communication .....	90
<b>8</b>	<b>Register Map .....</b>	<b>92</b>
8.1	Device Programmability.....	92
8.2	Register Map .....	96
	Faults Status Register .....	96
	Temperature Status Register .....	97
	Power Supply Status Register .....	98
	Functional Status Register .....	99
	OTP Status Register .....	100
	ADC Status Register .....	101
	Charge Pumps Status Register .....	101
	Device ID Register .....	102
	Faults Clear Register .....	102
	Power Supply Configuration Register.....	103
	ADC Configuration Register .....	105
	PWM Configuration Register.....	106
	Sensor Configuration Register .....	107
	Watchdog Configuration Register .....	108
	Watchdog Configuration Register 2 .....	109
	Gate Driver Current Control Register .....	110
	Gate Driver Pre-Charge Current Control Register.....	111
	TDRIVE Source Control Register.....	113
	TDRIVE Sink Control Register .....	113
	Dead Time Register.....	114
	Charge Pump Configuration Register .....	115
	Current Sense Amplifier Configuration Register.....	116
	Current Sense Amplifier Configuration Register 2.....	118
	OTP Program Register .....	120
<b>9</b>	<b>Application Description .....</b>	<b>121</b>
9.1	Recommended External Components .....	121

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9.2	PCB Layout Recommendations .....	121
9.3	Typical Applications .....	125
<b>10</b>	<b>ESD Protection .....</b>	<b>128</b>
<b>11</b>	<b>Package Information.....</b>	<b>132</b>
<b>Revision history.....</b>		<b>134</b>

# 1 Pin Configuration

## 1.1 Pin Assignment

In Figure 2, the pinout of 6EDL7141 is presented.

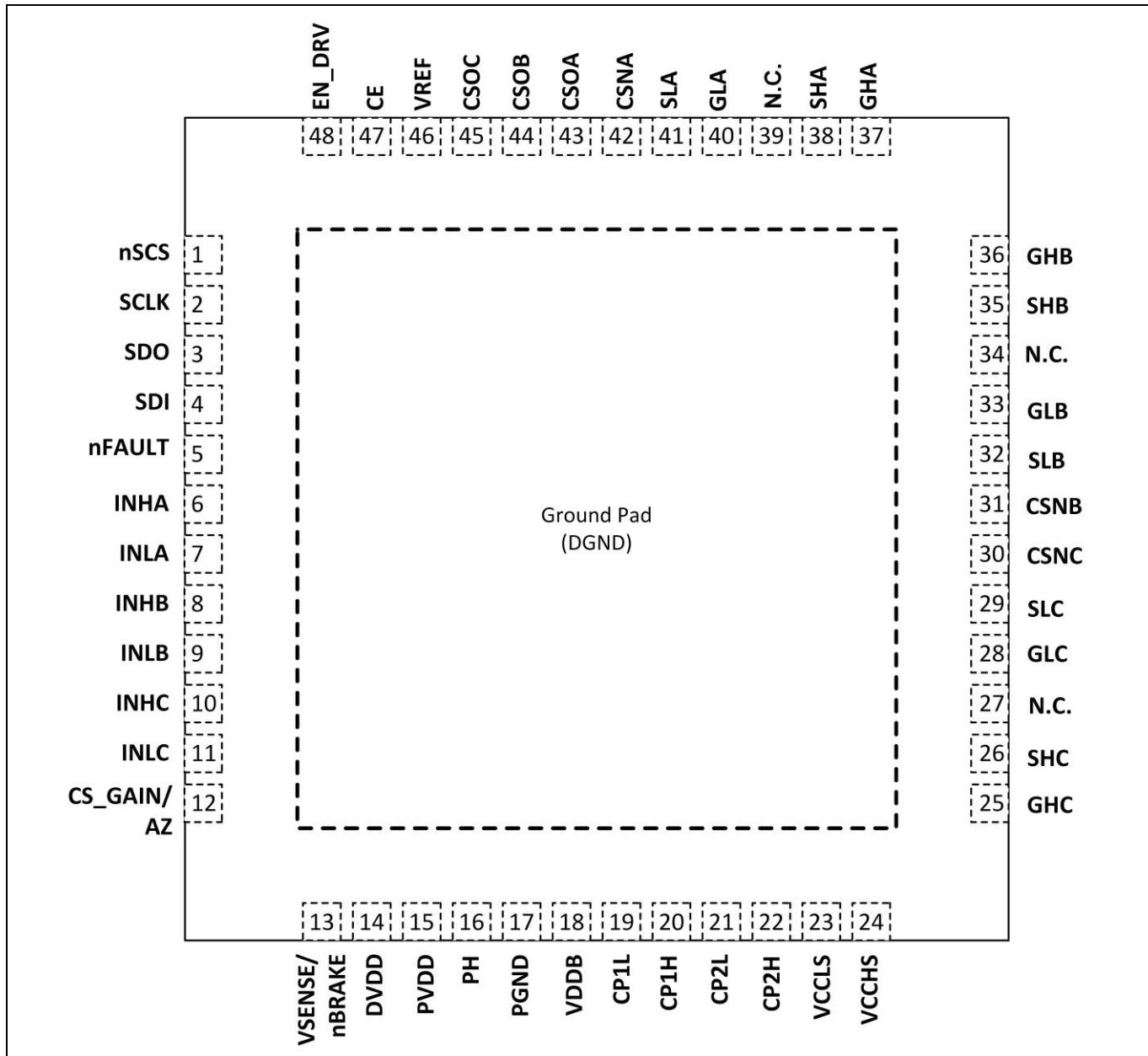


Figure 2 Pin configuration

## 1.2 Pin Definitions and Functions

Table 2 describes the different characteristics and functionalities assigned to the different pin of 6EDL7141 device.

I: Input, O: output, IO: Input and/or Output, D: Digital, A: Analog, AD: Analog and/or Digital, P: Power, G: Ground.

**Table 2 Pin definition**

Pin #	Pin Name	IO	Type	Description
1	nSCS	I	D	Chip Select for SPI. Active low
2	SCLK	I	D	SPI clock signal
3	SDO	O	D	SPI data output signal
4	SDI	I	D	SPI data input signal
5	nFAULT	O	D	When low indicates a fault has occurred; open drain; connect external pull-up to MCU power supply
6	INHA	I	D	PWM input signal for channel A high side. Common PWM signal for PWM mode 1. Connect to DGND if not used
7	INLA	I	D	PWM input signal for channel A low side. Input of Hall sensor A in 1PWM modes. Connect to DGND if not used
8	INHB	I	D	PWM input signal for channel B high side. Connect to DGND if not used
9	INLB	I	D	PWM input signal for channel B low side. Input of Hall sensor B in 1PWM modes. Connect to DGND if not used
10	INHC	I	D	PWM input signal for channel C high side. DIR signal for 1PWM modes. Connect to DGND if not used
11	INLC	I	D	PWM input signal for channel C low side. Input of Hall sensor C in 1PWM modes. Connect to DGND if not used
12	CS_GAIN/ AZ	I	A	Analog programming for the shunt amplifier gain. Dual function as Auto-Zero: input to control external Auto-Zero function
13	VSENSE/ nBRAKE	I	A/D	Analog programming of DVDD output voltage during start-up. Connect a pull down resistor to select DVDD voltage: $R \leq 3.3 \text{ k}\Omega \rightarrow DVDD = 3.3 \text{ V}$ $R \geq 10 \text{ k}\Omega \rightarrow DVDD = 5.0 \text{ V}$ After start-up, pin will be in nBRAKE mode: used for motor braking. Active low
14	DVDD	-	P	Supply for external MCU, Hall sensors, etc. Voltage is generated by integrated linear voltage regulator and defined by VSENSE pin or SPI
15	PVDD	-	P	Power supply of the device
16	PH	-	P	Buck phase node voltage. Connect to output inductor
17	PGND	-	G	Power ground used for buck converter, charge pumps and gate drivers
18	VDBB	-	P	Buck output voltage. Connect capacitor between VDBB and PGND.
19	CP1L	-	P	Bottom connection of the charge pump flying capacitor 1
20	CP1H	-	P	Top connection of the charge pump flying capacitor 1
21	CP2L	-	P	Bottom connection of the charge pump flying capacitor 2
22	CP2H	-	P	Top connection of the charge pump flying capacitor 2

**Pin Configuration**

<b>Pin #</b>	<b>Pin Name</b>	<b>IO</b>	<b>Type</b>	<b>Description</b>
23	VCCLS	-	P	Output of low side charge pump. Connect a capacitor from VCCLS to PGND.
24	VCCHS	-	P	Output of high side charge pump. Connect a capacitor from VCCHS to PVDD or PGND
25	GHC	O	A	High side gate driving signal for phase C. Not connected or connected to PVDD if not used
26	SHC	IO	A	High side source connection (phase node) for phase C. Positive input of shunt amplifier C for $R_{DSON}$ sensing. Not connected if not used
27	N.C.	-	-	Not connected
28	GLC	O	A	Low side gate driving signal for phase C. Not connected if not used
29	SLC	IO	A	Low side source connection for phase C. Positive input of shunt amplifier C for shunt sensing. Short to PGND if not used
30	CSNC	I	A	Current sense amplifier negative input for phase C. Short to PGND or DGND if not used
31	CSNB	I	A	Current sense amplifier negative input for phase B. Short to PGND or DGND if not used
32	SLB	IO	A	Low side source connection for phase B. Positive input of shunt amplifier B for shunt sensing. Short to PGND if not used
33	GLB	O	A	Low side gate driving signal for phase B. Not connected if not used
34	N.C.	-	-	Not connected
35	SHB	IO	A	High side source connection (phase node) for phase B. Positive input of shunt amplifier B for $R_{DSON}$ sensing. Not connected if not used
36	GHB	O	A	High side gate driving signal for phase B. Not connected or connected to PVDD if not used
37	GHA	O	A	High side gate driving signal for phase A. Not connected or connected to PVDD if not used
38	SHA	IO	A	High side source connection (phase node) for phase A. Positive input of shunt amplifier A for $R_{DSON}$ sensing. Not connected if not used
39	N.C.	-	-	Not connected
40	GLA	O	A	Low side gate driving signal for phase A. Not connected if not used
41	SLA	IO	A	Low side source connection for phase A. Positive input of shunt amplifier A for shunt sensing. Short to PGND if not used
42	CSNA	I	A	Current sense amplifier negative input for phase A. Short to PGND or DGND if not used
43	CSOA	O	A	Current sense amplifier output for phase A. Not connected if not used
44	CSOB	O	A	Current sense amplifier output for phase B. Not connected if not used
45	CSOC	O	A	Current sense amplifier output for phase C. Not connected if not used

**Pin Configuration**

<b>Pin #</b>	<b>Pin Name</b>	<b>IO</b>	<b>Type</b>	<b>Description</b>
46	VREF	I	A	Optional reference voltage input offsetting the current sense (CS) outputs with respect to DGND. Not connected if not used
47	CE	I	A	Chip Enable. Starts up the device upon rising edge
48	EN_DRV	I	D	Enables the gate driver section and internal circuitry based on the configuration. Can be configured as watchdog clock. Internal pull down
	Ground Pad	-	P	Ground connection for digital section. Solder to PCB.

## 2 General Product Characteristics

### 2.1 Absolute Maximum Ratings

Table 3 shows the absolute maximum ratings for the device. Ratings are intended in the temperature range  $T_j = -40^\circ\text{C}$  to  $T_j = 150^\circ\text{C}$ . All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest), positive currents are flowing into the pin (unless otherwise specified).

**Table 3 Absolute maximum ratings**

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Supply voltage	PVDD	-0.3		70	V	
Supply voltage slew rate	$\text{SR}_{\text{PVDD}}$			2	V/ $\mu\text{s}$	During start-up
				0.25		During active mode
CE pin voltage	$V_{\text{CE}}$	-0.3		7	V	
Power ground to digital ground voltage	PGND – DGND	-0.3		0.3	V	
Low side gate driver supply voltage	VCCLS	-0.3		20	V	This is same as PVCC
VCCHS voltage	VCCHS	PVDD-0.3		90	V	$\text{VCCHS} = \text{PVDD} + \text{PVCC}$
VCCHS- $V_{\text{SHx}}$ voltage	VCCHS- $V_{\text{SHx}}$			90	V	
VCCHS- $V_{\text{GHx}}$ voltage	VCCHS- $V_{\text{GHx}}$			90	V	
Source high side voltage	$V_{\text{SHx}}$	-8		70	V	DC voltage
		-10		70		500ns pulse max
Source low side voltage/Shunt amplifier positive input voltage	$V_{\text{SLx}}$	-8		8	V	DC voltage
		-10		8		500ns pulse max
Gate high side voltage	$V_{\text{GHx}}$	-8		$\text{VCCHS}+0.3$	V	DC voltage,
		-10		$\text{VCCHS}+0.3$		500ns pulse max
Gate low side voltage	$V_{\text{GLx}}$	-8		$\text{VCCLS}+0.3$	V	DC voltage
		-10		$\text{VCCLS}+0.3$		500ns pulse max
Gate to Source high side voltage	$V_{\text{GHx}} - V_{\text{SHx}}$	-0.3		16	V	DC, $T_j = 25^\circ\text{C}$
		-2		16		500ns pulse max, $T_j = 25^\circ\text{C}$
Gate to Source low side voltage	$V_{\text{GLx}} - V_{\text{SLx}}$	-0.3		16	V	DC, $T_j = 25^\circ\text{C}$
		-2		16		500ns pulse max, $T_j = 25^\circ\text{C}$

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Shunt amplifier negative input voltage	V <sub>CSN</sub>	-0.3		DVDD+0.3		
Flying capacitor 1 voltage	V <sub>CP1H</sub> - V <sub>CP1L</sub> ,	-0.3		9	V	
CP1L pin voltage	V <sub>CP1L</sub> ,	-0.3		9	V	
CP1H pin voltage	V <sub>CP1H</sub> ,	-0.3		20	V	
Flying capacitor 2 voltage	V <sub>CP2H</sub> - V <sub>CP2L</sub>	-0.3		70	V	
CP2L pin voltage	V <sub>CP2L</sub>	-0.3		20	V	
CP2H pin voltage	V <sub>CP2H</sub>	-0.3		90	V	
Buck converter output voltage	V <sub>DDB</sub>	-0.3		9	V	
Phase voltage	V <sub>PH</sub>	-0.3		70	V	DC condition
		-5				Less than 20 ns pulse
DVDD regulator output voltage	DVDD	-0.3		6	V	
Input/Output pin voltage	V <sub>INHX</sub> , V <sub>INLX</sub> , V <sub>nFAULT</sub> , V <sub>SCLK</sub> , V <sub>nSCS</sub> , V <sub>SDI</sub> , V <sub>SDO</sub> , V <sub>CSOX</sub> , V <sub>REF</sub>	-0.3		DVDD + 0.3	V	
Maximum current for digital pins	I <sub>DIG_IN_MAX</sub>	-1		1	mA	
Analog input pin voltage	V <sub>EN_DRV</sub> , V <sub>VSENSE/nBRAKE</sub> , V <sub>CS_GAIN/AZ</sub>	-0.3		7	V	Analog or analog and digital pins
Maximum current for analog inputs	I <sub>AN_IN_MAX</sub>	-1		10	mA	
Maximum sink current for open-drain pins (nFAULT, nSCS)	I <sub>OD_SINK_MAX</sub>			7	mA	
VREF pin sink current	I <sub>REF_SINK</sub>	-50		50	µA	
Junction temperature	T <sub>J</sub>	-40		150	°C	
Storage temperature	T <sub>S</sub>	-55		150	°C	
Case temperature	T <sub>CASE</sub>			145	°C	

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These are stress ratings only which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.

Note: Absolute Maximum Ratings are not subject to production test, specified by design.

## 2.2 Recommended Operating Conditions

Operating at  $T_A = 25^\circ\text{C}$ . All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest), positive currents are flowing into the pin (unless otherwise specified).

**Table 4 Recommended operating conditions**

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Supply voltage	PVDD	5.5		60	V	
Supply voltage slew rate	$\text{SR}_{\text{PVDD}}$			2	V/ $\mu\text{s}$	During start-up
				0.25		During active mode
CE pin voltage range	$V_{\text{CE}}$	0		6	V	
External supply voltage regulator output voltage	DVDD	3.3		5.5	V	Configurable via VSENSE pin or SPI (OTP write)
Buck phase voltage continuous	$V_{\text{PH}}$	-0.3		60	V	DC condition
		-5				Less than 20 ns pulse
Inverter phase voltage	$V_{\text{SHx}}$	-8		60		
High side gate driver supply voltage	VCCHS	-0.3		75	V	
Gate driver supply voltage (PVCC)	VCCLS, VCCHS-PVDD	7		15	V	Programmable via SPI. This value is equal to PVCC
Gate driver maximum operating frequency	$f_{\text{PWM\_GD}}$			200	kHz	
Digital pin I/O voltage range	$V_{\text{INHx}}, V_{\text{INLx}}, V_{\text{nFAULT}}, V_{\text{CS\_GAIN/AZ}}, V_{\text{EN\_DRV}}, V_{\text{SCLK}}, V_{\text{nSCS}}, V_{\text{SDI}}, V_{\text{SDO}}$	-0.3		DVDD	V	When CS_GAIN/AZ pin works as digital input
Open-drain pins low voltage (nFAULT, nSCS)	$V_{\text{OD\_LV}}$			0.5	V	When sinking 5 mA, DVDD = 3.3 V
Shunt amplifier input voltage range	$V_{\text{SLx}}, V_{\text{CSNx}}$	-0.3		0.3	V	Sense amplifier configured for shunt resistor sensing
Analog pins voltage range	$V_{\text{CSOx}}, V_{\text{VSENSE/nBRAKE}}, V_{\text{CS\_GAIN/AZ}}$	0		DVDD	V	When CS_GAIN/AZ and VSENSE/nBRAKE pins work as analog pins
VREF input voltage range	$V_{\text{REF}}$	DVDD/4		DVDD/2		VREF is configured as input
Junction temperature range	$T_J$	-40		125	°C	

## 2.3 ESD Robustness

ESD robustness related data is listed in Table 5.

**Table 5 ESD robustness data<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
ESD robustness all pins	V <sub>ESD</sub>	-2000		2000	V	HBM <sup>2)</sup>
ESD robustness all pins	V <sub>ESD</sub>	-500		500	V	CDM <sup>3)</sup>
ESD robustness (corner pins)	V <sub>ESD</sub>	-750		750	V	CDM <sup>3)</sup>

1) Not subject to production test, specified by design

2) ESD robustness, Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS001 (1.5kΩ, 100 pF)

3) ESD robustness, Charge Device Model (CDM) according to JEDEC JESD22-C101

## 2.4 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).*

**Table 6 Thermal resistance parameters**

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Junction-to-ambient thermal resistance	R <sub>θJA</sub>		41.2		°C/W	T <sub>a</sub> = 25 °C, FR4 PCB, size: 60.0 × 40.0 × 1.5 mm <sup>3</sup> , stack 2S2P
Junction-to-case (top) thermal resistance	R <sub>θJC(top)</sub>		25.55		°C/W	
Junction-to-case (bottom) thermal resistance	R <sub>θJC(bot)</sub>		6.73		°C/W	

## 2.5 Electrical Characteristics

PVDD = 5.5 to 60 V, T<sub>a</sub> = 25°C, unless specified under test condition. All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest), positive currents are flowing into the pin (unless otherwise specified).

**Table 7 Electrical characteristics**

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
<b>Main Power Supply (PVDD)</b>						
Supply voltage	PVDD	5.5		60	V	
PVDD current, active mode	I <sub>PVDD_ACTIVE</sub>	20		50	mA	V <sub>EN_DRV</sub> > V <sub>EN_DRV_TH</sub> , V <sub>CE</sub> > V <sub>CE_TH_R</sub> , PVDD = 40V, typical application run
PVDD current, standby mode	I <sub>PVDD_STANDBY</sub>	3		8	mA	V <sub>EN_DRV</sub> < V <sub>EN_DRV_TH</sub> , V <sub>CE</sub> > V <sub>CE_TH_R</sub> , PVDD = 40V

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
PVDD current, OFF mode	I <sub>PVDD_OFF</sub>	25		40	µA	V <sub>EN_DRV</sub> < V <sub>EN_DRV_TH</sub> , V <sub>CE</sub> < V <sub>CE_TH_R</sub> , PVDD = 40V
<b>Gate Driver</b>						
Low side gate driver supply voltage target	V <sub>CCLS</sub>	7		15	V	Generated from charge pump. Gate driver supply voltage programmable via SPI
High side gate driver supply voltage target	V <sub>CCHS</sub>	10.8		74.3	V	Generated from charge pump. Gate driver supply voltage programmable via SPI according to V <sub>CCLS</sub>
High side gate driver output	V <sub>GHx</sub> -V <sub>SHx</sub>			V <sub>CCLS</sub> - 0.7	V	More details in section 2.6
Low side gate driver output	V <sub>GLx</sub> -V <sub>SLx</sub>			V <sub>CCLS</sub>	V	More details in section 2.6
Peak source current (high side and low side drivers)	I <sub>GD_SRC_PEAK</sub>		1.5		A	Current flowing from pin. Gate driver current programmable via SPI
Peak sink current (high side and low side drivers)	I <sub>GD_SNK_PEAK</sub>		1.5		A	Current into the pin. Gate driver current programmable via SPI
Hold gate current <sup>1)</sup>	I <sub>HOLD</sub>		250		mA	Low side gate driver
			50			High side gate driver
Source and sink current accuracy	I <sub>GD_ACCURACY</sub>	-20		20	%	
Charge pump clock frequency	f <sub>CP_CLK</sub>	190		1600	kHz	Programmable via SPI
Charge pump clock accuracy	f <sub>CP_CLK_ACC</sub>	-5		5	%	
Charge pump clock frequency spread spectrum	f <sub>CP_CLK_SS</sub>	0		30	%	
High side gate driver average current	I <sub>GD_VCCHS</sub>			60	mA	PVDD ≥ 9.5 V operation
				30		PVDD < 9.5 V operation
Low side gate driver average current	I <sub>GD_VCCLS</sub>			60	mA	PVDD ≥ 9.5 V operation
				30		PVDD < 9.5 V operation

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Charge pump ramp up time <sup>1)</sup>	$t_{CP\_START}$			250	μs	$C_{CPX} = 220 \text{ nF}$ , $C_{VCCLS} = 1 \mu\text{F}$ , $I_{LOAD} < 50 \mu\text{A}$ , PVCC = 12 V. PVDD $\geq 10 \text{ V}$ . Depends on capacitance values and features like charge pump pre-charge
				1	ms	$C_{CPX} = 220 \text{ nF}$ , $C_{VCCLS} = 1 \mu\text{F}$ , $I_{LOAD} < 50 \mu\text{A}$ , PVCC = 12 V. PVDD $< 10 \text{ V}$ . Depends on capacitance values and features like charge pump pre-charge
Gate driver PWM frequency	$f_{PWM\_GD}$			200	kHz	
Input pin pulse width	$t_{INx\_PW}$	80			ns	Applies to INHx and INLx pins. Pre-charge current disabled, current setting to 1.5A
Dead-time	$t_{DT\_RISE}$ , $t_{DT\_FALL}$	120			ns	This is the minimum dead time value possible. If input signals have dead time lower than this, this value applies otherwise input PWM signal dead time is used. Value is programmable via SPI.
Gate to Source passive weak pull-down resistor	$R_{GS\_PD\_WEAK}$	70	100	130	kΩ	Always active
Gate to Source active strong pull-down resistor	$R_{GS\_PD\_STRONG}$	0.25	1	2	kΩ	Pull-down resistor enabled when EN_DRV or PVDD are off and $V_{Gxy} - V_{Sxy} \geq 2 \text{ V}$ . Both high side and low side drivers
Propagation delay INHx to GHx	$t_{PROP\_HS}$	140		200	ns	Dead time not considered
Propagation delay INLx to GLx	$t_{PROP\_LS}$	140		200	ns	Dead time not considered
Propagation delay matching high-low side <sup>1)</sup>	$t_{PROP\_MATCH\_HL}$	0	25		ns	
Channel-to-channel propagation delay matching <sup>1)</sup>	$t_{PROP\_MATCH\_CH}$	0		10	ns	
Channel-to-channel dead time matching <sup>1)</sup>	$t_{DT\_MATCH\_CH}$	0		10	ns	
Gate to source comparator threshold	$V_{GS\_CPM\_TH}$		50		mV	
Gate to source comparator deglitch time <sup>1)</sup>	$t_{VGS\_CMP\_DEGLIT\_CH}$		500		ns	

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
<b>Synchronous Buck Converter</b>						
Buck converter output target voltage	$V_{DDB_{NOM}}$		6.5		V	PVCC_SETPT=b'11, PVDD $\geq$ 8 V, $I_{VDDB} = 0$ A
			7.0			PVCC_SETPT=b'10, PVDD $\geq$ 8.5 V, $I_{VDDB} = 0$ A
			8.0			PVCC_SETPT=b'0x, PVDD $\geq$ 9.5 V, $I_{VDDB} = 0$ A
Buck regulator output voltage at low input voltage (PVDD)	$V_{DDB_{NOM\_LV}}$	4.2		6.5	V	PVCC_SETPT=b'11, 5.5 V $\leq$ PVDD < 8 V Buck with fixed duty cycle. VDDB dependent on $I_{VDDB}$
		4.2		7.0		PVCC_SETPT=b'10, 5.5 V $\leq$ PVDD < 8.5 V Buck with fixed duty cycle. VDDB depends on $I_{VDDB}$
		4.2		8.0		PVCC_SETPT=b'0x, 5.5 V $\leq$ PVDD < 9.5 V Buck with fixed duty cycle. VDDB depends on $I_{VDDB}$
Buck converter output voltage load regulation <sup>1)</sup>	$\Delta V_{DDB_{LOAD}}$	-10		9	%	PVDD $>$ $V_{DDB_{NOM}} + 2.5$ V, $I_{VDDB}$ transient from 60 mA to 540 mA (10% to 90% load transient), $C_{VDDB} = 47 \mu F$ , $L = 22 \mu H$ , $f_{BUCK\_SW} = 500$ kHz
		-9.5		5		PVDD $>$ $V_{DDB_{NOM}} + 2.5$ V, $I_{VDDB}$ transient from 60 mA to 540 mA (10% to 90% load transient), $C_{VDDB} = 47 \mu F$ , $L = 10 \mu H$ , $f_{BUCK\_SW} = 1000$ kHz
Buck converter maximum average current	$I_{VDDB\_MAX}$			600	mA	PVDD $\geq$ 9.5 V. VDDB supplies charge pumps, DVDD linear regulator and VDDB pin
				200		PVDD at low input voltage range ( $V_{DDB_{NOM\_LV}}$ ). VDDB supplies charge pumps, DVDD linear regulator and VDDB pin
Buck converter inductor peak current limit	$I_{BUCK\_PEAK\_LIM}$		1		A	$f_{BUCK\_SW} = 500$ kHz
			1.3			$f_{BUCK\_SW} = 1000$ kHz
Buck OCP Hysteresis	$I_{OCP\_HYS}$		50		mA	

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Buck converter maximum duty cycle	DC <sub>BUCK_MAX</sub>		95		%	
Buck converter high side switch R <sub>DSON</sub>	R <sub>DSON_BUCK_HS</sub>	0.7	1.4	2.2	Ω	
Buck converter low side switch R <sub>DSON</sub>	R <sub>DSON_BUCK_LS</sub>	0.3	0.45	1.0	Ω	
Buck switching frequency	f <sub>BUCK_SW</sub>	450	500	590	kHz	Configurable via OTP write. May vary during load steps.
		850	1000	1150		
Buck converter soft start timing	t <sub>VDDDB_SFT_START</sub>			1500	μs	Actual value depends on buck output filter

## Linear Regulator DVDD

Regulator target output voltage	DVDD		3.3		V	Programmable via SPI or external pull down resistor on VSENSE pin: R<=3.3 kΩ → DVDD=3.3 V
			5			Programmable via SPI or external pull down resistor on VSENSE pin: R>=10 kΩ → DVDD=5.0 V
Output voltage accuracy	DVDD <sub>ACC</sub>	-2.5		2.5	%	
Load current	I <sub>DVDD</sub>			300	mA	
Static line regulation	ΔDVDD <sub>LINE</sub>			10	mV	VDDDB=6.5 V...8 V, I <sub>DVDD</sub> =300 mA
Static load regulation	ΔDVDD <sub>LOAD</sub>			40	mV	VDDDB=DVDD+1.5 V, I <sub>DVDD</sub> = 1 mA to 300 mA step
Analog programming pins period	t <sub>AN_T</sub>		25		μs	Each VSENSE and/or CS_GAIN
DVDD turn on delay	t <sub>DVDD_TON_DLY</sub>	200		800	μs	Programmable via SPI. Delay between VDDDB UVLO until DVDD ramp up start

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
DVDD soft start timing	$t_{DVDD\_SFT\_START}$	100		1600	μs	Configurable via SPI- Current limited by $I_{DVDD\_I\_LIM}$ . If due to larger $C_{DVDD}$ values, programmed timing is not achievable, start-up time is defined by $t_{DVDD\_SFT\_START} = \frac{C_{DVDD} * DVDD}{I_{DVDD\_I\_LIM}}$

## Current Sense Amplifier

Closed loop gain	$G_{CS}$	4		64	V/V	Configured either via external resistor or SPI
Gain error <sup>1)</sup>	$G_{CS\_ERROR}$	-1		1	%	Measured at $SLx-CSNx=0.025$ V
Offset input referred <sup>1)</sup>	$V_{CS\_OS}$		200	600	μV	Gain=32, inputs shorted
Offset temperature drift	$\Delta V_{CS\_OS} / \Delta T$		5		μV/ °C	
Current sense blanking time	$t_{CS\_BLANK}$	0		8	μs	Programmable via SPI
Amplifier output settling time <sup>1)</sup>	$t_{CSO\_SETTLING}$		600		ns	Time from input signal step to 1% of final output voltage. Input voltage step of 0.2 V. Gain 4 to 24
			1000			Settling time from input signal step to 1% of final output voltage. Input voltage step of 0.2 V. Gain 32 to 64
Unity gain bandwidth <sup>1)</sup>	GBW	5	8		MHz	
Common mode rejection ratio	CMRR	60	80		dB	Gain=8, $f_{SW}$ from 0 Hz to 80 kHz
Power supply rejection ratio <sup>1)</sup>	PSRR	60			dB	Gain=8, $f < 1$ MHz
		40				Gain=8, $f < 10$ MHz
Input bias current	$I_{CSN}$			50	μA	Current drawn into pin
Current sense output voltage range	$V_{CSO}$	0.3		DVDD-0.3	V	
Output voltage slew rate <sup>1)</sup>	$SR_{CSO}$	-10		10	V/μs	Gain=8, $R_L=470$ Ω, $C_L=330$ pF. $V_{SLx} = +/- 250$ mV
Propagation delay from gate driver ( $G_{xy}$ ) transition to CSOx activation <sup>1)</sup>	$t_{CSAMP\_PROP}$		130		ns	CSAMP in shunt mode
			400			CSAMP in $R_{DSON}$ mode

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Output target voltage reference (offset)-VREF	V <sub>CS_REF</sub>	1/4* DVDD		1/2* DVDD	V	Depending on DVDD selected value: DVDD=3.3 V / DVDD=5 V
Output voltage reference (offset) – VREF- accuracy	V <sub>CS_REF_ACC</sub>	-1.5		1.5	%	
Output short circuit limit	I <sub>CS_SC</sub>		20		mA	Pin CSOx shorted to ground
Auto-Zero active time	t <sub>AUTO_ZERO</sub>		1.7		μs	Normal mode
			2			Rdson sensing mode
Auto-Zero cycle time	t <sub>AUTO_ZERO_CYCLE</sub>			100	μs	If GHx is switching
				200		If GHx is not switching
CS_GAIN/AZ external Auto-Zero signal frequency	f <sub>AZ_CP_CLK_OFF</sub>	5		100	kHz	
CS_GAIN/AZ external Auto-Zero signal pulse width	t <sub>AZ_EXT_PW</sub>	0.1		3.5	μs	

## Current Sense Amplifier Over-Current Protection Comparator and DAC

Current sense over-current comparator hysteresis	V <sub>CS_OC_HYST</sub>			5	mV	
Over-current comparator input offset	V <sub>CS_OCP_OFFSET</sub>	-12		12	mV	V <sub>CS_OCP_THP</sub> = 200mV, V <sub>CS_OCP_THN</sub> = -200mV
Over-current deglitch time	t <sub>CS_OCP_DEGLITCH</sub>	0		8	μs	Programmable via SPI
Current sense input referred OCP threshold positive target level	V <sub>CS_OCP_THP</sub>	20		300	mV	Programmable via SPI
Current Sense Input referred OCP threshold negative target level	V <sub>CS_OCP_THN</sub>	-300		-20	mV	Programmable via SPI
Over-current blanking time	t <sub>OCP_BLANK</sub>	0		10	μs	Programmable via SPI

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		

## Analog to Digital Converter (ADC)

ADC resolution	ADC <sub>RES</sub>		7		bits	
ADC gain error	$\varepsilon_{ADC\_GAIN\_ERR}$	-0.5		0.5	%	
ADC offset error	$\varepsilon_{ADC\_OFFS\_ERR}$	2		2	LSB	
ADC input clock	f <sub>ADC_CLK</sub>		12.5		MHz	
ADC conversion time	t <sub>CONV</sub>		1.28		μs	

## Digital Inputs (INHx, INLx, SCLK, nSCS)

Input logic low voltage	V <sub>INPUT_IL</sub>	0		0.8	V	Applies also to nBRAKE function in VSENSE/nBRAKE pin
Input logic high voltage	V <sub>INPUT_IH</sub>	2			V	Applies also to nBRAKE function in VSENSE/nBRAKE pin
Internal pull-down resistor to GND	R <sub>PD_DIG</sub>		200		kΩ	Applies to INHx, INLx and SCLK pins
Internal pull-up resistor to DVDD	R <sub>PU_nSCS</sub>		200		kΩ	

## Digital Inputs (CE, EN\_DRV)

Internal pull-down resistor to GND CE	R <sub>PD_CE</sub>	550	800	1000	kΩ	
Internal pull-down resistor to GND EN_DRV	R <sub>PD_EN_DRV</sub>		500		kΩ	
CE threshold voltage rising	V <sub>CE_TH_R</sub>	2.7			V	
CE threshold voltage falling	V <sub>CE_TH_F</sub>			0.6	V	
CE pin sink current	I <sub>CE_SNK</sub>			10	μA	Current flowing into CE pin
EN_DRV threshold voltage	V <sub>EN_DRV_TH</sub>		0.5*D VDD		V	
EN_DRV watchdog function threshold voltage high	V <sub>EN_DRV_WD_TH_H</sub>		0.8*D VDD		V	
EN_DRV watchdog signal threshold voltage low	V <sub>EN_DRV_WD_TH_L</sub>		0.2*D VDD		V	
EN_DRV threshold voltage hysteresis	V <sub>EN_DRV_TH_HYS</sub>		4		%	Applies to V <sub>EN_DRV_TH</sub> , V <sub>EN_DRV_WD_THH</sub> and V <sub>EN_DRV_WD_THL</sub> thresholds

## Digital Output - nFAULT

**General Product Characteristics**

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Output logic low voltage	V <sub>OL</sub>			0.6	V	I <sub>O</sub> =5mA
nFAULT internal pull-up resistor to DVDD	R <sub>PU_nFAULT</sub>		200		kΩ	Pull up resistor for nFAULT

**Digital Output - SDO**

Output logic low voltage	V <sub>OL</sub>			0.6	V	I <sub>O</sub> =5mA
Output logic high voltage	V <sub>OH</sub>	2.3			V	
SDO internal pull-down resistor to DVDD	R <sub>PD_SDO</sub>		200		kΩ	When nSCS is high

**OTP Programming**

OTP programming supply voltage	PVDD <sub>OTP_PR OG</sub>	13			V	Below this value an OTP blocking will occur
OTP programming temperature	T <sub>OTP_PROG</sub>			150	°C	Above this value an OTP blocking will occur

**Watchdog**

Watchdog timer period for buck converter input	t <sub>WD_BUCK_T</sub>		1.5		ms	Applies to buck converter input selection only. Not configurable value
Watchdog EN_DRV frequency	t <sub>WD_EN_DRV_FRE Q</sub>	450	500	550	Hz	

**Overload Protections Gate Driver**

PVDD UVLO threshold rising	V <sub>PVDD_UVLO_R</sub>	4.95	5.1	5.25	V	
PVDD UVLO threshold falling	V <sub>PVDD_UVLO_F</sub>	4.85	5.0	5.15	V	
VCCHS UVLO threshold rising	V <sub>HS_UVLO_R</sub>	5.6	5.8	6.0	V	
VCCHS UVLO threshold falling	V <sub>HS_UVLO_F</sub>	4.3	4.5	4.7	V	
VCCLS UVLO threshold rising	V <sub>LS_UVLO_R</sub>	6.1	6.4	6.7	V	
VCCLS UVLO threshold falling	V <sub>LS_UVLO_F</sub>	4.3	4.5	4.7	V	

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
<b>Overload Protections Power Supply System</b>						
VDDB UVLO rising threshold	$V_{VDDB\_UVLO\_R}$	4.2	4.3	4.4	V	
VDDB UVLO falling threshold	$V_{VDDB\_UVLO\_F}$	4.1	4.2	4.3	V	
VDDB OVLO rising threshold	$V_{VDDB\_OVLO\_R}$	105	108	111	%	Percentage of target output value
VDDB OVLO falling threshold	$V_{VDDB\_OVLO\_F}$	102	105	108	%	Percentage of target output value
Buck OCP (inductor current) threshold	$I_{BUCK\_OCP\_TH}$		1.0		A	$f_{BUCK\_SW} = 500\text{kHz}$
			1.3			$f_{BUCK\_SW} = 1\text{MHz}$
Buck OCP hysteresis	$I_{BUCK\_OCP\_HYS}$		50		mA	
DVDD UVLO rising threshold	$V_{DVDD\_UVLO\_R}$		85		%	Percentage of target output value
DVDD UVLO falling threshold	$V_{DVDD\_UVLO\_F}$		75		%	Percentage of target output value
DVDD OVLO rising threshold	$V_{DVDD\_OVLO\_R}$		110		%	Percentage of target output value
DVDD OVLO falling threshold	$V_{DVDD\_OVLO\_F}$		105		%	
DVDD target output current limit	$I_{DVDD\_I\_LIM}$	50		450	mA	Configurable via SPI
DVDD target output current limit accuracy	$I_{DVDD\_I\_ACC}$	-10		10	%	
<b>Over-Temperature Protection</b>						
Over-temperature shut-down threshold <sup>1)</sup>	$OTS_{TH}$		150		°C	
OTS Hysteresis	$OTS_{HYS}$		10		°C	
Over-temperature warning threshold	$OTW_{TH}$		125		°C	Measured via internal ADC
Over-temperature warning hysteresis	$OTW_{HYS}$		10		°C	
<b>Locked Rotor Protection</b>						
Locked rotor detect time	$t_{LOCK}$	1		8	s	Programmable via SPI
<b>SPI Timing Requirements<sup>1)</sup></b>						
Clock period	$t_{CLK}$	60			ns	

## General Product Characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Clock high time	$t_{CLKH}$	20			ns	
Clock low time	$t_{CLKL}$	20			ns	
SDI input data setup time	$t_{SET\_SDI}$	10			ns	
SDI input data hold time	$t_{HD\_SDI}$	10			ns	
SDO output data delay time	$t_{DLY\_SDO}$	0		20	ns	SCLK high to SDO valid
SDO rise and fall time	$t_{RF\_SDO}$			10	ns	
nSCS enable time	$t_{EN\_nSCS}$			50	ns	nSCS low to SDO transition
nSCS disable time,	$t_{DIS\_nSCS}$			50	ns	nSCS high to SDO high impedance
nSCS hold time	$t_{HD\_nSCS}$	50			ns	Falling SCLK to rising nSCS
nSCS setup time	$t_{SET\_nSCS}$	50			ns	Falling nSCS to rising SCLK
nSCS sequential delay time	$t_{SEQ\_nSCS}$	450			ns	Rising nSCS to falling nSCS

1. Not subject to production test

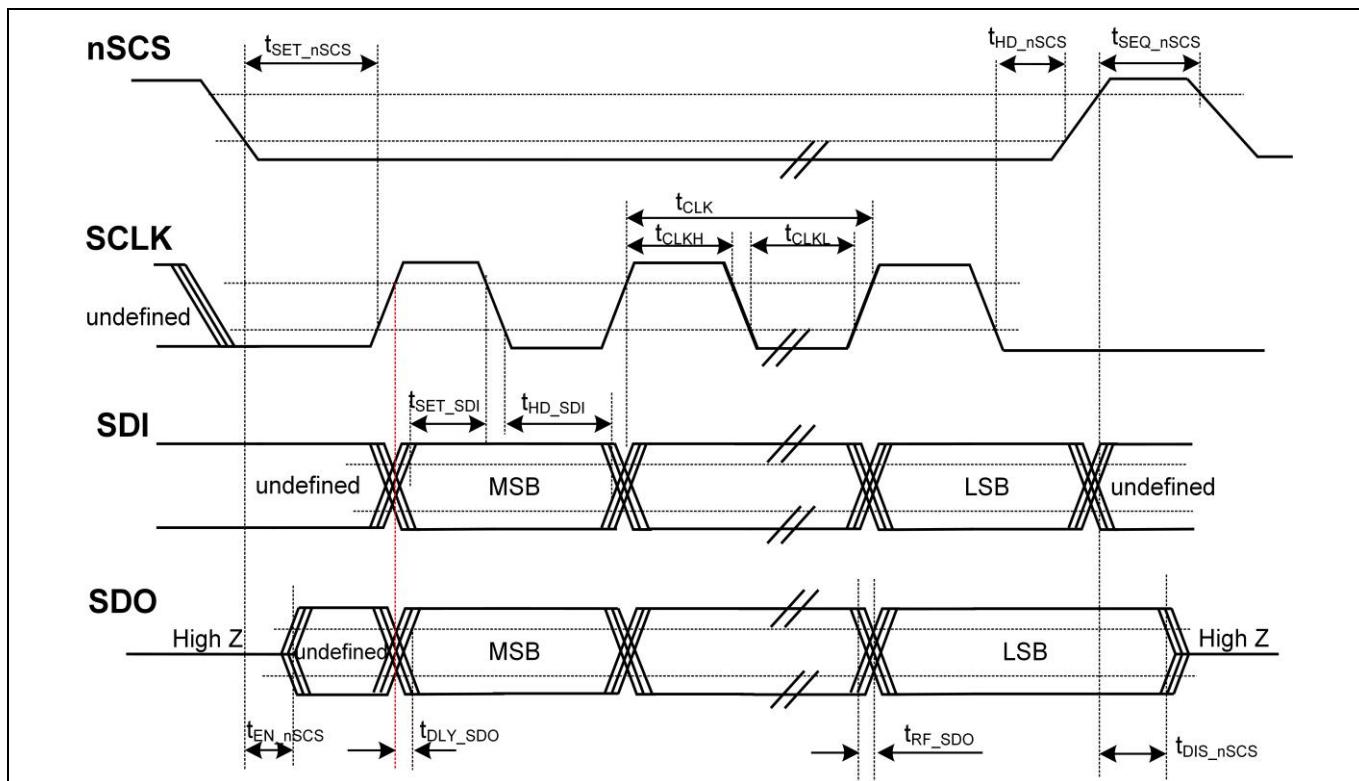
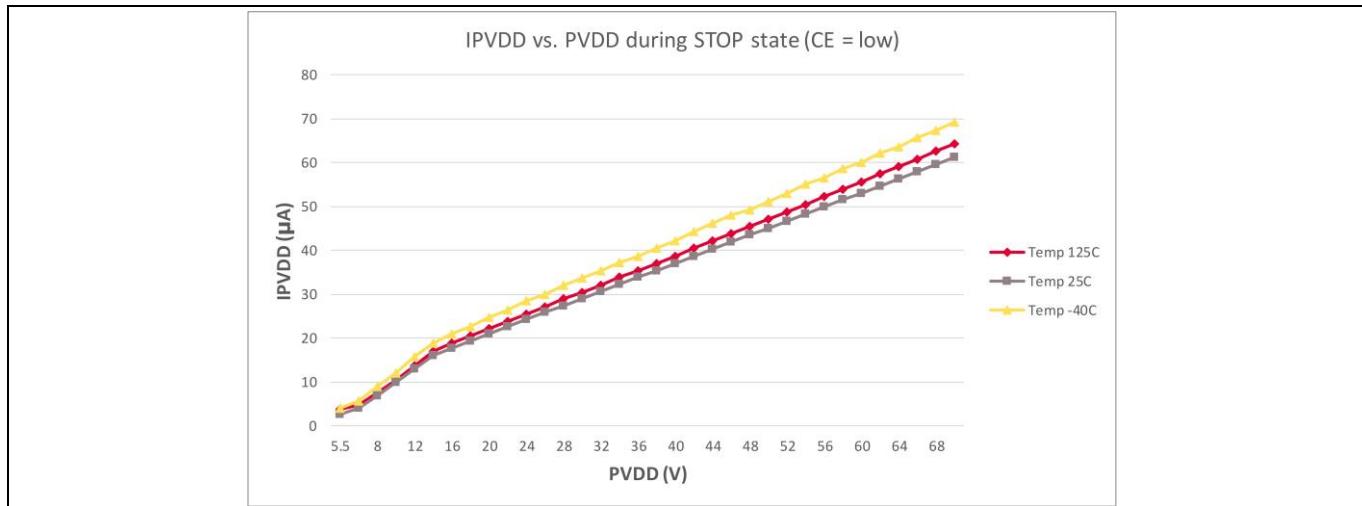


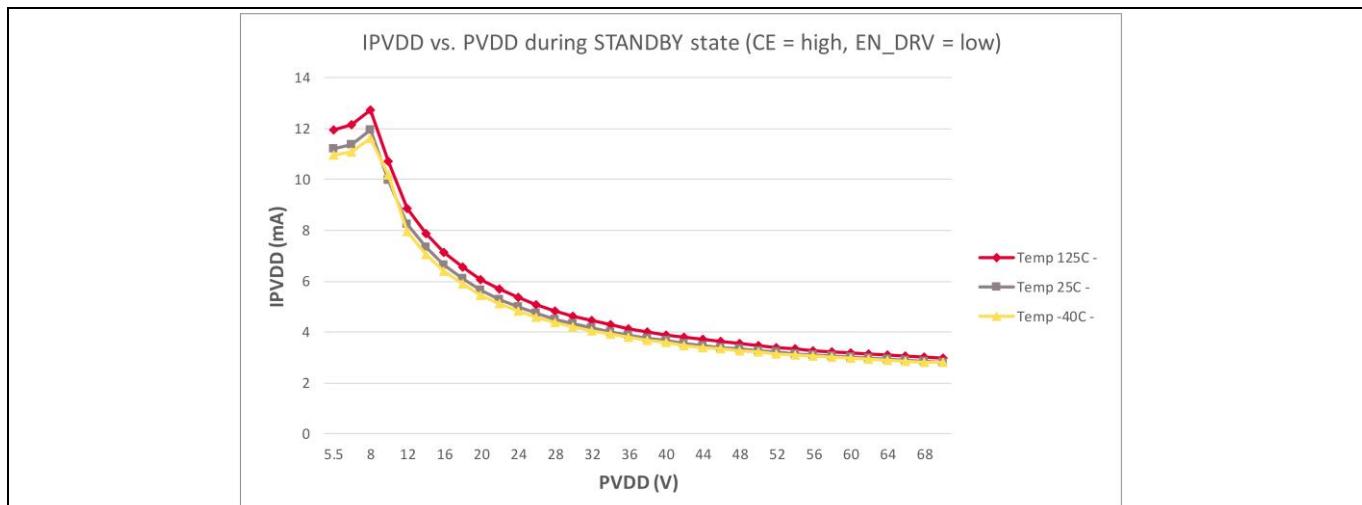
Figure 3 SPI timing diagram

## 2.6 Electrical Characteristic Graphs

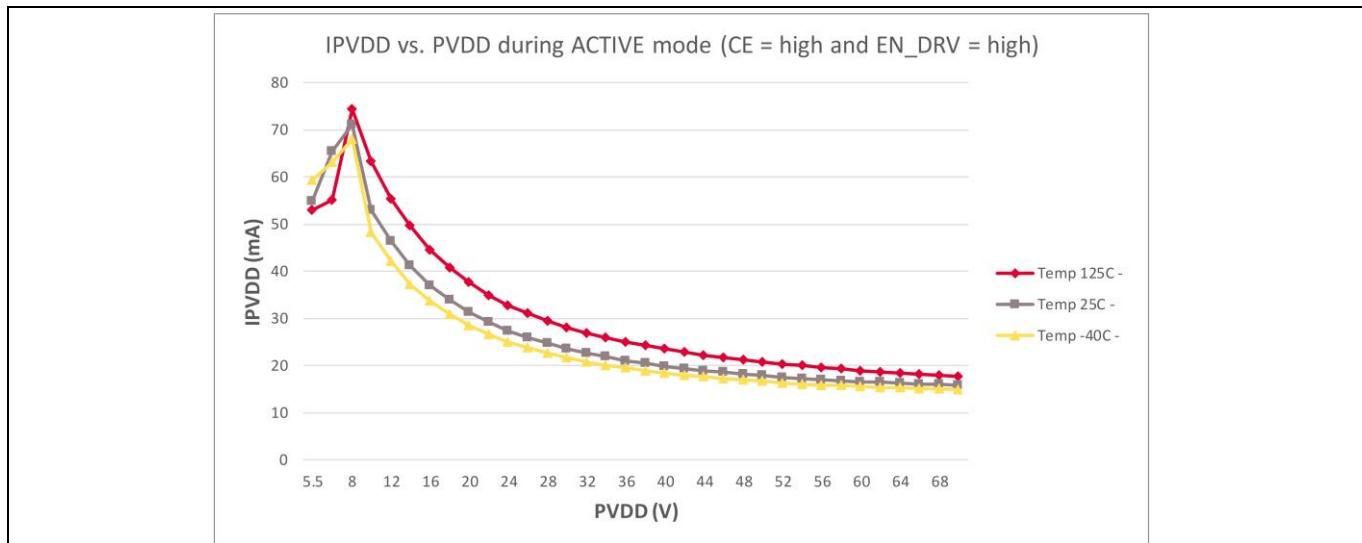
Following graphs provide information on the behavior of the device at different conditions. This data is not subject to production test.  $T_A = 25^\circ\text{C}$ , unless otherwise specified. All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest).



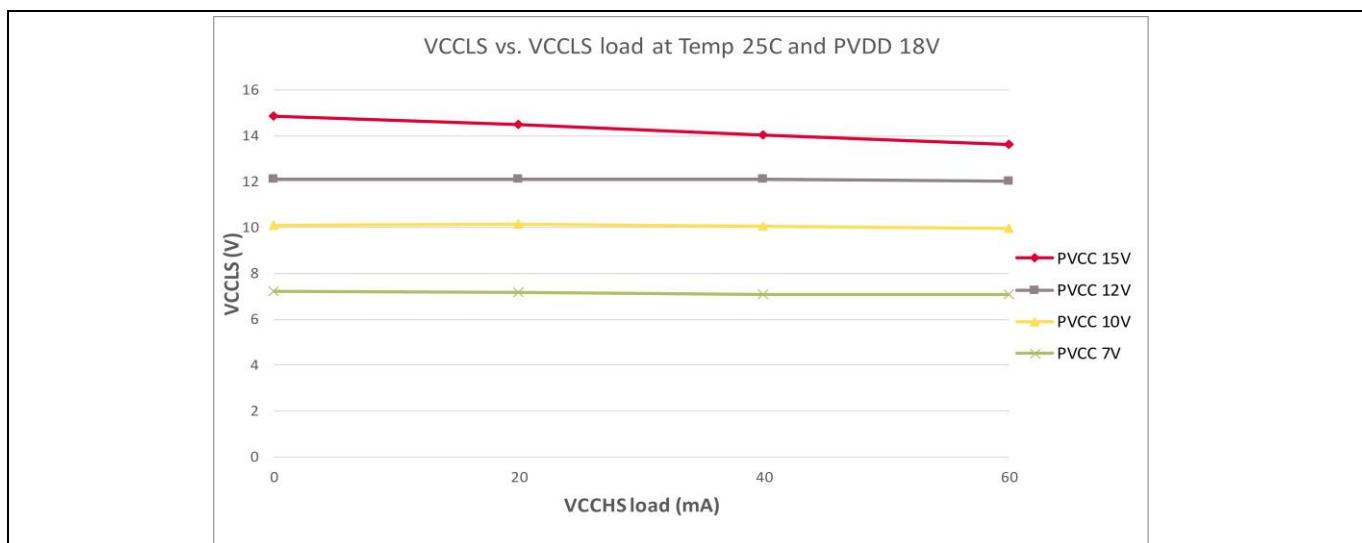
**Figure 4 Current consumption on PVDD pin vs PVDD voltage during STOP state -both CE and EN\_DRV are below active thresholds**



**Figure 5 Current consumption on PVDD vs PVDD voltage during STANDBY state - CE is above active threshold and EN\_DRV is below**

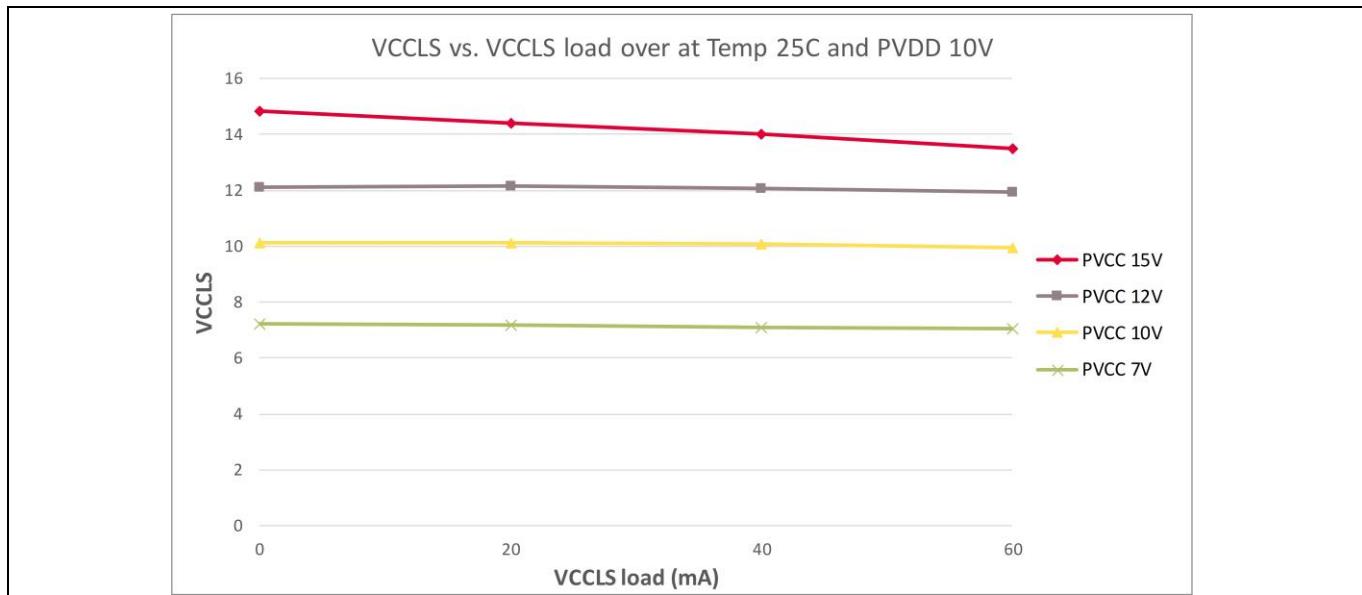
**General Product Characteristics**


**Figure 6 Current consumption on PVDD vs PVDD voltage during ACTIVE state in a typical application - both CE and EN\_DRV are both above active thresholds**

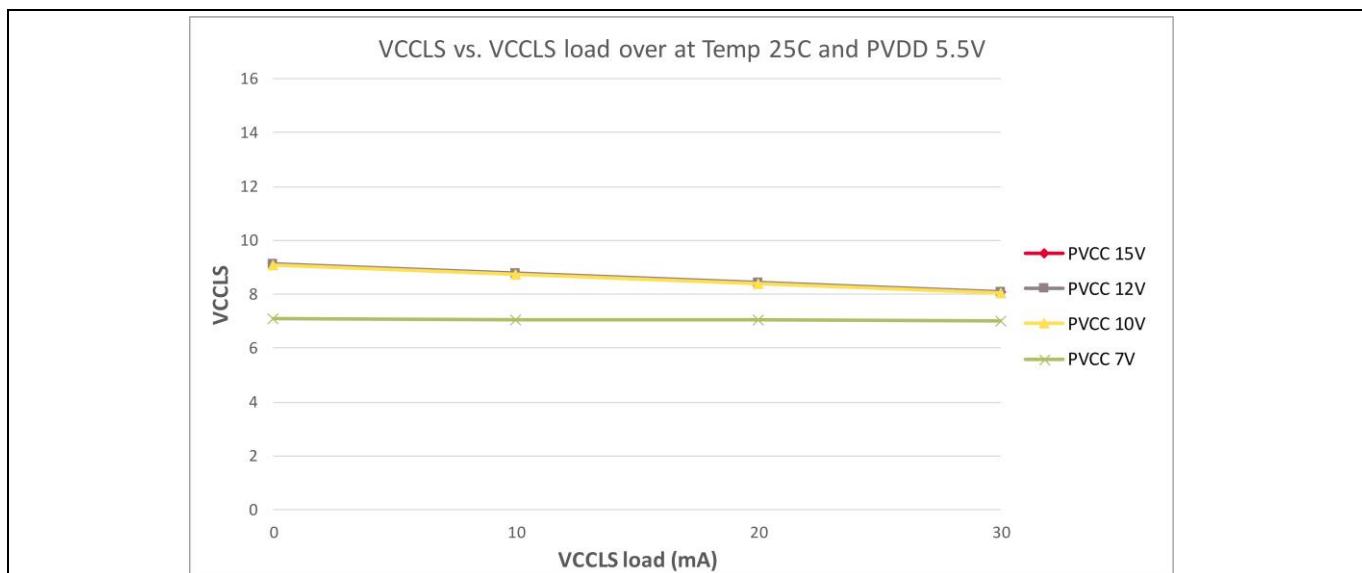


**Figure 7 VCCLS average voltage vs VCCLS load for different PVCC configurations at PVDD 18V-Typical application with  $C_{CP1(2)} = 220\text{nF}$  and  $C_{VCCLS} = 1\mu\text{F}$ . VCCHS load 20mA**

## General Product Characteristics

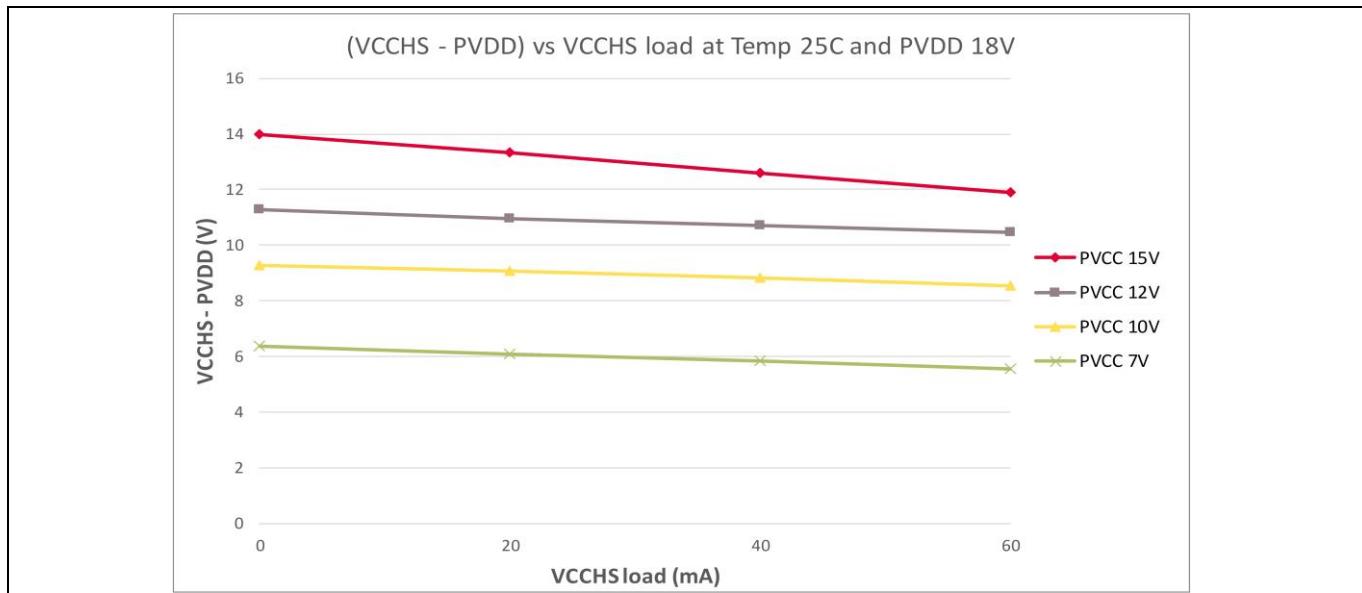


**Figure 8 VCCLS average voltage vs VCCLS load for different PVCC configurations at PVDD 10V-Typical application with  $C_{CP1(2)} = 220nF$  and  $C_{VCCLS} = 1\mu F$ . VCCHS load 20mA**

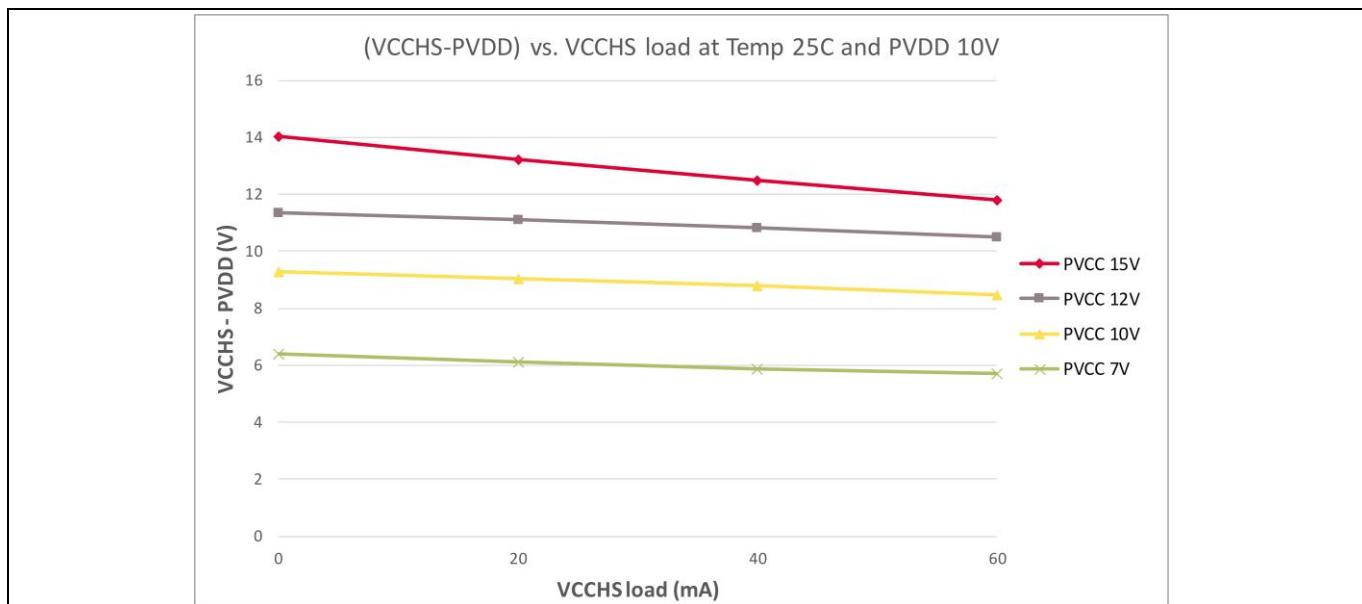


**Figure 9 VCCLS average voltage vs VCCLS load for different PVCC configurations at PVDD 5.5V. Typical application with  $C_{CP1(2)} = 220nF$  and  $C_{VCCLS} = 1\mu F$ . VCCHS load 20mA**

## General Product Characteristics

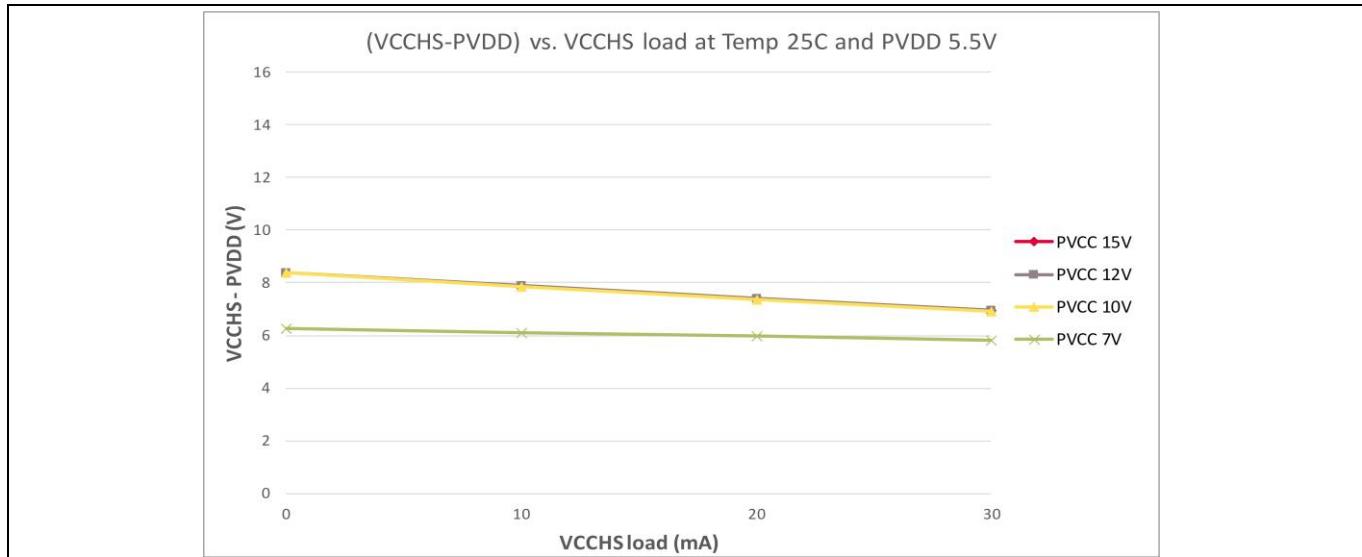


**Figure 10 High side gate driver supply (VCCHS-PVDD) average voltage vs VCCHS load for different PVCC configurations at PVDD 18V. Typical application with  $C_{CP1(2)} = 220\text{nF}$  and  $C_{VCCHS} = 1\mu\text{F}$ . VCCLS load 20mA**

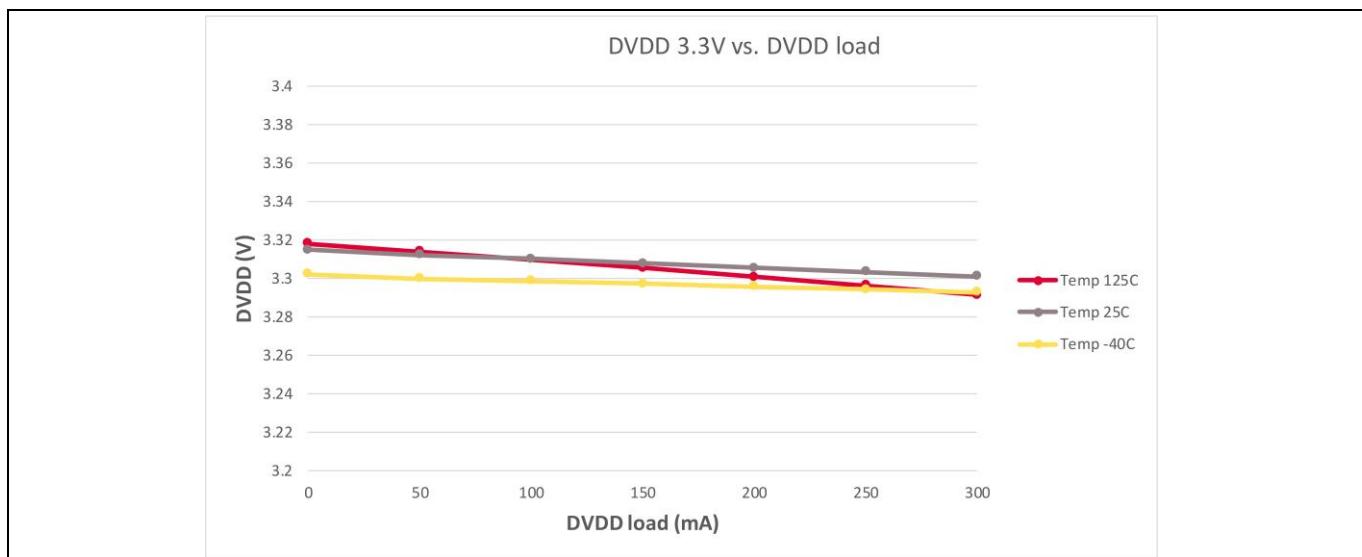


**Figure 11 High side gate driver supply (VCCHS-PVDD) average voltage vs VCCHS load for different PVCC configurations at PVDD 10V. Typical application with  $C_{CP1(2)} = 220\text{nF}$  and  $C_{VCCHS} = 1\mu\text{F}$ . VCCLS load 20mA**

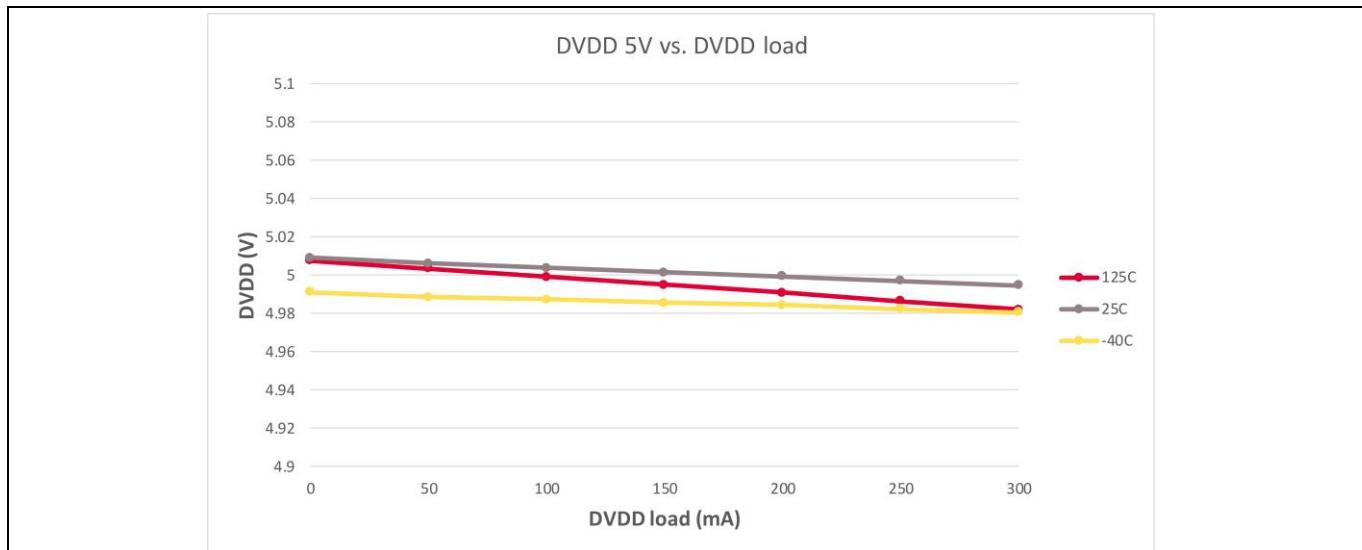
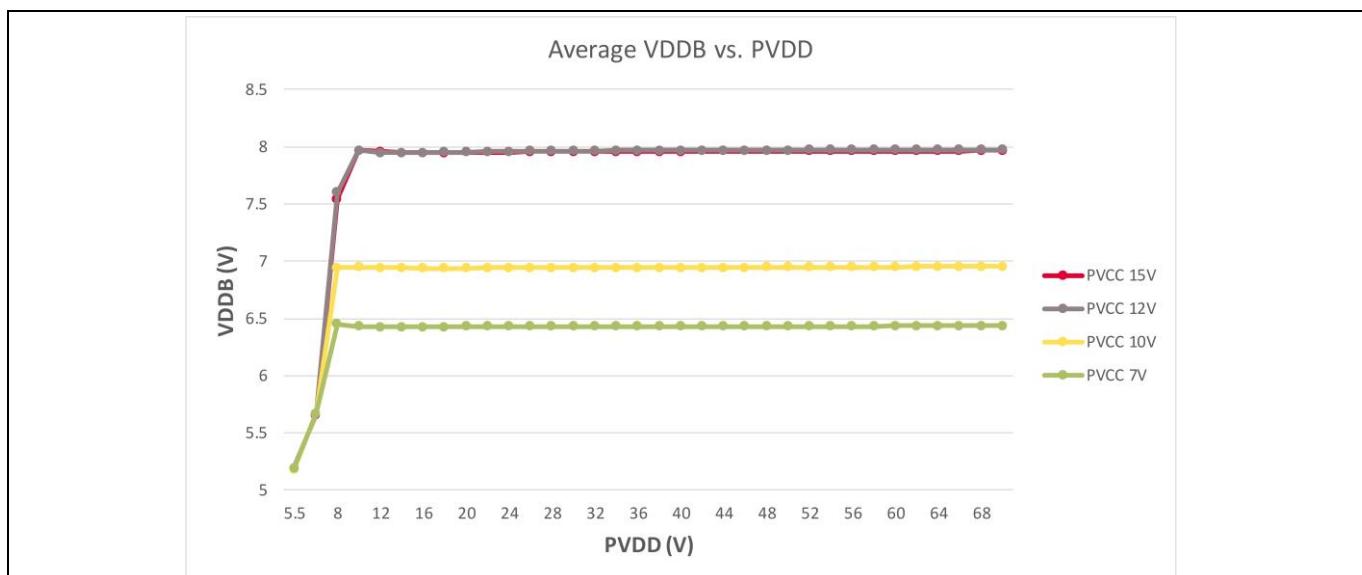
## General Product Characteristics



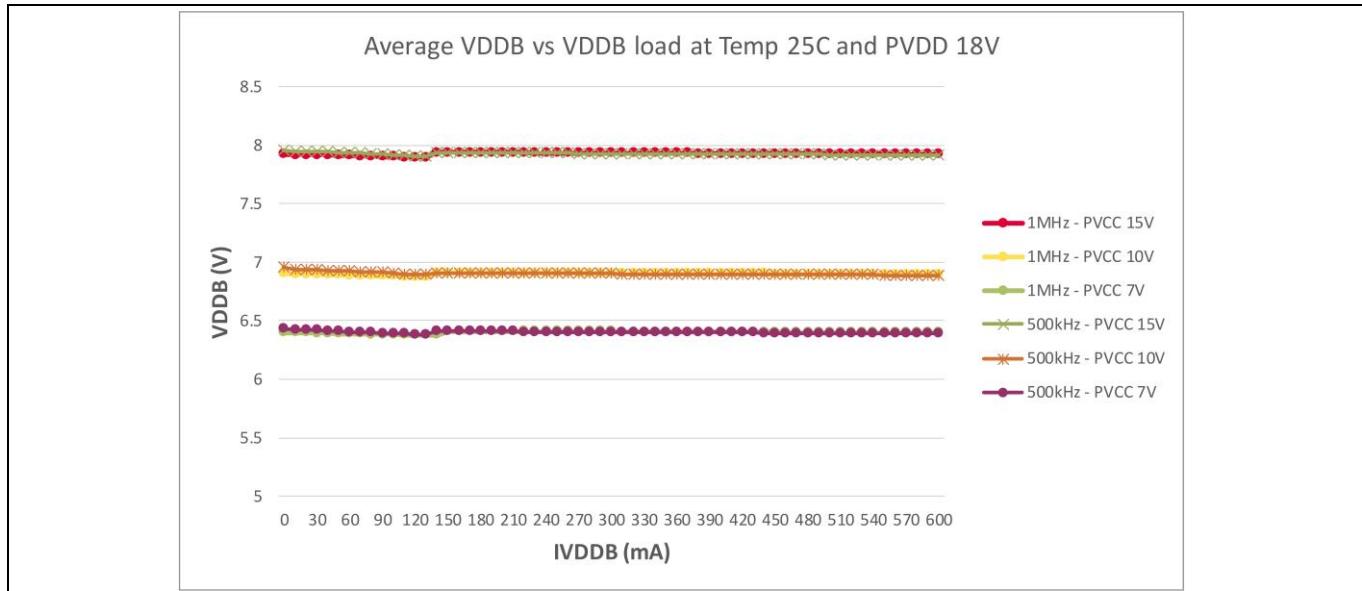
**Figure 12 High side gate driver supply (VCCHS-PVDD) average voltage vs VCCHS load for different PVCC configurations at PVDD 5.5V. Typical application with  $C_{CP1(2)} = 220\text{nF}$  and  $C_{VCCHS} = 1\mu\text{F}$ . VCCLS load 20mA**



**Figure 13 DVDD 3.3V output voltage vs DVDD load at different temperatures**

**General Product Characteristics**

**Figure 14 DVDD 5.0V output voltage vs DVDD load at different temperatures**

**Figure 15 Buck converter average output voltage (VDDB) vs. PVDD voltage. Typical configuration, with VDDB load 200mA and DVDD load of 50mA, buck converter switching frequency 500kHz, PVDD 18V**

## General Product Characteristics



**Figure 16 Buck converter average output voltage (VDDB) vs VDDB load (IVDDB) for different PVCC and buck switching frequency operations. Typical configuration with PVDD 18V.**

### 3 Product Features

#### 3.1 Functional Block Diagram

Figure 17 shows a simplified block diagram including main building blocks. In following sections, each of this building blocks and main device features will be introduced in greater detail.

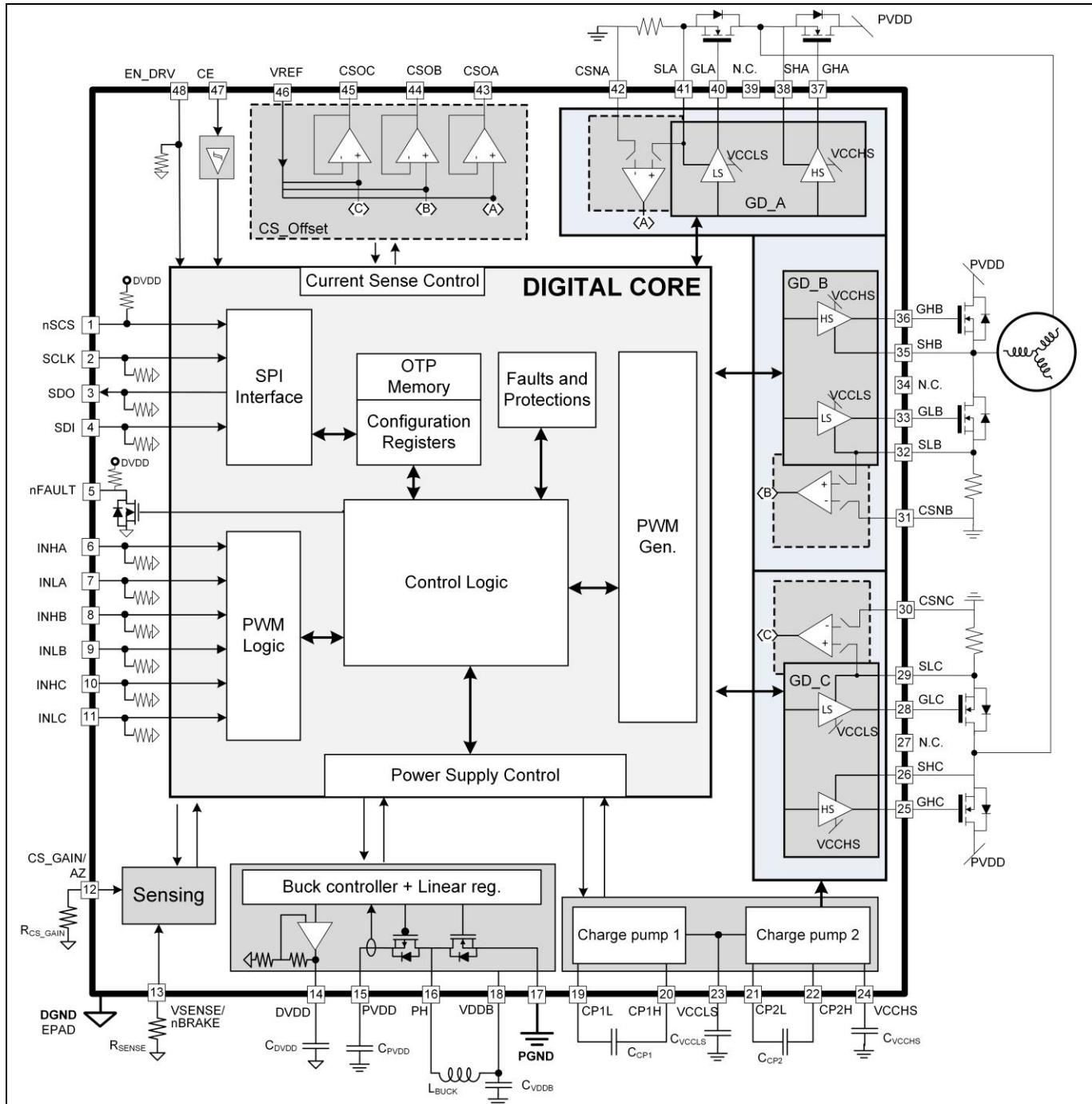


Figure 17 Functional block diagram

### 3.2 PWM Modes

6EDL7141 offers four different PWM modes and a sub-variant to address different MCU needs. The first mode is 6PWM and drives the gate driver in a classic way by using 6 PWM signals from the MCU. 6EDL7141 implements additionally three other modes, where it applies intelligence to simplify the PWM generation on the microcontroller side. That together with integrated protection features results in a highly robust and faster development for drives applications. An intelligent dead time unit will ensure no shoot through happens at any condition. A highly configurable braking mode provides safe reaction to motor or system events.

6EDL7141 supports following PWM modes that can be selected via bitfield PWM\_MODE:

1. 6PWM
2. 3PWM
3. 1PWM and commutation pattern
4. 1PWM with Hall sensor commutation
5. 1PWM mode with Hall sensor commutation and alternating recirculation

Following subsections provide further details on each of the PWM modes and sub-modes.

**Note:** *It is possible to use only one or two phases instead of the 3 phases, like for instance in a full bridge configuration. In such case, it is recommended to keep INHx and INLx signals of the unused phases shorted to DGND and the GHx, GLx, SHx and SLx signals open.*

#### 3.2.1 PWM with 6 Independent Inputs – 6PWM

When the PWM\_MODE register is set to b'0 then 6EDL7141 is configured for 6 independent PWM inputs. In this mode the system microcontroller (MCU) provides 3 pairs of complementary PWM signals with dead time between high side and low side PWM. A minimum dead time will be observed by 6EDL7141, for safety reasons, in order to avoid strong shoot through condition.

VSENSE/ nBRAKE pin can be used for braking the motor in a controlled manner. See 3.2.6 for more information on braking modes.

Table 8 shows the truth table for 6PWM mode while Figure 18 shows a system diagram for this mode.

**Table 8 Truth table for 6PWM mode.**

INHx	INLx	VSENSE/nBRAKE	GHx	GLx	SHx
1	1	1	LOW	LOW	High-Z
1	0	1	HIGH	LOW	HIGH
0	1	1	LOW	HIGH	LOW
0	0	1	LOW	LOW	High-Z
X	X	0	Brake cfg.	Brake cfg.	Brake cfg.

**Note:** X means any level

**Note:** Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z

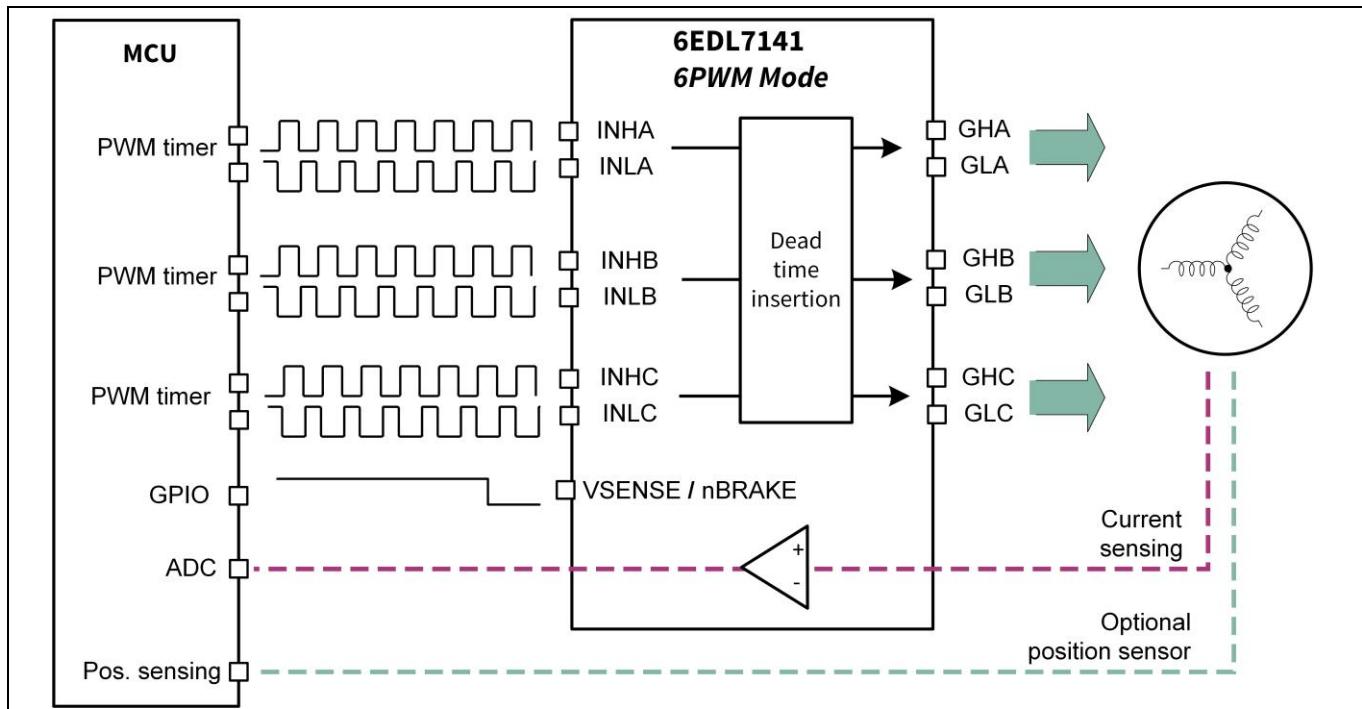
**Product Features**

Figure 18 6PWM mode scheme

**3.2.2 PWM with 3 Independent Inputs – 3PWM**

6EDL7141 can be configured to 3PWM mode by setting PWM\_MODE bitfield to value b'001. In such case, only 1 PWM signal (high side) per phase is necessary. 6EDL7141 will automatically generate the low side signals according to Table 9 and will insert a configurable dead time. Dead time is independently programmable for high to low (fall of phase node voltage) and low to high (rise of phase voltage) transitions through bitfields DT\_RISE and DT\_FALL.

INLx signals are ignored in this mode.

VSENSE/nBRAKE pin can be used for braking the motor. See 3.2.6 for more information on braking modes.

Figure 19 depicts a system diagram for this PWM mode.

**Table 9 Truth table for 3PWM mode.**

INHx	INLx	VSENSE/nBRAKE	GHx	GLx	SHx
1	0	1	HIGH	LOW	HIGH
0	0	1	LOW	HIGH	LOW
X	1	1	LOW	LOW	High-Z
X	X	0	Brake cfg.	Brake cfg.	Brake cfg.

Note: X means any level

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z

## Product Features

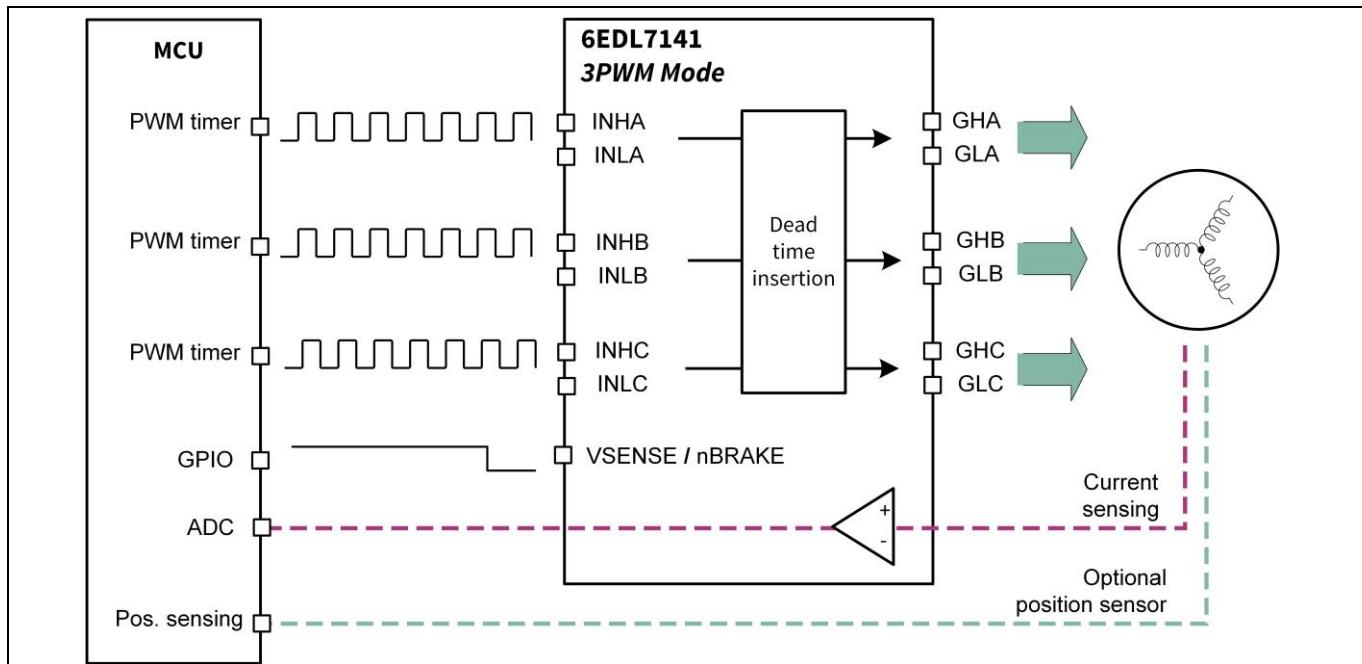


Figure 19 3PWM mode scheme

### 3.2.3 PWM with 1 Input and Commutation Pattern – 1PWM

When the PWM\_MODE register is set to b'010 then 6EDL7141 is configured to 1PWM mode. In this case, the duty cycle and frequency of signal INHA is used to determine the duty cycle (or amplitude) and the frequency of the PWM outputs generated by 6EDL7141. The rest of inputs are captured to decide the commutation pattern or state of the outputs. INHC signal can be used to implement 12 step block or trapezoidal commutation or trapezoidal. Dead time is automatically inserted according to programmed values in bitfields DT\_RISE and DT\_FALL.

Figure 20 shows a schematic diagram of 1PWM mode

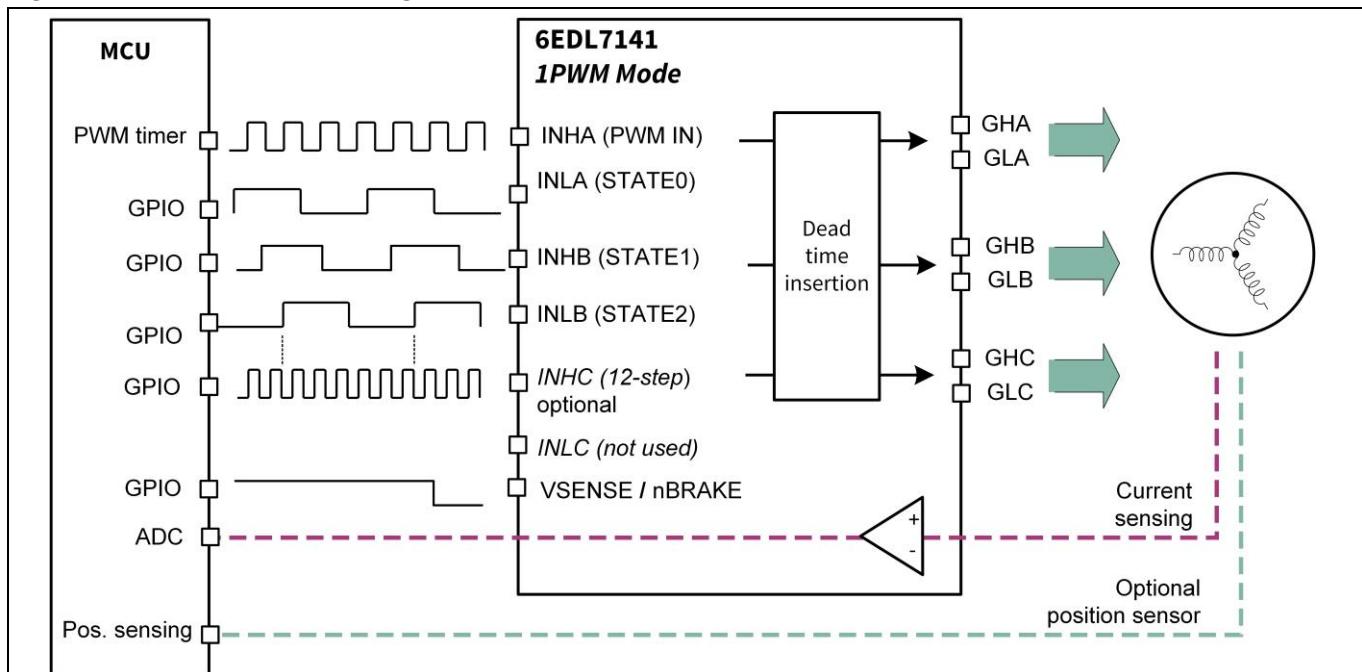


Figure 20 1PWM mode scheme

## Product Features

Additionally, the user has the option to select between two main commutation schemes programmable via register bitfield PWM\_FREEW\_CFG:

- **Diode freewheeling** – bitfield PWM\_FREEW\_CFG =b'0: in this case, the freewheeling current will flow through the low side MOSFET body diodes. The truth table for this mode is shown in Table 10.
- **Active freewheeling** – bitfield PWM\_FREEW\_CFG =b'1: in this case the low side MOSFETs will be switched synchronously to reduce conduction losses on the body diode conduction. The truth table for this mode is shown in Table 11. Note:

### 12 Step Trapezoidal or Block Commutation

Input INHC can be optionally used to create a 12 step trapezoidal commutation. This method energizes up to two phases at the same time in contrast to 6 step, where only one is active at any time. In 12 step trapezoidal commutation, torque ripple is improved and the angle created between stator and rotor flux vectors can be controlled within 30degree accuracy instead of 60degree in 6 step trapezoidal commutation. This method improves motor efficiency and torque ripple, however requires additional position information. This information can be processed by a microcontroller to produce signals INHA, INLA, INHB, INLB and INHC according to Table 10 or Table 11. As can be seen, from a system perspective, the INHC signal must toggle at every 30degree rotation (electrical).

In case the INHC signal is not toggled, the device will apply the commutation as shown in Table 10 or Table 11. As an example, if INHC is left low, a classic 6 step trapezoidal commutation pattern will be produced. In case INHC is pulled high, the pattern will show a 30 degree advanced with respect to a standard 6 step trapezoidal commutation. The user can use this variants or toggle the INHC pin every 30 degree of rotation to create a 12 step commutation pattern.

VSENSE/ nBRAKE pin can be used for braking the motor. See 3.2.6 for more information on braking modes.

Here is a summary of inputs and output functionalities:

- INHA - PWM input, defines PWM output duty cycle and frequency
- INLA, INHB, INLB - Provide timing for modulation pattern changes
- INHC – Signalizes 12 step states. Must toggle every electrical 30degree
- INLC – This input is ignored in this mode. Recommended pull down.
- VSENSE/ nBRAKE signal – When active, 6EDL7141 will force the motor to brake.
- GHA, GLB, GHB, GLB, GHC, GLC – Complementary PWM Output signals

Table 10 shows the possible states for this PWM mode using diode freewheeling while Table 11 does it for active freewheeling.

**Table 10      Truth table for 1PWM mode with diode freewheeling.**

State	INPUTS								OUTPUTS			
	INLA, INHB, INLB,	INHC	VSENSE/ nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
AB	011	0	1	PWM	LOW	LOW	HIGH	LOW	LOW	HIGH	LOW	-
AB_CB	010	1	1	PWM	LOW	LOW	HIGH	PWM	LOW	HIGH	LOW	HIGH
CB	010	0	1	LOW	LOW	LOW	HIGH	PWM	LOW	-	LOW	HIGH
CB_CA	110	1	1	LOW	HIGH	LOW	HIGH	PWM	LOW	LOW	LOW	HIGH
CA	110	0	1	LOW	HIGH	LOW	LOW	PWM	LOW	LOW	-	HIGH
CA_BA	100	1	1	LOW	HIGH	PWM	LOW	PWM	LOW	LOW	HIGH	HIGH

**Product Features**

State	INPUTS									OUTPUTS		
	INLA, INHB, INLB,	INHC	VSENSE/ nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
BA	100	0	1	LOW	HIGH	PWM	LOW	LOW	LOW	LOW	HIGH	-
BA_BC	101	1	1	LOW	HIGH	PWM	LOW	LOW	HIGH	LOW	HIGH	LOW
BC	101	0	1	LOW	LOW	PWM	LOW	LOW	HIGH	-	HIGH	LOW
BC_AC	001	1	1	PWM	LOW	PWM	LOW	LOW	HIGH	HIGH	HIGH	LOW
AC	001	0	1	PWM	LOW	LOW	LOW	LOW	HIGH	HIGH	-	LOW
AC_AB	011	1	1	PWM	LOW	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Align	111	X	1	PWM	LOW	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Stop	000	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
Brake	XXX	X	0	Brake cfg.								

Note: X means any level

Note: SHx when HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage according to PWM signals. '-' represents floating state, meaning both high side and low side MOSFETs are OFF

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z

**Table 11 Truth table for 1PWM mode with active freewheeling.**

State	INPUTS									OUTPUTS		
	INLA, INHB, INLB,	INHC	VSENS E/nBRA KE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
AB	011	0	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
AB_CB	010	1	1	PWM	!PWM	LOW	HIGH	PWM	!PWM	HIGH	LOW	HIGH
CB	010	0	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
CB_CA	110	1	1	LOW	HIGH	LOW	HIGH	PWM	!PWM	LOW	LOW	HIGH
CA	110	0	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
CA_BA	100	1	1	LOW	HIGH	PWM	!PWM	PWM	!PWM	LOW	HIGH	HIGH
BA	100	0	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
BA_BC	101	1	1	LOW	HIGH	PWM	!PWM	LOW	HIGH	LOW	HIGH	LOW
BC	101	0	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
BC_AC	001	1	1	PWM	!PWM	PWM	!PWM	LOW	HIGH	HIGH	HIGH	LOW
AC	001	0	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
AC_AB	011	1	1	PWM	!PWM	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Align	111	X	1	PWM	!PWM	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Stop	000	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
Brake	XXX	X	0	Brake cfg.	Brake cfg	Brake cfg	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.

Note: X means any level

## Product Features

Note: *SHx when HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage. ‘-’ is floating state, meaning both high side and low side MOSFETs are OFF*

Note: *Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z*

### 3.2.4 PWM with 1 Input and Commutation with Hall Sensor Inputs – 1PWM with Hall Sensors

6EDL7141 integrates three Hall sensor comparators (section 3.6.8) to detect pattern of movement in the motor. This can be used for rotor locked detection but can also be utilized to drive the PWM commutation pattern automatically allowing simplified PWM pattern in the MCU. This will enable cost sensitive applications in which a low end controller or some type of simple circuit is used to create basically a clock signal for INHA input.

To enable this PWM\_MODE bitfield needs to be configured to value b'011. The truth table presented in Table 12 dictates the commutation pattern. In this mode, 6EDL7141 together with Hall sensor inputs decides the switching pattern of the PWM output signals. The duty cycle and frequency of the output signals is determined by INHA duty cycle and frequency.

Dead time is inserted automatically according to programmed values in DT\_RISE and DT\_HALL.

In a similar way as section 3.2.3, the user has the option to select between two main commutation schemes programmable via bitfield PWM\_FREEW\_CFG in PWM\_CFG register: diode and active freewheeling. No truth table is shown for diode mode. This can be constructed by substituting “!PWM” cells in Table 12 by “LOW”.

Similarly to other PWM modes, VSENSE/nBRAKE pin can be used for braking the motor. See 3.2.6 for more information on braking modes.

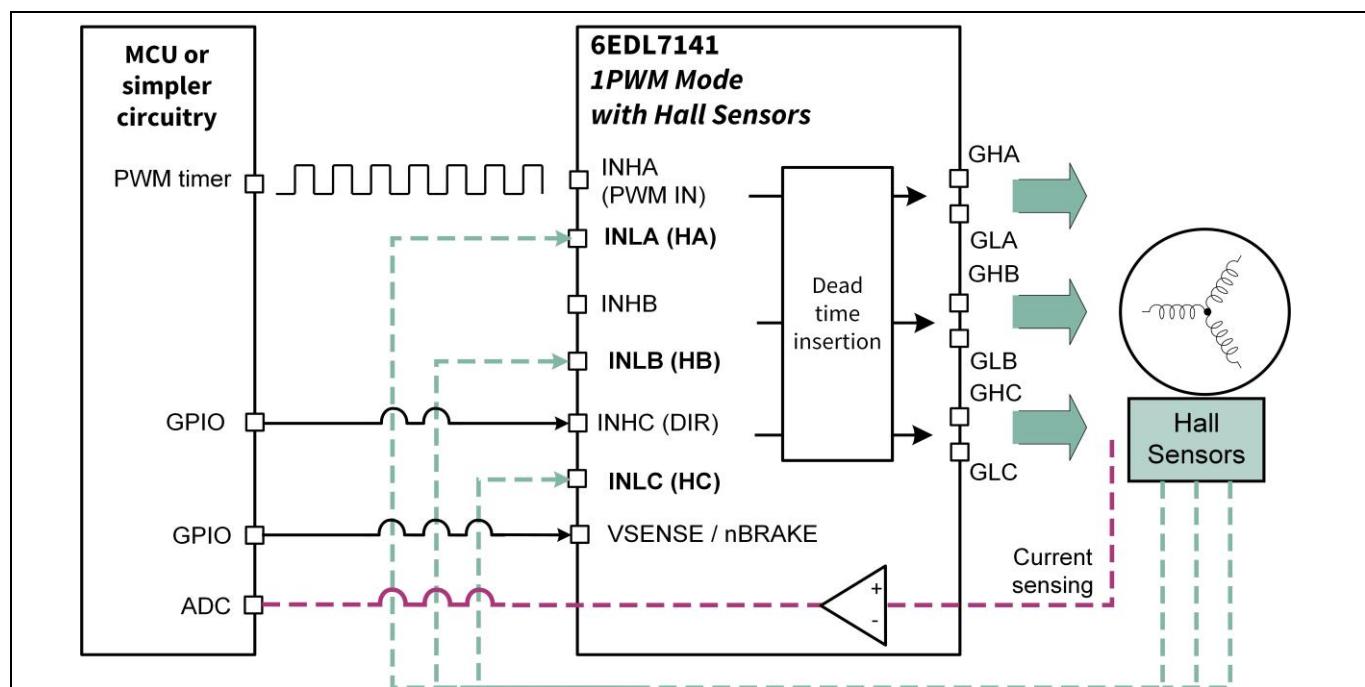


Figure 21 1PWM mode with hall sensors. Self-controlled pattern switching

**Table 12** Truth table for 1 PWM mode with active freewheeling.

INPUTS			OUTPUTS								
INLx [A,B,C]	INHC-Dir	VSENSE/ nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
101	1	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
100	1	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
110	1	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
010	1	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
011	1	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
001	1	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
101	0	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
100	0	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
110	0	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
010	0	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
011	0	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
001	0	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
XXX	X	0	Brake cfg.								
111	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
000	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-

Note: *X means any level. XXX means any other combination on inputs not shown*

Note: *Grey cells represent forbidden states and should be avoided*

Note: *SHx when HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage. ‘-’ represents floating state, meaning both high side and low side MOSFETs are OFF*

Note: *For diode freewheeling mode, substitute “!PWM” cells by “LOW”*

Note: *Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z*

These are the signals functionality for this mode:

- INHA - PWM input, defines duty cycle and frequency of PWM output signals
- INLA, INLB, INLC - Hall Sensor Inputs (HA, HB, HC) will define the PWM output pattern depending on motor position.
- VSENSE/ nBRAKE signal – when active, 6EDL7141 will force a brake event.
- INHC - Direction control. Provided by a microcontroller, will define direction of motor rotation.
- GHA, GLA, GHB, GLB, GHC, GLC – PWM output signals, high side and low sides.

A schematic representation of the commutation states is presented in Figure 22.

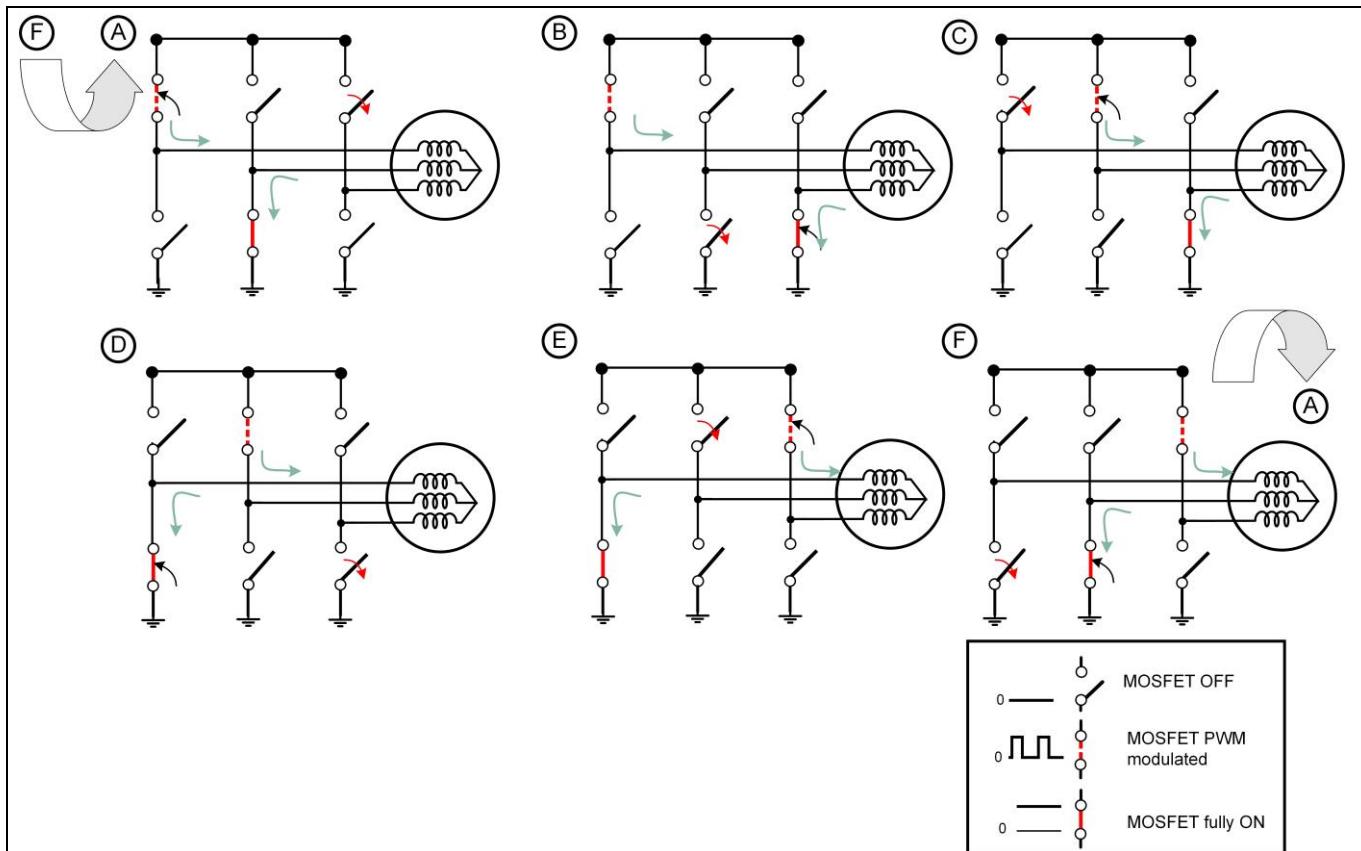


Figure 22 6 states switching overview. Diode freewheeling mode is represented here for simplification. Single direction considered.

### 3.2.5 PWM with 1 Input and Commutation with Hall Sensor Inputs and Alternating Recirculation – 1PWM with Hall Sensors and Alternating Recirculation

Thermal management in power tools systems is a key factor for achieving higher power densities. A more advanced thermal management might allow smaller heat sink components or smaller PCB area. This PWM mode focuses on distributing the MOSFET stress more evenly between all MOSFETs in the inverter. This concept alternates the recirculation of the freewheeling current between high side and low side MOSFETs. This is achieved by extending the truth table shown in Table 12 into Table 13.

On the first rotation (electrical), the inverter will recirculate the current through the high side MOSFETs (PWM modulated MOSFET) and the low side MOSFET will be always ON. In the second electrical rotation, the low side MOSFETs will recirculate the freewheeling current (PWM modulated MOSFET), and therefore, the high side is the one fully ON. This cycle repeats in further rotations. A graphical representation for the switching states is presented in Figure 23. In this figure, states A to F represent high side modulation while states G to L represent the low side modulation. The state machine will return to state A after state L, starting over again the cycle.

PWM\_FREEW\_CFG configures this mode as well either as diode or active freewheeling. No truth table is shown for diode mode. This can be constructed by substituting “!PWM” cells with LOW in Table 13.

**Product Features****Table 13 Truth table for 1 PWM mode with active freewheeling and alternating recirculation**

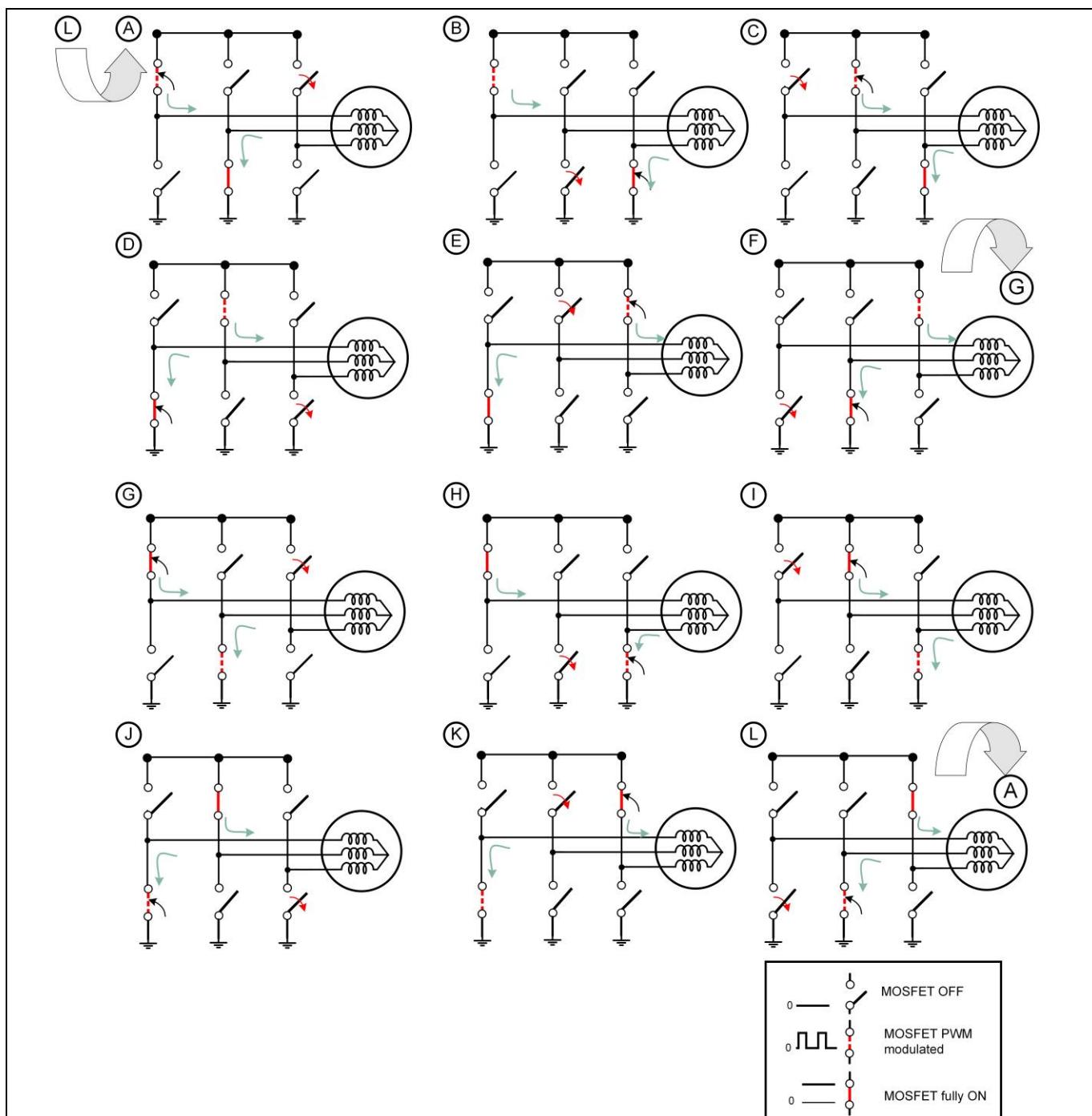
INPUTS			OUTPUTS								
INLx [A,B,C]	VSENSE/ nBRAKE	Fully ON	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
<b>INHC (Dir)=1</b>											
101	1	Low side	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
100	1	Low side	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
110	1	Low side	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
010	1	Low side	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
011	1	Low side	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
001	1	Low side	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
101	1	High side	HIGH	LOW	LOW	LOW	!PWM	PWM	HIGH	-	LOW
100	1	High side	LOW	LOW	HIGH	LOW	!PWM	PWM	-	HIGH	LOW
110	1	High side	!PWM	PWM	HIGH	LOW	LOW	LOW	LOW	HIGH	-
010	1	High side	!PWM	PWM	LOW	LOW	HIGH	LOW	LOW	-	HIGH
011	1	High side	LOW	LOW	!PWM	PWM	HIGH	LOW	-	LOW	HIGH
001	1	High side	HIGH	LOW	PWM	!PWM	LOW	LOW	HIGH	LOW	-
<b>INHC (Dir)=0</b>											
101	1	Low side	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
100	1	Low side	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
110	1	Low side	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
010	1	Low side	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
011	1	Low side	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
001	1	Low side	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
101	1	High side	!PWM	PWM	LOW	LOW	HIGH	LOW	LOW	-	HIGH
100	1	High side	LOW	LOW	!PWM	PWM	HIGH	LOW	-	LOW	HIGH
110	1	High side	HIGH	LOW	!PWM	PWM	LOW	LOW	HIGH	LOW	-
010	1	High side	HIGH	LOW	LOW	LOW	!PWM	PWM	HIGH	-	LOW
011	1	High side	LOW	LOW	HIGH	LOW	!PWM	PWM	-	HIGH	LOW
001	1	High side	!PWM	PWM	HIGH	LOW	LOW	LOW	LOW	HIGH	-
XXX	0	X	Brake cfg.								
111	1	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
000	1	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-

Note: X means any level. Grey cells represent forbidden states and should be avoided

Note: SHx when HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage. ‘-’ represents floating state, meaning both high side and low side MOSFETs are OFF

Note: For diode freewheeling mode, substitute “!PWM” cells by “LOW”

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z



**Figure 23 12 states switching overview for alternating recirculation. 6 new states are included (G to L) compared to other 1PWM modes. Diode clamping is represented here for simplification. Single direction considered**

### 3.2.6 PWM Braking Modes

In all PWM modes presented previously, the device can go into a controlled braking mode. This braking mode will drive PWM signals in a way that the motor goes to a safe state in a controlled manner. This is of critical importance for some power tools applications where a sudden or uncontrolled braking can destroy elements of the tool or become a hazard to the user safety. Following events can trigger the braking action in 6EDL7141:

- Pull down of pin VSENSE/nBRAKE

# 6EDL7141

Datasheet

## Product Features

- Overcurrent protection (OCP) fault on current sense amplifiers -programmable
- Watchdog timer fault-programmable

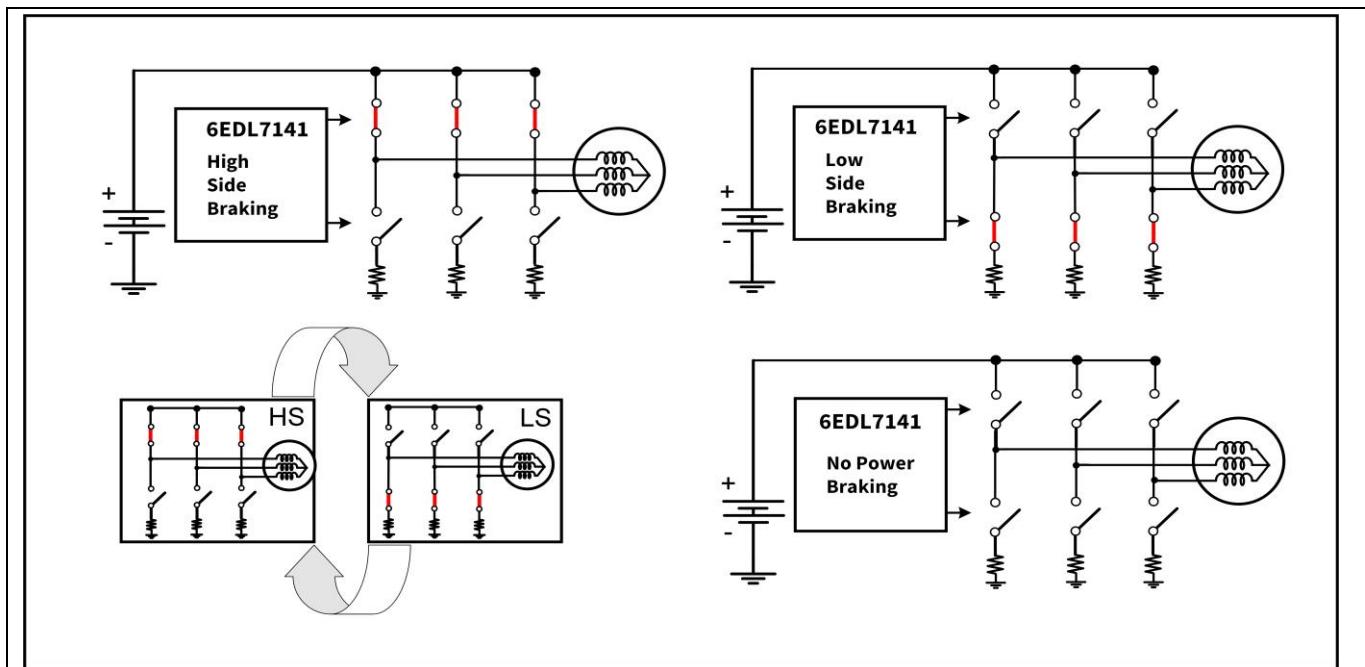
From them, pin VSENSE/nBRAKE is the only that can be actively used by, for example a microcontroller to start a braking event. All other 3 are the reaction to a fault-detection.

Pin VSENSE/ nBRAKE shall be high for normal operation of the motor. However, as soon as a falling edge is detected in it, the gate driver logic will activate high side MOSFETs or low side MOSFETs therefore braking the motor actively.

6EDL7141 braking circuitry can be configured as illustrated in Figure 24 in the following modes by programming bitfield BRAKE\_CFG in register PWM\_CFG:

- **Low side MOSFET braking:** upon a braking event, all low side MOSFET will be activated and all high side MOSFET switched off.
- **High side MOSFET braking:** upon a braking event, all high side MOSFET will be activated and all low side MOSFET switched off
- **Alternate braking mode:** upon every new braking event, the system alternates between high side MOSFET braking and low side MOSFET braking. With alternate braking, stress on MOSFETs is distributed equally, therefore improving system robustness.
- **Non-power braking-high impedance (high Z) outputs:** upon a braking event all switches are forced to high Z mode. Currents present in motor windings will recirculate through MOSFET body diodes or other available structures in the inverter. This mode is recommended if a MOSFET short occurs in the inverter.

The system microcontroller (MCU) can modify brake related bitfields during run time of the system to adapt to given conditions.



**Figure 24      System overview for the different braking modes supported**

Before the braking action starts, 6EDL7141 prepares the inverter as fast as possible for a safe braking. Depending on the inverter state at the moment of the braking request, the device will need to switch off some MOSFETs and insert dead times. For example, if the braking signal arrives when phase A is, high side switched-off and low side switched-on, and assuming a high side braking configuration, then 6EDL7141 will immediately switch off the low

**Product Features**

side MOSFET, insert the configured dead time and finally switch on the high side MOSFET of phase A with the rest of high side MOSFETs.

### 3.2.7 Dead Time Insertion

The PWM unit in 6EDL7141 inserts automatically a dead time between complementary signals (GHx – GLx). DT\_RISE bitfield defines the dead time period for rising transition (of phase node voltage) while DT\_FALL defines independently the period for the falling transition. A minimum dead time (see Electrical Characteristics table for detailed values and conditions) will always be observed to avoid strong shoot through condition.

Figure 25 shows a detailed signal diagram of a 1PWM mode dead time insertion including the timing definitions. A propagation time ( $t_{PROP\_HS}$  and  $t_{PROP\_LS}$ ) elapses between the input signal and the actual gate driver output signals. These timing definitions are applicable to all other PWM modes.

Dead time and slew rate control features are designed in a safe way so that a change in slew rate will update in a synchronous manner to the PWM switching. This hinders any possible shoot through during the possible update of the slew rate during operation due to miss-alignment of timings.

**Note:** *The application software, must ensure that dead time is sufficient for the slew rate configuration and the MOSFETs selection. Current sense amplifier OCP can be used to detect excessive current in the system.*

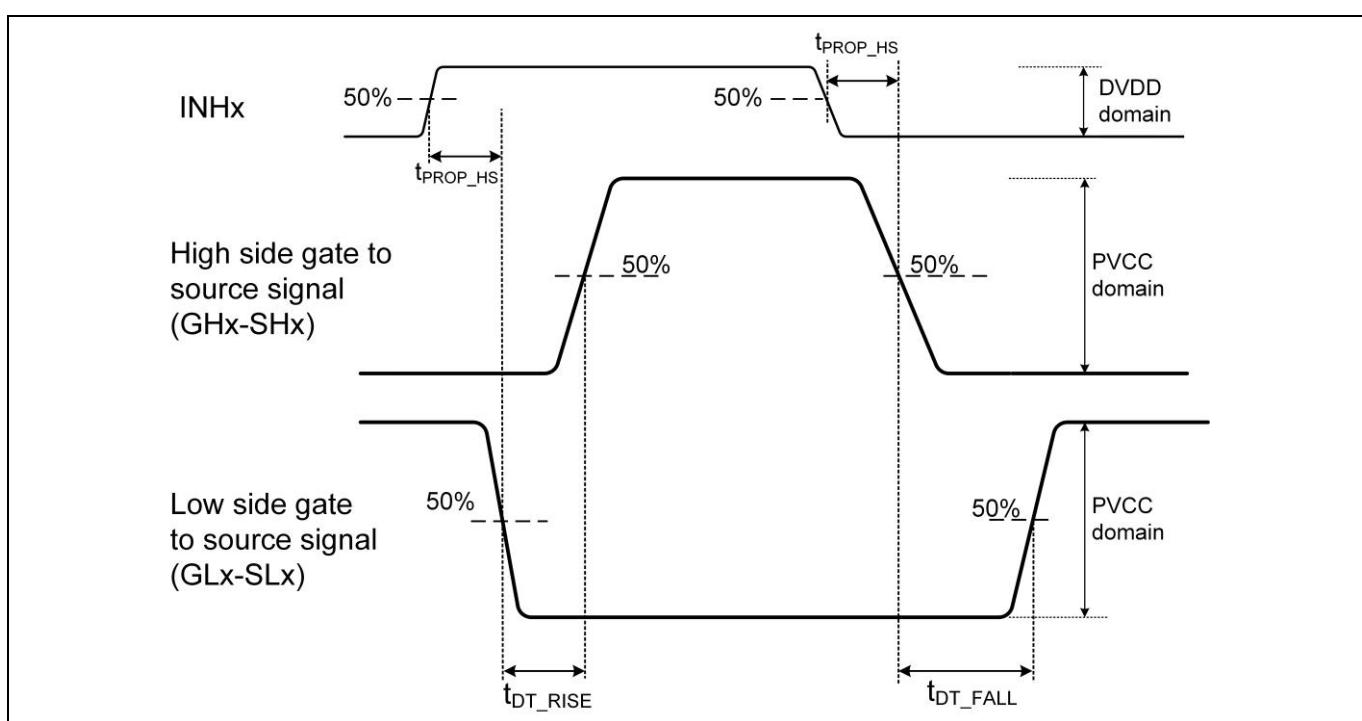


Figure 25 PWM insertion ideal timing diagram for 1PWM mode

### 3.3 Integrated Three Phase Gate Driver

6EDL7141 three phase integrated gate driver is a floating driver capable of driving with configurable slew rate and driving voltage, a 3 phase 2 level inverter with up to 1.5A of both sourcing and sinking peak currents.

Programmable charge pumps supply the gate drivers ensuring 100% duty cycle and configurable driving voltage for maximum optimization of the gate driver.

Numerous protections are included to ensure safe operation of the gate driver system under stress conditions including improved phase node ( $V_{SHx}$ ) tolerance to negative voltage spikes (see Absolute Maximum Ratings table).

Configurations and settings are shared by all three half bridge drivers. This section describes the following features of the integrated three phase gate driver:

- Gate Driver Architecture
- Slew Rate Control
- Charge Pump Configurations
- Protections

#### 3.3.1 Gate Driver Architecture

Three identical pairs of high side and low side drivers are integrated. High and low side drivers are designed with the same architecture. However, supply domains for both sections are developed differently. Precise charge pumps are utilized to supply both drivers, VCCLS to the low side gate drivers, and VCCHS to the high side gate drivers. An overview of the general architecture is shown in Figure 26.

The low side section of the gate driver is supplied by VCCLS. When the device is under normal operation, VCCLS is “PVCC” volts above ground. VCCLS voltage is generated by “LS Charge Pump” from VDDB voltage –integrated buck converter output voltage. An external “flying” capacitor  $C_{CP1}$  is required for the charge pump to work properly.

The high side section of the gate driver is supplied by VCCHS. A separated charge pump generates “PVCC” volts above PVDD for properly bias of the high side MOSFET drivers. Similarly to low side section, a “flying” capacitor  $C_{CP2}$  is necessary for proper operation of the charge pump. PVCC voltage is programmable via SPI registers and defines the gate driving voltage of the inverter power MOSFETs.

Additional decoupling capacitors  $C_{VCCLS}$  and  $C_{VCCHS}$  are required for VCCLS and VCCHS pins respectively. These and other required components recommended values are shown in Table 22.

The selection of those capacitors will have an impact in different parameters in the charge pump including the voltage ripple in VCCLS/HS, as well as the start-up time or the maximum load that the gate driver can sustain.

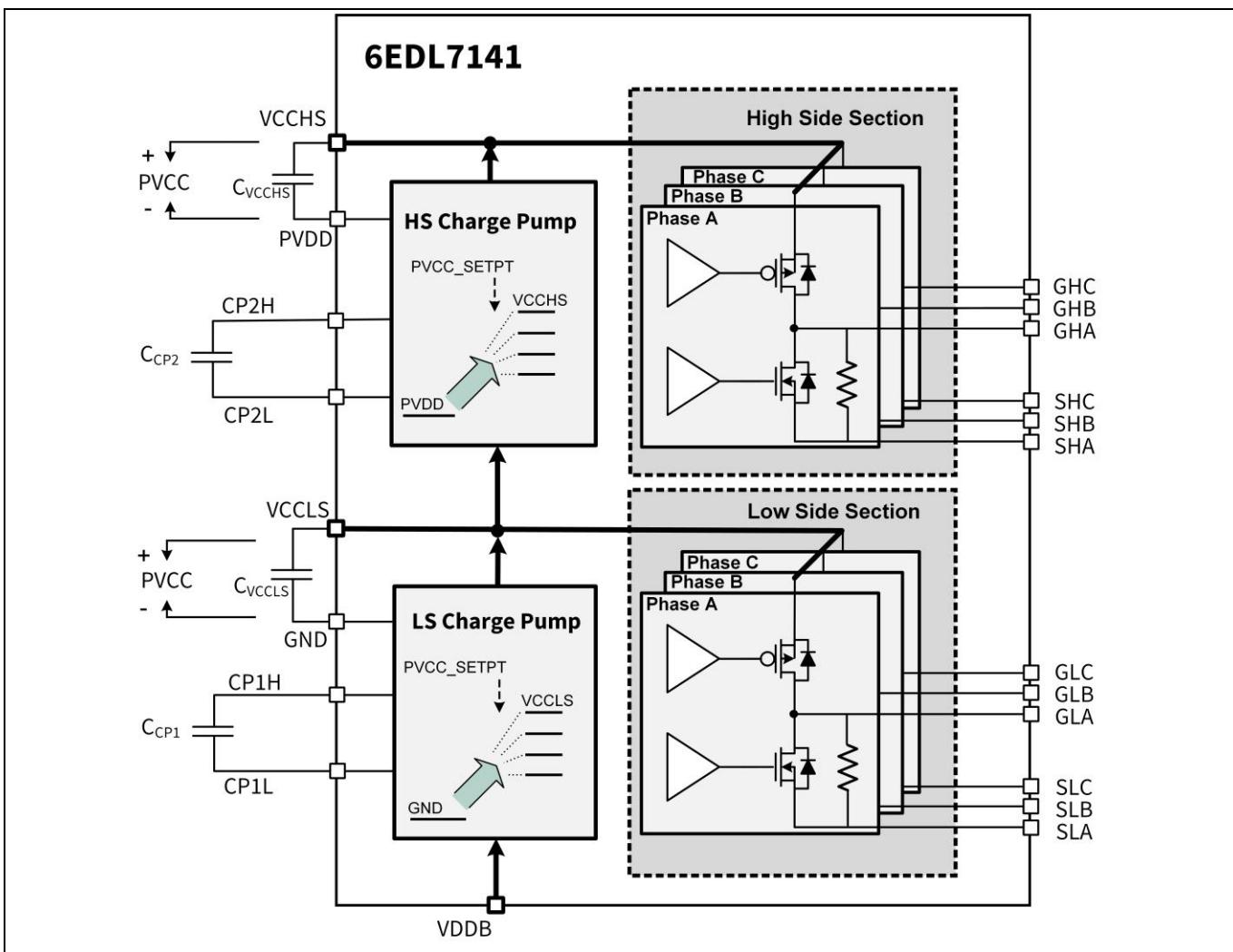


Figure 26 Gate driver architecture overview

### 3.3.2 Slew Rate Control

Control of MOSFET  $V_{DS}$  rise and fall times is one of the most important parameters for optimizing drive systems, affecting critical factors like:

- Switching losses,
- Dead time optimization,
- $V_{DS}$  ringing with possible avalanche event in MOSFETs. Avalanche is a critical factor in MOSFETs that can lead to device destruction or reliability issues,
- EMI design and optimizations,
- Control of negative spike in SHx pins,
- Possible snubber design (MOSFET snubber or bridge bypass capacitors)

6EDL7141 is capable of adjusting the slew rate of the MOSFET switching ( $V_{DS}$ ). Slew rate control functionality controls independently the rise (low to high) and fall (high to low) slew rates of the drain-to-source voltage by adjusting the gate current applied to MOSFET gate.

**Note:**  $R_g$  resistors might be used, however, user must consider the voltage drop on the resistor when driving the MOSFET with the constant current provided by 6EDL7141.

## Product Features

### 3.3.2.1 Slew Rate Control Parameters and Usage

User can configure the gate driver current and timings with following parameters via SPI accessible registers:

- $I_{HS\_SRC}$  – bitfield IHS\_SRC: gate driver current value for switching **ON high side** MOSFETs
- $I_{HS\_SINK}$  – bitfield IHS\_SINK: gate driver current value for switching **OFF high side** MOSFETs
- $I_{LS\_SRC}$  – bitfield ILS\_SRC: gate driver current value for switching **ON low side** MOSFETs
- $I_{LS\_SINK}$  – bitfield ILS\_SINK: gate driver current value for switching **OFF low side** MOSFETs
- $I_{PRE\_SRC}$  – bitfield IPRE\_SRC: **pre-charge** gate driver current value for switching **ON both high and low side** MOSFETs. Needs to be enabled via bitfield IPRE\_EN, otherwise pre-charge will be set to max current.
- $I_{PRE\_SNK}$  – bitfield IPRE\_SNK: **pre-discharge** gate driver current value for switching **OFF both high and low side** MOSFETs. Needs to be enabled via bitfield IPRE\_EN, otherwise pre-discharge will be set to max current.
- $T_{DRIVE1}$  – bitfield TDRIVE1: amount of time that  $I_{PRE\_SRC}$  is applied. Shared configuration between high and low side drivers
- $T_{DRIVE2}$  – bitfield TDRIVE2: amount of time that  $I_{HS\_SRC}$  and  $I_{LS\_SRC}$  are applied. Shared configuration between high and low side drivers
- $T_{DRIVE3}$  – bitfield TDRIVE3: amount of time that  $I_{PRE\_SNK}$  is applied. Shared configuration between high and low side drivers
- $T_{DRIVE4}$  – bitfield TDRIVE4: amount of time that  $I_{HS\_SINK}$  and  $I_{LS\_SINK}$  are applied. Shared configuration between high side and low side drivers

A possible configuration is graphically presented in Figure 27. This represents a 6PWM mode in which the microcontroller inserts a specific dead time between INHx and INLx signals. The driving scheme is applicable to other PWM modes. Propagation delays are not depicted for simplification of the diagram (see Figure 25 for details on propagation delay).

Once the gate is commanded to apply a change to the output, the gate driver will apply a constant current defined by the user programmable value  $I_{PRE\_SRC}$  for a time defined by  $T_{DRIVE1}$ . After  $T_{DRIVE1}$  period, the MOSFET gate voltage should ideally have reached the threshold voltage ( $V_{GS(th)}$ ). After  $T_{DRIVE1}$ , the gate driver applies next gate current configuration for a period defined by  $T_{DRIVE2}$ . The current applied in this period is decisive to determine both  $dI/dt$  and  $dV/dt$  of the MOSFETs as it will charge the  $Q_{sw}$  of the MOSFETs. User can alternatively decide to reduce this period to cover only  $Q_{gd}$  portion, therefore controlling  $dI/dt$  region with the  $T_{DRIVE1}$  period for independent control. To ensure proper fine tuning, 6EDL7141 offers separate configuration registers for the high side and low side ( $I_{HS\_SRC}$  and  $I_{LS\_SRC}$  respectively) for this second period.

Once  $T_{DRIVE2}$  period is elapsed, the gate driver applies full current (1.5 A) to ensure fastest turn on of the MOSFET. This will fully charge the MOSFET gate ( $Q_{od} = Q_g - Q_{sw} - Q_{gs(th)}$ ) till the programmed PVCC value.

A similar process takes place in the discharge of the MOSFET

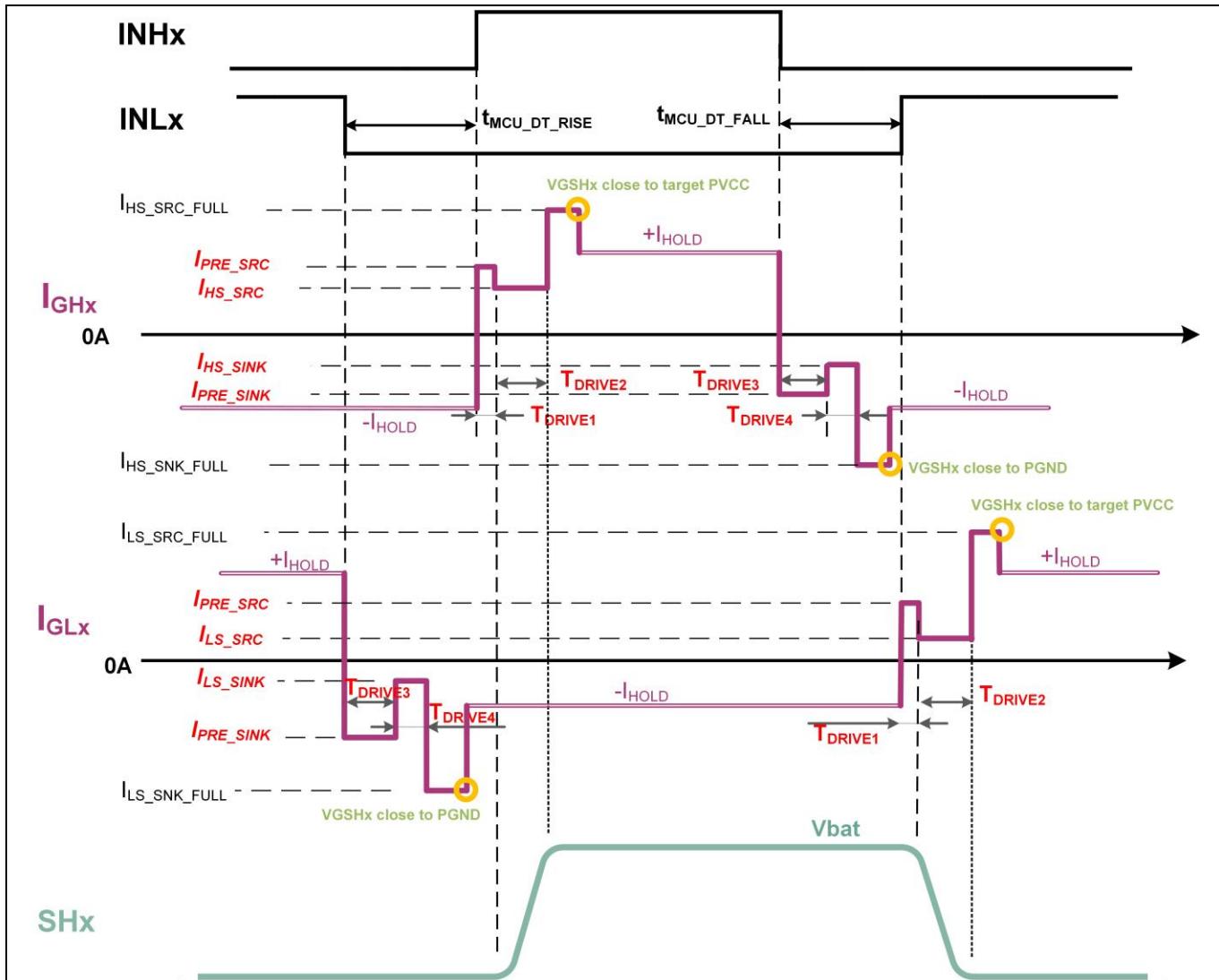
**Attention:** *Consider that slew rate variation affects the actual dead time value. User must select dead time accordingly*

## VGS Comparators

6EDL7141 integrates gate to source comparators. These are used to detect when the  $V_{GS}$  signal is almost at the target value PVCC, i.e.  $V_{GSX} \geq PVCC - V_{GS\_CPM\_TH}$  during charging phase and  $V_{GSX} \leq V_{GS\_CPM\_TH}$  during the discharge phase. When any of these happen, the comparator trips and sets the gate current to  $I_{HOLD}$  value. This is to reduce power consumption and help reducing the impact of the self-turn-on effect, for example when the high side MOSFET is turning on while the low side MOSFET is off. In this case, the hold current in the low side MOSFET will help tightening down the gate of that MOSFET to the source with  $I_{HOLD}$  strength. In Figure 27  $I_{HOLD}$  is shown as dashed and depending on  $V_{GS}$  value will be applied sooner or later. In Figure 28 the thresholds for activating  $I_{HOLD}$  current are shown.

**Product Features**

The comparator integrates a deglitching stage that avoids noise to activate the comparator erroneously during noisy events. The deglitching time is defined by  $t_{VGS\_CMP\_DEGLITCH}$ .



**Figure 27 Slew rate control timing for a complete switching cycle on a 6PWM mode-dead time inserted by MCU. Propagation delays ( $INxy \rightarrow Gxy$ ) not considered for simplification. Parameters on red refer to programmable values**

Figure 28 shows a detail of the charging and discharging transitions for a high side MOSFET. Similar applies to a low side MOSFET. The different gate charge areas of the MOSFET are shown. Thanks to the flexible timing structure and the high  $T_{DRIVE}$  resolution, user has full control of the gate current applied during critical charge areas like  $Q_{sw}$  which is the key parameter controlling the MOSFET  $V_{DS}$  slew rate. This at the same time can be done while maintaining fast charging of other areas like  $Q_{od}$  which typically is relatively large compared to  $Q_{sw}$  and therefore, as it does not affect neither  $dV/dt$  nor  $dI/dt$ , can be accelerated by increasing gate current.

Additionally, the pre-charge area ( $Q_{g(th)}$ ), depending on the particular MOSFET, can benefit from a larger gate current than the one applied to the  $Q_{sw}$  region where maximum control is required. Thanks to the pre-charge current configuration, higher gate currents can be selected for  $Q_{gs(th)}$  reducing importantly the pre-charge timing, which otherwise could have needed several hundreds of ns to reach to  $V_{gs(th)}$ .

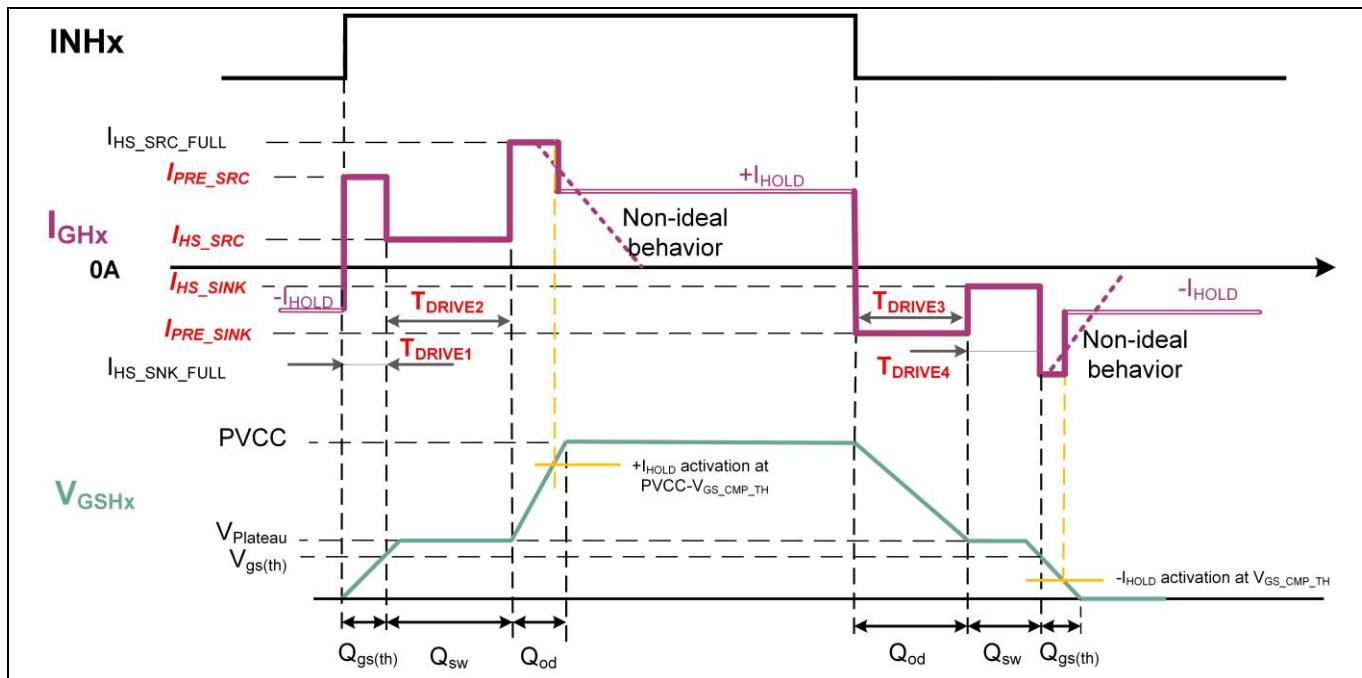
The pre-charge current can be selected from 17 different values. 16 defined by  $I_{PRE\_SRC/SNK}$  and additionally 1.5A, which is the maximum peak current capability of the gate driver. In case of large MOSFETs,  $Q_{gs(th)}$  during turn on

**Product Features**

or  $Q_{od}$  during turn off, might benefit from using the whole gate driver capability. In order to enable the full strength during the pre-charge area, register `I_PRE_EN` has to be set in register `IDRIVE_PRE_CFG`.

**Note:** When transitioning from one current setting to another, user can experience some transition period until new current value is up and stable. During this period, the current might become lower than programmed for a brief period before reaching the target value.

**Note:** When the gate to source voltage is getting close to the target voltage, either `PVCC` when charging or `PGND` when discharging, the gate driver will not be able to fully maintain the target  $I_G$  current. This effect deviates from the ideal behavior shown before and can follow similar behavior to the dashed lines in Figure 28. This is independent from the  $I_{HOLD}$  values described before.

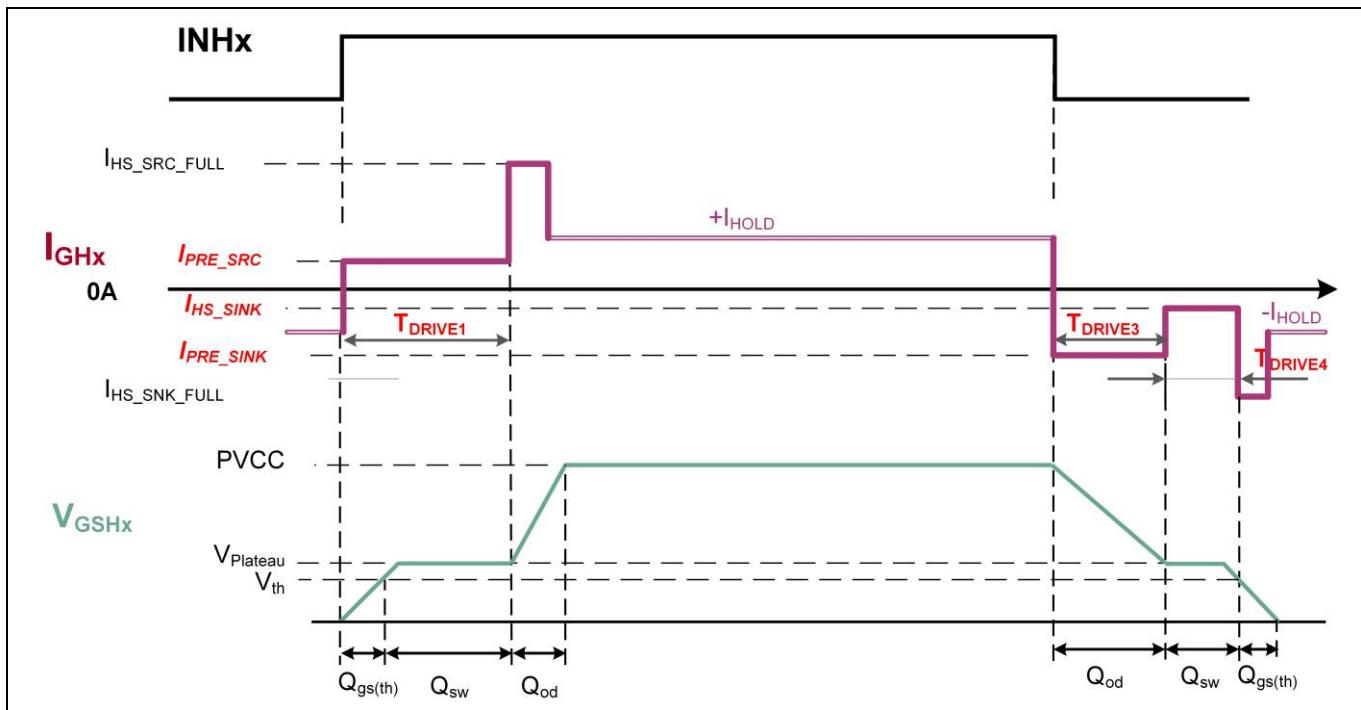


**Figure 28 Detail of MOSFET gate charge during the charging and discharging transitions**

In cases where  $Q_{g(th)}$  is too small to apply a larger current than the one used for slew rate control, user can set  $T_{DRIVE2}$  to value 0. This will result in the gate driver start driving the MOSFETs with  $T_{DRIVE1}$  and once the period is elapsed it will apply 1.5A ignoring  $T_{DRIVE2}$  configuration. This ensures optimal settings for both large and small MOSFETs and right fit for different technologies like OptiMOS™ or StrongIRFET™. Similarly,  $T_{DRIVE2}$ ,  $T_{DRIVE3}$  and/or  $T_{DRIVE4}$  can be set to 0 resulting in those configurations being skipped. Figure 29 shows an example of this behavior where  $T_{DRIVE2} = 0$  while other  $T_{DRIVEX}$  settings are different than zero.

**Note:** When driving with a single timing setting, it is recommended to use either  $T_{DRIVE1}$  or  $T_{DRIVE3}$  as driving period and make  $T_{DRIVE2}$  or  $T_{DRIVE4}$  equal to 0. The opposite is possible, however might result in selected timing ( $T_{DRIVE2}$  or  $T_{DRIVE4}$ ) becoming slightly shorter than the programmed value due to internal propagation delays. User must decide which solution fits better to the application

## Product Features

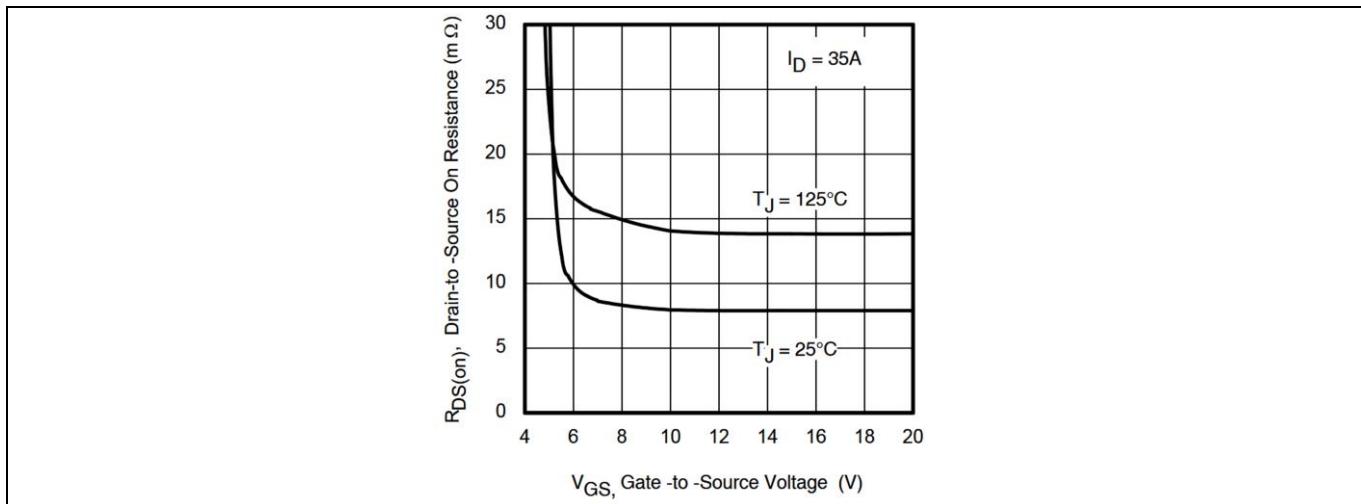


**Figure 29 Detail of MOSFET gate charge during the charging and discharging transitions.  $\text{T}_{\text{DRIVE2}}=0$  example**

### 3.3.3 Gate Driver Voltage Programmability

Different drives systems might benefit from different MOSFET technologies. An example is the common usage of logic level MOSFET vs standard or normal level MOSFETs, which show a higher threshold voltage ( $\text{V}_{\text{gs}(\text{th})}$ ). For the same gate to source voltage, a logic level MOSFET presents lower  $\text{R}_{\text{DSON}}$  value than a normal level MOSFET.

Increasing the driving voltage helps reducing the  $\text{R}_{\text{DSON}}$  of the MOSFET channel during conduction and as a result the conduction losses of the system. This is shown in Figure 30. However, increasing the driving voltage increases the rise switching times (rise and fall) leading eventually to higher switching losses. User must choose the right driving voltage depending on the system conditions.



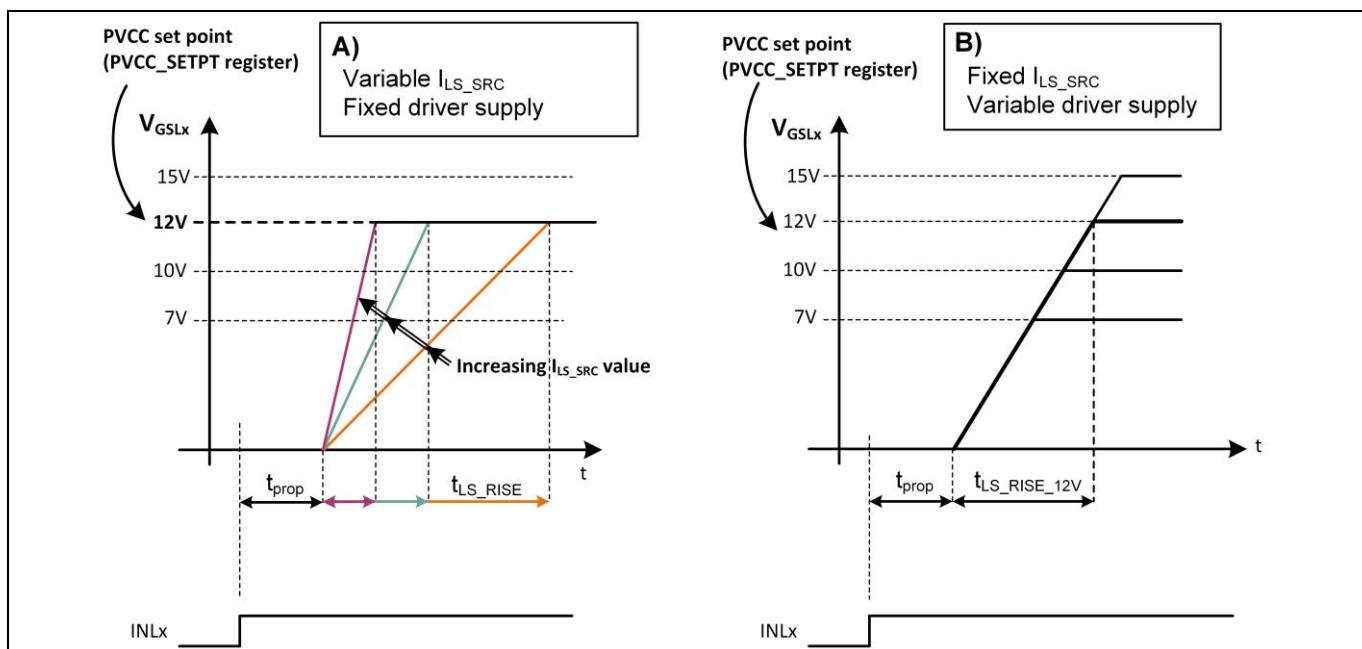
**Figure 30 Typical  $\text{R}_{\text{DSON}}$  vs  $\text{V}_{\text{GS}}$  characteristic in MOSFETs. Higher  $\text{V}_{\text{GS}}$  voltage reduces the  $\text{R}_{\text{DSON}}$  of the MOSFET**

**Product Features**

6EDL7141 allows designers to adjust the MOSFET driving voltage (PVCC voltage) via SPI registers. The same value PVCC applies to both high and low side charge pumps with four possible values: 7V, 10V, 12V, 15V. This is done via bitfield PVCC\_SETPT.

**Note:** *It is expected that the high side charge pump produces a slightly lower voltage due to internal circuitry (diode). See Electrical Characteristic Graphs.*

Figure 31 shows an ideal example of how supply voltage of the driver and slew rate control can play a role together in an ideal turn on of a low side MOSFET. Section A of the figure shows how to set the slew rate of  $V_{GS}$  external MOSFET, by programming different current values (in this case  $I_{LS\_RISE}$ ). Section B shows the case in which, provided a fixed gate driver current  $I_{LS\_SRC}$ , PVCC is varied.



**Figure 31** **Gate driver slew rate configurability in an ideal low side MOSFET switching: A) given a fixed supply voltage ( $PVCC=12V$ ), variable  $I_{LS\_RISE}$  B) Fixing the charging current, changes in PVCC produce different rise times**

## 3.4 Charge Pump Configuration

User can adjust charge pumps operation in 6EDL7141 depending on the specific needs. Following sections describe this configurations.

### 3.4.1 Charge Pump Clock Frequency Selection

Charge pumps are based on switched capacitor circuits that work at a given switching frequency. 6EDL714 offers the possibility to choose four different clock frequencies via SPI programming of bitfield CP\_CLK\_CFG in register CP\_CFG. The selection of charge pump capacitors both flying and tank capacitors must be chosen according to this configuration and both affect start-up time of VCCLS and VCCHS rails as well as possible voltage ripple in those pins.

### 3.4.2 Charge Pump Clock Spread Spectrum Feature

When activated, this feature introduces artificially a frequency variation (see Electrical Characteristics table for values) into the charge pump clock signal. The frequency at which the charge pump operates will vary between

## Product Features

those limits reducing the emission intensity on the target frequency value by distributing that energy over a wider range of frequencies.

### 3.4.3 Charge Pump Pre-Charge for VCCLS

Pre-charge of the charge pumps is a feature that, if enabled via SPI register, pre-charges the VCCLS rail right below the buck converter output voltage (VDDB) before the EN\_DRV pin is activated.

In this case, when EN\_DRV is activated to enable the driver stage, the charge pumps need to ramp up the voltage in  $C_{VCCLS}$  from the existing pre-charge voltage until the PVCC selected value, therefore reducing considerably the start-up time for the charge pump when compared to the default situation in which  $C_{VCCLS}$  needs to charge the whole PVCC voltage.

To enable the pre charge of VCCLS, bitfield CP\_PRECHARGE\_EN in register SUPPLY\_CFG must be set.

### 3.4.4 Charge Pump Tuning

The start-up time for the charge pumps, defined as the time that the VCCLS voltage requires to get to the target programmed voltage (PVCC Set point), depends on several factors:

- Target voltage programmed via PVCC\_SETPT register: the higher the longer the start-up time
- Charge pump clock frequency: higher clock frequency results in faster start-up time
- Charge pump tank capacitors ( $C_{VCCLS}, C_{VCCHS}$ ): using VCCLS as example, a smaller value of  $C_{VCCLS}$  will result in:
  - Higher VCCLS ripple
  - Faster start-up time
- Charge pump flying capacitors ( $C_{CP1}, C_{CP2}$ ): smaller capacitors lead to slower start-up time

The selection of those parameters have an impact as well in the VCCLS and VCCHS voltage ripple. If fast start-up time is not a design target, it is recommended to increase the  $C_{VCCLS}$  value to reduce ripple and to improve load transients. For a given  $C_{VCCLS}$  value, the selection of  $C_{CP1}$  will impact also the ripple in VCCLS and start-up time.

If start-up time needs to be optimized, charge pump pre-charge feature is recommended. This is explained in section 3.4.3

The start-up behavior of the charge pumps and rest of power supply is shown in detail in section Device Start-Up.

### 3.4.5 Gate Driver and Charge Pumps Protections

The gate driver includes following protections:

- VCCLS UVLO
- VCCHS UVLO
- Floating Gate Driver Pull Down
- Dead Time insertion - This is explained in section 3.2.7

#### 3.4.5.1 VCCLS Under-Voltage Lock-Out (VCCLS UVLO)

The UVLO avoids that the gate driver propagates PWM signals if the drive voltage is not above the UVLO threshold as specified in the Electrical characteristics table.

During start-up, the charge pump voltage VCCLS will ramp up until the UVLO rising threshold is crossed releasing the UVLO status, allowing then the PWM to propagate.

## Product Features

In case of overload of VCCLS rail beyond the specified maximum load of the charge pump, the VCCLS will drop. Eventually, the VCCLS voltage can cross the VCCLS UVLO falling threshold leading to both the immediate stop of the PWM signal being transmitted to the MOSFETs by setting the gate driver in Hi-Z (high impedance) mode and also reporting a fault to the Fault handler. Consequently, the nFAULT pin will be pulled down so the microcontroller in the system can decide how to proceed.

### 3.4.5.2 VCCHS Under-Voltage Lock-Out (VCCHS UVLO)

Similarly to VCCLS, a UVLO mechanism is integrated for VCCHS voltage rail. The UVLO rising and falling thresholds can be found in the Electrical characteristics table.

During start-up, the charge pump voltage VCCHS will ramp up until the UVLO rising threshold is crossed releasing the UVLO status, allowing then the PWM to propagate.

In case of overload of VCCHS rail beyond the specified maximum load of the charge pump, the VCCHS voltage will start dropping. VCCHS voltage can then cross the VCCHS UVLO falling threshold leading to both the immediate configuration of the gate driver to Hi-Z (high impedance mode) and also to the reporting to the Fault handler. As a result of the VCCHS UVLO, the nFAULT pin will be pulled down so the microcontroller in the system can decide how to proceed.

### 3.4.5.3 Floating Gate Strong Pull Down

MOSFETs in an inverter can be exposed to non-zero gate voltage levels when the controllers or gate drivers are off. Sometimes those voltages are enough to activate or partially activate the MOSFETs leading to system failure or destruction if for example, a high side MOSFET and a low side MOSFET in an inverter leg activate at the same time. In order to prevent this behavior it is common to assemble weak pull downs (in the order of 100k $\Omega$  resistors) between gate and source of the MOSFET to ensure that when the gate driver is off, the gate is pulled down to the source avoiding any turn on or partial turn on. As it is weak pull down, this does not have much impact when the gate driver is active and driving MOSFETs normally.

These six R<sub>G-S</sub> resistors however require a good amount of PCB area and need to be placed in a location where the power layout needs to be optimized with no compromises.

In order to address this, 6EDL7141 gate driver integrates a Floating gate Strong Pull Down mechanism that includes both a passive and an active pull down:

- Weak Pull Down: a weak pull down (R<sub>GS\_PD\_WEAK</sub>) is always connected between gate and source of each gate driver output. This ensures a weak pull downs during states where the gate driver is off, either because EN\_DRV is turned off or because the device is fully off (CE off). This mechanism is similar to the ones described above (R<sub>G-S</sub>).
- Strong Pull Down: additionally, during those gate driver off periods, if the external gate to source voltage increase for any reason as mentioned, an extra pull down, much stronger (R<sub>GD\_PD\_STRONG</sub>) is activated ensuring a tight pull down and hindering any possible partial turn on.

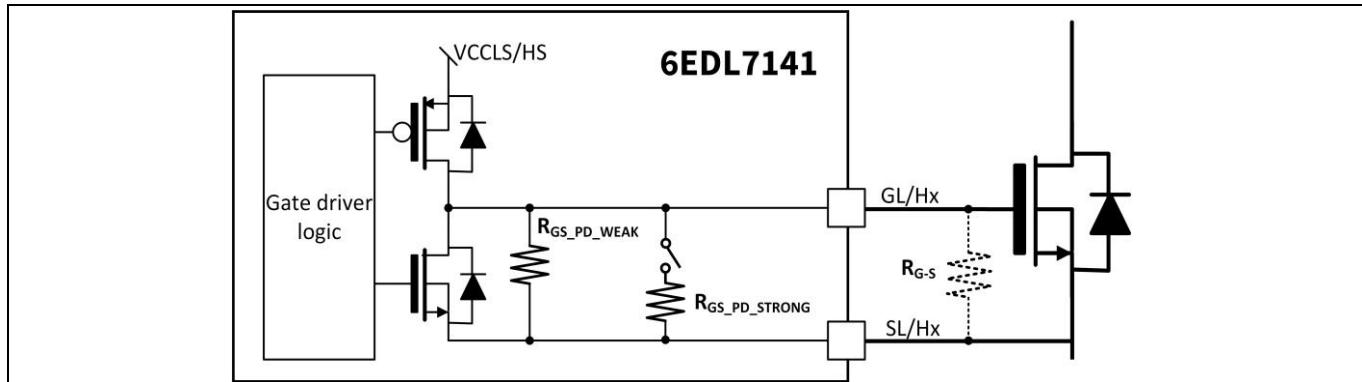


Figure 32 Floating gate driver pull down resistors. Strong pull down activates when gate driver is off and gate to source voltage increases

### 3.5 Power Supply System

The device embeds an advanced power supply system comprised of:

- Synchronous buck converter including both power switches
- DVDD linear voltage regulator programmable to output 5V or 3.3V
- Charge pump for low side gate driver (described in 3.3)
- Charge pump for high side gate driver (described in 3.3)

6EDL7141 has been designed for lowest Bill of Material (BOM). The synchronous buck converter does not require external components like diodes, voltage dividers or bootstrap capacitors yet at the same time reduces the low side conduction losses as it utilizes a NMOS instead of a diode.

The overall goal of the buck converter is to support the rest of the power supply system. With the help of an external filter (LC), it supplies both (high side and low side) charge pumps and the integrated DVDD voltage regulator. This architecture increases the efficiency of the device greatly compared to an only linear regulator system, yet maintains a very compact system solution. Furthermore, allows working at high supply voltage rating (PVDD).

DVDD linear voltage regulator is integrated to provide accurate and stable voltage to other external components either at 3.3V or 5V. In Figure 33, a schematic diagram of the complete power converter architecture and interconnections is showed.

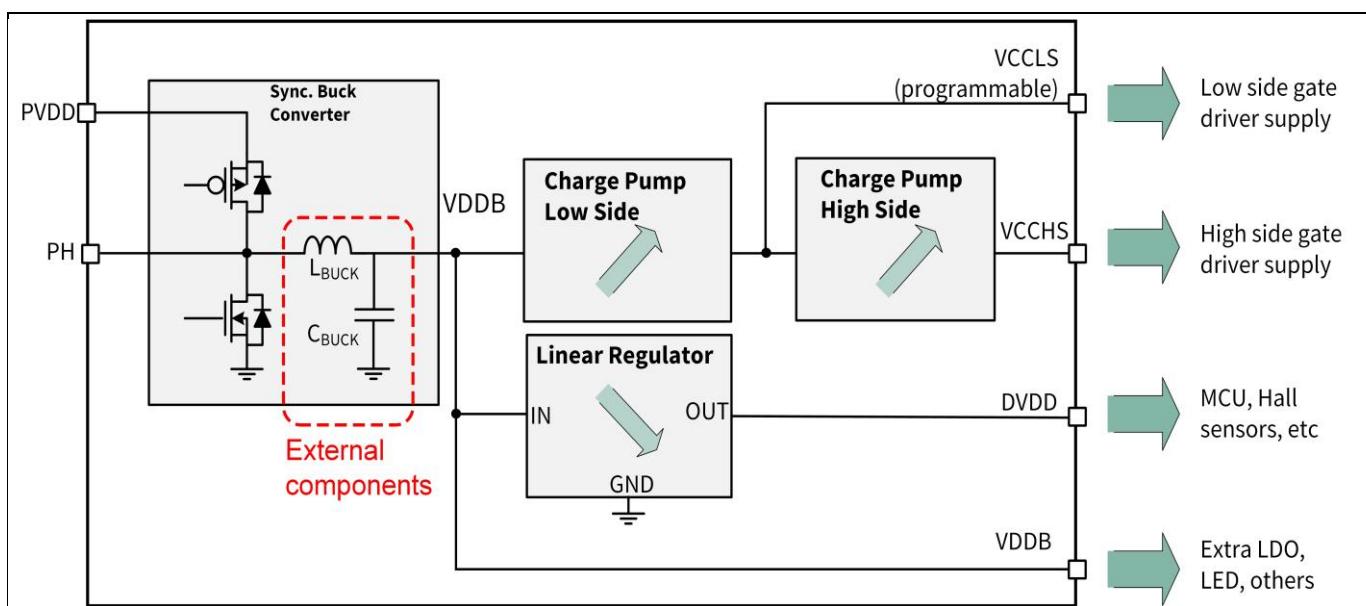


Figure 33 Block diagram of power converter architecture

Designers can use VDBB pin to supply external components as long as the current limits of the buck converter- including charge pumps and linear regulator- are not exceeded. Nevertheless, over-current protections (OCP) are implemented for both buck converter and the linear regulator, preventing any damage to the device when overloading VDBB pin. Additional over-temperature protections (OTS, OTW) are integrated to ensure the device is under correct thermal conditions at any time.

#### 3.5.1 Synchronous Buck Converter Description

Although integrated in the same package, the synchronous buck converter is designed completely independent of the rest of the gate driver circuitry. This makes the supply system robust against gate driver failures. As an

## Product Features

example, the buck converter and linear regulator will still operate even if a failure occurs in the gate driver section (e.g. VCCLS UVLO), ensuring right operation of a microcontroller and other circuits supplied by the buck converter or LDO integrated for example.

The control method utilized is Adaptive Constant ‘ON’ Time (ACOT). In contrast to a pure constant ON time control method, ACOT allows for ON time variations during transitions to avoid large frequency jumps. Together with feedforward techniques, the buck converter can operate with reduced switching frequency.

Two different switching frequencies (500 kHz and 1 MHz) can be selected via SPI –BK\_FREQ bitfield-for the buck converter. The recommended inductor and capacitor for each configuration is provided in section 9.1.

Recommended values for the inductor and capacitor are shown in Table 22.

**Note:** *It is recommended to only modify the buck converter frequency via OTP*

A detailed figure of both synchronous buck converter and linear voltage regulator circuits is depicted in Figure 34.

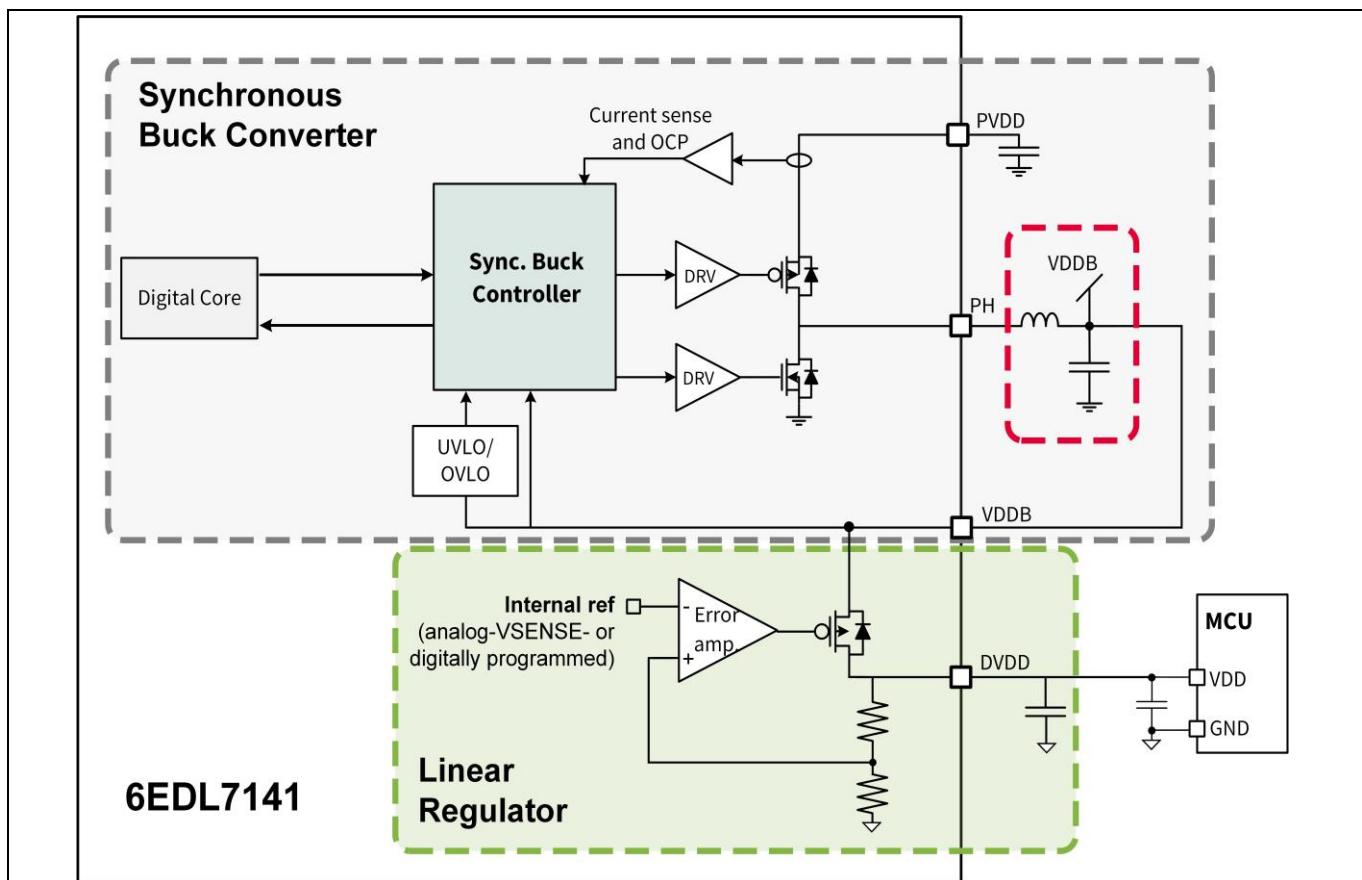


Figure 34 Detail of integrated synchronous buck converter controller and linear regulator

### 3.5.1.1 Buck Converter Output Voltage Dependency on PVCC\_SETPT

An important feature of the buck converter is the ability to automatically adjust VDDB target value depending on PVCC (target gate driver voltage) configured by user via SPI commands. This is done to optimize power losses in the device. For example, if the driving voltage PVCC is 7V, the target voltage of the buck converter is automatically set to 6.5V. In this case, the charge pumps still have enough room to reach PVCC = 7V on a ‘doubler’ configuration. The relationship between VDDB and PVCC is shown in Table 14.

**Table 14 Buck converter output target voltage vs PVCC\_SETPT setting**

PVCC_SETPT bitfield	PVCC target voltage (V)	VDDB (V)
b'11	7	6.5
b'10	10	7
b'00	12	8
b'01	15	8

Another important factor to consider in the synchronous buck converter output target voltage is PVDD or supply voltage. If 6EDL7141 is supplied with a relative low voltage then VDDB<sub>NOM\_LV</sub> rating applies (see Electrical characteristics table). In such situation the buck converter operates in open loop with the duty cycle saturation limit given by DC<sub>BUCK\_MAX</sub> (see Electrical characteristics table). If buck converter loading increases in that situation or PVDD voltage reduces further, VDDB voltage will drop. On the lower end, VDDB UVLO falling threshold protects from lower limits.

Therefore, depending on PVDD voltage, it is possible that VDDB cannot reach the target voltage, limiting as a consequence the actual PVCC voltage, which even in a doubler configuration might not be sufficient. The approximate possible PVCC voltage (= VCCLS) in the doubler configuration is given by following equation:

$$PVCC_{max} \approx \min(PVCC \text{ Target Voltage}, 2 * VDDB - 1V) \quad (1)$$

As an example, if PVDD = 7.5V, VDDB ≈ 6.5V (limited by low PVDD), if PVCC\_SETPT targets 15V, the doubler on the charge pump will be able to reach maximum of approximately 2 \* VDDB - 1V ≈ 12V. If then PVDD rises to 12V, the VCCLS will be able to regulate to 15V as this value is below/equal to the value = 2 \* VDDB (8V) - 1V = 15V.

See 2.6 for more details on relationship between VCCLS, VCCHS and PVDD.

### 3.5.1.2 Synchronous Buck Converter Protections

Following protections are implemented to ensure correct operation of the buck converter:

- **Output Under-Voltage Lock-Out (UVLO).** see Electrical Characteristics table for specific values.
- **Output Over-Voltage Lock-Out (OVLO).** see Electrical Characteristics table for specific values. If the value is reached the buck converter will switch off both high side and low side MOSFETs interrupting any further energy transfer to the output.
- **Over-Current Protection (OCP)** cycle by cycle. Given a situation in which the current increases till the OCP level (see Electrical Characteristics table for details), the buck converter controller will truncate the high side FET PWM signal until next PWM period start. The low side FET will be driven accordingly after insertion of dead time.

Once the OCP event takes place, a counter will start counting for each consecutive period that the peak current is reached. After 16 periods, the Buck OCP fault is triggered and nFAULT pin (see Table 17) will be set low to inform the MCU that can proceed with correcting actions. The Buck converter will continue operation in current limitation to ensure the MCU is supplied. If the OCP does not trigger for 3 consecutive PWM periods, the counter will reset and will not trigger the Buck OCP fault. If the Buck OCP fault is activated, the bitfield BK\_OCP\_FLT in register FAULTS\_ST will be set.

### 3.5.2 DVDD Linear Regulator

The integrated linear regulator generating DVDD can be set to provide either 3.3V or 5V by means of an external resistor R<sub>SENSE</sub> as described in Table 7 or alternatively via bitfield DVDD\_SETPT. The selected DVDD value can be read via SPI in bitfield DVDD\_ST in register FUNCT\_ST.

## Product Features

DVDD linear regulator can be used as well to provide an offset to the current sense amplifiers integrated, allowing negative current measurements. See 3.6.4 for more details.

The linear regulator is soft started during ramp up of the device as depicted in Figure 53 after a delay time  $t_{DVDD\_TON\_DLY}$  after the buck converter has reached its UVLO level ( $V_{VDDB\_UVLO\_R}$ ) and analog programming of CS\_GAIN/AZ and VSENSE/nBRAKE are finished. The DVDD ramp up timing can be configured via SPI via bitfield DVDD\_SFTSTRT.

A schematic view of DVDD linear regulator and the interaction with the buck converter is presented in Figure 34.

DVDD voltage can be used to supply a microcontroller (MCU) or additional elements in the circuit like Hall sensors, LEDs, etc. An OCP mechanism is provided.

### 3.5.2.1 DVDD Linear Regulator OCP

DVDD OCP can be configured between 4 different levels by writing register DVDD\_OCP\_CFG. If the OCP for DVDD is reached, a fault will be reported on pin nFAULT. The DVDD OCP works in two different stages:

- Pre-warning mode at 66% of selected OCP level:** nFAULT pin will be pulled down to signal the controller that an OCP warning has occurred. If the current level reduces before reaching 100% level, the operation will continue normally releasing the nFAULT pin. The pre-warning allows some extra time for the microcontroller to make a decision on how to react to the possible OCP event.
- Current limiting mode at 100% of selected OCP level:** if current increases beyond the configured OCP level, the DVDD regulator will start limiting the current provided. This will cause a DVDD voltage drop, eventually resulting in a DVDD UVLO fault if DVDD UVLO threshold is crossed. Thanks to this limitation, possible shorts on DVDD rail will not affect rest of the system keeping these other components safe.

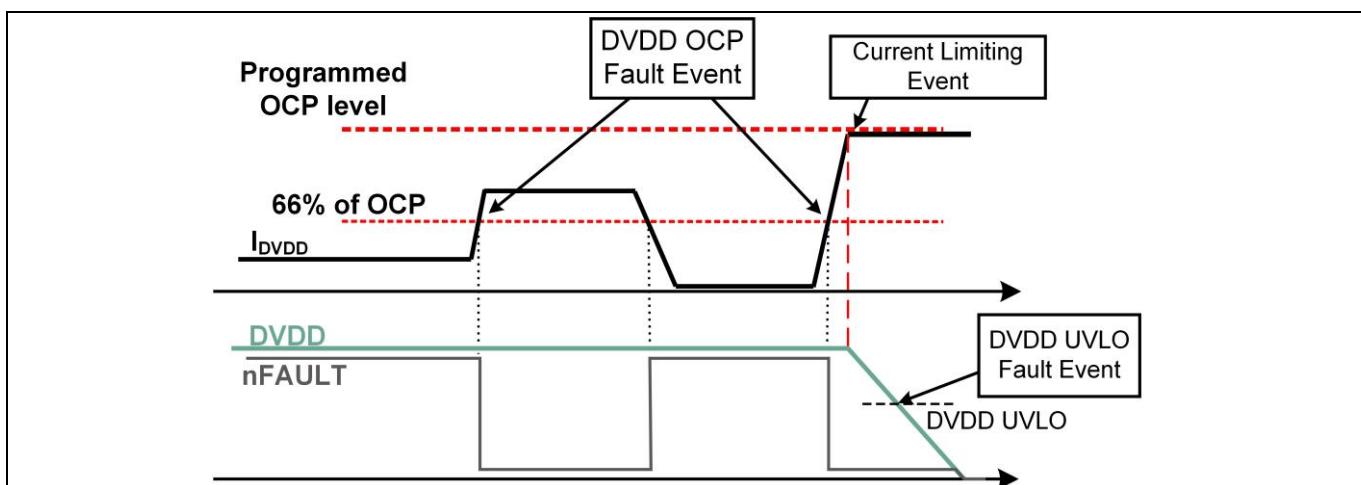


Figure 35 DVDD OCP behavior including pre-warning and current limiting modes

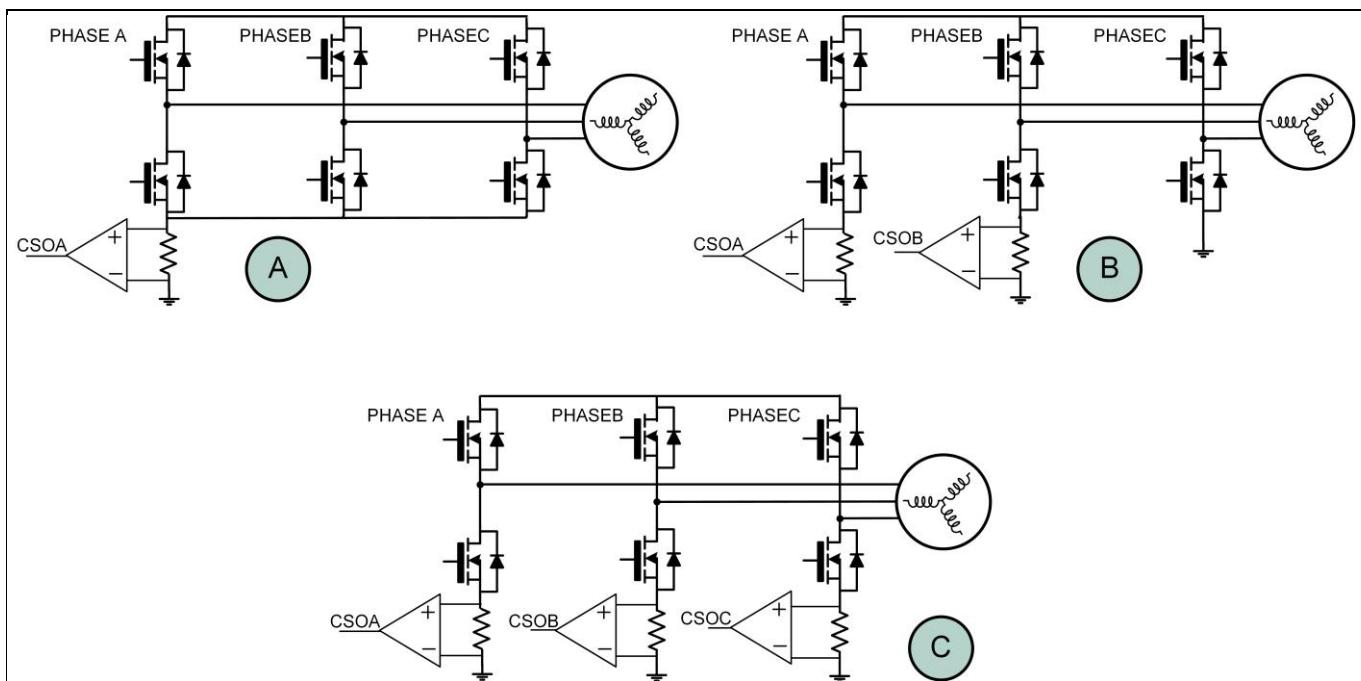
**Note:** The OCP in DVDD is suppressed during ramp up of the device to avoid that initial charge of DVDD decoupling capacitors (eventually large capacitors) triggers the OCP fault

Over-temperature faults (OTS, OTW) provide an additional level of protection. These will trip if too high temperature is developed in the device, for example when the DVDD linear regulator or the buck converter demand excessive load current.

### 3.6 Current Sense Amplifiers

The device integrates three current sense amplifiers that can be used to measure the current in the power inverter via shunt resistors. Single, double or triple shunt measurement are supported as shown in Figure 36.

CS\_EN bitfield enables each current sense amplifier individually. Gain and offset are generated internally and are programmable.



**Figure 36 Single (A), dual (B)and triple (C) shunt current sensing configurations are supported**

The current sense amplifier block contains the following sub-blocks explained in detail this section:

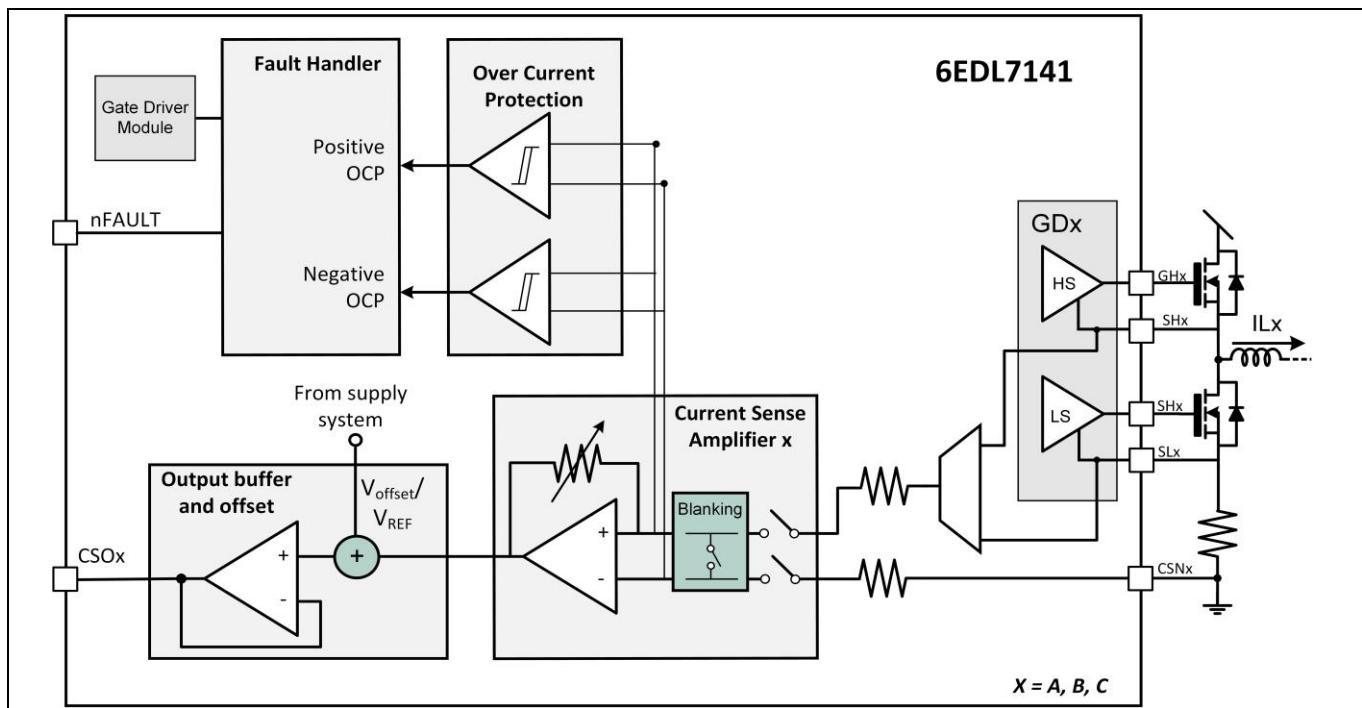
- **Current sense amplifier:** connected to external shunt resistor or internally to SHx and SLx pins for  $R_{DSON}$  sensing configuration. This module amplifies the shunt voltage or low side  $V_{DS}$  voltage to a more appropriate voltage level for a microcontroller ADC. It allows as well blanking the signal synchronized to PWM transitions, during periods where noise is disturbing the measurement.
- **Output buffer:** allows adding a variable offset voltage to the sense amplifier output. The offset amount can be set to 4 different values either by programming the internally generated level or by applying an external voltage at VREF input pin. With this implementation, negative current in current shunts can be measured. Additionally permits to optimize the controller ADC dynamic range according to system conditions.
- **Positive Over-Current comparator:** used for detecting the over-current condition on motor winding for positive shunt voltage. This comparator can be used to apply PWM truncation in block or trapezoidal commutation schemes, limiting the motor current to the configured OCP threshold.
- **Negative Over-Current comparator:** used for detecting the over-current condition on motor winding for negative shunt currents
- **OCP Digital-to-Analog Converter (DAC):** used for programming the threshold of the over-current comparators. One for positive level and a second one for negative level. Programming of DAC levels is shared among all three different OCP comparators.

Current sense amplifiers will automatically “Auto-Zero”. This happens during operation and ensures best accuracy of measurements during lifetime of the device. Additionally, 6EDL7141 includes a current sense amplifier user calibration mode that can be used to calculate residual offset when shunt current is known to be

**Product Features**

zero, for example, because there is no PWM yet propagated to the MOSFETs. A microcontroller firmware can remove this initial residual value from future measurements to improve accuracy.

Figure 37 shows these blocks and their interconnections.



**Figure 37 Current sense amplifier simplified block diagram**

Note: *It is recommended to disable current sense amplifiers that are not used*

### 3.6.1 $R_{DSON}$ Sensing Mode vs Leg Shunt Mode

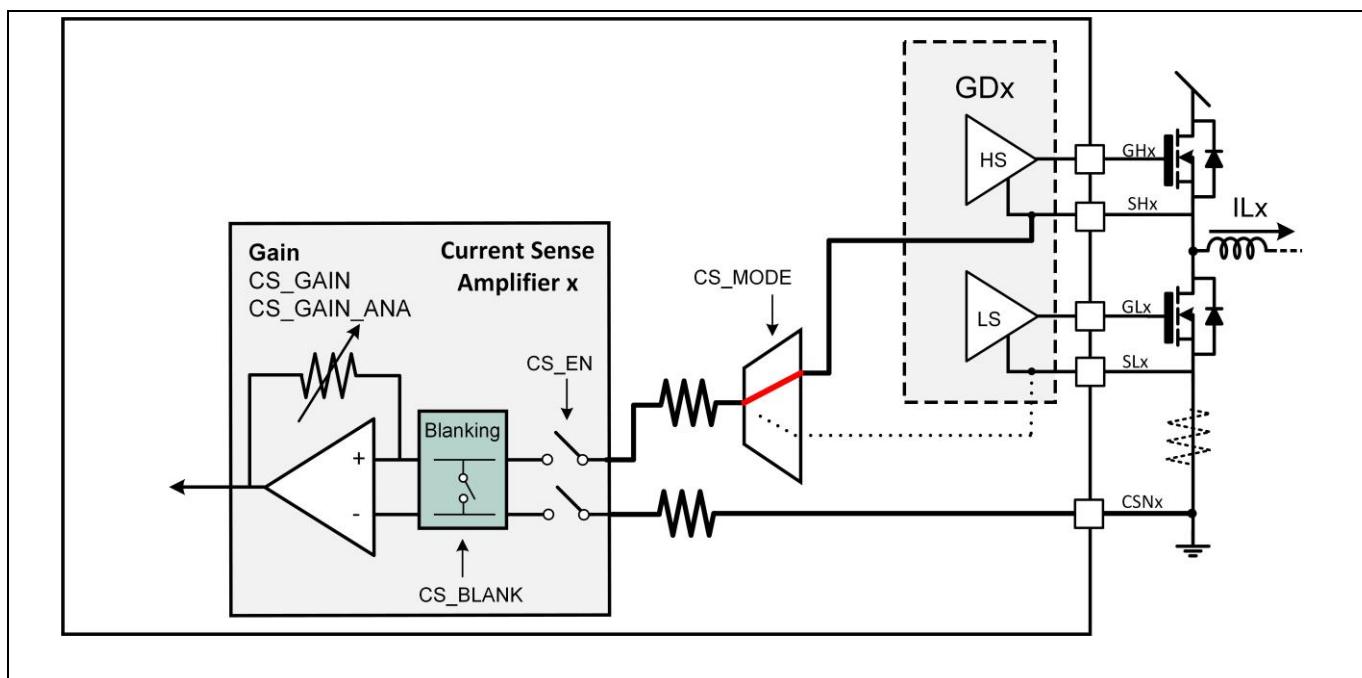
Current sense amplifiers in 6EDL7141 can be configured as leg shunt or  $R_{DSON}$  sensing, where the ‘ON’ resistance of the MOSFETs is used as shunt in a ‘lossless’ measurement approach.

In  $R_{DSON}$  mode, 6EDL7141 connects the drain of the low side MOSFET to the positive input of the current sense amplifier. The negative input is connected to the source as shown in Figure 38. This is in contrast to the external shunt configuration shown in Figure 39, where the positive input of the current sense amplifier is connected to the source of the low side MOSFET. Internal series resistors help filtering possible noise before the amplification takes place. Depending on the circuits and board design, a small filtering capacitor between SLx and CSNx pins can help cleaning up the current signal.

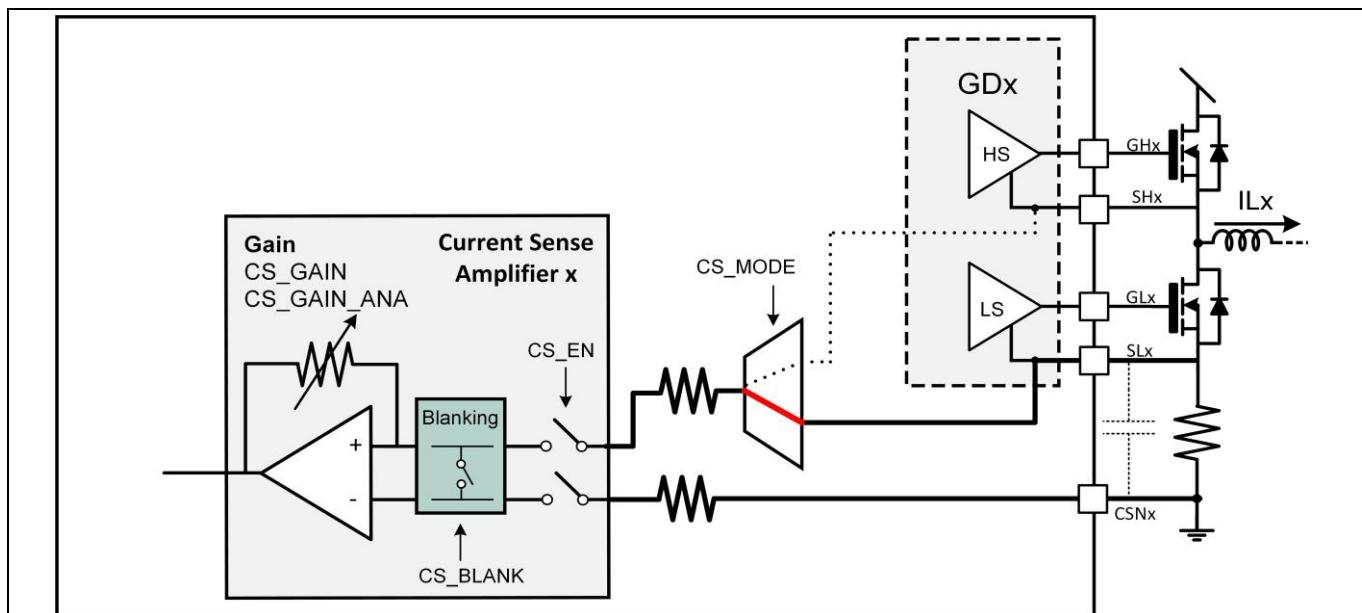
Note:  *$R_{DSON}$  mode is only possible in 3 shunt mode (mode C in Figure 36)*

Note: *In  $R_{DSON}$  mode, the CSAMP is forced to be CS\_TMODE = 0, meaning the current sense amplifiers are only active when low side is ON (GL ON mode). If this bitfield is written with a value different than b'0, the configuration will be ignored by the internal logic.*

Note: *Temperature compensation for the  $R_{DSON}$  measurement, if required, must happen at MCU.*



**Figure 38** System diagram of a low side  $R_{DS(on)}$  current sensing configuration utilizing integrated current sense amplifiers



**Figure 39** System diagram of an external shunt current sensing configuration utilizing integrated current sense amplifiers

### 3.6.2 Current Shunt Amplifier Timing Mode

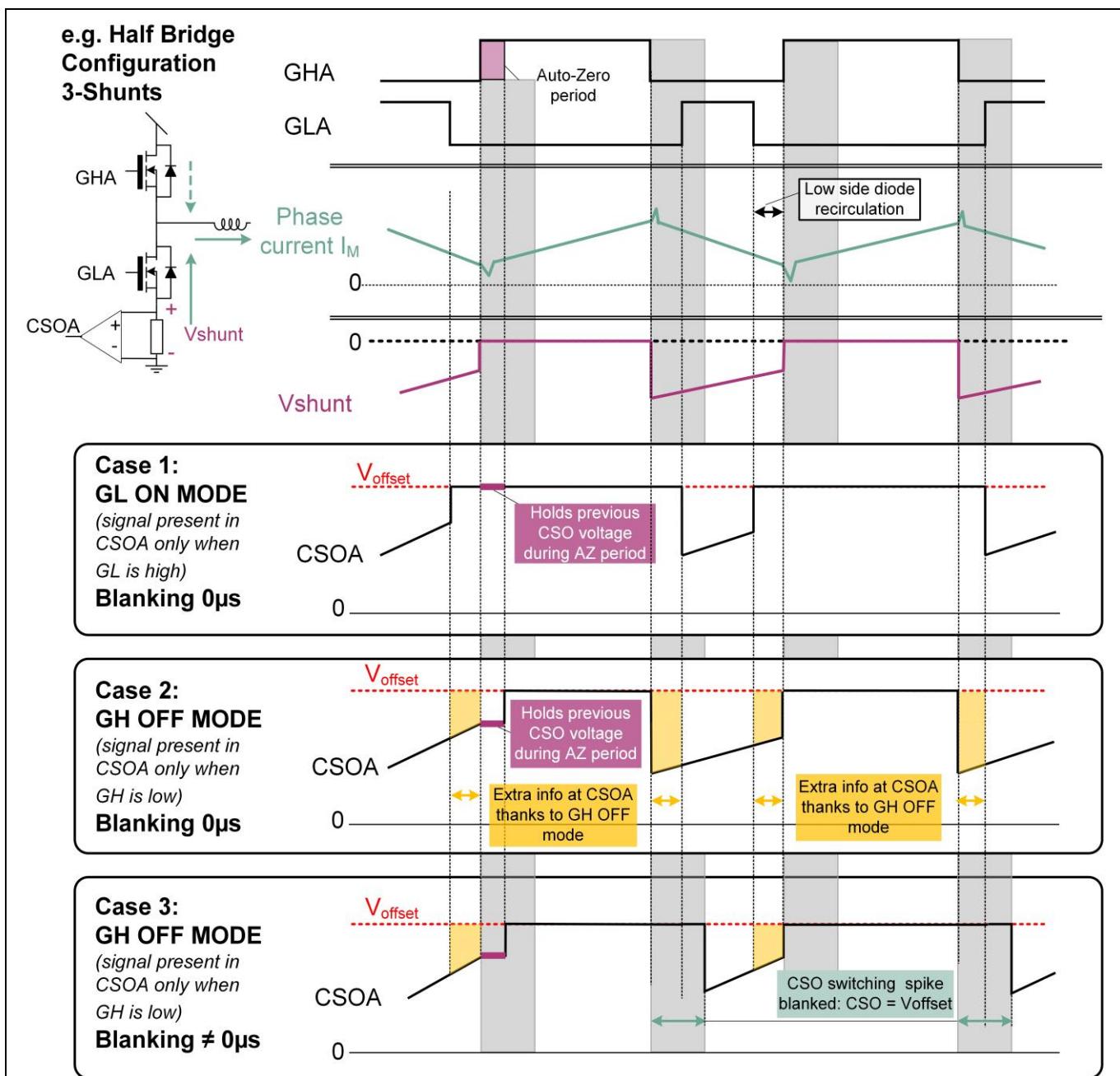
Often in drives applications, the current is sampled via leg shunts. In this case, the voltage in the shunt that needs to be amplified appears only when the low side MOSFET is turned on. In other cases, it might be useful to propagate the signal continuously. 6EDL7141 supports four different modes of operation of the current sense amplifiers regarding when the output pin CSO<sub>x</sub> is connected to the amplifier stage. These four modes are:

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**Product Features**

- **Always OFF:** current sense amplifier output disabled. This is achieved by disabling the amplifier in register CSAMP\_CFG via bitfield CS\_EN.
- **GL ON:** in this mode, CSOx pin is connected to the amplifier only when the same leg or phase GLx signal is active. In single shunt mode, CSOx will be connected according to the OR'ing of all two or three GLx signals. If two or three amplifiers are enabled, then the signals for enabling CSOx will be dedicated to that GLx signal. This mode is forced if  $R_{DSON}$  sensing is selected to avoid possible overvoltage damage in the internal circuitry. In order to enable this mode, the amplifier must be enabled via CS\_EN bitfield in CSAMP\_CFG register and the timing mode selected via write to CS\_TMODE bitfield in SENSOR\_CFG.
- **GH OFF:** similarly to GL ON, this mode connects the CSOx outputs during GL ON period but extends that connection to the dead times both rising and falling. This is same than GH OFF. In some cases like during diode recirculation current, the diode might carry current that can be useful especially in cases where the PWM pulses are very narrow. Same as GL ON, single shunt will logic OR the GLx activations and three shunt modes will activate according to each GLx signal only. In order to enable this mode, the amplifier must be enabled via CS\_EN bitfield in CSAMP\_CFG register and the timing mode selected via write to CS\_TMODE bitfield in SENSOR\_CFG.
- **Always ON:** this mode connects continuously the activated amplifier CSOx signals to the amplifier independently of PWM signals. In order to enable this mode, the amplifier must be enabled via CS\_EN bitfield in CSAMP\_CFG register and the mode selected via write to CS\_TMODE bitfield in SENSOR\_CFG.

Figure 40 (cases 1 and 2) shows a comparison of the current sense amplifier working in both modes GL ON and GH OFF.



**Figure 40 Current sense amplifier ideal timing mode example. Mode GL ON and GH OFF operation in a half bridge example with leg shunt current sense configuration-3 active amplifiers. GH OFF can potentially propagate current information when the diode recirculates current. Auto Zero injected on GHx rising**

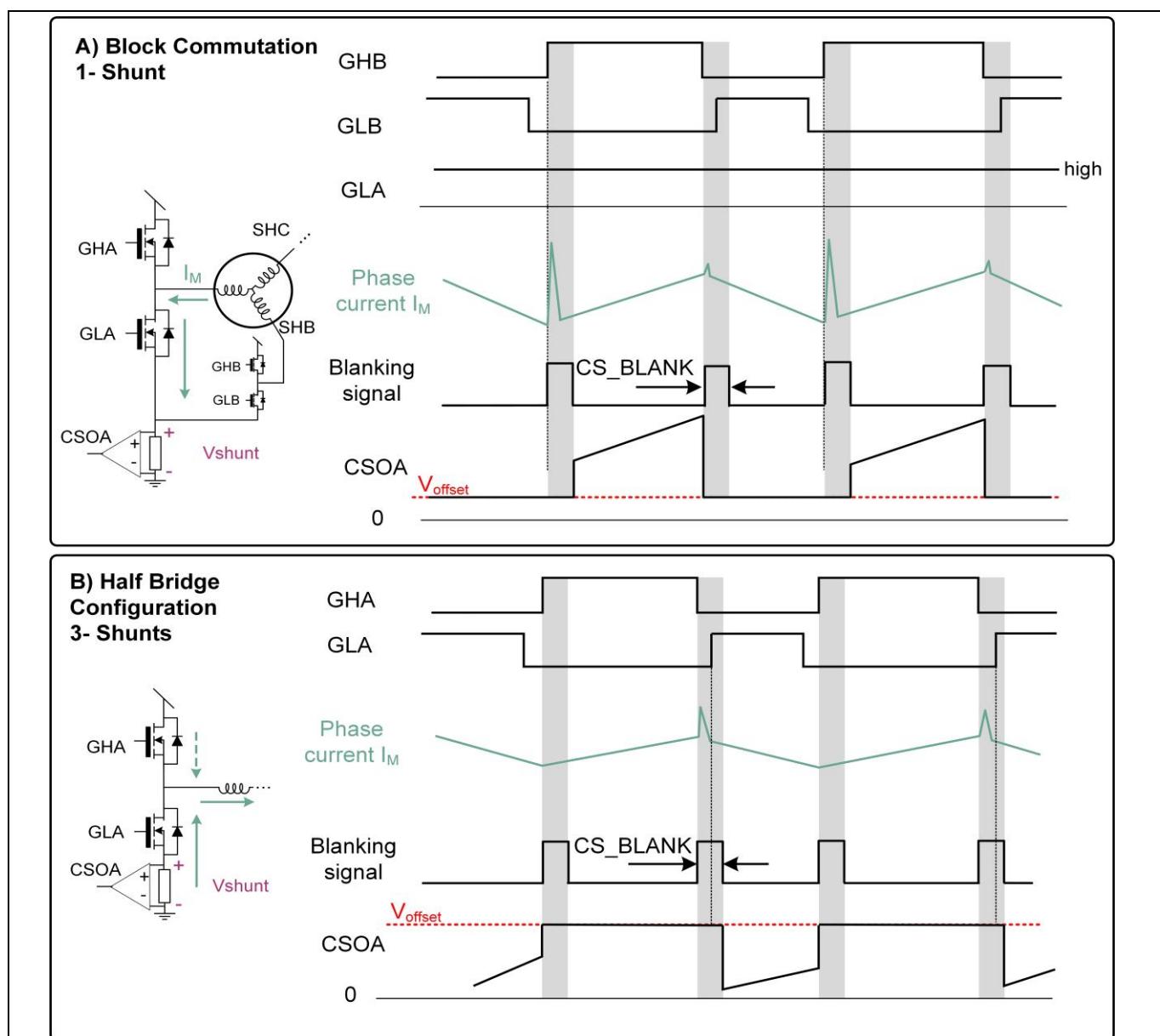
### 3.6.3 Current Shunt Amplifier Blanking Time

A programmable blanking period can be configured in the current sense amplifiers. The goal of adding some blanking time is to avoid propagating a distorted signal to the microcontroller ADCs during MOSFET switching transitions. Since both, phase node voltage  $SH_x$  and  $SL_x$  pins ( $CSNy$ ) are subject to ringing due to the switching activity, the blanking module disconnects the inputs for a configurable time ( $CS\_BLANK$ ). This action occurs in synchronicity with  $GH_x$  signal (rising and falling edges) driving the external MOSFETs.

**Product Features**

During the blanking time, pin CSOx will show  $V_{offset}$  voltage until the programmed blanking time period expires and inputs are connected again to the current sense amplifier. Two examples are shown in Figure 41. Example A) represents a trapezoidal commutation scheme with 1 shunt similar to the one in Figure 62. In such case the high side of one phase (phase B) is switching, while the low side of another phase (phase A) is always ON, allowing the current to flow through the motor windings. As the low side MOSFET of phase A is ON for 120 degree of rotation, the current sense amplifier is amplifying the shunt voltage continuously except blanking and recirculation periods. These blanking periods corresponds to both high side rising and falling edges (ORing to all phases applied). In this case the voltage across the shunt is positive.

The example in B) corresponds to a generic half bridge configuration (e.g. synchronous buck converter). In this case, when high side is turned on, the current in the inductor increase, while in the complementary cycle when the high side switches off and the low side turns on after dead time, the current flows through the low side and starts decreasing. During the low side conduction, the current sense amplifier generates the shown output proportional to the voltage across the shunt, in this case negative.



**Figure 41** Timing diagram of a current measurement utilizing blanking time feature for suppressing current spikes during MOSFET switching. **A) Trapezoidal commutation with 1 shunt configuration. B) Generic half bridge configuration.**

### 3.6.4 Current Sense Amplifier Offset Generation: Internal or External (VREF pin)

6EDL7141 integrates an internal linear voltage regulator (DVDD) that can be used for offset generation in all integrated current sense amplifiers. The generated DVDD voltage can be scaled down to different programmable values to adjust the desired offset voltage level. Bitfield CS\_REF\_CFG controls this scaling factor.

Some microcontrollers generate internally the reference for an integrated ADC out of the supply voltage. In this way the microcontroller can accurately measure in a ratio-metric way the output of the current sense amplifiers increasing noise immunity. Figure 42 shows a block diagram representing this implementation.

The current sense amplifiers offset voltage can alternatively be provided via an externally generated voltage through VREF pin. Bitfield VREF\_INSEL selects between scaled DVDD (internally generated) or VREF input pin as source for the offset voltage applied to all 3 current sense amplifiers.

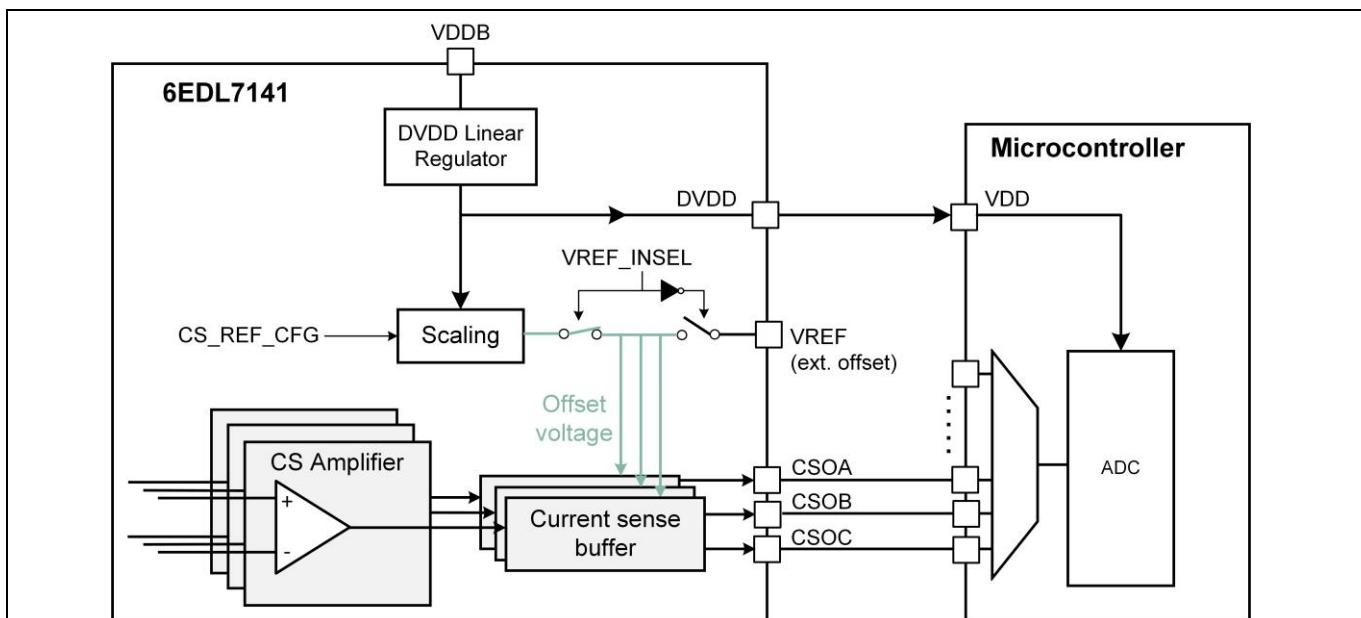


Figure 42 Current sense amplifier offset generation block diagram

### 3.6.5 Overcurrent Comparators and DAC for Current Sense Amplifiers

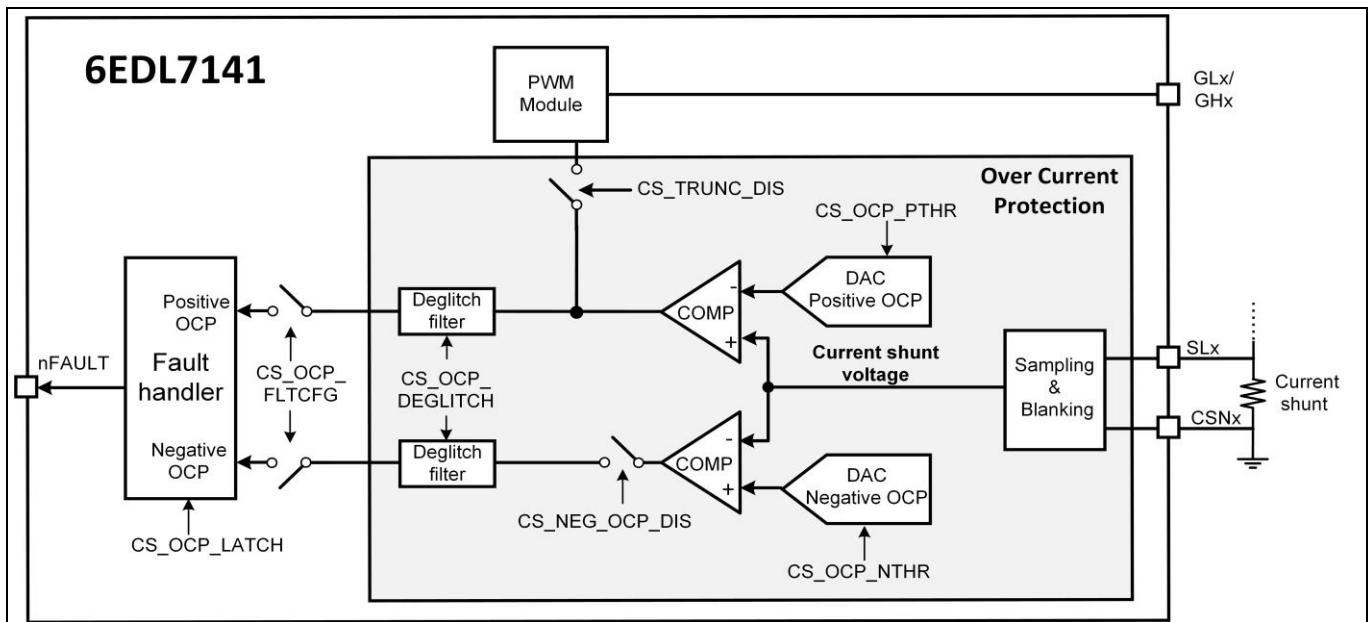
Two overcurrent comparators are implemented for monitoring the current in both positive and negative direction with an extensive level of programmability. Figure 43 shows a schematic diagram of this implementation. Both comparators monitor the current flowing through the shunts. The triggering level is independent from the gain setting of the shunt amplifiers and is defined as the voltage across the shunt. The comparator features a hysteresis (specified as  $V_{OC\_HYST}$ ) for consistent operation.

Positive and negative triggering levels for the comparator are set with two independent Digital to Analog Converters (DAC). These DACs are programmed via bitfields CS\_OCP\_PTHR for positive overcurrent protection and CS\_OCP\_NTHR for negative overcurrent protection. For possible threshold levels see the registers description in section 8.

The output of the comparators can be deglitched by programming register CS\_OCP\_DEGLTICH before reaching the Fault handler, where the fault will be processed (See section 6) and eventually will pull down nFAULT pin reporting a fault to the microcontroller or other circuitry.

Alternatively, the comparator output propagates to the PWM modules. PWM truncation can be enabled via bitfield CS\_TRUNK\_DIS. If PWM truncation is activated, the PWM module immediately interrupts the PWM signal

without having to wait for the microcontroller to make such decision when the OCP level is reached. This ensures fastest possible reaction time to the OCP event. Truncation is detailed in section 3.6.5.4.



**Figure 43 Current sense amplifier protections schematic block diagram**

### 3.6.5.1 OCP Use Cases

The reaction to an OCP event is programmable via SPI. Following scenarios might be useful for different applications:

- **Apply PWM truncation** immediately after OCP event **and report on nFAULT** pin after OCP event- deglitching is disabled if truncation is enabled. This is useful in trapezoidal control schemes.
- **Disable reporting and keep truncation of PWM.** This can be useful during events where the reporting function to the microcontroller might not be necessary. This is useful in trapezoidal control schemes.
- **Trigger a configurable brake action** upon OCP event. If truncation is not desired, the brake event can be configured to e.g. brake the motor by shorting all low side MOSFETs. By using the deglitch function, the possible noise in the analog signal can be filter out to avoid false trip of the OCP. This configuration can be useful for FOC (Field Oriented Control) schemes given the flexibility. Braking is explained in more detail in sections 3.2.6 and 6.
- **Disable OCP protection**, both nFAULT reporting and truncation of PWM. In such case, OCP is ignored. This might be useful for transition states or stop procedures as well.

These configurations can be adjusted also during ACTIVE state of the device. It is also possible to select whether the OCP fault trips on a single event or more and whether is latched or not via bitfield CS\_OCP\_LATCH.

### 3.6.5.2 OCP Fault Reporting

OCP fault can be reported to the MCU via nFAULT pin. This will then result in nFAULT pull down therefore informing the MCU that a fault occurred.

CS\_OCPFLT\_CFG in register CSAMP\_CFG allows the user to set a target number of consecutive events (PWM cycles with current above OCP threshold) that will activate OCP fault. This means the user can configure the device to wait for several PWM periods before declaring a fault and therefore be more conservative. Three options are possible: no fault, trigger immediately (i.e. trigger on all events) or trigger on a number of counts (8 or 16). The logic for the counting mode works as follows:

1. Every time that an OCP event occurs, a counter increments. All three phases have dedicated counters.
2. If any counter (ORing) reaches the target value configured in CS\_OCPFLT\_CFG, then the fault is asserted and nFAULT pin is pulled low.
3. If before reaching the target value, the OCP event does not occur for 3 consecutive PWM cycles, the counter is reset to value 0, starting over next time an OCP event takes place.

### **3.6.5.3 OCP Fault Latching**

The OCP fault can be configured as latched or non-latched. This defines how the fault is cleared via register write. If configured as latched:

- and in counting mode (8 or 16): fault cannot be cleared until there is one whole PWM period without fault
- and in immediate or on all events mode: fault can be cleared only after the fault condition is released.

If not latched, the fault can be cleared any time. If conditions is still present after clear, the fault will be set again after the clear event.

Independently of the latch configuration, the status register will show that the fault happened.

### **3.6.5.4 PWM Truncation**

PWM truncation is a method to intrinsically limit the current flowing into the motor by switching off the PWM signal immediately after OCP detection. In this way, the GHx signals (all three) are pulled down automatically when the configured peak current level is reached. Low side remains unaffected until the PWM resets, increasing current in the motor again. This happens in a PWM cycle by cycle base. An example of how PWM truncation works, is depicted in detail in Figure 44.

**Note:** *Truncation occurs always on high side except for 1PWM mode with alternate recirculation, where the truncation occurs in low side during high side recirculation periods and on high side during low side recirculation periods.*

If PWM truncation is active, PWM truncation takes place upon OCP event in all phases. For example, if the protection is triggered in current sense amplifier A, then PWM signals in phases A, B and C will be truncated. This will enable single shunt systems to utilize any of the current sense amplifiers.

Blanking is applied to truncation logic on both rising and falling edge of high side as described in Figure 41, see register CS\_BLANK for blanking times. Blanking from all phases are OR'ed and prevent any miss-triggering of the PWM truncation during the blanking time selected by the user.

If truncation is enabled, the deglitching filter is automatically disabled. This means, if truncation is enabled, the nFAULT pin signalizes simply that a PWM truncation has occurred.

**Attention:** *Depending on the PWM modulation utilized, PWM truncation might not provide the desired results. In modulation schemes where it is possible more than one phase are energizing the motor at a given time like SVM FOC (Space Vector Modulated Field Oriented Control), it is recommended to disable truncation and use OCP fault instead.*

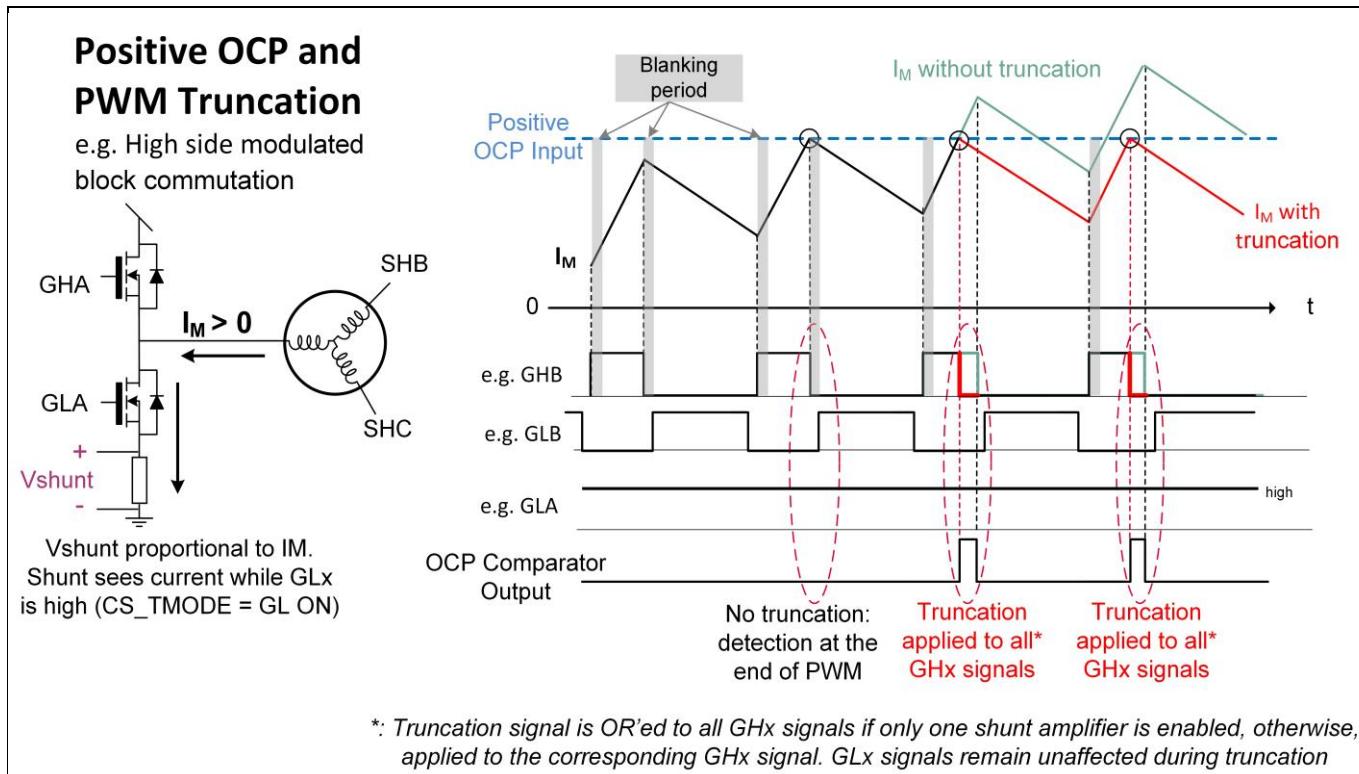


Figure 44 Positive OCP PWM truncation detail. IM refers to motor current

### 3.6.6 Current Sense Amplifier Gain Selection

Gain of the shunt amplifiers can be programmed digitally via bitfield CS\_GAIN to one of the following values: 4, 8, 12, 16, 20, 24, 32 and 64. Alternatively, the gain can be selected by connecting an external resistor ( $R_{CS\_GAIN}$ ) from pin CS\_GAIN to ground. In order to enable analog programming of the current sense amplifier via external resistor, the user must ensure that bitfield CS\_GAIN\_ANA is set accordingly. The value of  $R_{GAIN}$  is evaluated during startup of the device (see section 3.10.2). Table 15 provides the resistor values and register settings for gain selection in both analog and digital modes.

Table 15 Programming of current sense amplifier. Gain vs resistor size

Gain Value	Digital programming	Analog programming
	CS_GAIN (hex)	$R_{CS\_GAIN}$ (kΩ)
4	0x0	0
8	0x1	1.5
12	0x2	3.0
16	0x3	4.7
20	0x4	6.2
24	0x5	7.5
32	0x6	9.1
64	0x7	11

Note: For analog programming, resistors are recommended to be 1% tolerance or lower

The actual value of the current sense amplifier gain can be read in FUNCT\_ST register via bitfield CS\_GAIN\_ST.

### 3.6.7 Current Sense Amplifier DC Calibration

6EDL7141 features a calibration method for the current sense amplifiers. This helps eliminate any unwanted offset in the output of the operational amplifiers before starting motor operation for example.

The activation of the DC calibration mode (only during ACTIVE state-EN\_DRV high) via register CS\_EN\_DCCAL programming, will short the inputs of the amplifiers. Once the DC calibration is enabled, the output on CSOx pins can then be measured by precise ADC channels in an MCU to record any possible offset in the operational amplifiers. Any excess voltage in CSOx pin from VREF voltage can be subtracted in the MCU from any future measurements, for example by software means. It is recommended to perform DC calibration before the PWM is started, when the current in the shunts, is known to be zero.

Once the offset value is captured, the MCU should set CS\_EN\_DCCAL bitfield again to '0' to finalize the calibration process and reconnect the operation amplifier to the input pins. Then the PWM signals can start-up.

**Note:** *During calibration mode, if Auto-Zero is enable it will be executed every 100μs instead of 200μs.*

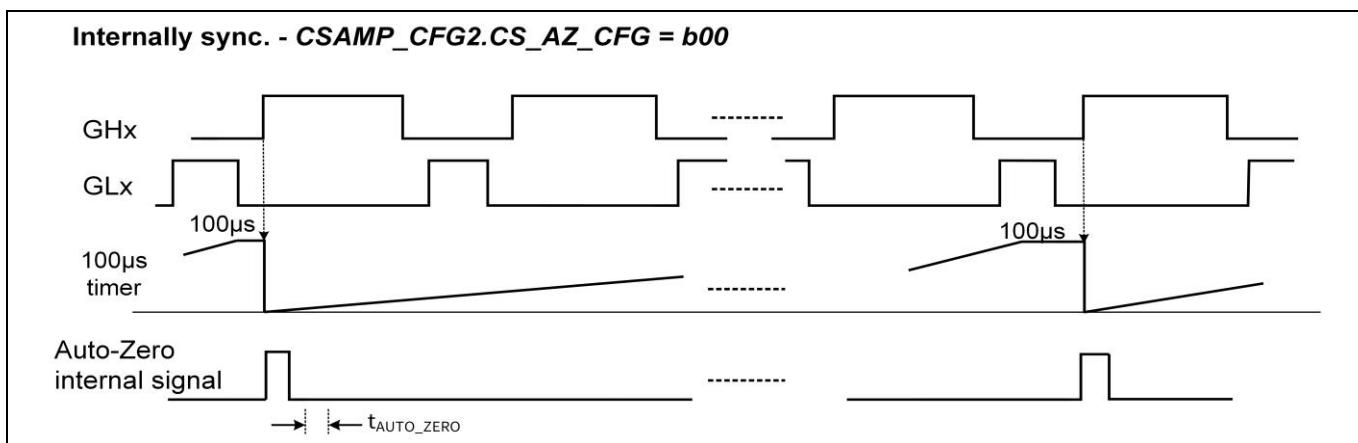
### 3.6.8 Auto-Zero Compensation of Current Sense Amplifier

Current sense amplifiers tend to accumulate offset during operation if they are not corrected. This can be due to temperature or aging effects. The Auto-Zero feature of the current sense amplifiers provides an automatic way of compensating any possible drifts in the amplifiers. Internally the amplifier shorts the inputs to correct any possible offset excess for a  $t_{AUTO\_ZERO}$  period of time. CSOx pin will hold the voltage before the Auto-Zero start during Auto-Zero period.

The Auto-Zero feature can be as well disabled via register bitfield AZ\_DIS in register CSAMP\_CFG.

#### 3.6.8.1 Internal Auto-Zero

If configured as internally triggered or synchronized (by writing register bitfield CS\_AZ\_CFG), the Auto-Zero period starts with GHx signal rising edge after at least 100μsec from last Auto-Zero period (x depends on the activated current sense amplifier, A, B or C). The synchronized start of Auto-Zero period is chosen to interfere minimum possible with the shunt current sensing. Details of signals behavior example can be seen in Figure 40 or in Figure 45.



**Figure 45 Auto-Zero operating modes. Internally synchronized with GHx signals. Auto-Zero occurs upon next GHx rising edge after timer has reached 100μs**

During start-up, the Auto-Zero function automatically activates to ensure that the amplifiers are optimized before the ACTIVE state is entered. This happens during charge pump start-up, this is from EN\_DRV turn on until charge pump UVLO is reached.

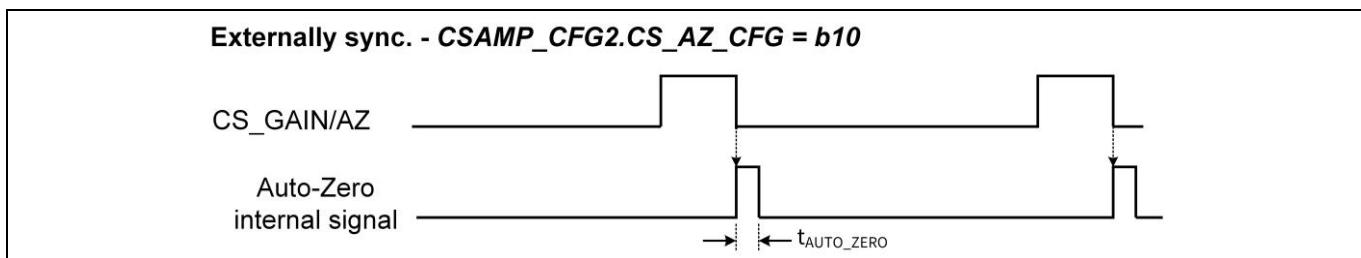
If no GHx rising edge happens for a given time ( $t_{AUTO\_ZERO\_CYCLE}$ ), for example if the low side is fully turned on for a long period in a 6-step commutation, then an internal watchdog will force an Auto-Zero compensation. Auto-Zero continuous during STANDBY state.

**Note:** *When the Auto-Zero period finishes and the CSOx reconnects to the amplifier, it is expected to see a minor voltage glitch. This can be blanked or filtered out for example before the signal is provided to an ADC.*

### 3.6.8.2 External Auto-Zero Synchronization via CS\_GAIN/AZ Pin

User can enable external synchronization of the Auto-Zero function by writing register bitfield CS\_AZ\_CFG. In such case, the internal synchronization with GHx signals is disabled and the falling edge of pin CS\_GAIN/AZ becomes the trigger for Auto-Zero correction period. This is depicted in Figure 46.

If externally triggered, the microcontroller in the system can decide according to the particular current sense method when to execute the Auto-Zero correction. Thanks to this feature the Auto-Zero effect can be moved, for example, far from the ADC sampling in the microcontroller so benefitting from the corrections but still being able to sample without the interference of the Auto-Zero process.



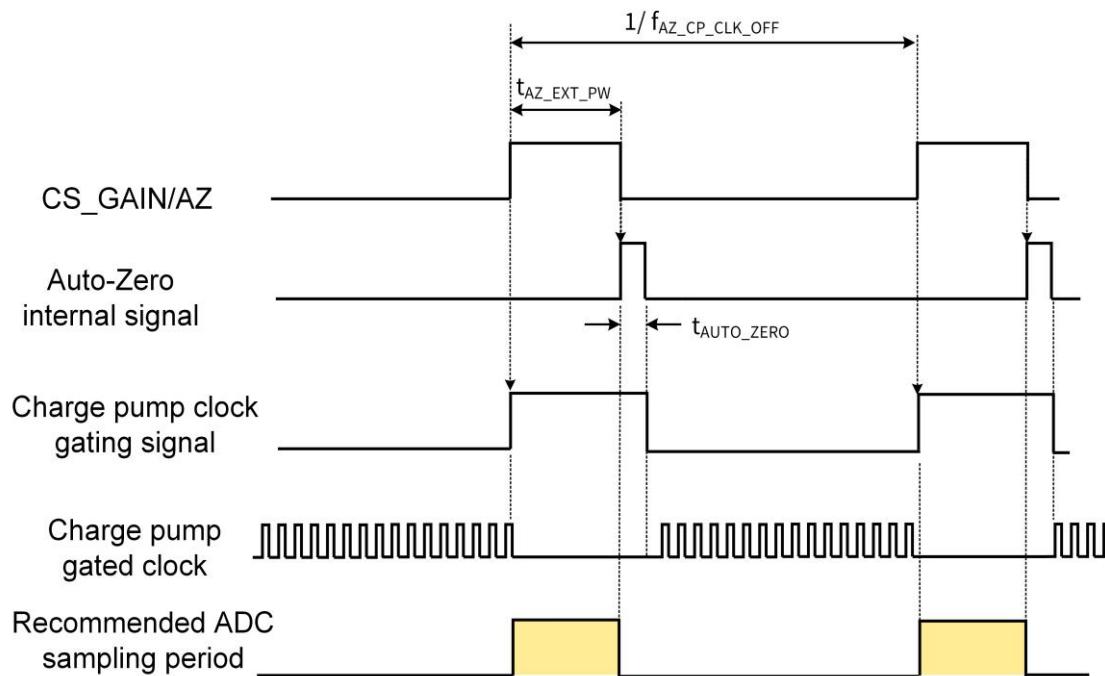
**Figure 46 Auto-Zero functionality with external synchronization. CS\_GAIN/AZ pin falling edge will trigger the Auto-Zero correction period**

### 3.6.8.3 External Auto-Zero Synchronization via CS\_GAIN/AZ Pin with Enhanced Sensing

6EDL7141 allows to stop the clock (clock gating) of the charge pump modules according to CS\_GAIN/AZ pin state. If this feature is activated, the charge pumps clock will be gated from the rising edge of CS\_GAIN/AZ pin until end of Auto-Zero period that starts after falling edge of same pin. The effect of the clock gating is the reduction of possible switching noise that can couple into PCB sensitive signals like CSOx or other ADC measured voltages by the system MCU or other sampling circuits.

**Attention:** *During clock gating period, the charge pump stops operation. As a result, VCCLS and VCCHS rails stops regulation and can drop their regulated voltages. In most cases, VCCLS and VCCHS capacitors will maintain enough voltage to keep driving efficiently the MOSFETs. User must check that Recommended Operating Conditions and Electrical Characteristics are respected. UVLO protections on both VCCLS and VCCHS are present in case a malfunction takes place, protecting the inverter.*

The operation of the charge pump clock gating mode is shown in Figure 47.

**Externally sync. + high precision sampling - CSAMP\_CFG2.CS\_AZ\_CFG = b11**


**Figure 47** **Signal diagram for the enhanced sensing mode using external synchronization of Auto-Zero function. The charge pump clock is gated to reduce switching noise coupling during periods where sensitive measurements are performed in the system like the ADC in a MCU**

### 3.7 Hall Comparators

The Hall sensor inputs on 6EDL7141 are capable of interfacing with digital Hall sensors with open-drain outputs. The device supports three identical channels. Each Hall sensor should be connected to one of the INLx digital pins. Hall comparators are designed to be used in 1PWM mode with Hall sensors, described in section 3.2.4 as well as for ‘locked rotor’ detection functionality described in 3.8.3.

The Hall inputs are digitally deglitched. That means those inputs ignore any extra Hall transitions for a configurable period of time. This is selected in bitfield HALL\_DEGLITCH that can be accessed via SPI commands. This prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

The polarity of the Hall sensor inputs can be read at any time by a MCU in register FUNCT\_ST, bitfield HALLIN\_ST.

DVDD linear voltage regulator can be used to supply Hall sensors either with 3.3V or 5V according to programming. In case Hall sensors are not powered from DVDD rail (i.e. other power supply) and DVDD supply is disabled for any reason, due to IDLE or OFF mode ( $CE < CE_{TH}$ ), the Hall inputs should not be driven by external voltages. In addition, they should be powered-up before starting the motor, or an invalid Hall state may cause malfunction in the motor operation.

### 3.8 Watchdog Timers

6EDL7141 integrates three independent watchdog timers that are SPI configurable. These are protection features used to ensure the correct functionality of different modules inside and outside the device, e.g. to ensure that a microcontroller is having correct behaviour by serving or ‘kicking’ 6EDL7141 watchdog. To configure watchdog timers in 6EDL7141, two registers are available: WD\_CFG and WD\_CFG2. The three independent watchdog timers are:

**Product Features**

- Buck converter watchdog:
- General purpose watchdog
- Rotor locked watchdog

Each watchdog timer core unit includes a digital timer (watchdog timer). A source signal is connected to that timer which resets whenever a toggle occurs on the signal. Otherwise the timer keeps counting up. If the watchdog timer limit is reached without a reset input, then a fault takes place and action will be performed according to Table 17.

The reaction to a watchdog fault is programmable to following actions:

- Reporting to status register only.
- Reporting to status register and nFAULT pin.
- Trigger a configurable braking event.
- Select whether watchdog fault is latched or not.

An example of watchdog operation is presented in Figure 48. In this example, a generic signal ‘WD\_Input’ is resetting the counter periodically (for example when reading the status register or toggling EN\_DRV at the proper frequency). If the input signal stops toggling, the watchdog timer expires after the watchdog period resulting in a watchdog fault.

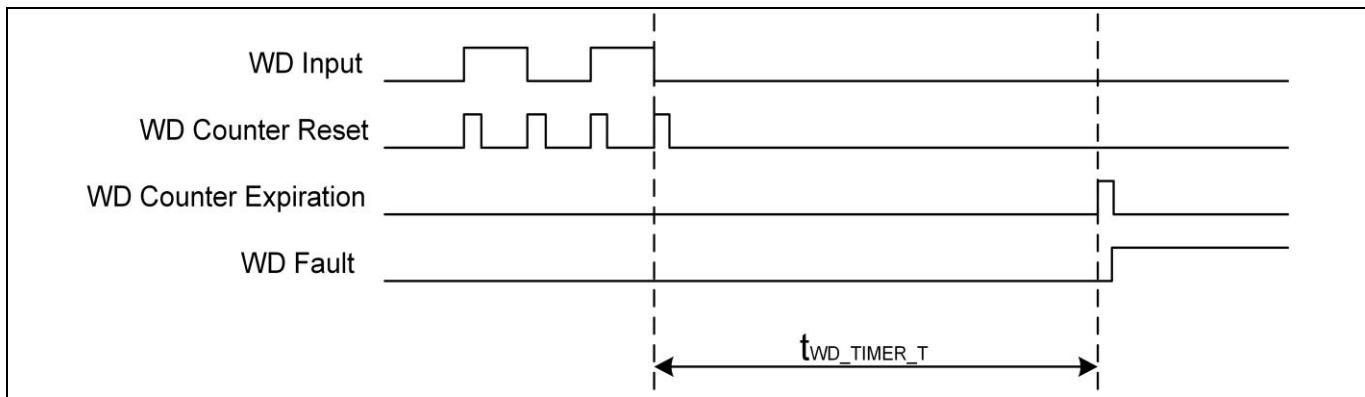


Figure 48     **Watchdog operation diagram**

### **3.8.1     Buck converter watchdog**

During start-up of the device, this watchdog monitors VDDB UVLO signal. When UVLO of VDDB is asserted, the watchdog is cleared. If UVLO of VDDB is not asserted within the watchdog period ( $t_{WD\_BUCK\_T}$ ), the system will stop (STOP state in the state machine is described in section 5) and stay disabled until a power cycle takes place. This watchdog can be used for safe start-up debugging. To enable this feature WD\_CFG2, bitfield WD\_BK\_DIS needs to be accessed.

### **3.8.2     General Purpose Watchdog**

This watchdog timer can be configured to use different general purpose inputs (timer reset signal) via register WD\_INPUT. Possible inputs are:

- **EN\_DRV** – coded in EN\_DRV, a clock signal can be utilized as watchdog timer clock input. The watchdog measure that the frequency and duty cycle of this signal are correct. The proper frequency works as a watchdog ‘kick’- see 3.9.1. Requires enabling the watchdog via WD\_EN and input selection via WD\_INSEL. After fault occurs, clearing of the fault must be done only after 2 periods (500Hz). Watchdog period programmed in WD\_TIMER\_T.

- **DVDD start-up:** during start-up, if this input is selected, the watchdog will be cleared upon DVDD UVLO signal assertion. If DVDD has not reached the correct value before the watchdog period, the DVDD regulator will retry to start. The number of attempts to restart DVDD regulator when start-up fails, can be configured in WD\_DVDD\_RSTRT\_ATT. Additionally, the time between restarts attempts is set in bitfield WD\_DVDD\_RSTRT\_DLY
- **Charge pumps start-up:** similarly, the start-up time of the charge pumps (both) can be monitored. The UVLO signal of both VCCHS and VCCLS will clear the watchdog, otherwise, a fault will be reported. To select this input, bitfield in WD\_INSEL has to be set accordingly.
- **Status register SPI read action:** in this configuration, the watchdog resets every time the FAULT\_ST status register is read via a SPI command. In this way, it checks that the MCU is active and that the SPI communication is working adequately.

The general purpose watchdog timer needs to be enabled via WD\_EN bitfield. Watchdog period programmed din WD\_TIMER\_T.

### **Brake on General Purpose Watchdog Fault**

The general purpose watchdog timer can be configured to trigger a brake event when the comparator trips. This is activated in bitfield WD\_BRAKE and is only possible to the conditions, when either 'EN\_DRV' or 'Status register read' are chosen as input. The brake event can be configured to either brake the motor by shorting all high side MOSFETs, all low side MOSFETs, alternate between those options or set all MOSFETs to high Z. This is explained in more detail in sections 3.2.6 and 6. This is configured in bitfields BRAKE\_CFG in PWM\_CFG register.

### **3.8.3 Locked-Rotor Protection Watchdog Timer**

6EDL7141 provides a locked or stalled rotor protection function by integrating a dedicated watchdog timer. The rotor locked watchdog timer inputs are the 3 Hall sensor signals (INLA, INLB and INLC). Therefore, this protection is only possible when using Hall sensor based control schemes or 1PWM modes.

Locked or stalled rotor can occur in the event of a mechanical malfunction or excessive load torque that causes the motor to stop rotating while enabled. The locked rotor function can be enabled by setting the bitfield WD\_RLOCK\_EN to b'01.

A locked rotor condition is detected if the Hall pattern is maintained for  $t_{LOCKED}$  period. The  $t_{LOCKED}$  time is configured via SPI (bitfield WD\_RLOCK\_T).

In order to increase robustness, an especial case of rotor locked detection is implemented. In some cases, the motor stalls in a position in which the Hall sensors can still provide a cyclic or repeated toggling. In some cases vibration or bending of the motor can cause this effect, in other cases, the Hall sensors get stalled close to the magnets. 6EDL7141 detects this condition as rotor locked. An example is of such Hall sensor inputs sequence that would report a fault is the following:

100, 101, 100, 101, 100, 101, .....

As soon as the locked rotor condition is detected, the device sets bitfields WD\_FLT and RLOCK\_FLT of the FAULT\_ST register to b'01. Upon detection of locked rotor condition the device enters high impedance state (high Z). Additionally, nFAULT pin will be pulled down. An MCU can read this signal and request a status update to the device or execute other corrective actions.

### **Hall Sensor Malfunction**

In case of Hall sensor failure, the rotor locked protection can help to bring the motor to a safe state. The malfunction of 2 or 3 Hall sensors will cause a rotor lock fault in 6EDL7141, however, a single Hall sensor failure cannot be detected as malfunction and does not trigger a fault.

The rotor locked condition can be reset by toggling EN\_DRV (switch off and on again).

### Hall Comparators when PWM Signals are on Hold

If the PWM input signals generated by the controller stop switching while the rotor locked protection is enabled, 6EDL7141 will recognize this as a failure and it will trigger the rotor locked protection after  $t_{LOCKED}$  period. In case this behavior is not desired, the user code in the controller that stopped the PWM switching must be preceded by a command (SPI) to disable the rotor locked protection.

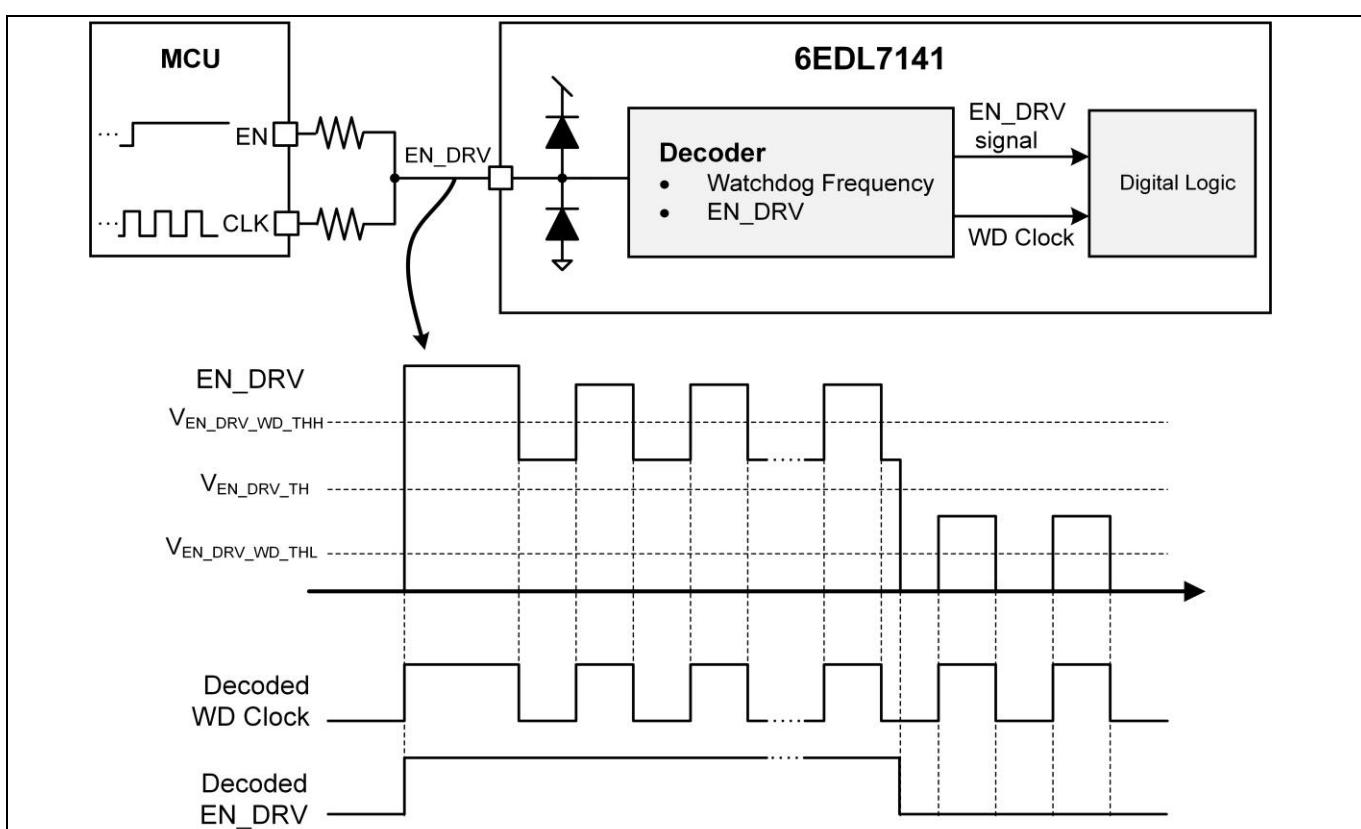
## 3.9 Multi-Function Pins

### 3.9.1 EN\_DRV Pin

The pin EN\_DRV has two different functionalities that can work simultaneously:

1. To start the charge pump operation and finally enable gate drivers and current sense amplifiers when pulled high: EN\_DRV > V<sub>EN\_DRV\_TH</sub> (see Electrical Characteristics table)
2. As watchdog clock input. This clock signal can be generated by the microcontroller in the system and permits 6EDL7141 to detect whether the microcontroller is generating the correct signal, and therefore to detect if the controller is working properly or not (e.g. software failure), increasing robustness of the whole system. In case the clock signal is not present or the period of this clock is outside of 10% of the expected value (see Electrical Characteristics table), the watchdog of 6EDL7141 will implement a pre-programmed action (More details in section 3.6.8.3).

In case both functions are used simultaneously, the microcontroller can use 2 GPIOs, one for EN\_DRV (GPIO) and one for the clock generation (GPIO or PWM signal for example). The analog summation of those two signals is decoded inside 6EDL7141. Figure 49 describes the connections and electrical signals in such configuration.



**Figure 49 Usage of EN\_DRV pin for both enabling driver stage and decoding of watchdog clock signal**

### 3.9.2 VSENSE/nBRAKE Pin

Pin VSENSE/nBRAKE supports 2 different functionalities:

1. During start-up, 6EDL7141 reads the resistor value connected to pin VSENSE/nBRAKE. Depending on the reading, 6EDL7141 selects the DVDD set point to either 3.3V or 5V. After the value is read, the device will start-up DVDD with the target DVDD set point.
2. During normal operation (after UVLO DVDD is released), the pin is an input (inverted logic) that can be pulled down (e.g.) by the MCU to initiate a brake event, bringing the motor to a standstill in a controlled way. If the pin is set high, the PWM signals propagate normally to the outputs.

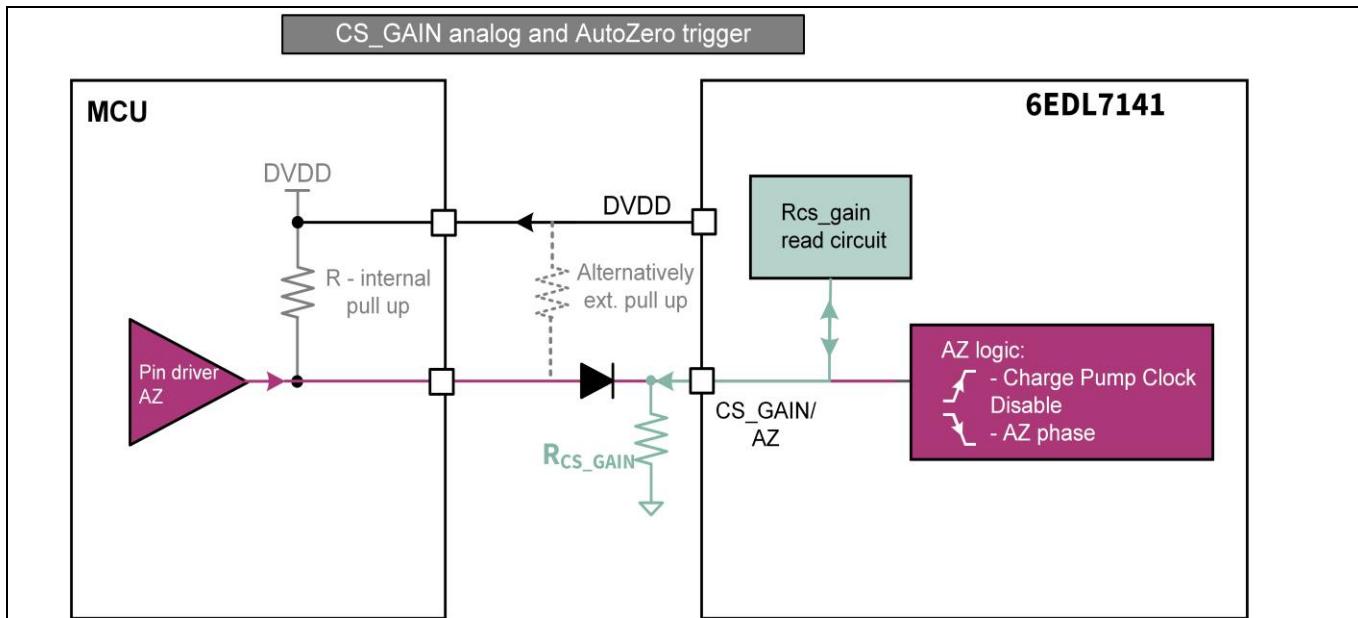
### 3.9.3 CS\_GAIN/AZ Pin

CS\_GAIN/AZ pin implements two different functionalities:

1. During start-up, the resistor connected to this pin is read leading to the configuration of the current sense amplifier gain. This is explained in detail in section 3.6.6.
2. Simultaneously, during normal operation, the pin can be used as an input to enable the external Auto-Zero functionality described in 3.6.8.

In order to avoid affecting the analog programming of the current sense amplifiers gain via an external resistor, the MCU is recommended to be connected to the CS\_GAIN pin with a series diode. In this way when DVDD is still not at the final target value, the MCU output circuitry will not load the CS\_GAIN pin leading to a wrong programming of the amplifier's gain. This proposed circuit is shown in Figure 50.

If digital programming of the current sense amplifier gain is desired,  $R_{CS\_GAIN}$  is not needed and the diode can be excluded from the circuit as well.



**Figure 50 CS\_GAIN/AZ multifunction pin usage example: one as CSAMP gain setting via resistor reading during start-up, two as external Auto-Zero function where MCU decides when to Auto-Zero CSAMP.**

Note:

The internal pull up in the MCU side depends on the specific microcontroller. Some microcontrollers might not offer enough pull up capability and an external pull up resistor might be required as shown.

### 3.10 ADC Module-Analog to Digital Converter

6EDL7141 integrates an ADC based on SAR architecture with 7 bits resolution. This ADC can be used to do redundant measurements to those executed in the MCU or to measure gate driver related voltages. The MCU can request the results of these internal measurements via SPI reads of ADC\_ST register. The ADC can measure following inputs during ACTIVE mode:

- Automatically in ADC conversion sequence:
  - On die **temperature** sensor (see 3.10.2)
  - **PVDD**: supply voltage
  - **VCCLS**: low side gate driver supply
  - **VCCHS**: high side gate driver supply
- Other (on demand) conversion inputs selected via bitfield ADC\_OD\_INSEL :
  - **I<sub>DIGITAL</sub>**: device digital section current consumption
  - **DVDD**: linear regulator output voltage
  - **VDDB**: buck converter output voltage

Those ADC inputs are continuously converted in sequence. After each conversion is finished, the result of the conversion can be processed through integrated digital filters. These are moving average filters with configurable number of samples. PVDD uses a dedicated filter (ADC\_FILT\_CFG\_P) while the rest share a second filter (ADC\_FILT\_CFG). The complete architecture of the ADC module is depicted in Figure 51.

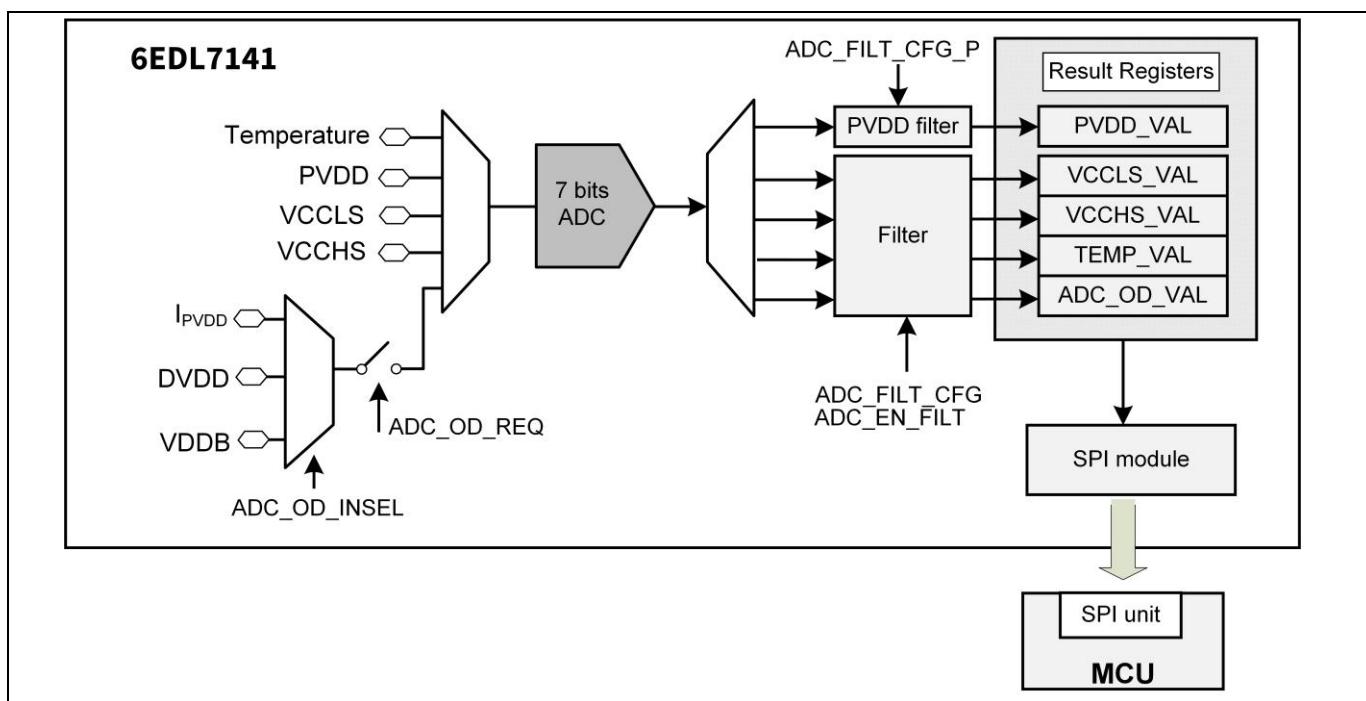


Figure 51 ADC module block diagram

Table 16 summarizes the ADC inputs characteristic including the scaling factors. These scaling factors can be used by a MCU to calculate back the real analog values in volts, amperes or degree Celsius.

**Table 16 ADC measurements overview**

Measurement	On demand conversion	Bitfield	Filter - register	Scaling factor
PVDD	N	PVDD_VAL	ADC_FILT_CF_G_P	= $(0.581 * PVDD_{VAL} + 5.52) V$
Temperature	N	TEMP_VAL	ADC_FILT_CF_G	= $(2 * TEMP_{VAL} - 94) ^\circ C$
VCCLS	N	VCCLS_VAL	ADC_FILT_CF_G	= $VCCLS_{VAL} * \frac{16}{127} V$
VCCHS	N	VCCHS_VAL	ADC_FILT_CF_G	= $VCCHS_{VAL} * \frac{16}{127} V$
Device current ( $I_{PVDD}$ )	Y	ADC_OD_VAL	ADC_FILT_CF_G	= $(0.24 * ADC_{OD}_{VAL}) mA$
DVDD	Y	ADC_OD_VAL	ADC_FILT_CF_G	= $ADC_{OD}_{VAL} * \frac{DVDD_{TARGET}}{127} V$
VDDB	Y	ADC_OD_VAL	ADC_FILT_CF_G	= $ADC_{OD}_{VAL} * \frac{VDDB_{TARGET}}{127} V$

For example, if DVDD voltage is the desired parameter, the MCU will read via SPI register ADC\_OD\_VAL. For example let's assume DVDD is set to be 3.3V and that the reading was 0x78=120 decimal value. The MCU or the user reading for example via a GUI, can calculate following:

$$DVDD = ADC_{OD}_{VAL} * \frac{3.3V}{2^7} = 120 * \frac{3.3V}{127} = 3.118V \quad (7)$$

### 3.10.1 ADC Measurement Sequencing and On Demand Conversion

In ACTIVE state, the ADC converts repeatedly in loop the following sequence of 6 measurements:

1. PVDD
2. Temperature sensor
3. PVDD
4. VCCLS
5. PVDD
6. VCCHS

This is shown in Figure 52. Results of those conversions will be placed in the dedicated result registers that can be read via SPI by the MCU. PVDD result is reported in SUPPLY\_ST register, VCCLS and VCCHS are reported in register CP\_ST and the temperature measurement is reported in register TEMP\_ST.

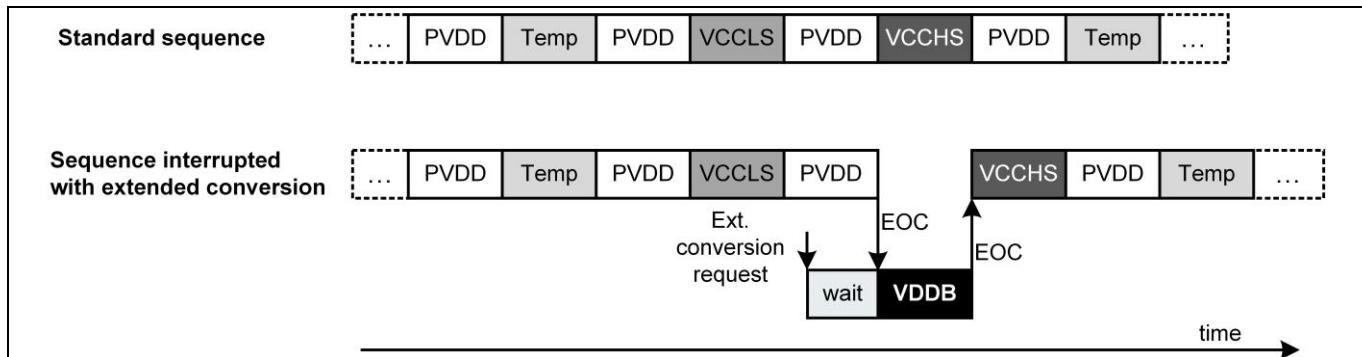
Additional to the standard sequence, the user can select to have other signals converted on demand. Any of this "on demand" conversion inputs, can be injected once in the standard sequence. This is done by selecting the signal to be converted in bitfield ADC\_OD\_INSEL, and setting to '1' the request bitfield ADC\_OD\_REQ.

**Note:** *The write of ADC\_CFG bitfields must happen in a single SPI write. A write to a single bitfield will overwrite the rest to the default value, so the full desired register value must be given in a single write or via read-modify-write sequence.*

If an on demand conversion is requested, the ADC waits to finish (End Of Conversion) any running conversion. Then the requested on demand conversion is started. When the on demand conversion is finished, bitfield ADC\_OD\_RDY is set. The MCU can poll this bitfield to make sure the result register contains newest value of the

**Product Features**

requested conversion. The result of the on demand conversion is located in bitfield ADC\_OD\_VAL and the sequence continues right where it was interrupted after the EOC of the on demand conversion. This is illustrated in Figure 52.



**Figure 52 ADC sequencing and interruption by extended conversion request of VDDB signal**

### 3.10.2 Die Temperature Sensor

An especially useful ADC measurement is the temperature of the die. **6EDL7141 integrates a temperature sensor that is sampled by the integrated ADC.** The temperature of the device can be read via SPI by accessing bitfield TEMP\_VAL in TEMP\_ST register. The value is measured with a resolution of 2 degrees Celsius. Additionally, over-temperature warning and faults are implemented. In register SENSOR\_CFG (OTS\_DIS), the over-temperature shut down protection can be disabled. The threshold values are provided in Table 7. The occurrence of these faults can be detected by reading bitfields OTW\_FLT and OTS\_FLT. According to Table 16, an example reading of 0x4A = 74 would convert into:

$$\text{Temperature} = \text{TEMP\_VAL} * 2^\circ\text{C} - 94^\circ\text{C} = 74 * 2^\circ\text{C} - 94^\circ\text{C} = 54^\circ\text{C} \quad (8)$$

## 4 Device Start-Up

The device start-up can be divided in two main periods:

- **Power supply start-up:** initiated by  $CE > V_{CE\_TH\_R}$  leads to ramp up of VDDB and DVDD rails.
- **Gate Driver and CSAMP start-up:** begins with EN\_DRV rise and results in charge pumps ramp up and current sense amplifiers activation

### 4.1 Power Supply Start-Up

Given a steady battery supply voltage (PVDD), the input pin CE will control the start-up of the power supply system. Figure 53 shows graphically the ramp up of buck converter voltage once CE voltage goes above  $V_{CE\_TH\_R}$  value. If external filter capacitor is too large, the ramp up time might be exceeding the values provided in Table 7 ( $t_{VDD\_SFT\_START}$ ). The integrated watchdog can be enabled to monitor and debug the start-up of VDDB, DVDD or charge pumps.

Soft-start for the buck converter is automatically implemented using an integrated DAC for generating the target reference. Once VDDB has reached its UVLO voltage, analog programming starts. This initiates a period of  $t_{AN\_T}$  duration in which the external resistors in CS\_GAIN/AZ and VSENSE/nBRAKE pins are read internally. The analog programming of these two functions can be disabled by user via OTP programming, therefore reducing the start-up time.

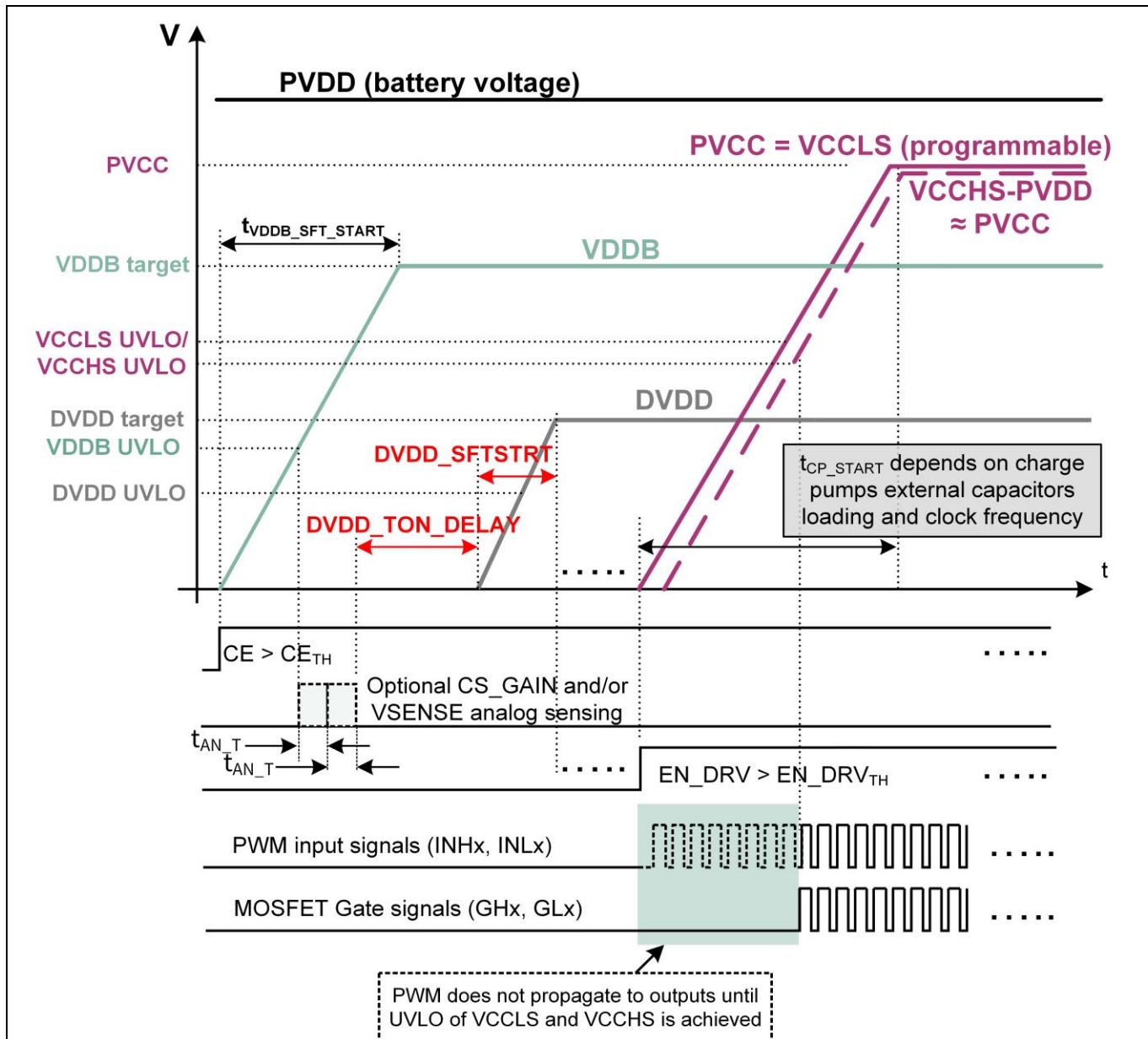
After these analog programming period(s) have elapsed, another OTP programmable delay (DVDD\_TON\_DELAY) is inserted ( $t_{DVDD\_TON\_DLY}$ ) before the DVDD voltage starts ramping up. Longer delays allow the buck converter voltage to stabilize before the DVDD starts charging. If faster start-up time is required, the delay can be shortened taking into consideration the buck output voltage and the external components used ( $L_{BUCK}$ ,  $C_{BUCK}$ ). DVDD will ramp up in a configurable time (DVDD\_SFTSTART). Tuning of this value can help ensuring proper start-up.

### 4.2 Gate Driver and CSAMP Start-up

Once DVDD is up and stable, the microcontroller can enable the gate driver. EN\_DRV pin needs to be set above  $V_{EN\_DRV\_TH}$  value to enable the driver section. Before this, no PWM signal will transfer to the gate of the MOSFETs. Once EN\_DRV is set above  $V_{EN\_DRV\_TH}$ , both low side and high side charge pumps ramp up to the target value PVCC. This time will depend on the different configurations (capacitors, charge pump frequency, PVCC voltage) as explained in 3.4.

The high side charge pump will start after enough voltage is built in the low side charge pump. After both high side and low side charge pumps UVLOs are reached, the PWM path is activated and the gate driver can output signals to the power MOSFET.

**Note:** *Depending on timing of PWM send to inputs and charge pump capacitor values, the gate driver could start driving the MOSFETs while the charge pumps are not fully at target voltage if the PWM signal is activated early. User can delay the start of PWM signals until charge pumps are fully charged if this is required.*



**Figure 53 Start-up behavior of supply voltages at steady PVDD supply. EN\_DRV and CE\_EN functionality. DVDD\_SFTSTART is an SPI programmable parameter**

If CE is generated from PVDD, for example via a voltage divider as shown in Figure 62, the start-up behavior will follow approximately the one in Figure 54 or similar. In such case, it is important to notice that the device will not start – i.e. the buck converter will not start switching- until both PVDD UVLO is released and the CE rising voltage thresholds ( $V_{CE\_TH\_R}$ ) are crossed, as can be seen in flowchart in Figure 55. The order of CE and PVDD can swap with similar results.

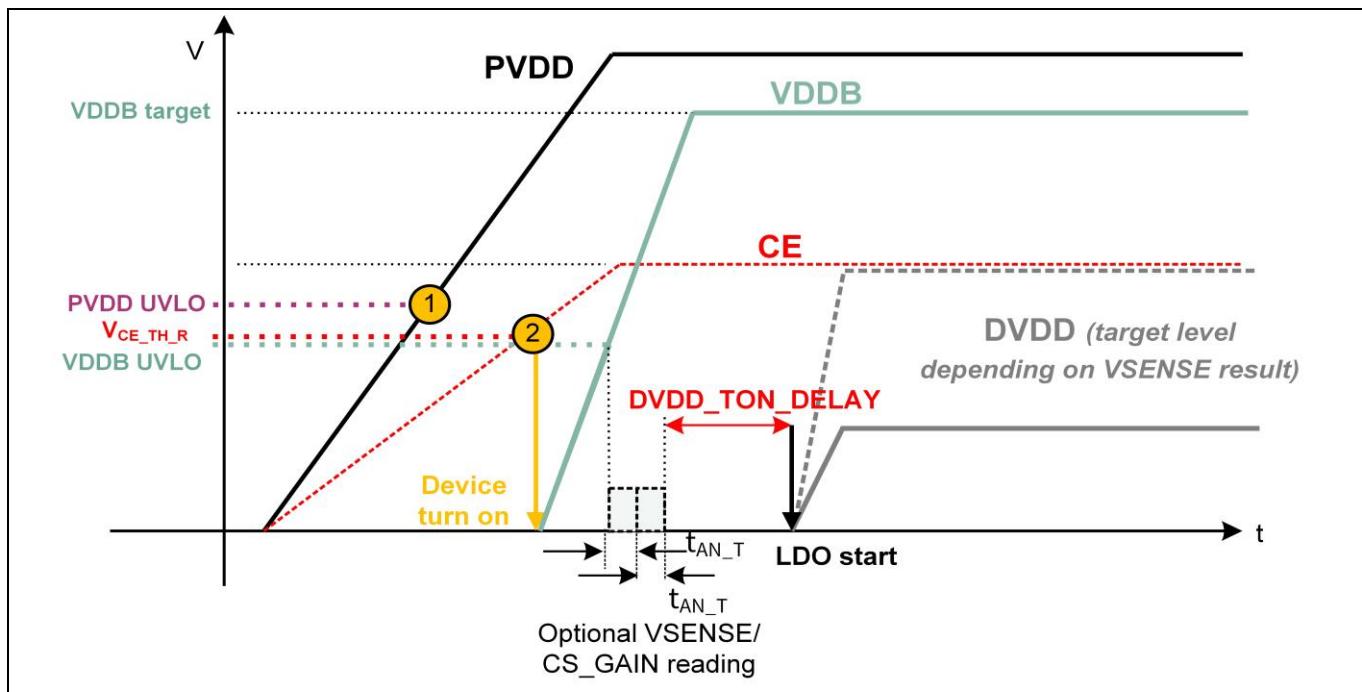


Figure 54 Start-up behavior detail when PVDD is ramping up and CE is created with a voltage divider from PVDD. Device will only turn on after events 1 and 2 occur, starting up the buck converter controller

## 5 Device Functional States

The functionality of the device is governed by a state machine. A flowchart of this state machine is shown in Figure 55.

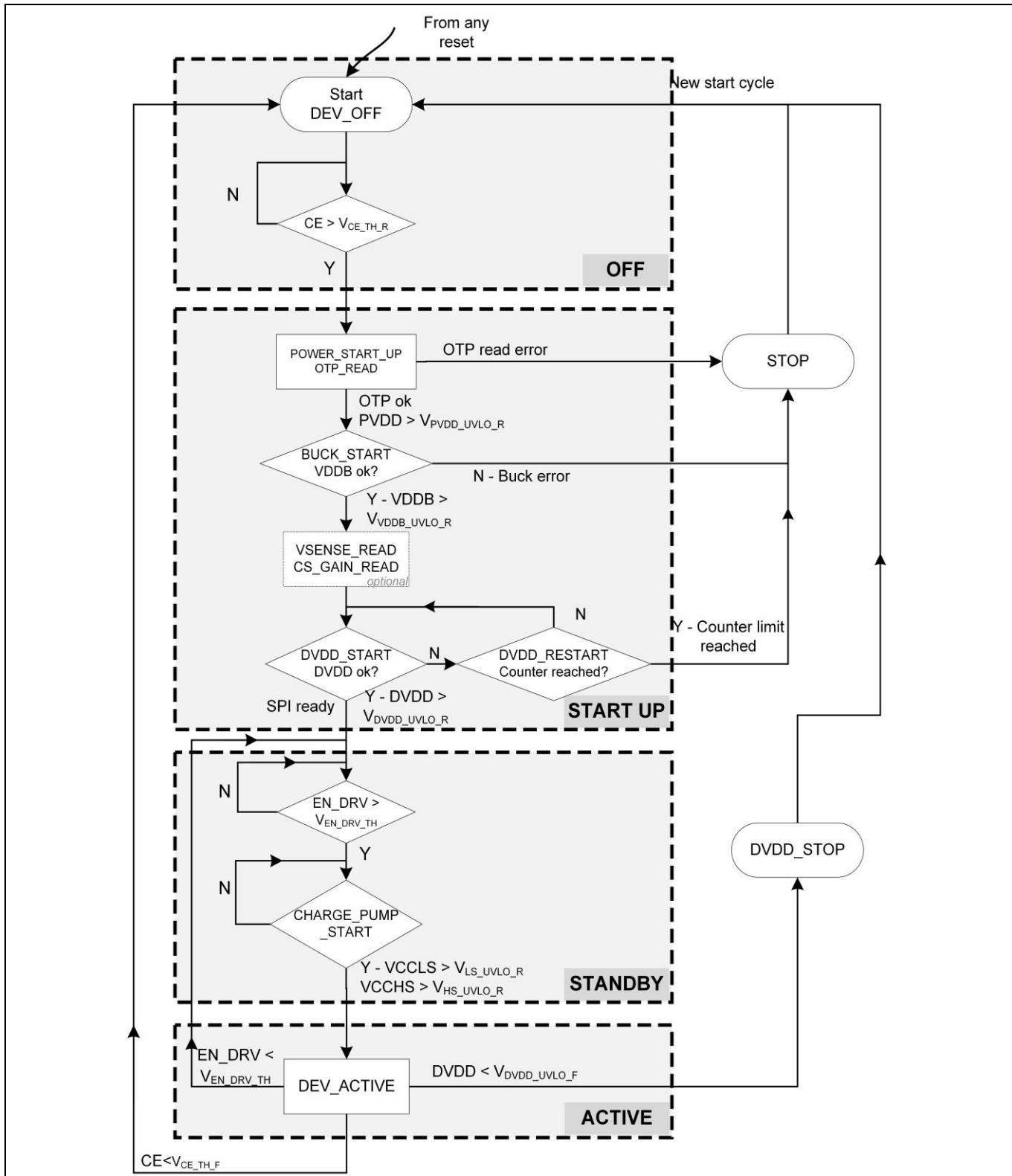


Figure 55 Flowchart diagram for power states of device

Four main modes can be considered for 6EDL7141: OFF\_STATE, START\_UP, STANDBY and ACTIVE. States are described as following:

- **DEV\_OFF** - This state is the default state when in reset.
- **POWER\_START\_UP, OTP\_READ** - In this state voltage in PVDD is ramping up and checked by the device. Once ok, the OTP memory is read. This is done before enabling any further blocks to ensure configuration is known. If a fault is signaled by the OTP block then the STOP state will be entered.
- **BUCK\_START** - The buck converter is enabled in this state and the VDDB needs to be correct before leaving this state. If the VDDB has not reached the target voltage in a certain time, then the buck will be shut down and the device set in the STOP state.

**VSENSE\_READ / CS\_GAIN\_READ** - The device will optionally (programmable) sense pins like VSENSE and CS\_GAIN for checking parameters to be programmed. If the register CS\_GAIN\_ANA is set to '0' then the CS gain will be set by the register CS\_GAIN. Otherwise, if CS\_GAIN\_ANA is set to '1', the analogue programming is enabled.

- **DVDD\_START** – at this point, once the buck converter output is stable, the linear voltage regulator for DVDD is ramped up according the start-up delay and soft start programming. At the end of this state, DVDD is at target voltage and stable. With this, the start-up procedure of the device finishes and enters a wait state until EN\_DRV signal arrives from a microcontroller for example. This will start the standby section.
- **CHARGE\_PUMP\_START** - The charge pumps are enabled. If target voltages are reached, the device moves to DEV\_ACTIVE.
- **DEV\_ACTIVE** (or ACTIVE state) - In this state the driver is ready to be used. The PWM path is enabled. If EN\_DRV signal goes low during active the device turns off both charge pumps and disables the PWM path by going into the STANDBY section.
- **DVDD\_STOP** - This state is entered from states after DVDD has been powered and DVDD rail fails. Device stops operation and requires a CE toggle or power cycle to restart. Buck converter and ADC remains active.
- **STOP** - If this state is entered it is because a serious fault with either the buck converter DVDD start-up. The device will not operate until a power cycle or EN\_DRV toggle takes place. SPI cannot be used during this state.

## 6 Protections and Faults Handling

6EDL7141 contains an extensive number of protections. These are:

- Over-Current Protections (OCP) for:
  - DVDD linear regulator
  - Buck converter
  - Motor leg shunt OCP
- Under-Voltage Lock Out (UVLO) protection for:
  - Gate driver supply voltage both high side and low side drivers
  - Supply voltage PVDD
  - DVDD linear regulator output voltage
  - Buck converter output voltage
- DVDD linear regulator Over Voltage Lock Out (OVLO) protections
- Rotor locked detection based on Hall sensor inputs
- Configurable watchdog
- Over-Temperature Shutdown (OTS) and Warning (OTW)
- OTP memory fault.

An arbitration state machine, takes all the fault inputs from the specific fault blocks and decides which fault needs to be serviced first in case several faults occur at same time (same clock cycle). Once a fault is acknowledged, the system takes the specific action as shown in Table 17 and the arbitration round stops until the fault is cleared.

The state machine is split in two main independent arbitration sections:

- **Supply faults** (B0 to B4). B0 is highest priority.
- **Other faults** (F0 to F7). The fault that happens first will be dealt first and others will be ignored until this fault is removed. If more than one fault happens at the same time, then the one with the highest priority will be processed. F0 is highest priority.

The resultant actions from both sections are OR'ed on nFAULT.

Otherwise if not latched, when the condition for the fault is released, the fault status is held, but the action will stop.

Additionally to any possible actions like switching off PWM signal, status bits will be updated to inform the MCU of any warning or/and fault occurrence. This is done regardless of priority and those status bits can be read via SPI commands by the microcontroller in the system.

**Note:** *It is highly recommended to understand faults reason by reading the status registers and clear faults as soon as they occur so new events can be captured. This is done by writing register FAULTS\_CLR via SPI interface*

Following registers provide information on the status of the device faults:

- FAULT\_ST: holds most of functional related faults. A fault might be triggered only after a number of events of a malfunction. Status will immediately record the event information.
- TEMP\_ST: provides status on temperature warning and the temperature reading itself
- SUPPLY\_ST: reports on status of all supplies UVLO/OVLO and OCPs
- FUNC\_ST: status of OCP faults for each of current sense amplifiers, Hall sensors, wrong hall pattern.

- OTP\_ST: programming and reading of OTP related faults

In order to clear faults the user has to write via SPI the bitfield CLR\_FAULTS in FAULTS\_CLR register. However, to clear a latched fault, a write to CLR\_LATCH register is required.

If ‘Motor leg shunt OCP’ fault is programmed to be latched the fault cannot be cleared until:

- If in OCP counting mode (8, 16 periods) there is one whole PWM period without an OCP event or STANDBY state is entered.
- If in immediate trigger mode then it can be cleared after the fault is gone.

**Table 17** Faults and protections table – lower number means higher priority

Name	Description	Programmability	Latched	nFAULT report	Active State	Prio	Action(s)
VCCLS UVLO	Charge pump low side UVLO fault	-	N	Y	DEV_ACTIVE	F1&2 (shared)	<ul style="list-style-type: none"> <li>External MOSFET outputs set to Hi-Z independently of fault handling. Weak pulldown of all gate driver outputs</li> </ul>
VCCHS UVLO	Charge pump high side UVLO fault	-	N	Y	DEV_ACTIVE	F1&2 (shared)	<ul style="list-style-type: none"> <li>External MOSFET outputs set to Hi-Z independently of fault handling. Weak pulldown of all gate driver outputs</li> </ul>
DVDD OVLO	DVDD OVLO fault	-	N	Y	All states after DVDD ok (after STANDBY)	B1	No action. MCU to perform action
DVDD OCP	DVDD OCP fault	Threshold level	N	Y	All states after DVDD ok (after STANDBY)	B3	No action. MCU to perform action
DVDD UVLO	DVDD UVLO fault	-	N(requires power cycle-CE toggle)	Y (however nFAULT supplied by DVDD)	All states after BUCK_START	B0 and F0	<ul style="list-style-type: none"> <li>External MOSFET outputs set to Hi-Z. Weak pulldown of all gate driver outputs</li> <li>Waits for power cycle (CE pin low and high)</li> <li>Buck converter continues operation</li> <li>When DVDD UVLO happens the functional state machine changes from DEV_ACTIVE to DVDD_STOP. Please refer to section 5 for details. From the application perspective, this fault is highest priority. Requires a power cycle (CE toggle)</li> </ul>
BUCK OCP	Buck Converter Over Current Protection	-	N	Y	All states after DVDD ok (after Standby)-Fault blanked during charge pump start	B2	<ul style="list-style-type: none"> <li>No action. MCU to perform action. Protection is blanked during start-up of charge pumps</li> </ul>
Motor leg shunt OCP	Current sense amplifier Over	Threshold level,	Programmable-	Y	DEV_	F4	<ul style="list-style-type: none"> <li>PWM truncation if configured.</li> </ul>

Name	Description	Programmability	Latched	nFAULT report	Active State	Prio	Action(s)
[2:0]	Current Protection for each phase	count on number of trips, reaction, PWM truncation	Latched if brake on OCP is active		ACTIVE		<ul style="list-style-type: none"> <li>If fault is configured as "Latched" then: sets driver into Hi-Z. Weak pulldown of all gate driver outputs.</li> <li>Brake as defined in PWM_CFG register when CS_OCP_BRAKE register enabled. Fault latched if braking active</li> </ul>
Locked rotor	Locked rotor watchdog overflow	Timing	Y	Y	DEV_ACTIVE	F5	<ul style="list-style-type: none"> <li>External MOSFETs outputs set to High Z. Weak pulldown of all gate driver outputs</li> <li>Requires toggle of EN_DRV to re-start normal operation again</li> </ul>
Watch dog timers	Watchdog timer overflow. Several inputs programmable	Timing, reaction. Depending on input	Programmable- Latched if brake on watchdog fault is enabled	Y (with input EN_DRV only, otherwise not)	Depending on input, either START UP or DEV_ACTIVE	F6	<p>If input:</p> <ul style="list-style-type: none"> <li>- EN_DRV - Hi-Z. Weak pulldown of all gate driver outputs</li> <li>- Buck input- No action required from user or device.</li> <li>- If charge pump input – nFAULT reported. Driver won't start-up.</li> <li>- Others: brake as defined in PWM_CFG register when WD_BRAKE register enabled. Always latched if braked enabled</li> </ul>
OTS	Over Temperature Shutdown	-	Y	Y	DEV_ACTIVE	F3	<ul style="list-style-type: none"> <li>External MOSFET outputs set to Hi-Z. Weak pulldown of all gate driver outputs</li> </ul>
OTW	Over Temperature Warning	-	N	N (only status register report)	DEV_ACTIVE	F8	No action. MCU to perform action
OTP Fault	OTP read fault or OTP user programming error	-	Y	Y	All states	F7	<ul style="list-style-type: none"> <li>External MOSFETs outputs set to Hi-Z</li> <li>Weak pulldown of all gate driver outputs</li> </ul>

## 7 Device Programming-OTP and SPI interface

6EDL7141 includes some smart features that can be programmed by user. The configuration of those features, including gain of amplifiers, driving voltage for gate drivers or fault reactions, is stored in registers while the device is active. The configuration of those functions can be changed during run time operation via SPI commands. These registers are volatile memory cells and therefore, its information will be lost every time the power supply is removed from the device.

For this reason, 6EDL7141 integrates an OTP NVM (One Time Programmable Non-Volatile Memory), that stores a given default configuration even when power supply is not available. Initially the device is programmed with the default register settings provided in section 8. During startup phase of the device (see state machine flowchart in Figure 55), the configuration in the OTP will be copied or mirrored into the volatile registers. These registers are the ones that govern the actual behavior of the device. This is shown in Figure 56.

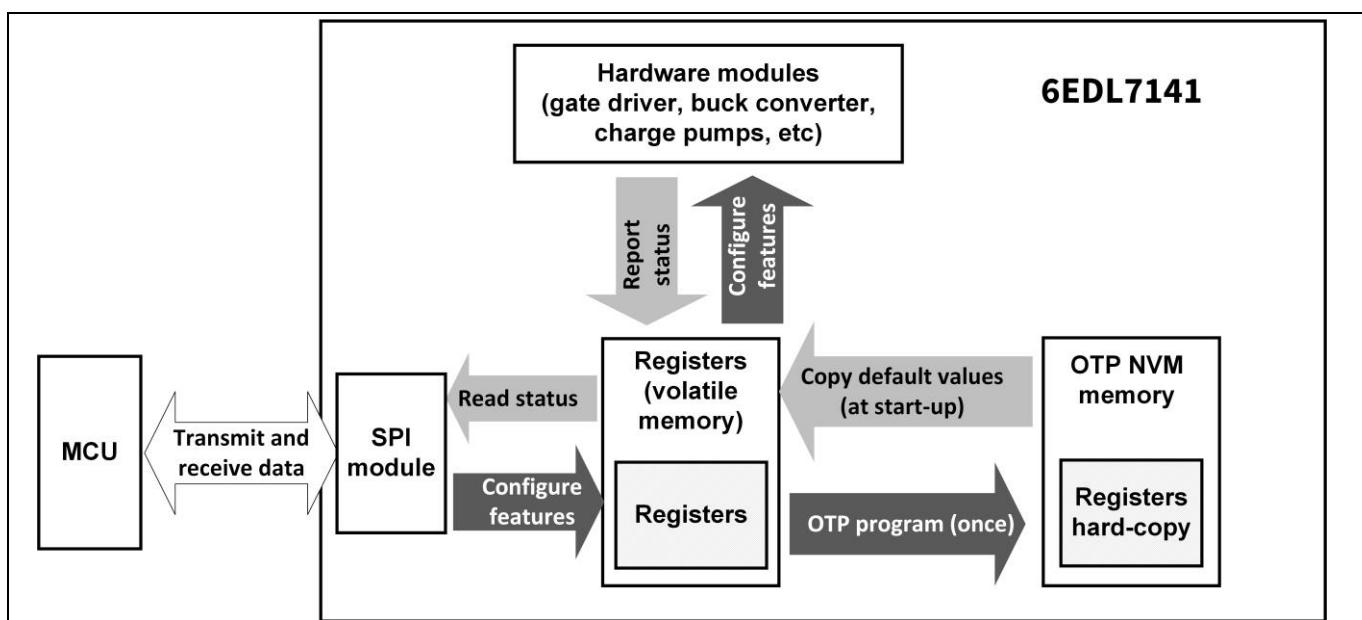


Figure 56 Programming overview

In case the default (“out of the fab”) configuration of the device stored in OTP is not the desired one, the designer can select a different configuration for its application and store it indefinitely in the OTP memory (hard-copy). See section 7.1.1 for detailed programming procedure. This action can be done only once. A second write to the OTP is not possible. However, configurations can be overwritten on volatile registers after start-up via SPI commands as mentioned above.

The user configuration can be tracked thanks to a software ID bitfield -USER\_ID- located in OTP\_PROG register.

**Note:** *It is therefore recommended that every writing action to the registers in 6EDL7141 is followed by a confirmation read to ensure that written and read data in registers match and thus confirming correct programming.*

### 7.1.1 OTP User Programming Procedure: Loading Custom Default Values

6EDL7141 OTP is used for user configuration storage. The OTP module implements a double error correction, plus one additional error detection when programming it.

**Device Programming-OTP and SPI interface**

OTP programming must only occur in a controlled environment. This requires the user to ensure that programming happens at the correct supply voltage, this is  $PVDD > PVDD_{OTP\_PROG}$ . Also the temperature must be below  $T_{OTP\_PROG}$ . Internally both parameters are monitored. This means that if programming is attempted outside of these parameters it will be blocked. If this occurs, then bitfield OTP\_PROG\_BLOCK will be set to '1' to indicate that one of the parameter is outside of the required range. Default values (as given in bold in section 8.2) will be used after start-up in such situation. Further programming attempts are possible. OTP\_PROG\_BLOCK will be reset either when the programming finishes successfully or after a power down.

Following programming steps should be performed to write OTP with a specific configuration:

1. Start device into STANDBY mode ( $EN\_DRV < V_{EN\_DRV\_TH}$ )
2. Write registers to the desired default values via SPI write commands
3. Program these values into OTP using OTP\_PROG bitfield
  - a. If the temperature is higher than  $T_{OTP\_PROG}$  or  $PVDD > PVDD_{OTP\_PROG}$ , then programming does not start and OTP\_PROG\_BLOCK is set to '1'. Conditions might be modified and the programming can be attempted again. If the programming fails twice, the device will be blocked signaled by  $OTP\_USED = b'1$ ,  $OTP\_PASS = b'0$
  - b. If temperature and PVDD values are in range, programming starts, copying register parameters into the OTP memory. This can only be done once.
4. (Recommended) Check if OTP programming succeeded via bitfields OTP\_USED and OTP\_PASS or OTP\_PROG\_FAIL:
  - a. If the programming of the OTP failed, then the device will be locked until a power cycle (CE pin pulled down and up) takes place. Signaled by  $OTP\_USED = b'1$  and  $OTP\_PASS = b'0$  or simply  $OTP\_PROG\_FAIL = b'1$ . Further programming of OTP is not possible. Memory content is considered corrupted and therefore the part should be discarded.
  - b. If programming succeeded, then normal function will continue. This is signaled by  $OTP\_USED = b'01$  and  $OTP\_PASS = b'01$  or simply  $OTP\_PROG\_FAIL = b'0$ . It is recommended to perform a power cycle (CE pin pulled down and up) for new values to take effect after a successful programming

Trying to write an already programmed OTP will be ignored. The OTP status is summarized in Table 18

**Table 18     OTP programming status**

<b>Device status</b>	<b>OTP_USED</b>	<b>OTP_PASS</b>	<b>OTP_PROG_BLOCK</b>	<b>OTP_PROG_FA IL</b>	<b>Status Description</b>
Non-programmed device	0	0	0	0	Default values used
Successful programming of OTP	1	1	X	X	User programming was successful. Upon start-up, the newly programmed default values will be loaded into registers for custom configuration
Programming blocked due to PVDD or temperature conditions	0	0	1	0	Part can be reprogrammed once condition are under limits
Programming started but failed during operation due to PVDD or temperature conditions	1	0	1	1	Part must be discarded
Programming started but failed due to OTP issue	1	0	0	1	Part must be discarded

## Device Programming-OTP and SPI interface

An OTP programming failure (wrong copy of registers into OTP memory) will force the device to enter STOP state during read out (see Figure 55). In such case, the fault is reported on nFAULT pin. The microcontroller, once informed about the fault, can request 6EDL7141 to provide status of memory by reading bitfields OTP\_USED, OTP\_PASS, or OTP\_PROG\_FAIL, and OTP\_PROG\_BLOCK..

If the user chooses to program OTP during start-up of the microcontroller software, this should check each time that OTP\_USED = b'01 before programming again. Otherwise incorrect programming could occur.

### 7.1.2 SPI Communication

All communication between 6EDL7141 and an external microcontroller happens through an integrated SPI interface. This module is used to program the configuration registers and therefore to command the device for example to change settings or program OTP memory.

SPI module is based on a 4-pin configuration. Data sampling happens during the falling edge of the SPI clock signal. All communication happens in a 24 bit length shift register.

- 7 bit address
- 16 bit data byte
- 1 bit command

Data is shifted in with MSB first.

Two commands are defined:

- 1 – Register write
- 0 – Register read

Figure 57 and Figure 58 show respectively write and read operations with SPI interface.

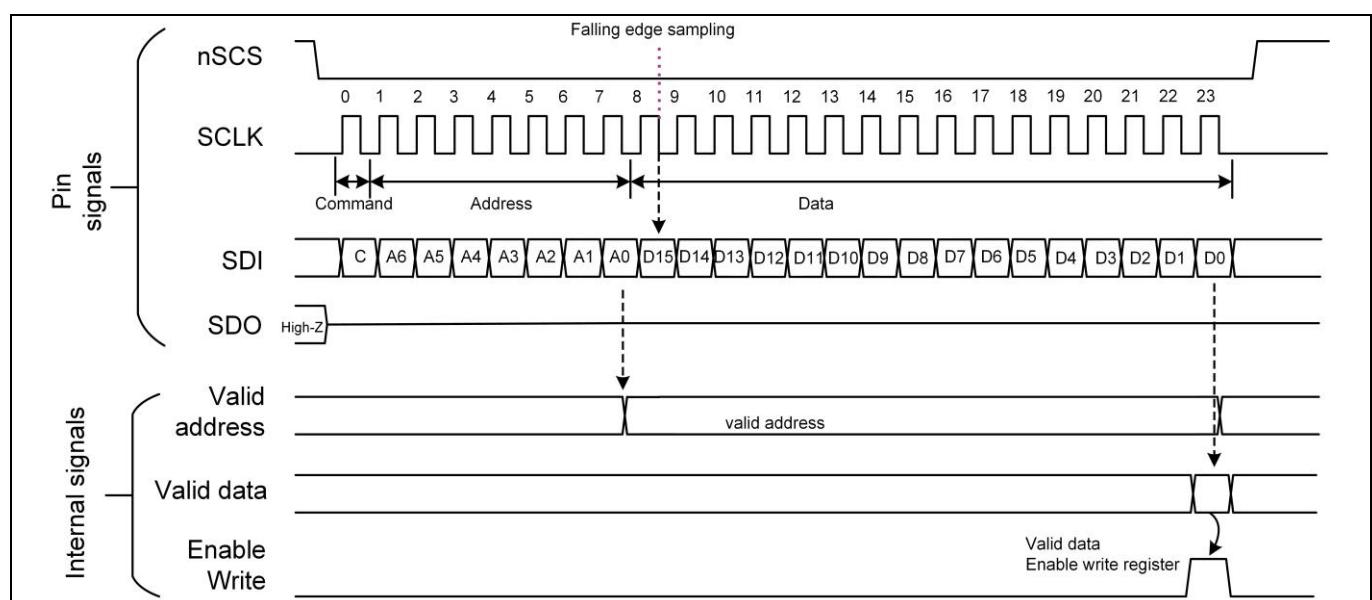


Figure 57 SPI write operation

## Device Programming-OTP and SPI interface

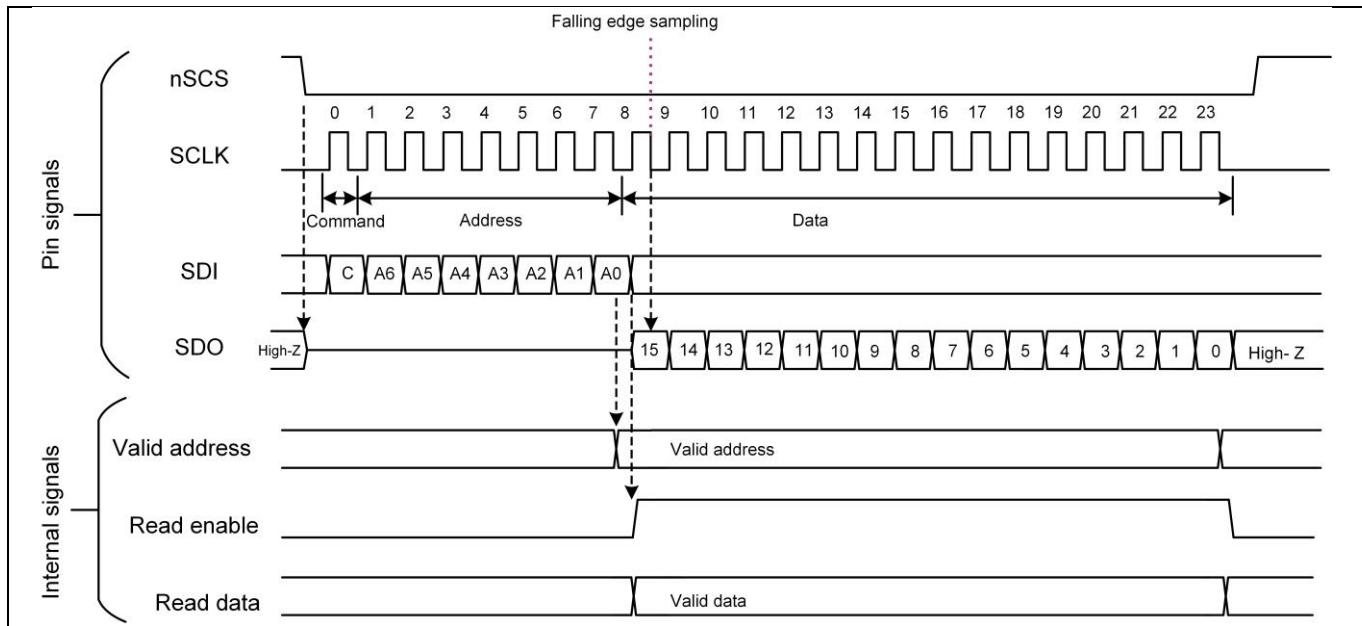


Figure 58 SPI read operation

## 7.1.2.1 SPI Communication Example

If for example, user wants to write new values TDRIVE1 = 50ns (0x01) and TDRIVE2 = 2540ns (0xFE), to register TDRIVE\_SRC\_CFG (address 0x19), then the content of the register needs to be 0xFE01 by collating TDRIVE2 and TDRIVE1 values. The microcontroller then needs to write following command in the SPI bus (SDI signal) once nSCS signal is pulled down:

**Binary: b 1001 1001 1111 1110 0000 0001**

**Hexadecimal: 0x99 FE 01**

If after write, a read is necessary, the following sequence must be applied by the microcontroller. This will read TDRIVE\_SRC\_CFG register by writing SDI signal:

**Binary: b 0001 1001 -----**

**Hexadecimal: 0x19 --**

## 8 Register Map

Table 19 shows a complete list of registers in 6EDL7141 accessible via SPI interface. Registers are explained in detail in this section.

**Table 19 Register map overview**

Short Name	Long Name	Offset Address	Page Link
FAULT_ST	Fault and warning status	00H	<a href="#">96</a>
TEMP_ST	Temperature status	01H	<a href="#">97</a>
SUPPLY_ST	Power supply status	02H	<a href="#">98</a>
FUNC_ST	Functional status	03H	<a href="#">99</a>
OTP_ST	OTP status	04H	<a href="#">100</a>
ADC_ST	ADC status	05H	<a href="#">101</a>
CP_ST	Charge pumps status	06	<a href="#">101</a>
DEVICE_ID	Device ID	07H	<a href="#">102</a>
FAULT_CLR	Fault clear	10H	<a href="#">102</a>
SUPPLY_CFG	Power supply configuration	11H	<a href="#">103</a>
ADC_CFG	ADC configuration	12H	<a href="#">105</a>
PWM_CFG	PWM configuration	13H	<a href="#">106</a>
SENSOR_CFG	Sensor configuration	14H	<a href="#">107</a>
WD_CFG	Watchdog configuration	15H	<a href="#">108</a>
WD_CFG2	Watchdog configuration 2	16H	<a href="#">109</a>
IDRIVE_CFG	Gate driver current configuration	17H	<a href="#">110</a>
IDRIVE_PRE_CFG	Pre-charge gate driver current configuration	18H	<a href="#">111</a>
TDRIVE_SRC_CFG	Gate driver sourcing timing configuration	19H	<a href="#">112</a>
TDRIVE_SINK_CFG	Gate driver sinking timing configuration	1AH	<a href="#">113</a>
DT_CFG	Dead time configuration	1BH	<a href="#">115</a>
CP_CFG	Charge pump configuration	1CH	<a href="#">115</a>
CSAMP_CFG	Current sense amplifier configuration	1DH	<a href="#">116</a>
CSAMP_CFG2	Current sense amplifier configuration 2	1EH	<a href="#">118</a>
OTP_PROG	OTP program	1F	<a href="#">120</a>

### 8.1 Device Programmability

The programmable registers in 6EDL7141 can be programmed at any time after SPI interface is active, however, some of the bitfield changes will not have an effect until certain conditions occur. This is to protect from wrong behaviors or to avoid glitches in the operation. Three categories are defined:

1. **Always programmable:** programming these bitfields will have an effect immediately after programming in any state of the device. The effect can be synchronized with PWM or braking events for some cases.
2. **Standby programmable:** programming these bitfields will have an effect only when EN\_DRV level is low. If programmed when EN\_DRV is high, the register will show the new value, but effect will not be applied until

**Register Map**

*EN\_DRV* is pulled down. This is to avoid system malfunctions. Therefore these registers are recommended to be programmed before *EN\_DRV* is activated.

3. **OTP only:** programming these bitfields will have an effect only if programmed in OTP and after device new power up (*PVDD*). These are settings affecting the start-up of the device, namely bitfields whose effect takes place even before *DVDD* ramps up, therefore must be burned into OTP to be effective on next power up.

As an example, if during ACTIVE state a write happens to a ‘Standby’ value, the value will be written and reads to this register will return the written value, however, the value is not (shadow) transferred to actual effective register until the device state machine goes into STANDBY state.

Table 20 provides a categorization for every configuration of the device (‘w’ type bitfield)

**Table 20 Register programmability**

Register Name	Bitfield Name	Programmability
SUPPLY_CFG	PVCC_SETPT	Standby
	CS_REF_CFG	Standby
	DVDD_OCP_CFG	Always
	DVDD_SFTSTRT	OTP only
	DVDD_SETPT	OTP only
	BK_FREQ	Standby
	DVDD_TON_DELAY	OTP only
	CP_PRE_CHARGE_EN	Standby
ADC_CFG	ADC_OD_REQ	Always – no OTP field, just register
	ADC_OD_INSEL	Always – no OTP field, just register
	ADC_EN_FILT	Always – no OTP field, just register
	ADC_FILT_CFG	Always
	ADC_FILT_CFG_PVDD	Always
PWM_CFG	PWM_MODE	Standby
	PWM_FREEW_CFG	Always
	BRAKE_CFG	Always
	PWM_RECIRC	Standby
SENSOR_CFG	HALL_DEGLITCH	Always
	OTS_DIS	Always
	CS_TMODE	Always
WD_CFG	WD_EN	Standby
	WD_INSEL	Standby
	WD_FLTCFG	Standby
	WD_TIMER_T	Standby
WD_CFG2	WD_BRAKE	Standby
	WD_EN_LATCH	Standby
	WD_DVDD_RSTRT_ATT	Standby
	WD_DVDD_RSTRT_DLY	Standby
	WD_RLOCK_EN	Always
	WD_RLOCK_T	Always

## Register Map

Register Name	Bitfield Name	Programmability
	WD_BK_DIS	OTP only
IDRIVE_CFG	IHS_SRC	Always
	IHS_SNK	Always
	ILS_SRC	Always
	ILS_SNK	Always
IDRIVE_PRE_CFG	I_PRE_SRC	Always
	I_PRE_SNK	Always
	I_PRE_EN	Always
TDRIVE_SRC_CFG	TDRIVE1	Always
	TDRIVE2	Always
TDRIVE_SINK_CFG	TDRIVE3	Always
	TDRIVE4	Always
DT_CFG	DT_RISE	Always
	DT_FALL	Always
CP_CFG	CP_CLK_CFG	Always
	CP_CLK_SS_DIS	Standby
CSAMP_CFG	CS_GAIN	Always – recommended to stop PWM first
	CS_GAIN_ANA	Standby (change to digital mode)- change to analog mode only possible if written in OTP followed by power cycle
	CS_EN	Always
	CS_BLANK	Always – recommended to stop PWM first
	CS_EN_DCCAL	Standby
	CS_OCP_DEGLITCH	Standby
CSAMP_CFG2	CS_OCP_PTHR	Always
	CS_OCP_NTHR	Always
	CS_OCP_LATCH	Standby
	CS_MODE	Standby
	CS_OCP_BRAKE	Standby
	CS_TRUNC_DIS	Always
	VREF_INSEL	Standby
	CS_AZ_CFG	Always
OTP_PROG	OTP_PROG	Standby (programming of OTP only in Standby)
	USER_ID	Always

**Register Map****Table 21 Register read/write coding description**

Code	Access type	Description
res	No access	Reserved
r	Read	Read only. A write produces no action
rw	Read/Write	Read or write by user
w	Write	Write only. A read returns 0

## Register Map

## 8.2 Register Map

## Faults Status Register

If the status of one of the bits switches to value b'1, the corresponding fault/warning has occurred. To clear the fault use the clear faults bit in the FAULTS\_CLR register

																Address:	00 <sub>H</sub>
																Reset Value	0000 <sub>H</sub>
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	0		OTP_FLT	WD_FLT	RLOCK_FLT	OTW_FLT	OTS_FLT	BK_OCP_FLT	DVDD_OV_FLT	DVDD_UV_FLT	DVDD_OCP_FLT	CP_FLT	CS_OCP_FLT				
res	r	r	r	r	r	r	r	r	r	r	r	r	r	r			

Field	Bits	Type	Description
CS_OCP_FLT	2:0	r	<b>Current sense amplifier OCP fault status</b> OCP (shunt amplifier OCP) fault status bXX0: No fault on phase A bXX1: Fault on phase A bX0X: No Fault on phase B bX1X: Fault on phase B b0XX: No Fault on phase C b1XX: Fault on phase C
CP_FLT	3	r	<b>Charge pumps fault status</b> Charge pump low side and high side combined fault status b0: No fault has occurred b1: A fault has occurred
DVDD_OCP_FLT	4	r	<b>DVDD OCP (Over-Current Protection) fault status</b> DVDD linear voltage regulator Over-Current-Protection fault status b0: No fault has occurred b1: A fault has occurred
DVDD_UV_FLT	5	r	<b>DVDD UVLO (Under-Voltage Lock-Out) fault status</b> DVDD UVLO fault status b0: No fault has occurred b1: A fault has occurred
DVDD_OV_FLT	6	r	<b>DVDD OVLO (Over-Voltage Lock-Out) fault status</b> DVDD OVLO fault status b0: No fault has occurred b1: A fault has occurred
BK_OCP_FLT	7	r	<b>Buck OCP fault status</b> Buck Over-Current-Protection fault status b0: No fault has occurred b1: A fault has occurred

## Register Map

<b>OTS_FLT</b>	8	r	<b>Over-temperature shutdown fault status</b> Over temperature shutdown event status b0: No fault has occurred b1: A fault has occurred
<b>OTW_FLT</b>	9	r	<b>Over-temperature warning status</b> Over temperature warning signal status b0: No warning signal has occurred b1: A warning signal has occurred
<b>RLOCK_FLT</b>	10	r	<b>Locked rotor fault status</b> Locked Rotor fault status using hall sensors b0: No fault has occurred b1: A fault has occurred
<b>WD_FLT</b>	11	r	<b>Watchdog fault status</b> Watchdog status b0: No fault has occurred b1: A fault has occurred
<b>OTP_FLT</b>	12	r	<b>OTP status</b> OTP (One Time Programmable) memory fault status b0: No fault has occurred b1: A fault has occurred
<b>0</b>	15:13	res	<b>Reserved</b> A read always returns 0

## Temperature Status Register

This register contains the temperature value for the MCU to be read

<b>TEMP_ST</b>																Address:	01 <sub>H</sub>
																Reset Value	0000 <sub>H</sub>
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0															<b>TEMP_VAL</b>		
res															r		

Field	Bits	Type	Description
<b>TEMP_VAL</b>	6:0	r	<b>Temperature reading</b> Temperature value in step of 2 degrees b000000: -94 degrees Celsius ..... every 2 degrees Celsius b1111111: 162 degrees Celsius
<b>0</b>	15:7	res	<b>Reserved</b> A read always returns 0

## Register Map

**Power Supply Status Register**

This register contains status of power supply related blocks

**SUPPLY\_ST**

Power Supply Status

Address: 02<sub>H</sub>Reset Value 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										VDDB_OVST	VDDB_UVST	DVDD_OVST	DVDD_UVST	VCCHS_UVST	VCCLS_UVST
res							r		r	r	r	r	r	r	r

Field	Bits	Type	Description
<b>VCCLS_UVS_T</b>	0	r	<b>Charge Pump low side UVLO status</b> b0: Below threshold b1: Above threshold
<b>VCCHS_UVS_T</b>	1	r	<b>Charge Pump high side UVLO status</b> b0: Below threshold b1: Above threshold
<b>DVDD_UVST</b>	2	r	<b>DVDD UVLO status</b> b0: Below threshold b1: Above threshold
<b>DVDD_OVST</b>	3	r	<b>DVDD OVLO (Over-Voltage Lock-Out) status</b> b0: Below threshold b1: Above threshold
<b>VDDB_UVST</b>	4	r	<b>VDDB UVLO status</b> b0: Below threshold b1: Above threshold
<b>VDDB_OVST</b>	5	r	<b>VDDB OVLO status</b> b0: Below threshold b1: Above threshold
<b>PVDD_VAL</b>	12:6	r	<b>PVDD ADC result reading value</b> This bitfields holds the analog to digital conversions value for PVDD input voltage
<b>0</b>	15:13	r	<b>Reserved</b> A read always returns 0

## Register Map

**Functional Status Register**

Status of various functional signals.

**FUNCT\_ST**Address: 03<sub>H</sub>Reset Value 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								CS_GAIN_ST	DVDD_ST	HALLPOL_ST	HALLIN_ST				
res								r	r	r	r				

Field	Bits	Type	Description
<b>HALLIN_ST</b>	2:0	r	<b>Hall sensor inputs status</b> HALL sensor input status for each phase. b0: signal is low b1: signal is high bit 0: Phase A bit 1: Phase B bit 2: Phase C
<b>HALLPOL_ST</b>	3	r	<b>Hall sensor polarity equal indicator</b> Status bit that indicate if all phases of the hall sensors have the same polarity at the same time. b0: Hall sensors have different polarity b1: Hall sensors have the same polarity
<b>DVDD_ST</b>	4	r	<b>DVDD set point status</b> DVDD set point read value. The reading is independent of whether DVDD is analog or digitally programmed b0: 3.3 V b1: 5 V
<b>CS_GAIN_ST</b>	7:5	r	<b>Status of the current sense amplifiers gain</b> Shows the value of the current sense amplifier gain independently of whether programmed digitally or via external resistor b000: 4 V/V b001: 8 V/V b010: 12 V/V b011: 16 V/V b100: 20 V/V b101: 24 V/V b110: 32 V/V b111: 64 V/V
<b>0</b>	15:8	r	<b>Reserved</b> A read always returns 0

## Register Map

**OTP Status Register**

OTP memory status information is found in this register.

**OTP\_ST**

																Address:	04 <sub>H</sub>
																Reset Value	0000 <sub>H</sub>
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0												OTP_PR OG_FAIL	OTP_ PROG_BLOCK	OTP_ PASS	OTP_ USED	r	r
res																r	r

Field	Bits	Type	Description
<b>OTP_USED</b>	0	r	<b>OTP used</b> This bitfield shows if OTP memory has been written by user or still holds factory defaults: b0: OTP memory is not used: factory defaults b1: OTP memory is used: new custom values loaded
<b>OTP_PASS</b>	1	r	<b>User OTP programming status</b> Is set if user OTP programming has passed without error. b0: Not programmed or not passed. b1: Programming passed without error.
<b>OTP_PROG_BLOCK</b>	2	r	<b>User OTP programming blocked</b> Signals if OTP programming has been attempted when voltage or temperature outside range. b0: Programming was not blocked b1: Programming blocked
<b>OTP_PROG_FAIL</b>	3	r	<b>OTP Programming fail</b> If set, indicates that the programming of the OTP has failed. b0: No failure. b1: Programming failed
<b>0</b>	15:4	res	<b>Reserved</b> A read always returns 0

## ADC Status Register

ADC status registers.

### ADC\_ST

																Address:	$05_H$
																Default Name Value	$0000_H$
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0								<b>ADC_OD_VAL</b>								<b>ADC_OD_RDY</b>	
res								r								r	

Field	Bits	Type	Description
<b>ADC_OD_RDY</b>	0	r	<b>ADC on demand conversion result ready</b> This bitfields indicates if ADC result for one of the extended conversions is ready to be read b0: Not ready b1: Ready
<b>ADC_OD_VAL</b>	7:1	r	<b>ADC on demand result value</b> ADC result value for on demand conversions
<b>0</b>	15:8	res	<b>Reserved</b> A read always returns 0

## Charge Pumps Status Register

Charge pumps status registers.

### CP\_ST

																Address:	$06_H$
																Default Name Value	$0000_H$
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0								<b>VCCLS_VAL</b>								<b>VCCHS_VAL</b>	
res								r								r	

Field	Bits	Type	Description
<b>VCCHS_VAL</b>	6:0	r	<b>VCCHS ADC result reading value</b> This bitfields holds the analog to digital conversions value for VCCHS voltage
<b>VCCLS_VAL</b>	13:7	r	<b>VCCLS ADC result reading value</b> This bitfields holds the analog to digital conversions value for VCCLS voltage
<b>0</b>	15:14	res	<b>Reserved</b> A read always returns 0

## Register Map

**Device ID Register**

Device ID

**DEVICE\_ID**

Device ID

Address:

07<sub>H</sub>

Reset Value

0006<sub>H</sub>

Field	Bits	Type	Description
<b>DEV_ID</b>	<b>3:0</b>	r	<b>Device ID</b> Device identifier for user version control
<b>0</b>	15:4	r	<b>Reserved</b> A read always returns 0

**Faults Clear Register**

Clear different faults in the device.

**FAULTS\_CLR**

Address:

10<sub>H</sub>

Reset Value

0000<sub>H</sub>

Field	Bits	Type	Description
<b>CLR_FLTS</b>	0	w	<b>Clear all faults</b> Setting this bitfield will clear all faults in the device excluding latched faults. A reading always returns 0. b0: No action. b1: Clear all fault status bits except latched ones
<b>CLR_LATCH</b>	1	w	<b>Clear all latched faults</b> Setting this bitfield will clear all (and only) latched faults in the device. A reading always returns 0. b0: No action. b1: Clear latched fault status bits
<b>0</b>	15:2	res	<b>Reserved</b> A read always returns 0

## Power Supply Configuration Register

This register contains bitfields to configure and control power supplies in the device.

### SUPPLY\_CFG

												Address:	$11_H$		
												Reset Value	$6000_H$		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CP_PRE_CHARGE_EN</b>	<b>DVDD_TON_DELAY</b>	<b>BK_FREQ</b>	<b>DVDD_SETPT</b>		<b>DVDD_SFTSTRT</b>		<b>DVDD_OCP_CFG</b>	<b>CS_REF_CFG</b>	<b>PVCC_SETPT</b>						
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
<b>PVCC_SETPT</b>	1:0	rw	<b>PVCC set point</b> Configures the target PVCC (gate driving voltage) voltage level <b>b00: 12V</b> b01: 15V b10: 10V b11: 7V
<b>CS_REF_CFG</b>	3:2	rw	<b>Current sense reference configuration (internal VREF voltage)</b> Selects the VREF voltage that is applied as offset in all 3 current shunt amplifiers: <b>b00: ½ DVDD</b> b01: 5/12 DVDD b10: 1/3 DVDD b11: ¼ DVDD
<b>DVDD_OCP_CFG</b>	5:4	rw	<b>DVDD OCP threshold configuration</b> DVDD OCP threshold selection <b>b00: 450mA</b> b01: 300mA b10: 150mA b11: 50mA
<b>DVDD_SFTSTRT</b>	9:6	rw	<b>DVDD soft-start configuration</b> DVDD linear regulator soft start programming 100us stepping 100us up to 1.6ms <b>b0000: 100 us</b> b0001: 200 us ..... 100 us steps ..... b1111: 1.6 ms

## Register Map

<b>DVDD_SETPT</b>	11:10	rw	<b>DVDD set point configuration</b> This bitfield configures DVDD output voltage: <b>b0x use VSENSE pin for analog programming</b> b10 DVDD = 3.3V – digitally programmed b11 DVDD = 5V – digitally programmed
<b>BK_FREQ</b>	12	rw	<b>Buck converter switching frequency selection</b> This bitfield configures the switching frequency of the buck converter <b>b0- Low frequency (500kHz)</b> b1: High frequency (1MHz)
<b>DVDD_TON_DELAY</b>	14:13	rw	<b>DVDD turn on delay configuration</b> The device will wait for the configured time before turning on the DVDD starting counting from VDDB UVLO during start-up of the device b00 - 200us b01 - 400us b10 - 600us <b>b11 - 800us</b>
<b>CP_PRECHARGE_EN</b>	15	rw	<b>Charge pump pre-charge configuration</b> Enables during start-up the pre-charge of the charge pump <b>1'b0 : pre-charge disabled</b> 1'b1 : pre-charge enabled

## ADC Configuration Register

**Note:** *The complete content of the register must be written at once (read-modify-write). Writing a single bitfield at a time will set to default all other bitfields.*

Configuration of ADC related functions.

															Address:	12 <sub>H</sub>
															Reset Value	0000 <sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0								res		rw		rw		rw		w

Field	Bits	Type	Description
<b>ADC_OD_REQ</b>	0	w	<b>ADC on demand conversion request</b> Setting this bitfield will inject an additional measurement in the standard sequence. This additional measurement is selected in ADC_IN_SEL bitfield. A read always return 0. b0: No action. b1: Request the conversion of the signal selected in ADC_IN_SEL
<b>ADC_OD_IN_SEL</b>	2:1	rw	<b>ADC input selection for on demand conversions</b> This bitfield configures the input to the ADC: <b>b00: I<sub>DIGITAL</sub>: device digital area current consumption</b> b01: DVDD b10: VDDB b11: Reserved
<b>ADC_EN_FILT</b>	3	w	<b>Enable filtering for on demand ADC measurement</b> Enables moving averaging filter for on demand ADC measurements. A read always return 0 b0: No action. b1: Enable filtering
<b>ADC_FILT_CFG</b>	5:4	rw	<b>ADC generic filtering configuration</b> Selects the moving averaging filter characteristic for the ADC measurements except PVDD measurements: <b>b00: 8 samples averaging filter</b> b01: 16 samples averaging filter b10: 32 samples averaging filter b11: 64 Samples averaging filter

## Register Map

<b>ADC_FILT_C FG_PVDD</b>	7:6	rw	<b>PVDD ADC measurement result filtering configuration</b> This bitfield selects the moving averaging filter characteristic for PVDD measurement: <b>b00: 32 samples</b> b01: 16 samples b10: 8 samples b11: 1 sample
<b>0</b>	15:8	res	<b>Reserved</b> A read always returns 0

## PWM Configuration Register

Configuration of PWM related configurations.

<b>PWM_CFG</b>																Address:	13 <sub>H</sub>
																Reset Value	0000 <sub>H</sub>
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0							res		rw		rw		rw		rw		
									<b>PWM_RECIRC</b>		<b>BRAKE_CFG</b>		<b>PWM_FREEW_CFG</b>		<b>PWM_MODE</b>		

Field	Bits	Type	Description
<b>PWM_MODE</b>	2:0	rw	<b>PWM commutation mode selection</b> PWM Mode selection: <b>b000: 6PWM mode</b> b001: 3PWM mode b010: 1PWM mode b011: 1PWM with Hall sensors b100: b111: Reserved
<b>PWM_FREEW_CFG</b>	3	rw	<b>PWM freewheeling configuration</b> This bitfield selects which rectification or freewheeling is desired (only for 1 PWM input modes) <b>b0: Active freewheeling</b> b1: Diode freewheeling
<b>BRAKE_CFG</b>	5:4	rw	<b>Brake configuration</b> Brake scheme configuration. <b>b00: Low Side</b> b01: High Side b10: High Z (no power) b11: Brake toggle-alternates between low and high side braking on every braking event

## Register Map

<b>PWM_RECIR_C</b>	6	rw	<b>PWM recirculation selection (only if PWM_MODE = b011:)</b> Setting this bitfield will activate the alternating recirculation feature of the 1PWM with Hall Sensors and Alternating Recirculation PWM mode. Only functional if PWM_MODE=b011. <b>b0: Disable alternating recirculation mode</b> b1: Enable alternating recirculation mode
<b>0</b>	15:7	res	<b>Reserved</b> A read always returns 0

## Sensor Configuration Register

Sensors configuration.

**SENSOR\_CFG** Address: 14<sub>H</sub>  
 Reset Value 0001<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0							<b>CS_TMODE</b>	<b>OTS_DIS</b>	<b>HALL_DEGLITCH</b>							
res							rw	rw	rw							

Field	Bits	Type	Description
<b>HALL_DEGLITCH</b>	3:0	rw	<b>Hall Sensor deglitch</b> Deglitch time configuration for Hall sensor inputs in steps of 640ns b0000: 0ns <b>b0001: 640 ns</b> ... in steps of 640 ns b1111- 9600 ns
<b>OTS_DIS</b>	4	rw	<b>Over-temperature shutdown disable</b> This bitfield allows to disable the shutdown feature due to over temperature in the device: <b>b0: Enable shutdown protection</b> b1: Disable shutdown protection
<b>CS_TMODE</b>	6:5	rw	<b>Current sense amplifier timing mode</b> This bitfield configures how the current sense amplifier operates regarding the timing related to the PWM signals: <b>b00: CS amplifier outputs are active when GLx signal is high</b> b01: CS amplifier outputs are active when GHx signal is low b1x: CS amplifier outputs are always active
<b>0</b>	15:7	res	<b>Reserved</b> A read always returns 0

## Register Map

**Watchdog Configuration Register**

Watchdog controls.

**WD\_CFG**Address: 15<sub>H</sub>Reset Value 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															

Field	Bits	Type	Description
<b>WD_EN</b>	0	rw	<b>Watchdog enable</b> Watchdog timer enable <b>b0: Watchdog timer is disabled</b> b1: Watchdog timer is enabled
<b>WD_INSEL</b>	3:1	rw	<b>Watchdog input selection</b> This bitfield selects the input to the watchdog timer among following options: <b>b000: EN_DRV pin (measure input signal frequency)</b> b001: Reserved b010: DVDD (linear regulator) b011: VCCLS and VCCHS, (charge pumps) b100: Status register read b101: Reserved b110: Reserved b111: Reserved
<b>WD_FLTCFG</b>	4	rw	<b>Watchdog fault configuration</b> This bitfield controls the reaction to a watchdog fault event: <b>b00: Status register only</b> b01: Status register and pull down of nFAULT pin
<b>WD_TIMER_T</b>	14:5	rw	<b>Watchdog timer period value</b> This bitfields configures the period of the watchdog timer. After this time is elapsed with no re-start of the timer by the watchdog input, a watchdog fault is triggered. In 100us steps. Not applicable for VDDB (buck) watchdog input. <b>b0000000000: 100 us</b> b0000000001: 200 us ..... b1111111111: 102.4ms
<b>0</b>	15	res	<b>Reserved</b> A read always returns 0

## Register Map

**Watchdog Configuration Register 2**

Watchdog configurations register extension.

**WD\_CFG2**

Address:

16<sub>H</sub>

Reset Value

0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			WD_BK_DIS		WD_RLOCK_T		WD_RLOCK_EN		WD_DVDD_RSTRT_DLY		WD_DVDD_RSTRT_ATT		WD_EN_LATCH		WD_BRAKE

res	rw														
-----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

Field	Bits	Type	Description
<b>WD_BRAKE</b>	0	rw	<b>Brake on watchdog timer overflow</b> This bitfields provides the option to configure a braking event when the watchdog overflow occurs <b>b0: Normal reaction to fault</b> b1: Brake on watchdog fault (Automatically latched). The braking mode is configured in PWM_CFG register. Status register is updated accordingly
<b>WD_EN_LATCH</b>	1	rw	<b>Enable latching of watchdog fault</b> Enable latching of watch dog fault <b>b0: Fault not latched</b> b1: Fault latched
<b>WD_DVDD_RSTRT_ATT</b>	3:2	rw	<b>Restart delay for DVDD</b> Number of restart attempts for DVDD WD <b>b00: 0 attempts</b> b01: 1 attempt b10: 2 attempts b11: 3 attempts
<b>WD_DVDD_RSTRT_DLY</b>	7:4	rw	<b>DVDD restart delay</b> Time after WD trigger signal until restart is attempted again for DVDD. In steps of 0.5ms <b>b0000: 0.5 ms</b> b0001: 1 ms ..... b1110: 7.5 ms b1111: 8 ms
<b>WD_RLOCK_EN</b>	8	rw	<b>Enable rotor locked detection</b> Enable rotor lock dedicated watchdog timer input <b>b0: Disabled</b> b1: Enabled

## Register Map

<b>WD_RLOCK_T</b>	11:9	rw	<b>Rotor locked watchdog timeout</b> Watchdog timer period value (overflow value). In steps of 1s <b>b000: 1 second</b> b001: 2 s ..... b111: 8 s
<b>WD_BK_DIS</b>	12	rw	<b>Buck watchdog disable</b> Buck watchdog (start-up) disable <b>b0: Buck watchdog enabled</b> b1: Buck watchdog disabled
<b>0</b>	15:13	res	<b>Reserved</b> A read always returns 0

## Gate Driver Current Control Register

Gate driver current settings for slew rate control.

IDRIVE_CFG	Address:	17 <sub>H</sub>
	Reset Value	BBBBH
15    14    13    12    11    10    9    8    7    6    5    4    3    2    1    0		
<b>ILS_SINK</b>	<b>ILS_SRC</b>	<b>IHS_SINK</b>
rw	rw	rw

Field	Bits	Type	Description
<b>IHS_SRC</b>	3:0	rw	<b>High-side source current</b> High side gate driver rise or pull-up gate current applied during period T <sub>DRIVE2</sub> b0000 - 10mA b0001 - 20mA b0010 - 30mA b0011 - 40mA b0100 - 50mA b0101 - 60mA b0110 - 80mA b0111 - 100mA b1000 - 125mA b1001 - 150mA b1010 - 175mA <b>b1011 - 200mA</b> b1100 - 250mA b1101 - 300mA b1110 - 400mA b1111 - 500mA

## Register Map

<b>IHS_SINK</b>	7:4	<b>rw</b>	<b>High-side sink current</b> High-side gate driver fall or pull-down gate current applied during period $T_{DRIVE4}$ Same coding as IHS_SRC
<b>ILS_SRC</b>	11:8	<b>rw</b>	<b>Low-side source current</b> Low side gate driver rise or pull-up gate current applied during period $T_{DRIVE2}$ Same coding as IHS_SRC
<b>ILS_SINK</b>	15:12	<b>rw</b>	<b>Low-side sink current</b> Low side gate driver fall or pull-down gate current applied during period $T_{DRIVE4}$ Same coding as IHS_SRC

## Gate Driver Pre-Charge Current Control Register

Low side gate driver control parameters

<b>IDRIVE_PRE_CFG</b>															Address:	$18_H$
															Reset Value	$00BB_H$
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0					<b>I_PRE_EN</b>	<b>I_PRE_SINK</b>					<b>I_PRE_SRC</b>					
res					<b>rw</b>	<b>rw</b>					<b>rw</b>					

Field	Bits	Type	Description
<b>I_PRE_SRC</b>	3:0	<b>rw</b>	<b>Pre-charge source current setting (<math>T_{DRIVE1}</math>)</b> Rise or pull-up gate current applied during pre-charge phase ( $T_{DRIVE1}$ ) b0000 - 10mA b0001 - 20mA b0010 - 30mA b0011 - 40mA b0100 - 50mA b0101 - 60mA b0110 - 80mA b0111 - 100mA b1000 - 125mA b1001 - 150mA b1010 - 175mA <b>b1011 - 200mA</b> b1100 - 250mA b1101 - 300mA b1110 - 400mA b1111 - 500mA

**Register Map**

<b>I_PRE_SINK</b>	7:4	rw	<b>Pre-charge sink current setting (<math>T_{DRIVE3}</math>)</b> Fall or pull-down current during pre-charge phase ( $T_{DRIVE3}$ ) Same coding as I_PRE_SRC
<b>I_PRE_EN</b>	8	rw	<b>Gate driver pre-charge mode enable</b> Enables extra pre-charge current configurations. In case of disabled, 1.5A are applied during $T_{drive1}$ and $T_{drive3}$ periods <b>b0: Pre-charge current enabled.</b> Values I_PRE_SINK and I_PRE_SRC are applied during $T_{DRIVE1}$ and $T_{DRIVE3}$ respectively <b>b1: Pre-charge mode disabled.</b> 1.5A applied during $T_{DRIVE1}$ and $T_{DRIVE3}$
<b>0</b>	15:9	res	<b>Reserved</b> A read always returns 0

## Register Map

**TDRIVE Source Control Register**

$T_{DRIVE1}$  and  $T_{DRIVE2}$  configuration registers for ate driver sourcing mode.

**TDRIVE\_SRC\_CFG**

																Address:	$19_H$
																Reset Value	$FF00_H$
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
TDRIVE2								TDRIVE1									
rw								rw									

Field	Bits	Type	Description
<b>TDRIVE1</b>	7:0	rw	<b>T<sub>DRIVE1</sub> timing</b> $T_{DRIVE1}$ value for high and low side. First turn on or pre-charge period <b>b00000000 - 0ns</b> b00000001 - 50ns (values between 0ns and 50ns not allowed) 10ns steps b11111111 - 2590ns
<b>TDRIVE2</b>	15:8	rw	<b>T<sub>DRIVE2</sub> timing</b> $T_{DRIVE2}$ value for high and low side. b00000000 - 0ns b00000001 - 10ns 10ns steps <b>b11111111 - 2550ns</b>

**TDRIVE Sink Control Register**

Tdrive3 and Tdrive4 configuration registers for ate driver sourcing mode.

**TDRIVE\_SINK\_CFG**

																Address:	$1A_H$
																Reset Value	$FF00_H$
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
TDRIVE4								TDRIVE3									
rw								rw									

Field	Bits	Type	Description
<b>TDRIVE3</b>	7:0	rw	<b>T<sub>DRIVE3</sub> timing</b> $T_{DRIVE3}$ value for high and low side. First turn off or pre-discharge period <b>b00000000 - 0ns</b> b00000001 - 50ns (values between 0ns and 50ns not allowed) 10ns steps b11111111 - 2590ns

## Register Map

<b>TDRIVE4</b>	15:8	rw	<b>T<sub>DRIVE4</sub>timing</b> T <sub>DRIVE4</sub> value for high and low side. b00000000 - 0ns b00000001 - 10ns 10ns steps <b>b11111111 - 2550ns</b>
----------------	------	----	---

**Dead Time Register**

Dead time configurations.

<b>DT_CFG</b>																Address:	1B <sub>H</sub>
																Reset Value	3131 <sub>H</sub>
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
<b>DT_FALL</b>										<b>DT_RISE</b>							
rw										rw							

Field	Bits	Type	Description
<b>DT_RISE</b>	7:0	rw	<b>Dead time rise (of phase node voltage)</b> Dead time rise (low to high) value b00000000: 120 ns b00000001: 200 ns In steps of 80ns ... <b>b00110001: 4040ns</b> ... b10010101: 12040 ns b10010110: b11111111: Unused (defaults to 120ns)
<b>DT_FALL</b>	15:8	rw	<b>Dead time fall (of phase node voltage)</b> Dead time fall (high to low) value b00000000: 120 ns b00000001: 200 ns In steps of 80ns ... <b>b00110001: 4040ns</b> ... b10010101: 12040 ns b10010110: b11111111: Unused (defaults to 120ns)

## Register Map

**Charge Pump Configuration Register**

Charge pump related controls.

**CP\_CFG**

Address:

1C<sub>H</sub>

Reset Value

0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0														<b>CP_CLK_SS_DIS</b>	<b>CP_CLK_CFG</b>
res														rw	rw

Field	Bits	Type	Description
<b>CP_CLK_CFG</b>	1:0	rw	<b>Charge pump clock frequency configuration</b> This bitfield configures the charge pump clock switching frequency. <b>b00: 781.25 kHz</b> b01: 390.625 kHz b10: 195.3125 kHz b11: 1.5625 MHz
<b>CP_CLK_SS_DIS</b>	2	rw	<b>Charge pump clock spread spectrum disable</b> <b>b0: Spread spectrum is enabled</b> b1: Spread spectrum disabled
<b>0</b>	15:3	res	<b>Reserved</b> A read always returns 0

## Current Sense Amplifier Configuration Register

Current sense amplifier configurations.

### CSAMP\_CFG

Address: 1D<sub>H</sub>

Reset Value 0028<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CS_OCPFLT_CFG</b>	<b>CS_OCP_DEGLITCH</b>	<b>CS_EN_DCCAL</b>		<b>CS_BLANK</b>					<b>CS_EN</b>	<b>CS_GAIN_ANA</b>		<b>CS_GAIN</b>			

rw

rw

rw

rw

rw

rw

rw

Field	Bits	Type	Description
<b>CS_GAIN</b>	2:0	rw	<b>Gain of current sense amplifiers</b> Selects gain of current sense amplifier when digitally programmed <b>b000: 4 V/V</b> b001: 8 V/V b010: 12 V/V b011: 16 V/V b100: 20 V/V b101: 24 V/V b110: 32 V/V b111: 64 V/V
<b>CS_GAIN_ANA</b>	3	rw	<b>CS Gain analogue programming enable</b> CS Gain analogue programming enable b0: Gain is selected via register configuration (CS_GAIN bitfield) <b>b1: Gain is defined by CS_GAIN pin resistor as per Table 15</b>
<b>CS_EN</b>	6:4	rw	<b>Enable of each current shunt amplifier</b> Enable of each current shunt amplifier bit 0: phase A <b>bit 1: phase B</b> bit 2: phase C b0: Amplifier disabled <b>b1: Amplifier enabled</b>

## Register Map

<b>CS_BLANK</b>	10:7	rw	<b>Current shunt amplifier blanking time</b> Current shunt amplifier blanking time <b>b0000: 0 ns</b> b0001: 50 ns b0010: 100 ns b0011: 200 ns b0100: 300 ns b0101: 400 ns b0110: 500 ns b0111: 600 ns b1000: 700 ns b1001: 800 ns b1010: 900 ns b1011: 1 us b1100: 2 us b1101: 4 us b1110: 6 us b1111: 8 us
<b>CS_EN_DCC_AL</b>	11	rw	<b>Enable DC Calibration of CS amplifier</b> DC calibration of CS amplifier <b>b0: No calibration is executed</b> b1: DC calibration mode executed: all power stages in high Z: powered but not driving
<b>CS_OCP_DE_GLITCH</b>	13:12	rw	<b>Current sense amplifier OCP deglitch</b> OCP deglitch timing configuration of the OCP on current sense amplifiers-deglitch disabled if CS_TRUNC_DIS = b1 (PWM truncation disabled in register CSAMP_CFG2) <b>b00: 0 µs</b> b01: 2 µs b10: 4 µs b11: 8 µs
<b>CS_OCPFLT_CFG</b>	15:14	rw	<b>Current sense amplifier OCP fault trigger configuration</b> OCP fault trigger configuration <b>b00: Count 8 OCP events</b> b01: Count 16 OCP events b10: Trigger on all OCP events b11: No fault trigger (PWM Truncation continues as defined in bitfield CS_TRUNC_DIS in register CSAMP_CFG2)

## Current Sense Amplifier Configuration Register 2

Current sense amplifier configurations extension register.

### CSAMP\_CFG2

Address: **1E<sub>H</sub>**

Reset Value **0833<sub>H</sub>**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS_AZ_CFG	CS_NEG_OCP_DIS	VREF_INSEL	CS_TRU_NC_DIS	CS_OCP_BRAKE	CS_MODE	CS_OCP_LATCH	CS_OCP_NTHR					CS_OCP_PTHR			

Field	Bits	Type	Description
<b>CS_OCP_PT HR</b>	3:0	rw	<p><b>Current sense amplifier OCP positive thresholds</b></p> <p>This bitfield configures the threshold level for the positive OCP</p> <p>4'b0000: 300mV          4'b0001: 250mV          4'b0010: 225mV  <b>4'b0011: 200mV</b>          4'b0100: 175mV          4'b0101: 150mV          4'b0110: 125mV          4'b0111: 100mV          4'b1000: 90mV          4'b1001: 80mV          4'b1010: 70mV          4'b1011: 60mV          4'b1100: 50mV          4'b1101: 40mV          4'b1110: 30mV          4'b1111: 20mV</p>

## Register Map

<b>CS_OCP_NT HR</b>	7:4	rw	<b>Current sense amplifier OCP negative thresholds</b> This bitfield configures the threshold level for the negative OCP <b>4'b0000: -300mV</b> 4'b0001: -250mV 4'b0010: -225mV <b>4'b0011: -200mV</b> 4'b0100: -175mV 4'b0101: -150mV 4'b0110: -125mV 4'b0111: -100mV 4'b1000: -90mV 4'b1001: -80mV 4'b1010: -70mV 4'b1011: -60mV 4'b1100: -50mV 4'b1101: -40mV 4'b1110: -30mV 4'b1111: -20mV
<b>CS_OCP_LA TCH</b>	8	rw	<b>OCP latch choice</b> OCP fault can be selected with this bitfield to be a latched: <b>b0: Unlatched</b> b1: Latched
<b>CS_MODE</b>	9	rw	<b>Current sense amplifier sensing mode</b> Select between shunt resistor and $R_{DSON}$ sensing modes <b>b0: Shunt resistor</b> b1: $R_{DSON}$ sensing-CS_TMODE forced to be GL ON only
<b>CS_OCP_BR AKE</b>	10	rw	<b>Current sense amplifier brake on OCP configuration</b> Brake on OCP <b>b0: No braking upon OCP fault.</b> b1: Brake on OCP fault (fault set to latched). The braking mode is configured in PWM_CFG register
<b>CS_TRUNC_ DIS</b>	11	rw	<b>PWM truncation disable</b> Disables the truncation of PWM when an OCP occurs. This does not affect fault triggering. b00: PWM truncation enabled <b>b01: PWM truncation disabled</b>
<b>VREF_INSEL</b>	12	rw	<b>VREF source selection</b> This bitfield controls whether the current sense amplifier buffer offset (reference) is generated internally or is applied externally through the device pin VREF <b>b0: Use internal</b> b1: Use external

**Register Map**

<b>CS_NEG_OC_P_DIS</b>	13	rw	<b>Current sense negative OCP disable</b> This bitfield disables the negative Over Current Protection in the current shunt amplifiers including both the PWM truncation and fault reporting <b>b0: Negative OCP fault is enabled</b> b1: Negative OCP fault is disabled
<b>CS_AZ_CFG</b>	15:14	rw	<b>Current sense Auto-Zero configuration</b> This bitfield configures the Auto-Zero feature <b>b00: Auto-Zero enabled with internal synchronization</b> b01: Auto-Zero disabled b10: Auto-Zero enabled with external synchronization b11: Auto-Zero enabled with external synchronization and charge pump clock gating

**OTP Program Register**

OTP program command and user ID.

																Address:	1F <sub>H</sub>
																Reset Value	0000 <sub>H</sub>
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0										USER_ID				OTP_PROG			
res										rw				w			

Field	Bits	Type	Description
<b>OTP_PROG</b>	0	w	<b>Program OTP</b> Setting this bitfield will start programming of OTP
<b>USER_ID</b>	4:1	rw	<b>User ID</b> Space for user to enter an ID into OTP for version control
<b>0</b>	15:5	res	<b>Reserved</b> A read always returns 0

## Application Description

# 9 Application Description

Following are application recommendation for 6EDL7141 best performance.

## 9.1 Recommended External Components

6EDL7141 requires some external components for proper operation. Recommended components and values are listed in Table 22.

**Table 22 Recommended external components**

Element	Pin1	Pin2	Recommended value	Rating	Notes
$C_{PVDD}$	PVDD	PGND	4.7µF	According to PVDD	
$C_{DVDD}$	DVDD	DGND	10µF + 0.1µF	16V	According to MCU or other ICs specs
$C_{VCCHS}$	VCCHS	PVDD	$1\mu F < C_{VCCHS} < 2.2\mu F$	25V if connected to PVDD or according to (PVDD+PVCC) if connected to PGND	Depending on VCCHS ripple and start-up requirements
$C_{VCCLS}$	VCCLS	PGND	$1\mu F < C_{VCCLS} < 4.7\mu F$	25V	Depending on VCCLS ripple and start-up requirements
$C_{CP1}$	CP1H	CP1L	$220nF < C < 1\mu F$	16V or 25V	0.47µF recommended
$C_{CP2}$	CP2H	CP2L	$220nF < C < 1\mu F$	According to PVDD	0.47µF recommended
$L_{BUCK}$	PH	VDBB	22µH	According to max expected peak current - (device limit $I_{BUCK\_PEAK\_LIM}$ )	500kHz configuration
			10µH		1MHz configuration
$C_{BUCK}$	VDBB	PGND	47 µF	16V	500kHz configuration
			47 µF		1MHz configuration
$R_{SENSE}$	VSENSE/nB RAKE	DGND	$R=3.3k\Omega \rightarrow DVDD=3.3V$ $R=10k\Omega \rightarrow DVDD=5.0V$ Diode for nBRAKE (see section 3.9.2)	-	Selects DVDD 3.3V or 5V respectively. Tolerance 5% or better
$R_{CS\_GAIN}$	CS_GAIN/AZ	DGND	See Table 15 for gain	-	1% tolerance is recommended
$R_{AZ}$	CS_GAIN/AZ	DVDD	1kΩ-10kΩ	-	Pull up to DVDD. Diode might be required (see section 3.9.3)
$R_{nFAULT}$	nFAULT	DVDD	1kΩ-10kΩ	-	

## 9.2 PCB Layout Recommendations

Layout is critical to ensure high quality signal and sensing. Different recommendations are provided in this section for best electrical and EMI results.

### Grounding and Supply

PGND is the ground used for the following sections in 6EDL7141:

- Buck converter

## Application Description

- Charge pumps
- Gate drivers for low and high side

DGND is used for:

- Digital logic,
- Current sense amplifiers
- DVDD

It is recommended to cover well components that refer to PGND with PGND solid planes and to cover DGND referred components with DGND solid plane. Also ensure that there is no overlap between PGND and DGND planes to avoid cross coupling.

However, PGND and DGND have to be connected to the same electrical potential and must be connected to each other in one place in the PCB. The location depends on many factors. Sometimes close to the negative (return) of the supply or battery can lead to best results.

Decoupling capacitors for supply pin (PVDD) should be as close as possible to the pin 15 (PVDD) and pin 17 (PGND). It can as well be helpful to use a small 0.1uF capacitor for high frequency glitches suppression.

Generally speaking shielding of signals like gate signals but also sensing signals is important to avoid coupling and noise injection from other noisy areas.

If battery is expected suddenly drop close to the UVLO level of PVDD, it is recommended to have large capacitors that can maintain the supply voltage during those transients. Eventually, a diode (e.g. Schottky) can be used in series with PVDD and before the decoupling capacitor. This can avoid that the PVDD decoupling capacitors discharge to the battery or other circuits when the battery transient crosses below the PVDD UVLO level of 6EDL7141.

Similarly, CE pin if derived from the battery voltage with voltage dividers, might be affected by these transients. It can be a good idea to use a small capacitor in CE pin to ensure noise is not switching off the device. Current consumption of CE pin is extremely low. If the only way to discharge the CE capacitor is through 6EDL7141, the device might stay on for long periods. It could be useful to design a discharge path in case this is a problem.

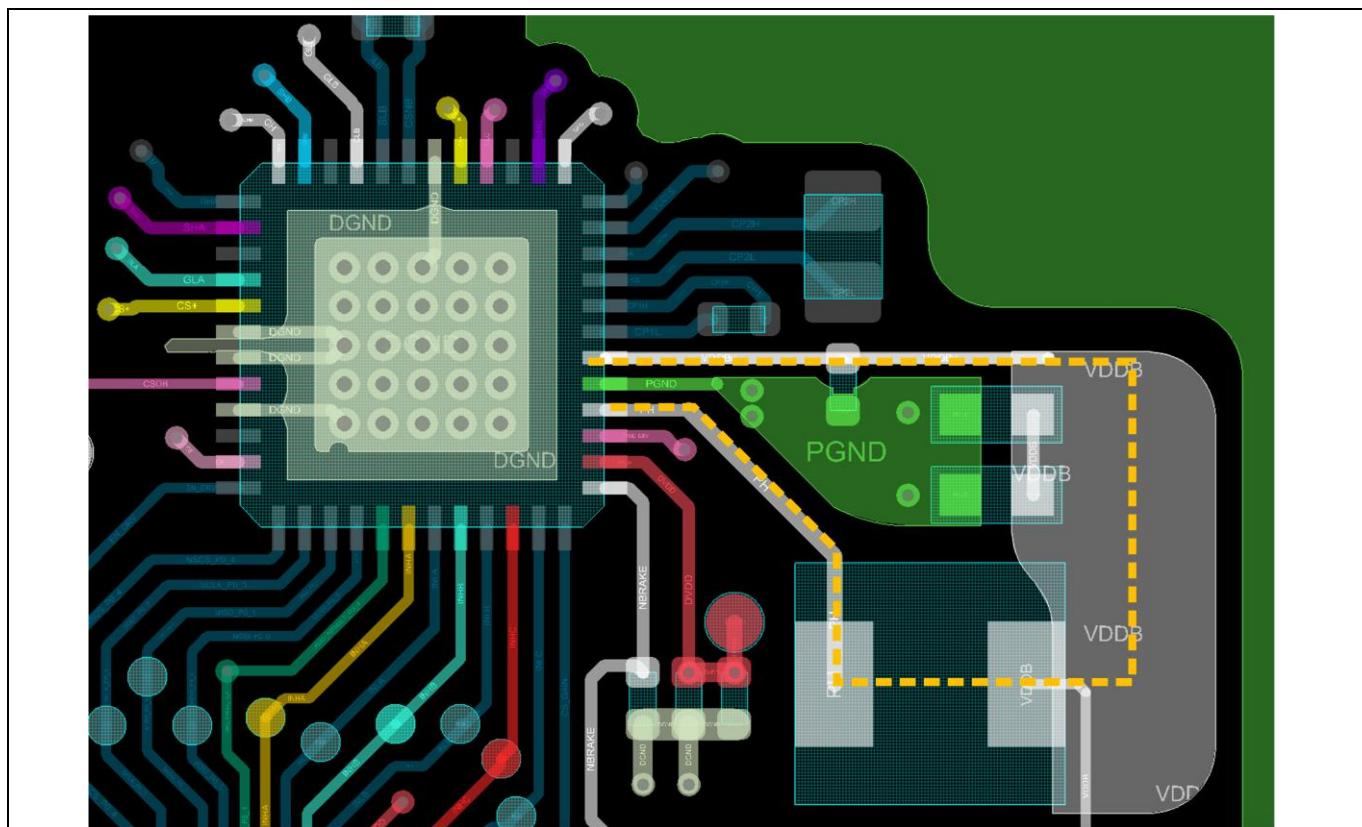
## Buck Converter and DVDD

The relatively high switching frequency and high voltage switching (PVDD to PGND) of the buck converter makes it a sensitive block in the device to pay extra attention during design phase.

Main goal is to reduce buck switching loop as much as possible ( $V_{PH}$ -Inductor-Capacitor-VDDDB). In 6EDL7141, most elements in the synchronous buck are integrated mitigating the EMI emissions, like external diode or low side MOSFET as well as the feedback or reference resistors.

Apart from the loop itself, it is very important to reduce in particular the  $V_{PH}$  traces to the shortest possible and avoid any large copper amount in the inductor connection. This node is switching PVDD voltage at high frequency and therefore can be a source of noise in other elements especially this trace must be as far as possible from sensitive analog sensing like current sensing.

Figure 59 shows a possible buck converter layout with minimized  $V_{PH}$  trace and buck loop area.

**Application Description**

**Figure 59 Buck converter layout recommendation.  $V_{PH}$  trace and buck loop area (highlighted) must be minimized**

DVDD linear regulator must be decoupled with capacitors placed as close as possible to the DVDD pin and connect as short as possible to DGND on the other terminal. MCU and other components supplied by DVDD voltage are recommended to use additional decoupling local capacitors at those components. This is helpful to suppress possible noise captured by the routing of those traces.

**Gate Driver and Charge Pumps**

Maintain as symmetric as possible gate signals including symmetry between phases (similar length for phase A, B and C) to avoid propagation delay mismatches. Keep as well gate current loops as short as possible and try to have as close as possible send and return signals.

The source signals of low side SLx, are shared between source of low side MOSFETs and top side sensing for shunt elements. It is recommended to optimize for the current sensing (symmetric tap of shunt terminal and parallel routing till current sense inputs), however, if current sense is not used, optimizing for gate driver performance is a good option.

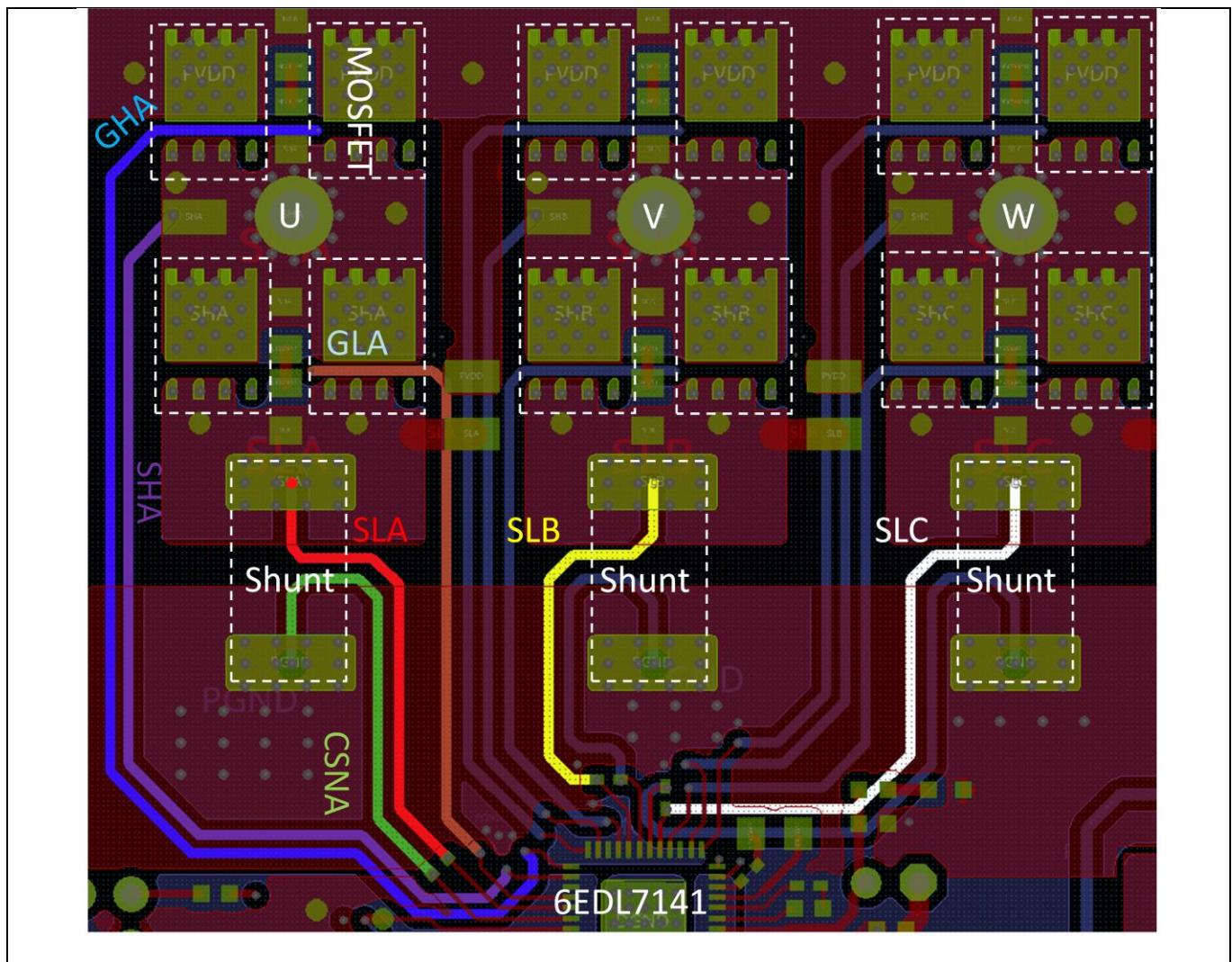
Charge pump loops should be as small as possible, the charge pump flying capacitors must be placed close to the pins 19, 20, 21, 22. Similar for the tank capacitors in VCCHS (pin 24) and VCCLS (pin 23). It is possible to place some of these capacitors in different layers as long as distance to the device is shortest possible.

Figure 60 shows an example of 6EDL7141 layout highlighting gate driver signals for high side and low side of phase A and the current sensing in a dual MOSFETs inverter.

Gate resistor can be used, however, user must know that the slew rate control of 6EDL7141 provides means to tune how fast MOSFETs switch in a programmable manner. Having  $R_g$  resistors will add additional voltage drop between 6EDL7141 and the gate of the MOSFET. Similarly, snubber elements (in parallel with MOSFETs) and

**Application Description**

bypass capacitors (high side drain to low side source) in the inverter can be used, nevertheless, the flexibility of the slew rate controller allows to remove those minimizing the BOM specially in a busy area of the layout, so more space can be used for the power section for example for better heat distribution in the PCB.



**Figure 60 Gate driver and current sensing layout example. Signals are routed in a middle layer.**

**Current Sensing**

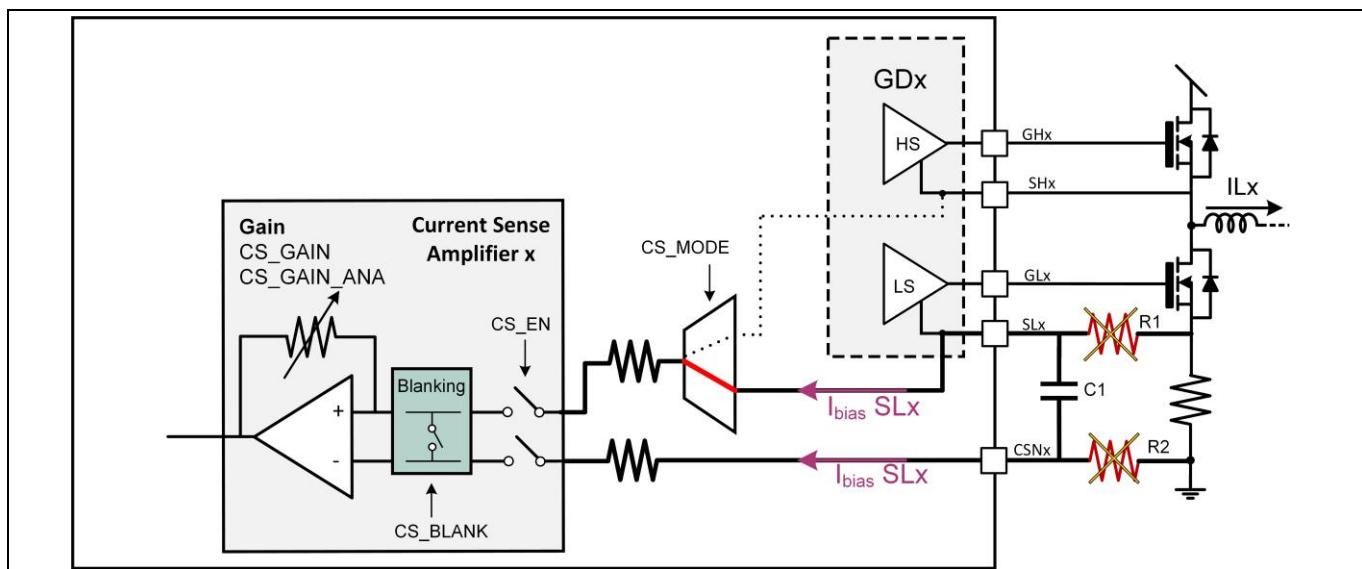
RC filter at SL<sub>x</sub> and CSN<sub>x</sub> must be done with care and is not preferred. R1 and R2 as shown in Figure 61, present voltage drop due to amplifier bias current and/or gate driver current, which affect the R<sub>shunt</sub> current sensing accuracy.

R1 limits the current of low-side (LS) gate driver and acts in fact as R<sub>g</sub>. A parallel capacitor (C1 as shown below) between SL<sub>x</sub> and CSN<sub>x</sub> can be used. This can increase switching noise during MOSFET switching, at the same time improve steady state value. Larger C values will accentuate this effect. Depending on application this value can be adjusted. The parallel capacitor should be close to the SL<sub>x</sub> and CSN<sub>x</sub> inputs pins on PCB and values between 100pF to 1nF can be a good starting point.

It is strongly recommended to use RC filter between current sense amplifier outputs (CSO<sub>x</sub>) and the ADC inputs in the MCU. Typical cut off frequency of 1MHz can be a good compromise between filtering capability and dynamic behavior, but user must decide depending on overall performance target.

**Application Description**

Kelvin connection of shunt resistor is highly recommended as shown in Figure 60. Traces of SLx (red) and CSNx (blue) are routed in a middle layer in this case and covered with solid ground planes.



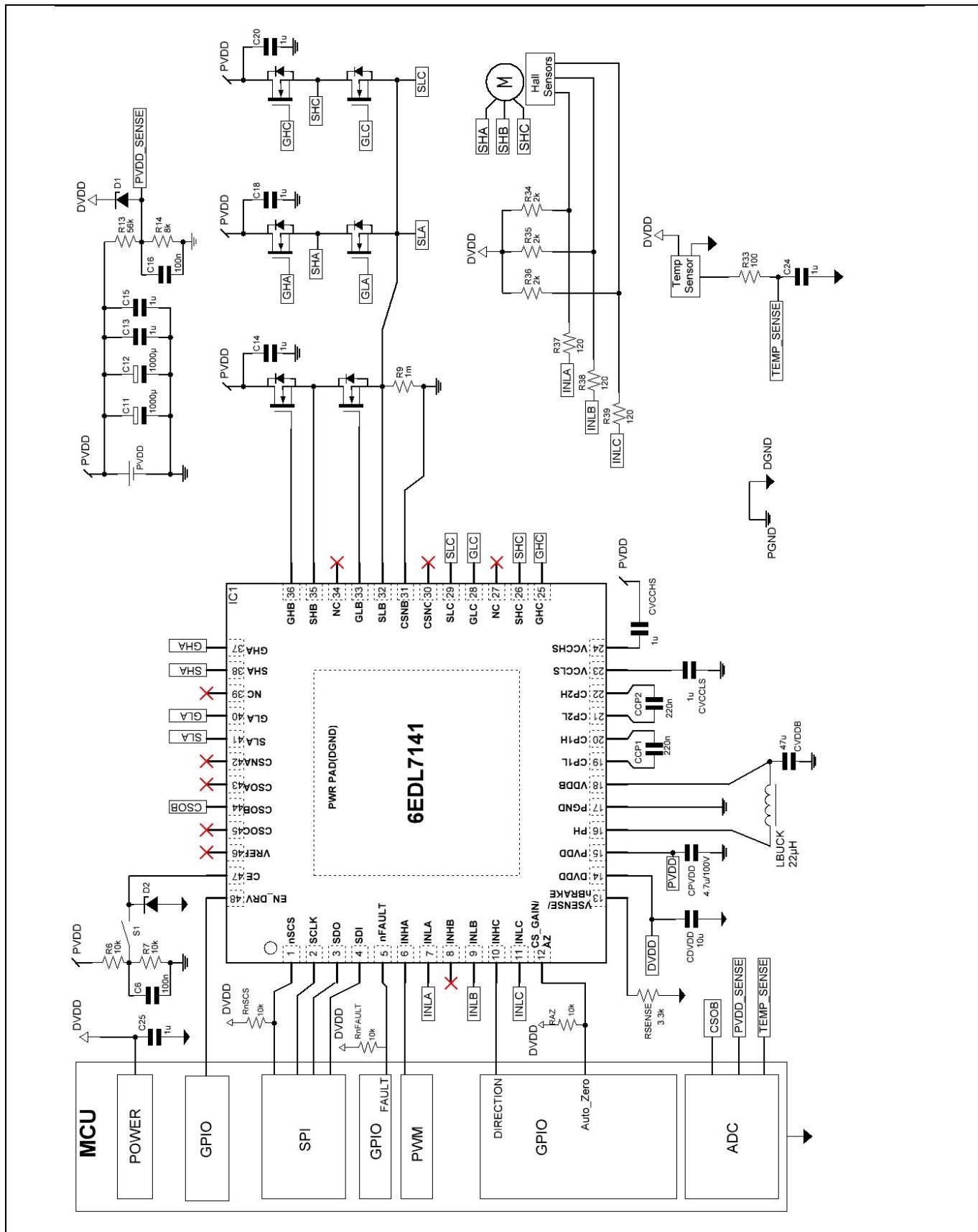
**Figure 61 Current sense amplifier input filtering**

### 9.3 Typical Applications

Hall sensors can directly be connected to 6EDL7141 inputs INLA, INLB and INLC. An example configuration of this solution is presented in Figure 62. In this case, 6EDL7141 is configured as 1PWM mode implementing trapezoidal control. A signal “Direction” is generated by MCU GPIO to change the motor turning direction. SPI interface allows the programming of 6EDL7141. DVDD MCU supply voltage is set to 3.3V by using  $R_{SENSE}$  resistor.

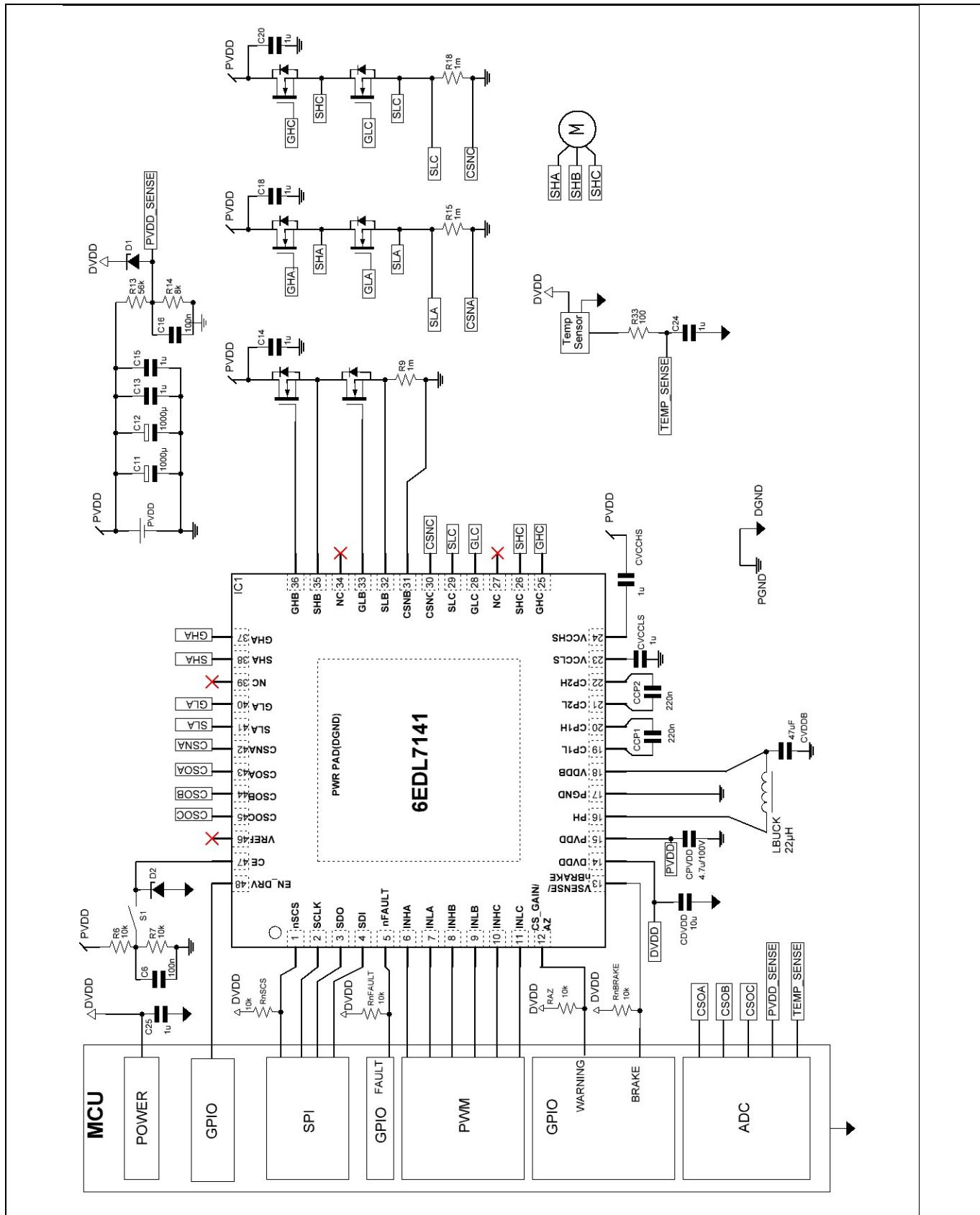
Figure 63 shows an alternative application. In this case the schematic implements a typical sensorless control method for BLDC motors. DVDD is programmed via OTP configuration (SPI register) and can be configured to either 3.3V or 5V. 6PWM mode is used in this version. All 3 integrated current sense amplifiers are used to amplify the current flowing through current shunts. Current sense amplifier outputs are connected to the microcontroller for proper control of the motor. Pin nBRAKE allows the MCU to brake the motor by pulling down that pin when necessary. The pin nFAULT signal reports to the MCU any malfunction occurring in 6EDL7141.

## Application Description



**Figure 62 Example schematic for trapezoidal control of BLDC motors using 1PWM mode with Hall sensors and a single shunt current measurement. Voltage dividers and capacitors voltage rating must be calculated for the specific target PVDD voltage**

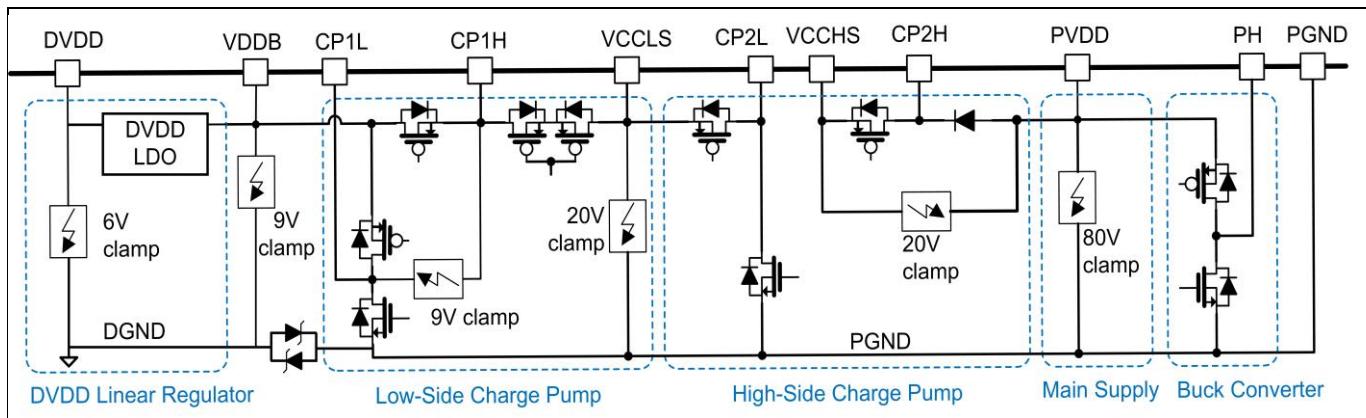
## Application Description



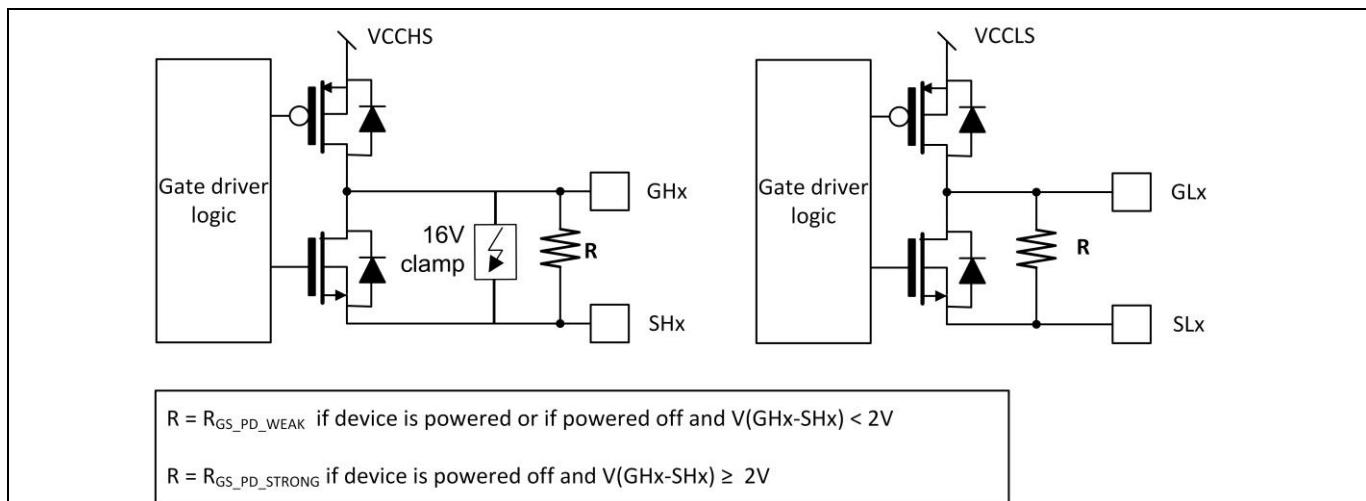
**Figure 63 Example schematic for sensorless control of BLDC motors using 6PWM mode a 3 shunts for current measurement. Voltage dividers and capacitors voltage rating must be calculated for the specific target PVDD voltage**

## 10 ESD Protection

Following diagrams show ESD protections and pin internal diagrams for different pins in 6EDL7141.



**Figure 64 ESD protection diagram for power supply related pins**



**Figure 65 Pin diagram for gate driver output pins**

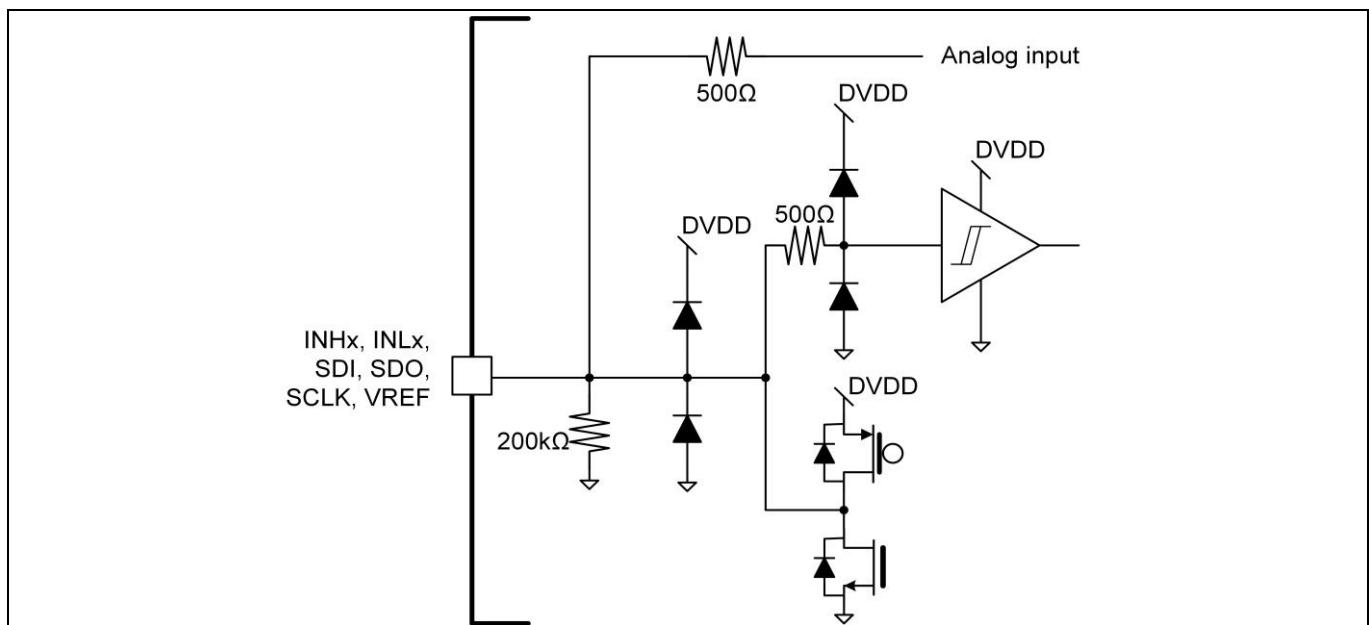


Figure 66 ESD protection and pin diagram for digital pins active high

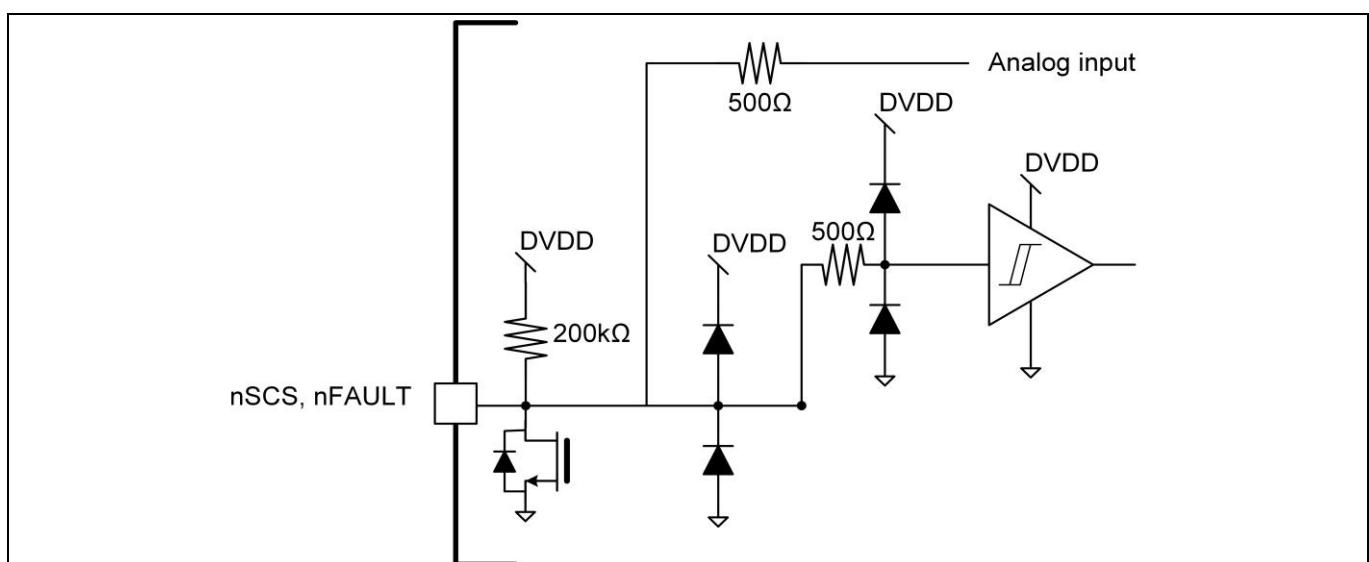


Figure 67 ESD protection and pin diagram for digital pins active low

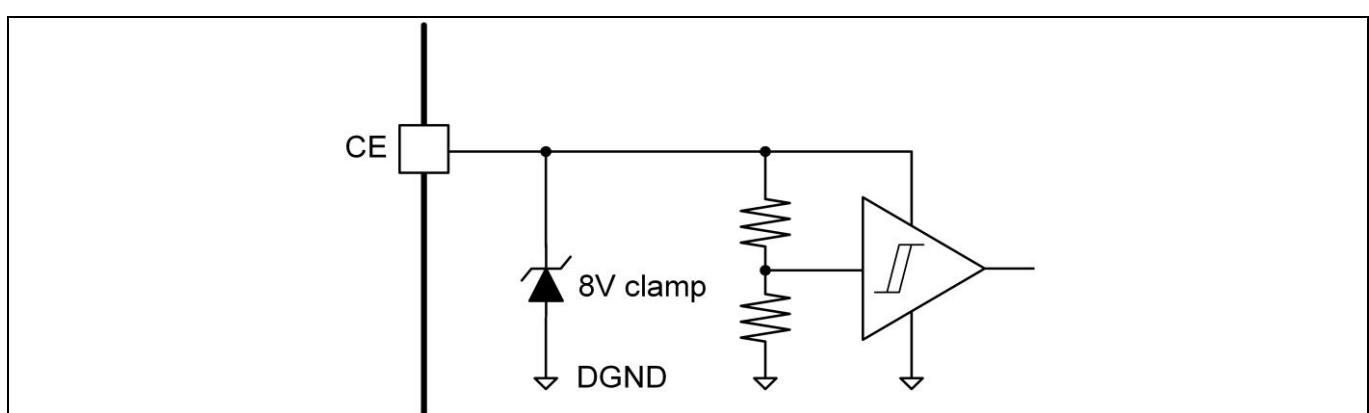


Figure 68 ESD protection and pin diagram for CE pin

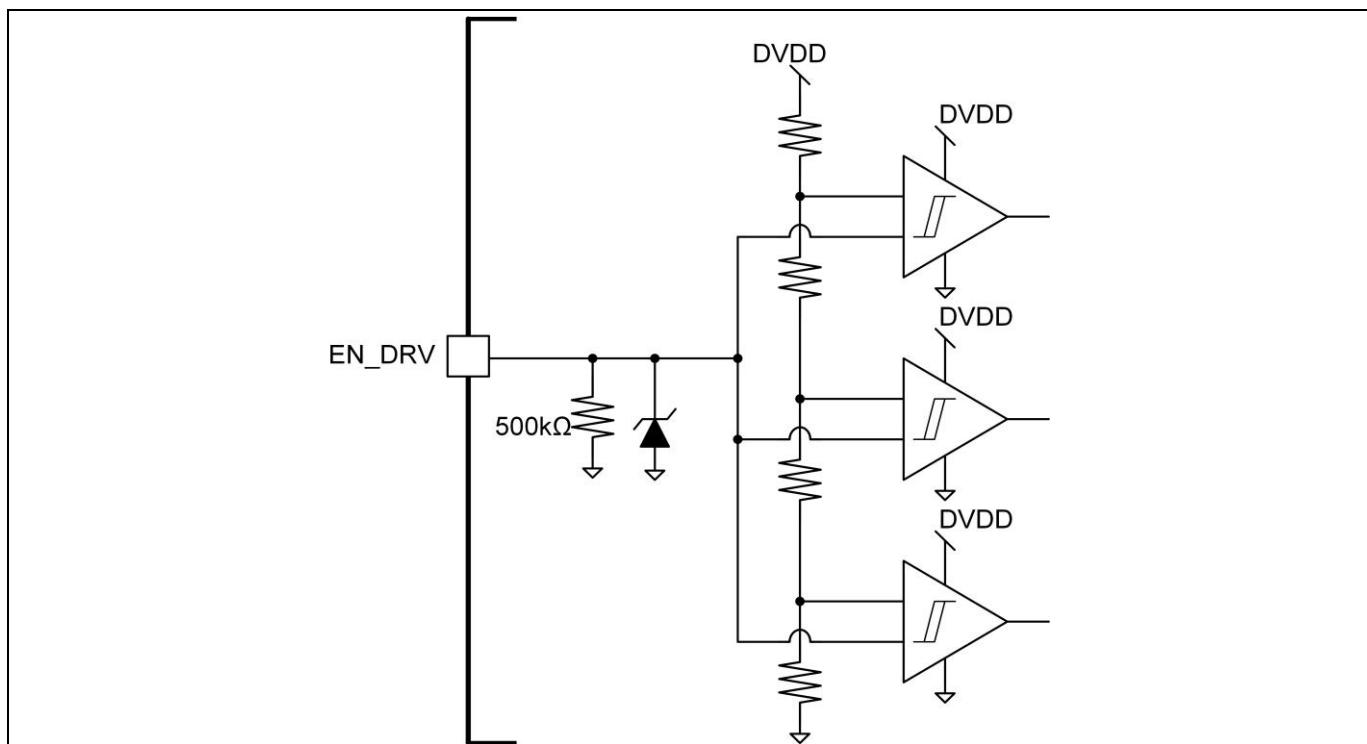


Figure 69 ESD protection and pin diagram for EN\_DRV pin

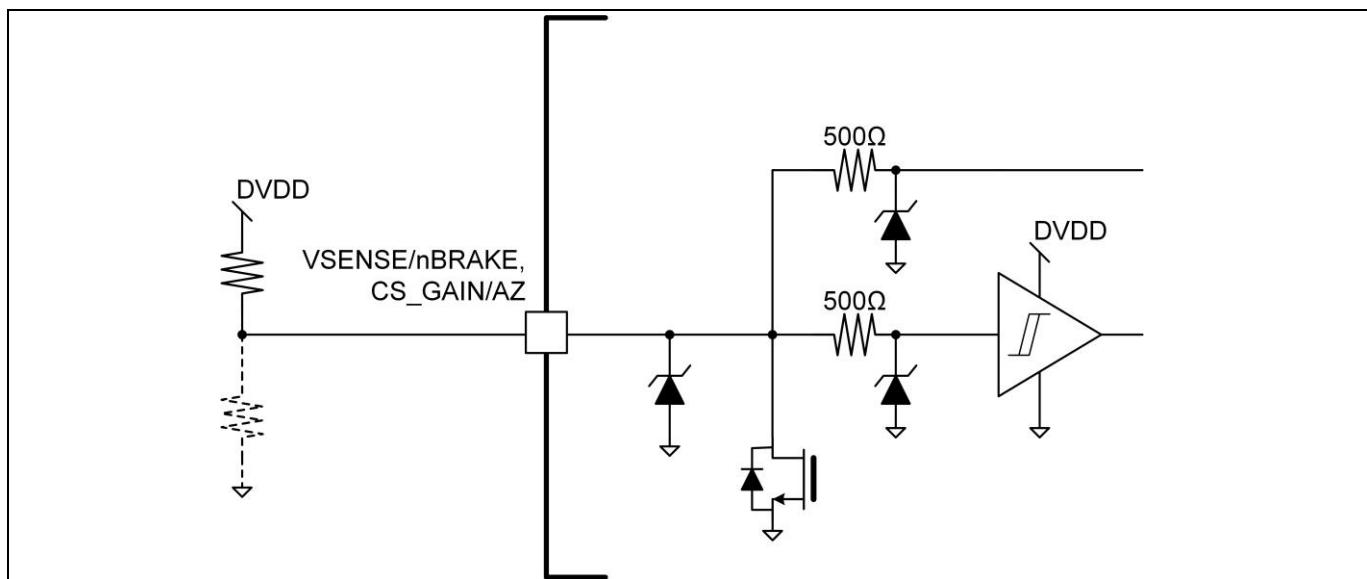


Figure 70 ESD protection and pin diagram for VSENSE/nBRAKE and CS\_GAIN/AZ pins

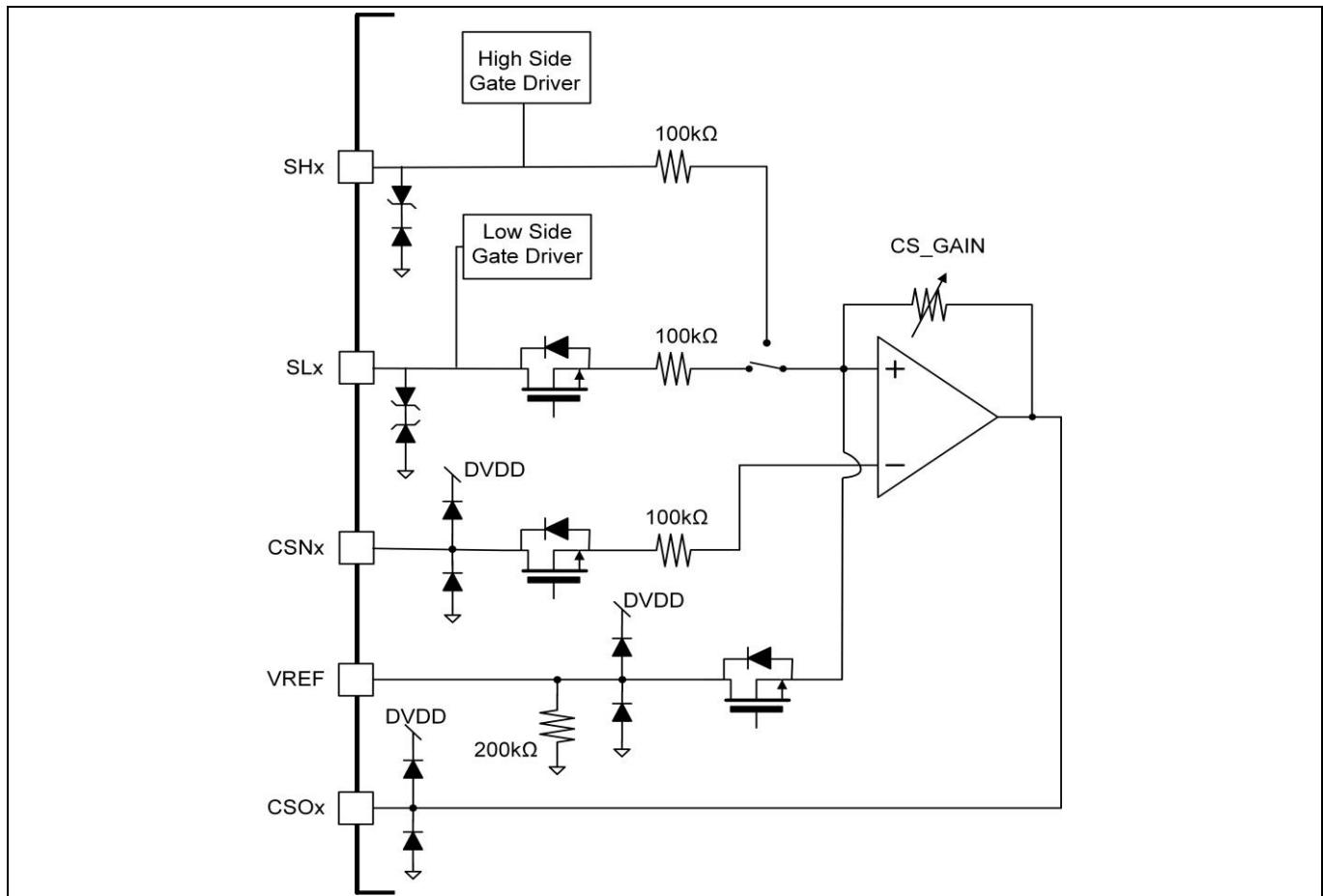


Figure 71 ESD protection and pin diagram for current sense amplifier related pins

## 11 Package Information

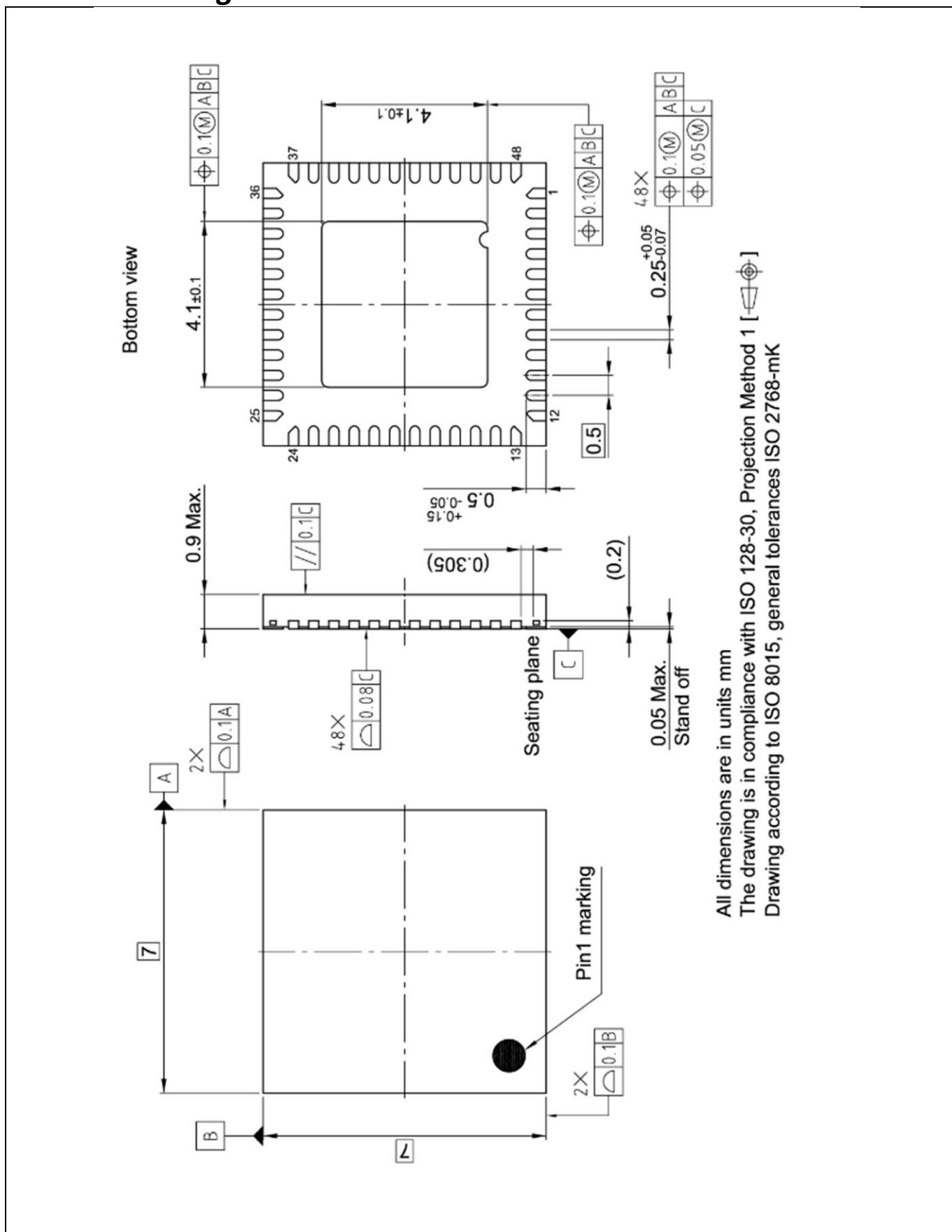


Figure 72 PG-VQFN-48-78 package outline

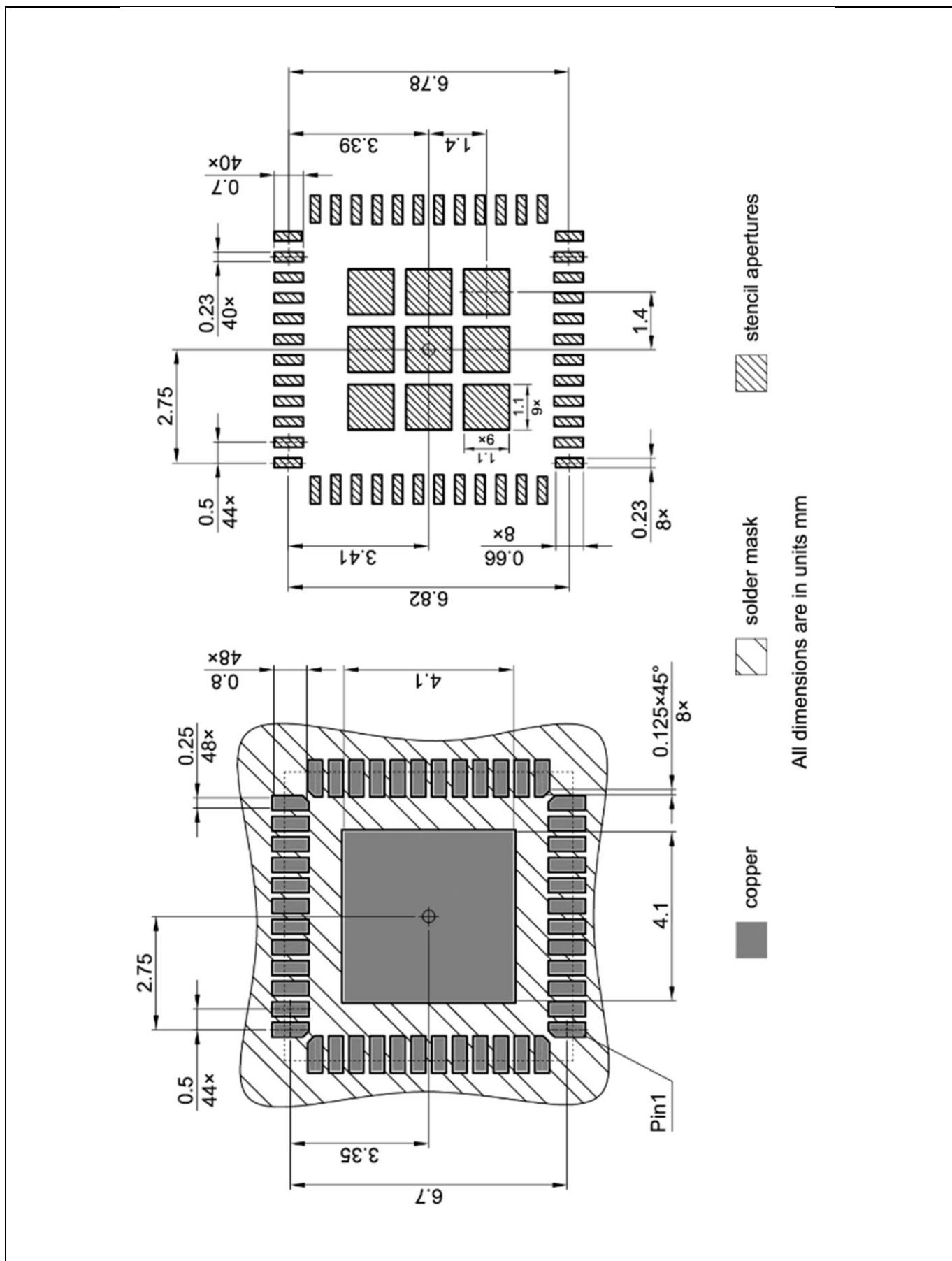


Figure 73 PG-VQFN-48-78 PCB footprint dimensions

**Revision history****Revision history**

<b>Page or Reference</b>	<b>Description of change</b>
v1.00	First public version
v1.02	<p>Datasheet update</p> <ul style="list-style-type: none"> <li>• Editorial changes including Absolute Maximum Ratings table notes.</li> <li>• Simplified ESD diagram for nFAULT, nSCS pins.</li> <li>• Minor editorial changes in Product Features section.</li> <li>• New graphs added in Electrical Characteristic Graphs section. Added additional test conditions.</li> <li>• Improvements in Figure 18, Figure 27, Figure 28, Figure 29 and Figure 37.</li> <li>• Correction in description of Standby type of register programmability in section 8.1: EN_DRV level low condition versus edge.</li> <li>• Added Figure 73 (package footprint dimensions figure)</li> <li>• Changes in Electrical Characteristics table <ul style="list-style-type: none"> <li>◦ PVDD active, standby and OFF consumption</li> <li>◦ <math>t_{CP\_START}</math> added new value on PVDD &lt; 10V</li> <li>◦ Test coverage correction in <math>t_{PROP\_MATCH\_CH}</math>, <math>t_{DT\_MATCH\_CH}</math> and <math>V_{GS\_CPM\_TH}</math></li> <li>◦ <math>\Delta VDDB_{LOAD}</math> correction</li> <li>◦ <math>V_{CS\_REF\_ACC}</math> improved to 1.5%</li> </ul> </li> </ul>
v1.04	<p>Datasheet update</p> <ul style="list-style-type: none"> <li>• ESD diagram modification – VDDB PMOS was inverse.</li> <li>• Added details in Figure 41 and improved description of this figure</li> <li>• Figure 46 corrected.</li> <li>• CVDDB value updated in Figure 62 and Figure 63</li> <li>• Absolute Maximum Ratings table: <ul style="list-style-type: none"> <li>◦ Added more details on CPxy pins</li> <li>◦ Modified '<math>V_{CP1H} - V_{CP1L}</math>' and '<math>V_{CP2H} - V_{CP2L}</math>'.</li> <li>◦ Increased max value for VCCHS.</li> </ul> </li> </ul>

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