EE114b Final Project

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***Abstract*—In this paper, we present the design and analysis of a broadband differential-output transimpedance amplifier (TIA) based on the 65nm CMOS technology for optical communication applications. The amplifier accepts a single-ended current input and provides a differential voltage output driving two 50Ω transmission lines, dc-isolated with two large capacitors. The design achieves a transimpedance gain of 77.84 dB and a 3dB bandwidth of 10.09 GHz.**

I. Specifications

Our transimpedance amplifier achieved the following specifications:

- DC power dissipation: **20.18 mW**
  This is less than half of the requirement of <50 mW
- Transimpedance: **77.84 dB** (≈ 7.798 kΩ)
  This is more than 1.5x the requirement of >5 kΩ
- Bandwidth: **10.09 GHz**
  This is more than twice the requirement of >5 GHz
- AC gain peaking: **0 dB**
  This is less than the requirement of <1 dB
- Differential output swing: **420.4 mV**
  This is more than 4x the requirement of >100 mV
- Differential output slew rate: **6.12 V/ns**
  This is more than 6x the requirement of >1 V/ns
- Input referred current noise for 1 GHz< f <3 GHz: **<16.32 pA/$\sqrt{\text{Hz}}$**
  This is less than the requirement of < 25 pA/$\sqrt{\text{Hz}}$
- Total extra capacitance: **1.1 pF**
  This is less than the requirement <50 pF
- Total extra inductance: **27.2 nH**
  This is less than the requirement of <30 nH
- Inductor series resistance: **3 Ω/nH**

II. Circuit Schematic

The circuit schematic of our transimpedance amplifier is shown in Fig. 1. It consists of a regulated cascode (RGC) input stage, two common-source (CS) stages (one is cascoded and the other with a capacitive source degeneration), a differential pair, and source follower buffers for each of the differential outputs.

III. Analysis

A. RGC Stage

The RGC stage allows for a low input impedance, reducing the effect of the dominant pole created by the photodiode's capacitance. With this stage isolated and inductorless, the low frequency input impedance is given by

$$Z_{in}(0) \approx R_3 \parallel \frac{1}{g_{m1}(1+g_{m2}R_2)} \approx 12\ \Omega \tag{1}$$

Furthermore, the small signal gain of this stage is

$$A_v \approx R_1 \frac{g_{m1}R_3(1+g_{m2}R_2)}{g_{m1}R_3(1+g_{m2}R_2)+1} \approx 575\ \Omega \tag{2}$$

which is close to the simulated gain of approximately 530 Ω. The time constants in this stage are

$$\tau_{PD} = (C_{PD}+C_{gs2})\left(R_3 \parallel \frac{1}{g_{m1}(1+g_{m2}R_2)}\right) \approx 6.37\text{ ps} \tag{3}$$

$$\tau_{gs1} = C_{gs1}\left(R_2 - R_3(1+g_{m2}R_2)\frac{g_{m2}R_2-1}{1+g_{m1}R_3(1+g_{m2}R_3)}\right) \approx 2.1\text{ ps} \tag{4}$$

$$\tau_{gd1} = C_{gd1}\left(R_1 + R_2\frac{1+g_{m1}(R_1+R_2)}{1+g_{m1}R_3(1+g_{m2}R_2)}\right) \approx 9.24\text{ ps} \tag{5}$$

$$\tau_{gd2} = C_{gd2}\left(R_2 + R_3(1+g_{m2}R2)\frac{R_1+R_2}{R_1-g_{m1}R_2R_3}\right) \approx 4.7\text{ ps} \tag{6}$$

Hence, combining these time constants gives an estimated bandwidth

$$f_{3dB,RGC} \approx \frac{1}{2\pi\sum_i \tau_i} \approx 7.1\text{ GHz} \tag{7}$$

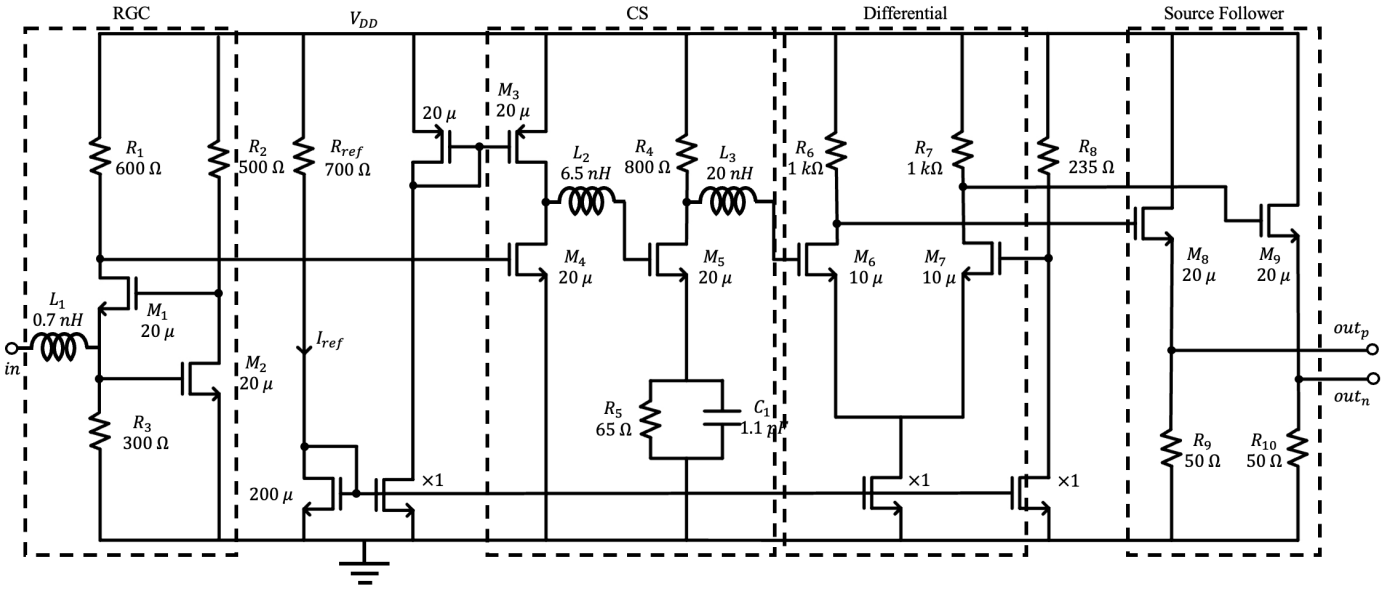

Fig. 1. The circuit schematic of the transimpedance amplifier. The input port is labeled *in*, and the differential output ports are labeled out_p and out_n. The power supply is labeled $V_{DD} = 1.1$ V.

with the simulated measurement to be $\approx$ 6.3 GHz. With the addition of a capacitive load created by the input of the CS stage, the bandwidth is further reduced as seen in Fig. 2. With the addition of an inductor at the input, a complex pole is created with a peaking frequency of

$$f_{peak} = \frac{1}{2\pi\sqrt{L_1(C_{PD} + C_{gs2})}} \approx 8.4 \text{ GHz} \tag{8}$$

Hence, inductive peaking here is utilized to enhance the bandwidth at higher frequencies.

B. CS Stages

The low-frequency gain of the first CS cascode stage can be calculated as

$$A_{CS1} = g_{m4}(r_{o4}||r_{o3}) = 4.33 \text{ V/V}, \tag{9}$$

which is in good agreement with the simulation (section V, Fig. 2 and 3). The time constants can be calculated to be

$$\tau_{gs4} \approx C_{gs4}R_1 = 11.02 \text{ ps} \tag{10}$$

$$\tau_{gd4} \approx C_{gd4}(R_1 + r_{o3}) = 9.09 \text{ ps} \tag{11}$$

The bandwidth of this stage alone is then

$$f_{3dB,CS1} =\approx \frac{1}{2\pi\sum_i \tau_i} = 7.91 \text{ GHz}. \tag{12}$$

For the second CS stage, with a capacitive source degeneration, the low-frequency gain is given by

$$A_{CS2} \approx g_{m5}(\frac{R_4}{1 + g_{m5}R_5}||r_{o5}) = 3.05 \text{ V/V}. \tag{13}$$

The time constants of this stage are

$$\tau_{gs5} = C_{gs5}(R_5 + (r_{o3}||r_{o4})) = 3.37 \text{ ps} \tag{14}$$

$$\tau_{gd5} = C_{gd5}(R_4 + (r_{o3}||r_{o4})) = 8.79 \text{ ps} \tag{15}$$

$$\tau_{C_1} \approx C_1\frac{R_5}{1 + g_{m5}R_5} = 42.5 \text{ ps} \tag{16}$$

The bandwidth of this stage alone is then

$$f_{3dB,CS2} \approx \frac{1}{2\pi\sum_i \tau_i} = 3.23 \text{ GHz}. \tag{17}$$

The source degeneration was added to introduce a zero at

$$z_1 = \frac{1}{2\pi R_5 C_1} \approx 2.2 \text{ GHz} \tag{18}$$

Due to the capacitive loading and the first CS stage, the bandwidth was collectively reduced to 2.3 GHz (without inductors) as seen in Fig. 4. Hence, this zero is added to enhance the bandwidth in addition to the inductors.

C. Differential Pair

With the NMOS on both sides being biased equally ($g_{m6} \simeq g_{m7}, r_{o6} \simeq r_{o7}$, and $R_6 = R_7$), the low-frequency differential gain can be calculated to be

$$A_{diff} = g_{m6}(R_6||r_{o6}) \simeq 3.41. \tag{19}$$

This agrees with the simulation results (see section V, Fig. 5 and 6). The time constants are associated with the parasitic capacitances of M_6 and M_7, which can be calculated as follows:

$$\tau_{gs6} \approx C_{gs6}(R_4||r_{o5}) = 2.66 \text{ ps} \tag{20}$$

$$\tau_{gd6} = C_{gd6}((R_4||r_{o5}) + (R_6||r_{o6}) + g_{m6}(R_6||r_{o6})(R_4||r_{o5})) = 12.2 \text{ ps} \tag{21}$$

$$\tau_{gs7} \simeq C_{gs7}R_8 = 1.60 \text{ ps} \tag{22}$$

$$\tau_{gd7} \simeq C_{gd7}(R_7 + R_8 + g_{m7}R_7R_8) = 9.85 \text{ ps} \quad (23)$$

The bandwidth of this stage alone is then estimated to be

$$f_{3dB,diff} \approx \frac{1}{2\pi \sum_i \tau_i} = 6.07 \text{ GHz}. \quad (24)$$

This bandwidth is extended by an inductor added to the input, which effectively pushes the poles introduced by the parasitic capacitances to higher frequencies.

D. Source Follower Buffers

These stages act as buffers with a low-frequency gain given by ($g_{m8} = g_{m9}, r_{o8} = r_{o9}$, and $R_9 = R_{10}$)

$$A_{buffer} = \frac{g_{m8}(R_9||R_L||r_{o8})}{1 + g_{m8}(R_9||R_L||r_{o8})} = 0.38, \quad (25)$$

which again agrees with the simulation results (section V, Fig. 6 and 7). The time constants associated with these stages can be calculated as follows:

$$\tau_{gd8} = \tau_{gd9} = C_{gd8}(R_6||r_{o6}) = 3.23 \text{ ps} \quad (26)$$

$$\tau_{gs8} = \tau_{gs9} = C_{gs8}\frac{(R_9||R_L) + (R_6||r_{o6})}{1 + g_{m8}(R_9||R_L)} = 6.98 \text{ ps} \quad (27)$$

The estimated bandwidth of this buffer alone is

$$f_{3dB,buffer} \approx \frac{1}{2\pi \sum_i \tau_i} = 15.6 \text{ GHz}. \quad (28)$$

This is much larger than the bandwidth of the previous stages, so it would not have much effect on the bandwidth limit.

E. Noise Analysis

Since the first stage has a high gain ($\approx 500\,\Omega$), the dominant input-referred noise comes from the first stage. The input-referred noise was calculated as:

$$\overline{i^2_{n,\text{in}}} = 4kT\Bigg[\frac{1}{R_1} + \frac{R_2}{|A_v|^2R_1^2} + \frac{1}{R_3R_1^2\big(g_{m2} + 1/R_3\big)^2} \quad (29)$$

$$+\frac{\gamma g_{m2}}{R_1^2\big(g_{m2} + 1/R_3\big)^2} + \frac{\gamma g_{m1}R_2^2}{|A_v|^2R_1^2\big(1 + g_{m1}R_3\big)^2}\Bigg] \quad (30)$$

which yields an input referred noise of 5.8 pA$/\sqrt{Hz}$.

IV. Design Considerations

A. Input Stage

Due to the high capacitance of the diode at the input, the RGC stage is chosen due to its extremely low input impedance resulted from the feedback loop. This isolates the diode capacitance from bandwidth determination. This stage also provides a high transimpedance gain, making the noise from this stage the dominant input-referred noise source. The input inductor was added to form an LC ladder network, allowing for inductive peaking to occur to shift the bandwidth.

B. Intermediate Stages

The first CS cascode stage operates at a larger bias current, providing high gain. The cascode is used to alleviate the limit on the available headroom for a large current. The second CS stage provides slightly lower gain and has a lower output impedance, which reduces the time constants of the parasitic capacitances of the differential pair and makes the input resistance seen by M_6 closer to that seen by M_7, leading to a more balanced differential stage. A zero is added on top of a pole to extend the bandwidth. Furthermore, a larger inductor is placed after each CS stage to form a LC ladder that will provide inductive peaking at varying frequencies to further extend the bandwidth. Finally, the differential pair uses just normal resistors with low bias current due to limited headroom, and the transistors' widths are smaller than the other stages to maximize the output resistance and thus gain and also minimize the parasitic capacitances.

C. Output Buffer

Since the gain from the previous stages is already high enough, the source follower stage is chosen as a buffer to simplify the biasing. The small source resistance increases the bias current and the transconductance of the transistors, improving the gain, and decreases the output impedance, while the minimum source resistance is limited by the load resistance of 50 Ω. The NMOS transistors are used for this stage because of the high DC input voltage ($\approx 0.6 - 0.7$ V) from the differential pair output.

D. Current Sources

Due to limited headroom, since the parasitic capacitances of the transistors used as current sources do not affect the performance of the amplifier, a large width of 200 μm is selected to minimize the gate voltage of these transistors. A reference of ≈ 1 mA is chosen for a reasonable transistor's cutoff frequency.

V. Simulation Results

The simulation results for the output frequency response of each stage (including the preceding stages), the transient response of the final differential output for determination of output voltage swing and slew rate, and the input-referred current noise are shown in Fig. 2 - 10. Table I shows the small signal parameters of the transistors at the designed DC operating point.

Acknowledgment

We would like to thank Professor Ali Hajimiri for generously sharing his knowledge and expertise, which greatly enriched this project. We also appreciate the help and support from the TAs throughout the course. This project would not have been possible without their guidance and assistance.

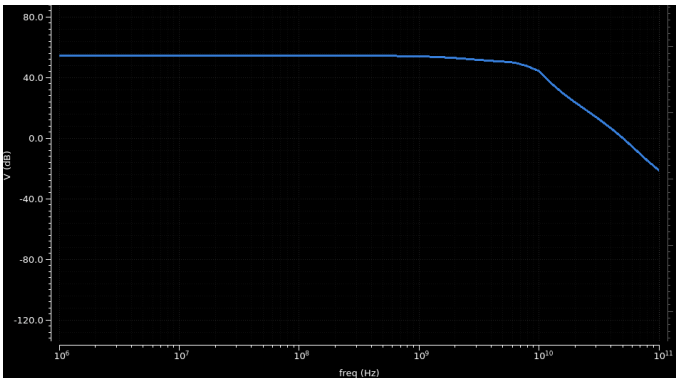

Fig. 2. The simulated frequency response at the output of the first (RGC) stage. The gain is 54.48 dB (530 Ω), and the bandwidth is 3.57 GHz.

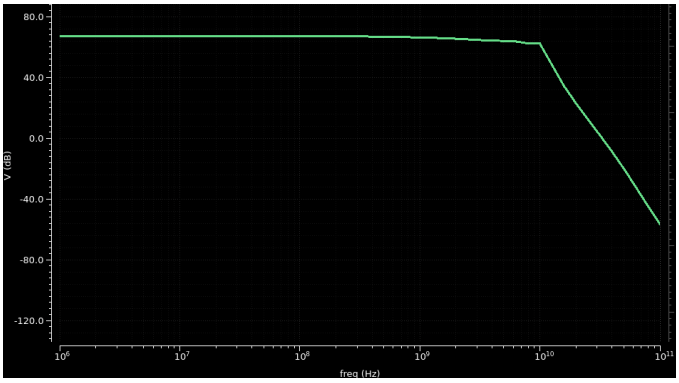

Fig. 3. The simulated frequency response at the output of the common-source cascode (the first CS) stage. The total gain is 67.20 dB (2.29 kΩ), and the bandwidth is 3.98 GHz.

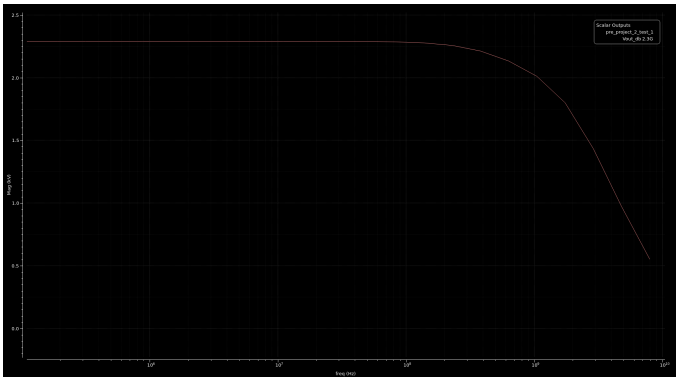

Fig. 4. The simulated frequency response at the output of the common-source cascode (the first CS) stage omitting inductors. The total gain is 67.20 dB (2.29 kΩ), and the bandwidth is 2.3 GHz.

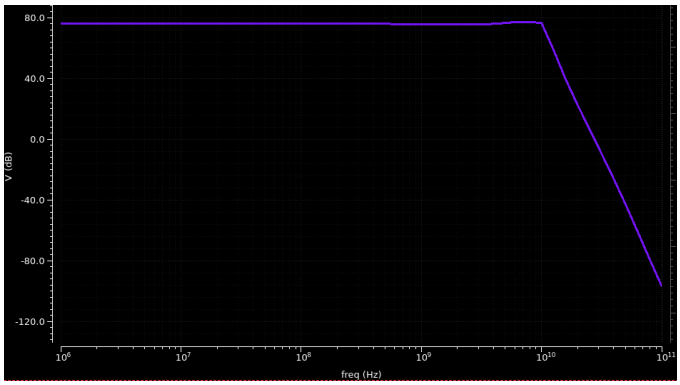

Fig. 5. The simulated frequency response at the output of the second common-source stage. The total gain is 76.19 dB (6.45 kΩ), and the bandwidth is 10.45 GHz.

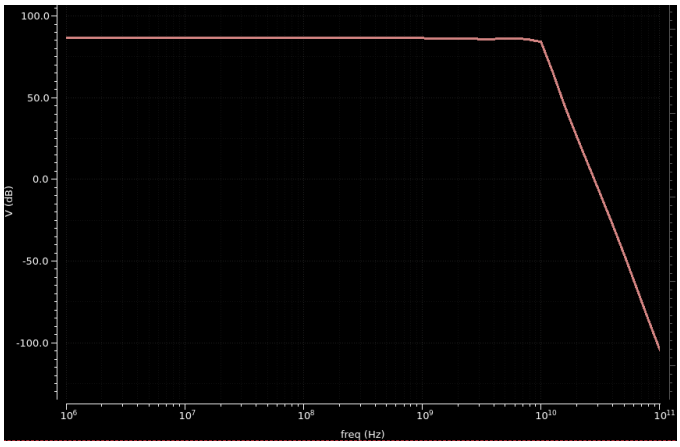

Fig. 6. The simulated frequency response of the differential output of the differential pair. The total gain is 86.84 dB (21.98 kΩ), and the bandwidth is 10.10 GHz.

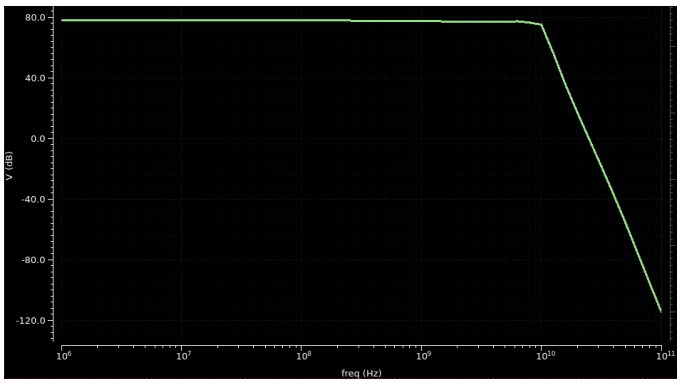

Fig. 7. The simulated frequency response of the differential output after the source follower buffers, each connected to a 1μF capacitor and a 50Ω load. The total gain is 77.84 dB (7.80 kΩ), and the bandwidth is 10.09 GHz.

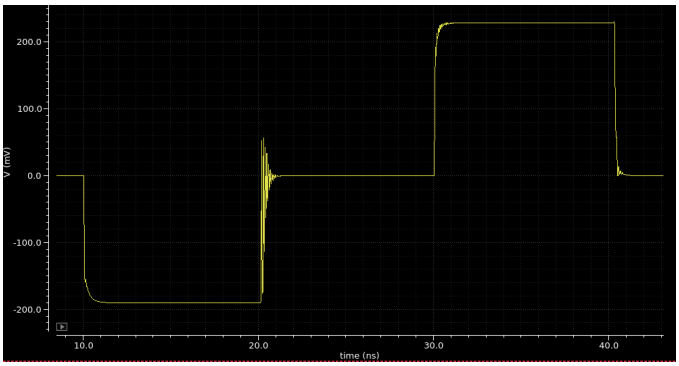

Fig. 8. The simulated response of the amplifier when the input current is two rectangular pulses, one with positive amplitude and one with negative amplitude of 1 mA. From this, the differential output swing is determined to be 420.4 mV.

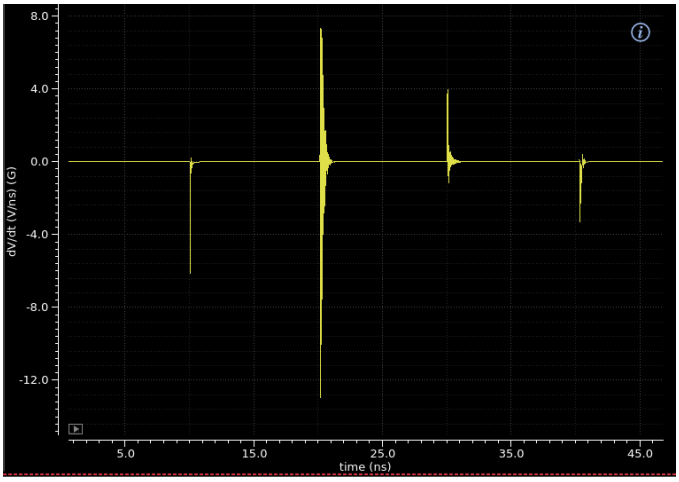

Fig. 9. The derivative of the simulated response of the amplifier when the input current is two rectangular pulses, one with positive amplitude and one with negative amplitude of 1 mA. From this, the differential output slew rate is calculated to be 6.12 V/ns.

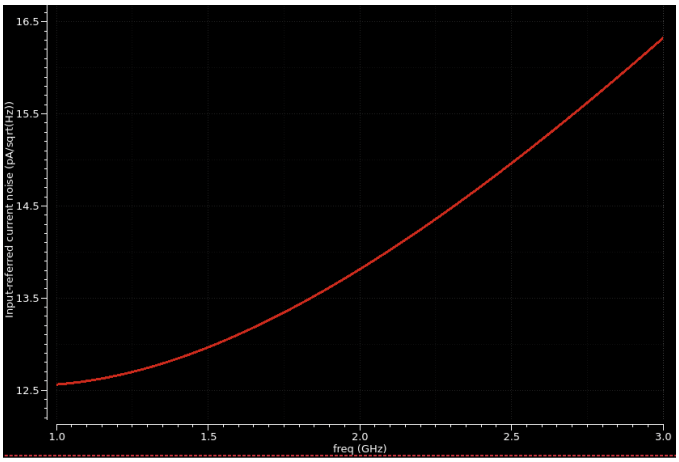

Fig. 10. The simulated input-referred current noise for the frequency range 1 GHz $< f <$ 3 GHz. The maximum current noise is 16.32 pA/$\sqrt{\text{Hz}}$ at 3 GHz.

TABLE I
SMALL SIGNAL PARAMETERS OF EACH TRANSISTOR

Transistor	**Small Signal Parameters**			
	$\mathbf{g_m}$ **(mS)**	$\mathbf{r_o}$ **(kΩ)**	$\mathbf{C_{gs}}$ **(fF)**	$\mathbf{C_{gd}}$ **(fF)**
M_1	13.78	0.448	15.48	9.881
M_2	9.179	0.876	12.12	6.151
M_3	11.18	0.465	21.11	6.752
M_4	22.04	0.340	18.38	8.539
M_5	10.45	0.759	12.89	7.347
M_6	6.012	1.311	6.832	3.723
M_7	6.008	1.312	6.829	3.722
M_8	27.04	0.282	19.74	5.694
M_9	27.05	0.282	19.75	5.694

REFERENCES

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