P2 Migration Guide

Pre-release version 2022-03-14

This is an pre-release migration guide and the contents are subject to change.

The Particle P2 module is the next generation Wi-Fi module from Particle. It is footprint compatible with our prior module, the P1, but is built on an upgraded chipset, supporting advanced features such as 5 GHz Wi-Fi, a 200MHz CPU, and built-in Bluetooth BLE 5.0.

Feature	P2	P1	Argon
User application size	1024 KB (1 MB)	128 KB	256 KB
Flash file system[1]	2 MB		2 MB
MCU	RTL8721DM	STM32F205RGY6	nRF52840
	Realtek Semiconductor	ST Microelectronics	Nordic Semiconductor
CPU	Cortex M33 @ 200 MHz	Cortex M3 @ 120 MHz	Cortex M3 @ 64 MHz
	Cortex M23 @ 20 MHz		
RAM[2]	512 KB	128 KB	256 KB
Flash[3]	16 MB	1 MB	1 MB
Hardware FPU	✓		✓
Secure Boot	✓		
Trust Zone	✓		
Wi-Fi	802.11 a/b/g/n	802.11 b/g/n	802.11 b/g/n
2.4 GHz	✓	✓	✓
5 GHz	✓		
Bluetooth	BLE 5.0		BLE 5.0
NFC Tag			External antenna required
Antenna	Shared for Wi-Fi and BLE	Wi-Fi only	Separate Wi-Fi and BLE antennas
	Built-in PCB antenna (Wi-Fi & BLE)	Built-in PCB antenna (Wi-Fi)	Built-in chip antenna (BLE)
			Required external antenna (Wi-Fi)
	Optional external (Wi-Fi & BLE)[4]	Optional external (Wi-Fi)[4]	Optional external (BLE)[4]
Peripherals	USB 2.0	USB 1.1	USB 1.1
Digital GPIO	22	24	20
Analog (ADC)	6	13	6
Analog (DAC)		2	
UART	1	2	1
SPI	2	2	2
PWM	6	12	8
I2C	1	1	1
CAN		1	
I2S		1	1
JTAG		✓	

SWD	✓	✓	✓

[1]A small amount of the flash file system is used by Device OS, most is available for user data storage using the POSIX filesystem API. This is separate from the flash memory used for Device OS, user application, and OTA transfers.

[2] Total RAM; amount available to user applications is smaller.

[3] Total built-in flash; amount available to user applications is smaller. The Argon also has a 4 MB external flash, a portion of which is available to user applications as a flash file system.

[4] Onboard or external antenna is selectable in software.

Hardware

NO 5V TOLERANCE!

On Gen 2 devices (STM32F205), most pins are 5V tolerant. This is not the case for Gen 3 (nRF52840) and the P2 (RTL872x). You must not exceed 3.3V on any GPIO pin, including ports such as serial, I2C, and SPI.

PINS A3, A4, AND DAC (A6)

Pins A3 (module pin 22), A4 (module pin 21), DAC/A6 (module pin 24) do not exist on the P2 and are NC.

You will need to use different pins if you are currently using these pins.

SPI

Both the P1 and P2 have two SPI ports, however the pins are different for `SPI` (primary SPI).

	P1	P2
SPI SCK	A3	D20 / S2
SPI MISO	A4	D19 / S1
SPI MOSI	A5	D18 / S0

The following are all SPI-related pins on the P1 and P2:

Pin	P1 Pin Name	P1 SPI	P2 Pin Name	P2 SPI
21	A4	SPI (MISO)	NC	
22	A3	SPI (SCK)	NC	
23	A5	SPI (MOSI)	A5 / D14	
40	P1S0		S0 / D15	SPI (MOSI)
41	P1S1		S1 / D16	SPI (MISO)
42	P1S2		S2 / D17	SPI (SCK)
44	P1S3		S3 / D18	SPI (SS)
45	D2	SPI1 (MOSI)	D2	SPI1 (MOSI)
49	A2	SPI (SS)	A2 / D13	
51	D3	SPI1 (MISO)	D3	SPI1 (MISO)
52	D4	SPI1 (SCK)	D4	SPI1 (SCK)
53	D5	SPI1 (SS)	D5	SPI1 (SS)

SPI - Gen 2 devices (including P1)

	SPI	SPI1
Maximum rate	30 MHz	15 MHz
Default rate	15 MHz	15 MHz
Clock	60 MHz	30 MHz

- Available clock divisors: 2, 4, 8, 16, 32, 64, 128, 256

SPI - P2

	SPI	SPI1
Maximum rate	25 MHz	50 MHz
Hardware peripheral	RTL872x SPI1	RTL872x SPI0

I2C

The P2 supports one I2C (two-wire serial interface) port on the same pins as the P1:

Pin	P1 Pin Name	P1 I2C	P2 Pin Name	P2 I2C
35	D1	Wire (SCL)	D1 / A4	Wire (SCL)
36	D0	Wire (SDA)	D0 / A3	Wire (SDA)

- The P2 I2C port is not 5V tolerant
- The P1 includes internal 2.2K pull-up resistors on D0/D1, the P2 does not

SERIAL (UART)

The primary UART serial (`Serial1`) is on the TX and RX pins on both the P1 and P2. There is no hardware flow control on this port on the P1 or P2.

The secondary UART serial (`Serial2`) is on different pins, however it does not conflict with the RGB LED, and also supports CTS/RTS hardware flow control.

Pin	P1 Pin Name	P1 Serial	P2 Pin Name	P2 Serial
31	RGBB	Serial2 (RX)	RGBB	
32	RGBG	Serial2 (TX)	RGBG	
45	D2		D2	Serial2 (RTS)
51	D3		D3	Serial2 (CTS)
52	D4		D4	Serial2 (TX)
53	D5		D5	Serial2 (RX)
63	RX	Serial1 (RX)	RX / D9	Serial1 (RX)
64	TX	Serial1 (TX)	TX / D8	Serial1 (TX)

	P1	P2
Buffer size	64 bytes	2048 bytes
7-bit mode	✓	✓
8-bit mode	✓	✓
9-bit mode	✓	
1 stop bit	✓	✓
2 stop bits	✓	✓
No parity	✓	✓
Even parity	✓	✓
Odd parity	✓	✓
Break detection	✓	
LIN bus support	✓	
Half duplex	✓	
CTS/RTS flow control		✓[1]

[1]CTS/RTS flow control only on Serial2. It is optional.

ANALOG INPUT (ADC)

For analog to digital conversion (ADC) using `analogRead()`, there are fewer ADC inputs on the P2:

Pin	P1 Pin Name	P1 ADC	P2 Pin Name	P2 ADC
21	A4	✓	NC	
22	A3	✓	NC	
23	A5	✓	A5 / D14	✓
24	DAC / A6	✓	NC	
30	WKP / A7	✓	D10 / WKP	
35	D1		D1 / A4	✓
36	D0		D0 / A3	✓
40	P1S0	✓	S0 / D15	
41	P1S1	✓	S1 / D16	
42	P1S2	✓	S2 / D17	
43	A1	✓	A1 / D12	✓
44	P1S3	✓	S3 / D18	
48	P1S5	✓	S5 / D20	
49	A2	✓	A2 / D13	✓
50	A0	✓	A0 / D11	✓

On the P2, there are no pins A3 (hardware pin 21) and A4 (hardware pin 22); these are NC (no connection). However, P2 pin D0 (hardware pin 36) can be used as an analog input and has the alias A3. The same is true for P2 pin D1 (hardware pin 35), which has the alias A4.

PWM (PULSE-WIDTH MODULATION)

The pins that support PWM are different on the P1 and P2.

Pin	P1 Pin Name	P1 PWM	P2 Pin Name	P2 PWM
21	A4	✓	NC	
23	A5	✓	A5 / D14	✓
30	WKP / A7	✓	D10 / WKP	
33	P1S6	✓	S6 / D21	
35	D1	✓	D1 / A4	✓
36	D0	✓	D0 / A3	✓
40	P1S0	✓	S0 / D15	✓
41	P1S1	✓	S1 / D16	✓
45	D2	✓	D2	
49	A2		A2 / D13	✓
51	D3	✓	D3	
63	RX	✓	RX / D9	
64	TX	✓	TX / D8	

All available PWM pins on the P2 share a single timer. This means that they must all share a single frequency, but can have different duty cycles.

DIGITAL TO ANALOG CONVERTER (DAC)

The P1 supports DAC one A3 and A6 (DAC). There is no DAC on the P2 or Gen 3 devices.

If you need a DAC, it's easy to add one via I2C or SPI on your base board.

Pin	P1 Pin Name	P1 DAC	P2 Pin Name	P2 DAC
22	A3	✓	NC	
24	DAC / A6	✓	NC	

WKP (A7)

	P1	P2
Module Pin	30	30
Pin Name	WKP	WKP
	A7	D11
Analog Input	✓	
PWM	✓	

On Gen 2 devices (STM32), only the WKP pin can wake from HIBERNATE sleep mode.

This restriction does not exist on the P2 and Gen 3 devices; any pin can be used to wake from all sleep modes.

CAN (CONTROLLER AREA NETWORK)

The P1 supports CAN on pins D1 and D2. There is no CAN on the P2 or Gen 3 devices (except the Tracker).

- The Tracker SoM includes CAN via a MCP25625 CAN interface with integrated transceiver.
- Both the MCP2515 and MCP25625 work with the library used on the Tracker and can be used to add CAN to the P2.

Pin	P1 Pin Name	P1 CAN	P2 Pin Name	P2 CAN
35	D1	✓	D1 / A4	
45	D2	✓	D2	

I2S (SOUND)

The P1 theoretically had I2S sound available on pins D1 and D2, however there has never been support for it in Device OS.

There is no software support for I2S on the P2 either, and while the RTL872x hardware supports I2S, the pins that it requires are in use by other ports.

Pin	P1 Pin Name	P1 I2S	P2 Pin Name	P2 I2S
45	D2	I2S3_SD	D2	
46	SETUP	I2S3_MCK	SETUP	
52	D4	I2S3_SCK	D4	
53	D5	I2S3_WS	D5	

INTERRUPTS

There are many limitations for interrupts on the STM32F205. All pins can be used for interrupts on

Gen 3 devices and the P2.

RETAINED MEMORY

Retained memory, also referred to as Backup RAM or SRAM, that is preserved across device reset, is not available on the P2. This also prevents system usage of retained memory, including session resumption on reset.

On Gen 2 and Gen 3 devices, retained memory is 3068 bytes.

The flash file system can be used for data storage on the P2, however care must be taken to avoid excessive wear of the flash for frequently changing data.

PIN FUNCTIONS REMOVED

The following pins served P1-specific uses and are NC on the P2. You should not connect anything to these pins.

Pin	Pin Name	Description
16	WL_JTAG_TDI	BCM43362 Debugging Pin.
17	WL_JTAG_TCK	BCM43362 Debugging Pin.
18	WL_JTAG_TRSTN	BCM43362 Debugging Pin.
19	WL_JTAG_TMS	BCM43362 Debugging Pin.
20	WL_JTAG_TDO	BCM43362 Debugging Pin.
21	A4	A4 Analog in, GPIO, SPI.
22	A3	A3 True analog out, analog in, GPIO.
24	DAC / A6	DAC/A6 True analog out, analog in, GPIO.
38	VBAT	Battery for internal real-time clock, backup registers, and SRAM. Supply 1.65VDC to 3.6 VDC at 19 µA..
38	VBAT_MICRO	Battery for internal real-time clock.
56	BTCX_STATUS	Coexistence signal: Bluetooth status and TX/RX direction.
57	BTCX_RF_ACTIVE	Coexistence signal: Bluetooth is active.
58	BTCX_TXCONF	Output giving Bluetooth permission to TX.
60	WL_SLEEP_CLK	BCM43362 Debugging Pin

PIN FUNCTIONS ADDED

The following pins were NC on the P1 but are used on the P2.

Pin	Pin Name	Description
12	VBAT_MEAS	Battery voltage measurement (optional).

FULL MODULE PIN COMPARISON

Software

WI-FI CONFIGURATION

The P2 and Argon utilize BLE for configuration of Wi-Fi rather than the SoftAP approach taken with the P1. Using BLE allow mobile apps to more easily set up the device Wi-Fi without having to modify the mobile device's network configuration.

Feature	P2	P1	Argon
Wi-Fi (SoftAP)		✓	
BLE	✓		✓

PLATFORM ID

The Platform ID of the P2 will different from that of the P1 (8) because of the vastly different hardware.

If you have a product based on the P1, you will need to create a separate product for devices using the P2. While you may be able to use the same source code to build your application, the firmware binaries uploaded to the console will be different, so they need to be separate products. This generally does not affect billing as only the number of devices, not the number of products, is counted toward your plan limits.

THIRD-PARTY LIBRARIES

Most third-party libraries are believed to be compatible. The exceptions include:

- Libraries that use peripherals that are not present (such as DAC)
- Libraries for MCU-specific features (such as ADC DMA)
- Libraries that are hardcoded to support only certain platforms by their PLATFORM_ID

Version History

Revision	Date	Author	Comments
pre	2021-11-04	RK	Pre-release
	2022-02-08	RK	Corrected D pin aliases for A5 and S0-S6
	2022-02-25	RK	Changed D pin aliases for D9 - D22, A5 is not SPI MOSI, Serial2 TX and RX were reversed
	2022-03-14	RK	Minor edits; no functional changes