TACNPR project

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SUBSHEETS (revision D):

Major changes since revA:

-revA: first release

-revB: integrated Ethernet

-revC: enhanced RF performance

-revD: Powerpole connector

CPU

MCU, SRAM, **SERIAL**

radio

Si4463 & RF switching RF-PA

RF LNA & PA

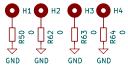
File: cpu-sheet.kicad_schFile: radio-sheet.kicad_sch

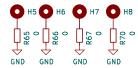
tacbucks

DC/DC converters linear-regs

3V3 lin.req. & terminals ethernet

W5500 Ethernet







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TACNPR project OH1GJV, OH2EAT, OH2FLO, OH3HZB, OH5GE



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Title: TACNPR				
Size: A4	Date: 2021-03-22			Rev: D
KiCad E.D.A. 8.0.6				ld: 1/7
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SRAM (23LC1024, 1Mbit) MCU: STM32L432KC (256 kB Flash) 23LC1024 R31 3V3_CPU SO/SIOHOLD/SIO3 3V3_CPU SI02 SCK 100n C48 C49 C50 4 VSS MOSI_SPI3 **=** C51 330 100n R91 3V3_LNA 10u GNDD GNDD U8 STM32L432KC GNDD GND_{R26} 330 GPIOR2 GPIOR1 GNDD 330 4 R45 GPIOR3 C54 STM32_NRST 4 NRST 2 2 2 100n 10k **CONN LEDs** R34 PA1 ∐ 10k GPIOR_HEADER PA2 VCP_TX PA2 = USART2_TX IRQ_SI4463 GNDD PA3 GND PA4 CS_SI4463 > LED_CON D17 PA5 CLK_SPI1) GNDD D18 GND PC14 PA6 MISO_SPI1 LED GND PC15 PA7 LED MOSI_SPI1 GNDD PA8 PA9 GPI0_10 GPI0_11 CS_SRAM LED_RX 15 PB1 PA10 20 CLK_SPI3 26 PB3 GNDD PA11 21 CS_W5500 GNDD PA12 22 **GPIO** ESD protection TP7 MISO_SPI3 LED_CON PA13 23 TP8 TestPoint MOSI_SPI3 28 programming CAT PB5 PA14 24 TestPoint O-100m SRV05-4 SSA PA15 25 3V3_CPU 3V8_OUT GPIO header SWCLK(PA14) GPI010_TERMINAL → PROG_CONN SWDIO(PA13) GNDD PA15 = USART2_RX GPI011_TERMINAL GPI010_TERMINAL 3V8_0UT (GPI011_TERMINAL) **USB ESD PROTECTION & CH340G SERIAL** GPIO_HEADER GND D6 LED 3V3_CPU R23 1.5k 100n 100n C78 470n 🔟 116 C76 CH340G SRV05-4 $\stackrel{\textstyle \downarrow}{\smile}$ GND USB_B_Micro TXD 2 0 VCP_RX RXD 3 0 VCP_TX GND 15 R232 R30 9 CTS1 10 DSR1 TestPoint TestPoint USB_DP UD+ USB_DM 0 6 UD-TACNPR / CPU sheet R32 12 DCD1 TestPoint 13 DTR1 TestPoint 14 RTS1 TestPoint DCD DTR (CPU, SRAM, GPIO, ETHERNET, USB SERIAL) Sheet: /cpu/ GND GGS File: cpu-sheet.kicad sch GND GND UM1 GND Title: TACNPR (CPU sheet) Size: A4 Rev: D KiCad E.D.A. 8.0.6 ld: 2/7

