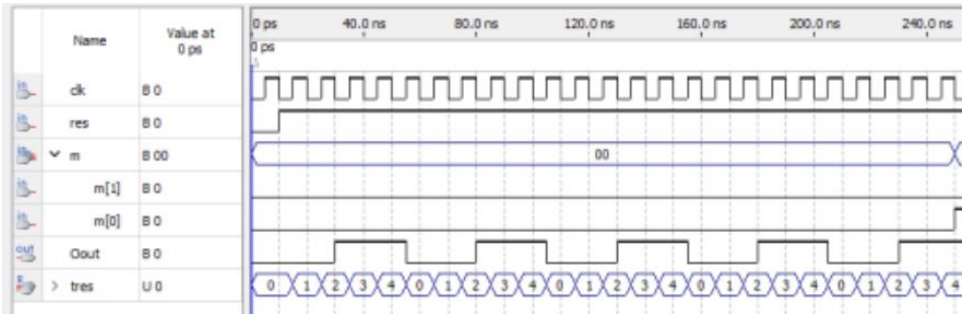
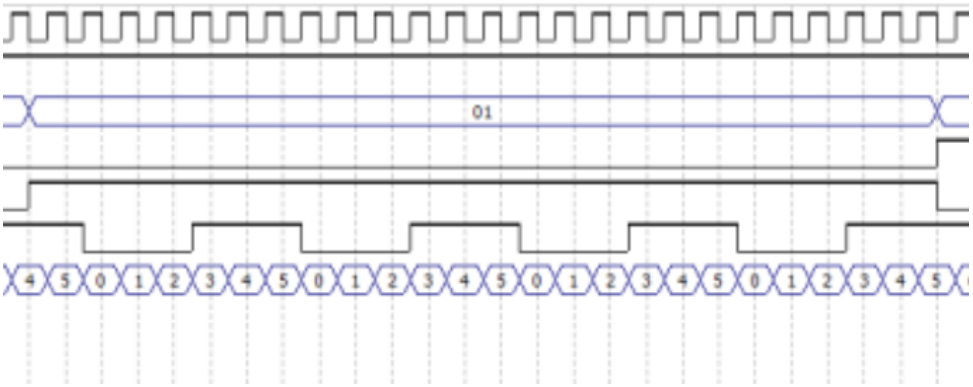
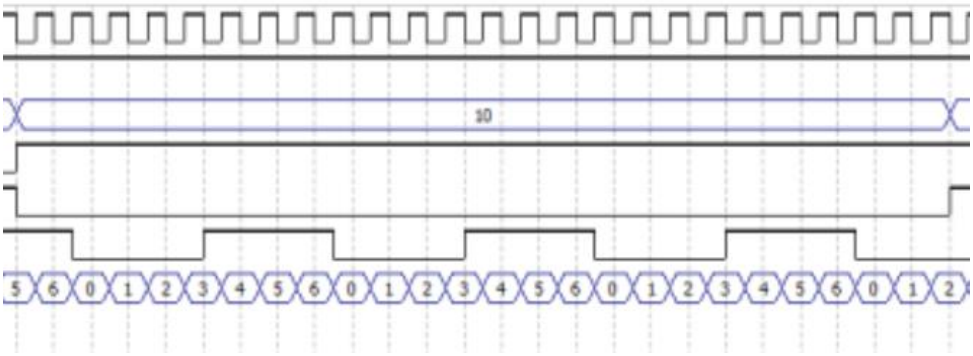
1.

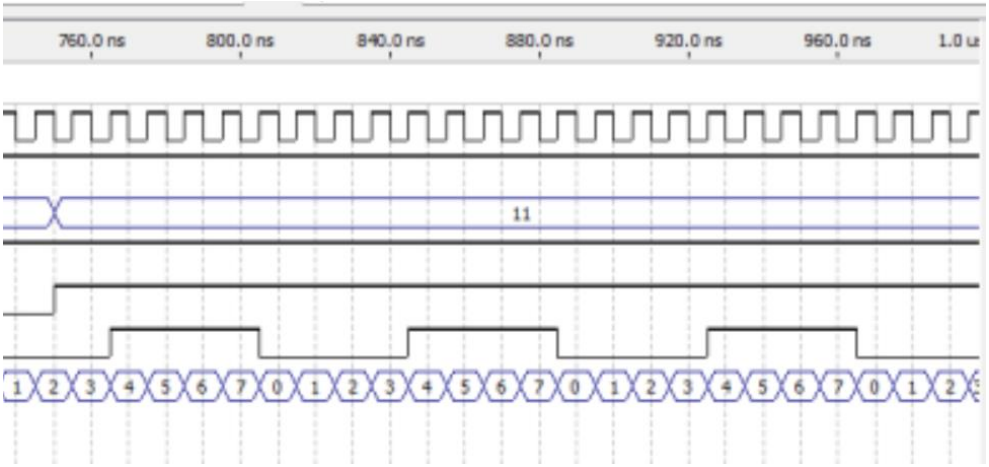
Code:

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_unsigned.all;
4
5  entity frequencyDivider is
6     port(
7        clk: in std_logic;
8        res: in std_logic;
9        m: in std_logic_vector(1 downto 0);
10       Oout: out std_logic
11    );
12 end frequencyDivider;
13
14 architecture frequencyDivider of frequencyDivider is
15    signal T: std_logic_vector(2 downto 0);
16 begin
17    process(clk, res, m)
18    begin
19       if res = '0' then T <= "000";
20       elsif clk'event and clk = '1' then
21          if m = "00" and T = "100" then T <= "000";
22          elsif m = "01" and T = "101" then T <= "000";
23          elsif m = "10" and T = "110" then T <= "000";
24          else T <= T + "001";
25          end if;
26       end if;
27    end process;
28
29    Oout <= '0' when T < 2 and m = "00" else
30            '1' when T > 2 and m = "00" else
31            '0' when T <= 2 and m = "01" else
32            '1' when T > 2 and m = "01" else
33            '0' when T < 3 and m = "10" else
34            '1' when T > 3 and m = "10" else
35            '0' when T <= 3 and m = "11" else
36            '1' when T > 3 and m = "11" else
37           not clk when m = "00" or m = "10";
38
39 end frequencyDivider;
```


Name
Value at 0 ps
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
clk
res
m
m[1]
m[0]
Oout
tres
00


01


10


760.0 ns
800.0 ns
840.0 ns
880.0 ns
920.0 ns
960.0 ns
11

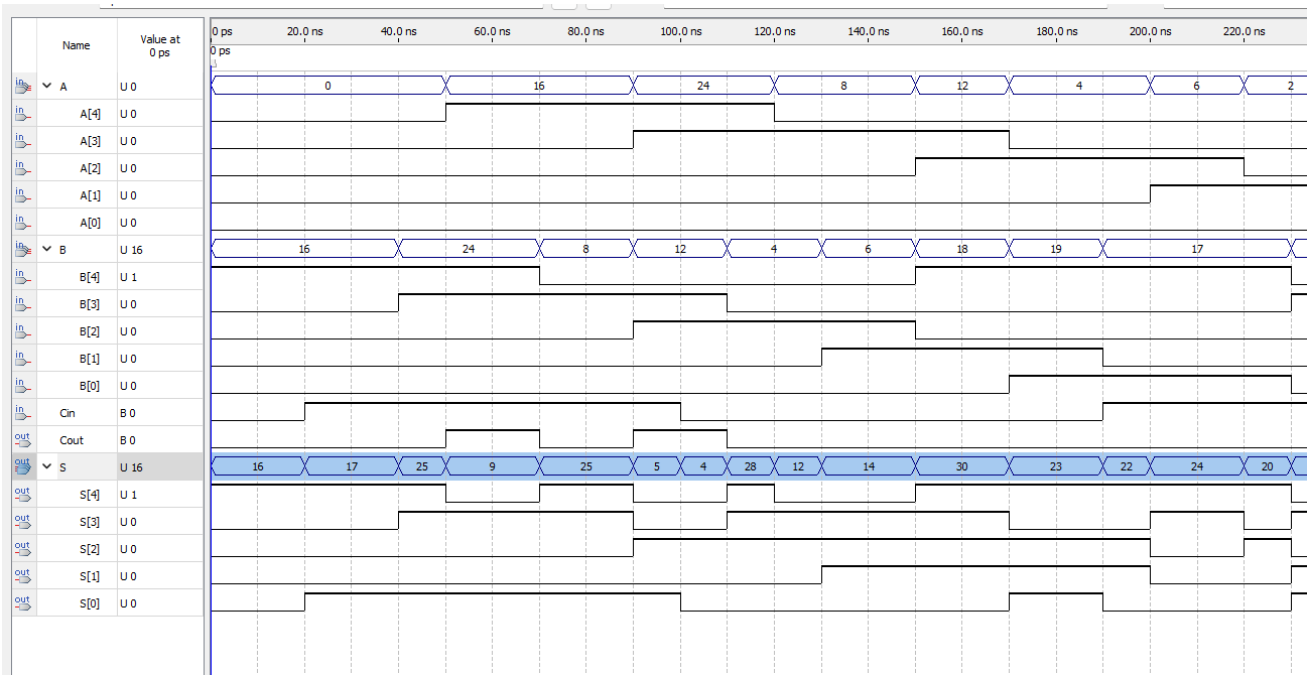
2.

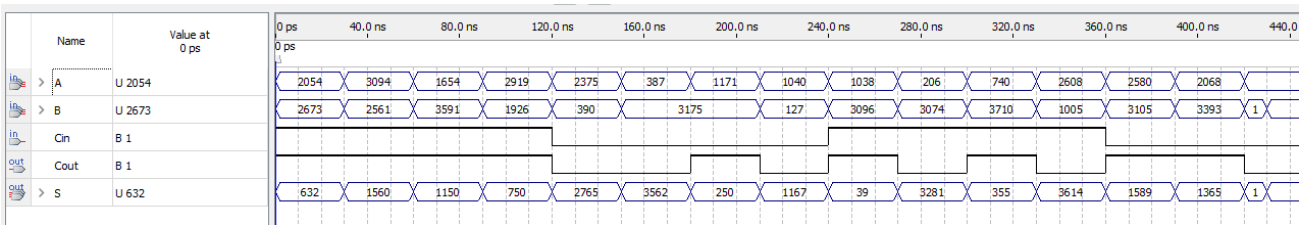
Code:

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity FA is
    port(
        A, B, Cin: in std_logic;
        S, Cout: out std_logic
    );
end FA;

architecture FA of FA is
begin
    S <= A xor B xor Cin;
    Cout <= ((A xor B) and Cin) or (A and B);
end FA;
```

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity FA_5bit is
    port(
        A, B: in std_logic_vector(4 downto 0);
        Cin: in std_logic;
        S: out std_logic_vector(4 downto 0);
        Cout: out std_logic
    );
end FA_5bit;

architecture FA_5bit of FA_5bit is
    component FA is
        port(
        A, B, Cin: in std_logic;
        S, Cout: out std_logic
    );
    end component;
    signal c1, c2, c3, c4: std_logic;
begin
    FA1: FA port map(
        A(0), B(0), Cin, S(0), c1
    );
    FA2: FA port map(
        A(1), B(1), c1, S(1), c2
    );
    FA3: FA port map(
        A(2), B(2), c2, S(2), c3
    );
    FA4: FA port map(
        A(3), B(3), c3, S(3), c4
    );
    FAOut: FA port map(
        A(4), B(4), c4, S(4), Cout
    );
end FA_5bit;
```

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity FA_12bit is
   port(
      A, B: in std_logic_vector(11 downto 0);
      Cin: in std_logic;
      S: out std_logic_vector(11 downto 0);
      Cout: out std_logic
   );
end FA_12bit;

architecture FA_12bit of FA_12bit is
   component FA is
      port(
         A, B, Cin: in std_logic;
         S, Cout: out std_logic
      );
   end component;
   component FA_5bit is
   port(
      A, B: in std_logic_vector(4 downto 0);
      Cin: in std_logic;
      S: out std_logic_vector(4 downto 0);
      Cout: out std_logic
   );
   end component;
   signal c1, c2, c3: std_logic;

begin
   FA1to5: FA_5bit port map(
      A(4 downto 0), B(4 downto 0), Cin, S(4 downto 0), c1
   );
   FA6to10: FA_5bit port map(
      A(9 downto 5), B(9 downto 5), c1, S(9 downto 5), c2
   );
   FA11: FA port map(
      A(10), B(10), c2, S(10), c3
   );
   FA12: FA port map(
      A(11), B(11), c3, S(11), Cout
   );
end FA_12bit;
```


Name
Value at 0 ps
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
140.0 ns
160.0 ns
180.0 ns
200.0 ns
220.0 ns
A U 0
A[4] U 0
A[3] U 0
A[2] U 0
A[1] U 0
A[0] U 0
B U 16
B[4] U 1
B[3] U 0
B[2] U 0
B[1] U 0
B[0] U 0
Cin B 0
Cout B 0
S U 16
S[4] U 1
S[3] U 0
S[2] U 0
S[1] U 0
S[0] U 0
0 16 24 8 12 4 6 2
16 24 8 12 4 6 18 19 17
16 17 25 9 25 5 4 28 12 14 30 23 22 24 20


Name
Value at 0 ps
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
360.0 ns
400.0 ns
440.0
A U 2054
B U 2673
Cin B 1
Cout B 1
S U 632
2054 3094 1654 2919 2375 387 1171 1040 1038 206 740 2608 2580 2068
2673 2561 3591 1926 390 3175 127 3096 3074 3710 1005 3105 3393 1
632 1560 1150 750 2765 3562 250 1167 39 3281 355 3614 1589 1365 1