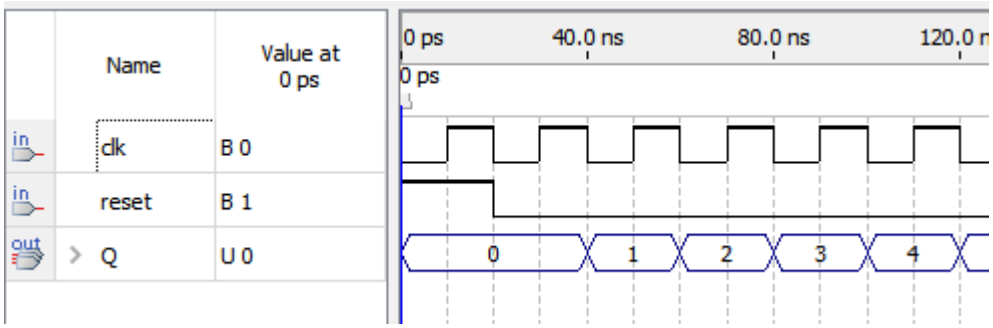
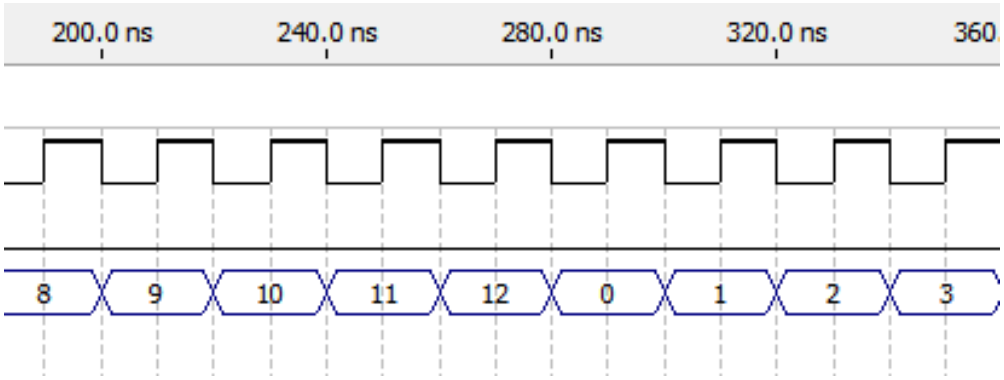
非同步 4bit 上數 counter 從 0~12

Code:

```
1  library ieee;
2
3  use ieee.std_logic_1164.all;
4  use ieee.std_logic_signed.all;
5
6  entity counter_up is
7     port(
8        reset, clk: in std_logic;
9        Q: out std_logic_vector(3 downto 0)
10    );
11 end counter_up;
12
13 architecture counter_up of counter_up is
14    signal da, db, dc, dd, r2: std_logic;
15 begin
16    process(clk, reset, r2)
17    begin
18       if reset = '1' then da <= '0';
19       elsif r2 = '1' then da <= '0';
20       elsif clk'event and clk = '0' then da <= not da;
21       end if;
22    end process;
23
24    process(da, reset, r2)
25    begin
26       if reset = '1' then db <= '0';
27       elsif r2 = '1' then db <= '0';
28       elsif da'event and da = '0' then db <= not db;
29       end if;
30    end process;
31
32    process(db, reset, r2)
33    begin
34       if reset = '1' or r2 = '1' then dc <= '0';
35       elsif db'event and db = '0' then dc <= not dc;
36       end if;
37    end process;
38
39    process(dc, reset, r2)
40    begin
41       if reset = '1' or r2 = '1' then dd <= '0';
42       elsif dc'event and dc = '0' then dd <= not dd;
43       end if;
44    end process;
45
46    Q <= dd & dc & db & da;
47    r2 <= '1' when dd = '1' and dc = '1' and da = '1' else '0';
48
49 end counter_up;
```

模擬圖:


Name
Value at
0 ps
clk
B 0
reset
B 1
Q
U 0
0 ps
40.0 ns
80.0 ns
120.0 n
0 ps
0
1
2
3
4


200.0 ns
240.0 ns
280.0 ns
320.0 ns
360
8
9
10
11
12
0
1
2
3