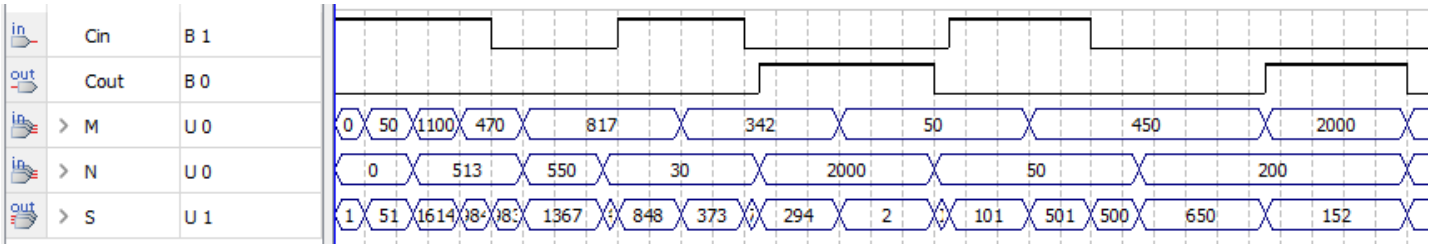
1.

Code:

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity NM_FA is
    generic(
    N: integer range 1 to 32 := 8;
    M: integer range 1 to 32 := 8
    );
    port(
    A: in std_logic_vector(N - 1 downto 0);
    B: in std_logic_vector(M - 1 downto 0);
    C: in std_logic;
    S: out std_logic_vector(M - 1 downto 0);
    Co: out std_logic
    );
end NM_FA;

architecture NM_FA of NM_FA is
    signal tp: std_logic_vector(M downto 0);
begin
    tp <= ('0' & A) + B + C;
    S <= tp(M - 1 downto 0);
    Co <= tp(M);
end NM_FA;
```

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity NM_FA_Gen is
    port(
    A: in std_logic_vector(7 downto 0);
    B: in std_logic_vector(7 downto 0);
    C: in std_logic;
    S: out std_logic_vector(7 downto 0);
    Co: out std_logic
    );
end NM_FA_Gen;

architecture NM_FA_Gen of NM_FA_Gen is
    component NM_FA is
        generic(
            N: integer range 1 to 32;
            M: integer range 1 to 32
        );
        port(
            A: in std_logic_vector(N - 1 downto 0);
            B: in std_logic_vector(M - 1 downto 0);
            C: in std_logic;
            S: out std_logic_vector(M - 1 downto 0);
            Co: out std_logic
        );
    end component;
begin
    U1: NM_FA generic map(8, 8) port map(A, B, C, S, Co);
end NM_FA_Gen;
```

模擬:


Cin
B 1
Cout
B 0
M
U 0
0
50
1100
470
817
342
50
450
2000
N
U 0
0
513
550
30
2000
50
200
S
U 1
1
51
1614
1367
848
373
294
2
101
501
500
650
152

2.

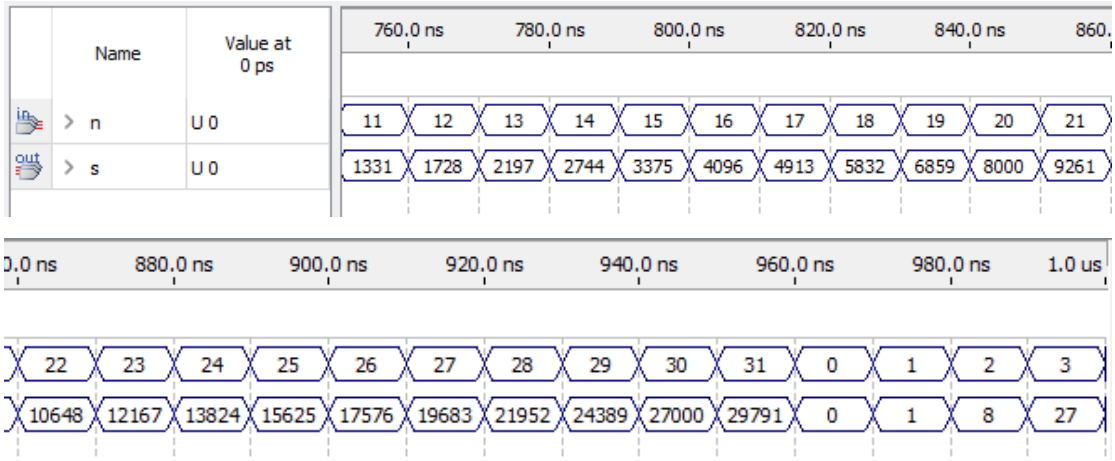
Code:

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_unsigned.all;
4
5  entity FA_N is
6     generic(
7        N: integer range 1 to 32 := 3
8     );
9     port(
10       A: in std_logic_vector(N - 1 downto 0);
11       B: in std_logic_vector(N - 1 downto 0);
12       C: in std_logic;
13       S: out std_logic_vector(N - 1 downto 0);
14       Co: out std_logic
15    );
16 end FA_N;
17
18 architecture FA_N of FA_N is
19    signal tp: std_logic_vector(N downto 0);
20 begin
21    tp <= ('0' & A) + B + C;
22    S <= tp(N - 1 downto 0);
23    Co <= tp(N);
24 end FA_N;
```

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity MUL_NM is
   generic(
      N: integer range 1 to 32 := 8;
      M: integer range 1 to 32 := 8
   );
   port(
      X: in std_logic_vector(N - 1 downto 0);
      Y: in std_logic_vector(M - 1 downto 0);
      P: out std_logic_vector(N + M - 1 downto 0)
   );
end MUL_NM;

architecture MUL_NM of MUL_NM is
   type CC is array (0 to M - 1) of std_logic_vector(n - 1 downto 0);
   type TT is array (0 to M - 3) of std_logic_vector(N downto 0);
   signal C: CC;
   signal T: TT;

   component FA_N is
      generic(N: integer range 1 to 32);
      port(
         A: in std_logic_vector(N - 1 downto 0);
         B: in std_logic_vector(N - 1 downto 0);
         C: in std_logic;
         S: out std_logic_vector(N - 1 downto 0);
         Co: out std_logic
      );
   end component;
begin
   process(X, Y)
   begin
      for i in 0 to M - 1 loop
         for j in 0 to N - 1 loop
            C(i)(j) <= X(j) and Y(i);
         end loop;
      end loop;
   end process;

LP: for i in 0 to M - 2 generate

FI: if i = 0 generate
         FA: FA_N generic map(N) port map('0' & C(i)(N - 1 downto 1),
         C(i + 1), '0', T(i)(N - 1 downto 0), T(i)(N));
      end generate;
MID: if i > 0 and i < M - 2 generate
         FA: FA_N generic map(N) port map(T(i - 1)(N downto 1), C(i + 1), '0',
         T(i)(N - 1 downto 0), T(i)(N));
      end generate;
FN: if i = M - 2 generate
         FA: FA_N generic map(N) port map(T(i - 1)(N downto 1), C(i + 1), '0',
         P(N + M - 2 downto M - 1), P(N + M - 1));
      end generate;
end generate LP;

   P(0) <= C(0)(0);
   process(T)
   begin
      for i in 1 to M - 2 loop
         P(i) <= T(i - 1)(0);
      end loop;
   end process;
end MUL_NM;
```

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity N3 is
    port(
        X: in std_logic_vector(3 downto 0);
        P: out std_logic_vector(11 downto 0)
    );
end N3;

architecture N3 of N3 is
    signal tp: std_logic_vector(7 downto 0);
    component MUL_NM is
        generic(
            N: integer range 1 to 32;
            M: integer range 1 to 32
        );
        port(
            X: in std_logic_vector(N - 1 downto 0);
            Y: in std_logic_vector(M - 1 downto 0);
            P: out std_logic_vector(N + M - 1 downto 0)
        );

    end component;
begin
    U1: MUL_NM generic map(4, 4) port map(X, X, tp);
    U2: MUL_NM generic map(4, 8) port map(X, tp, P);
end N3;
```

模擬:


Name
Value at
0 ps
n
U 0
s
U 0
760.0 ns
780.0 ns
800.0 ns
820.0 ns
840.0 ns
11 12 13 14 15 16 17 18 19 20 21
1331 1728 2197 2744 3375 4096 4913 5832 6859 8000 9261

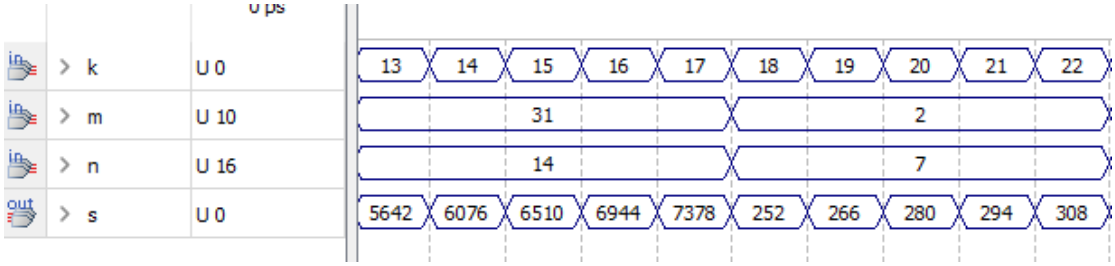
880.0 ns
900.0 ns
920.0 ns
940.0 ns
960.0 ns
980.0 ns
1.0 us
22 23 24 25 26 27 28 29 30 31 0 1 2 3
10648 12167 13824 15625 17576 19683 21952 24389 27000 29791 0 1 8 27

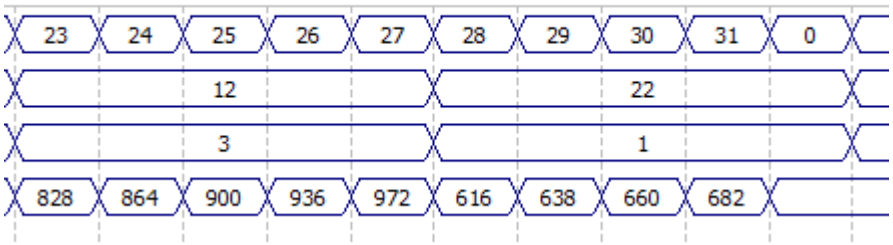
3.

只有 top_level 和第二題不同，其他皆相同

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity N3 is
    port(
        X: in std_logic_vector(2 downto 0);
        Y: in std_logic_vector(3 downto 0);
        Z: in std_logic_vector(4 downto 0);
        P: out std_logic_vector(11 downto 0)
    );
end N3;

architecture N3 of N3 is
    signal tp: std_logic_vector(6 downto 0);
    component MUL_NM is
        generic(
            N: integer range 1 to 32;
            M: integer range 1 to 32
        );
        port(
            X: in std_logic_vector(N - 1 downto 0);
            Y: in std_logic_vector(M - 1 downto 0);
            P: out std_logic_vector(N + M - 1 downto 0)
        );

    end component;
begin
    U1: MUL_NM generic map(3, 4) port map(X, Y, tp);
    U2: MUL_NM generic map(5, 7) port map(Z, tp, P);
end N3;
```

模擬:


0 ps
k
U 0
m
U 10
n
U 16
s
U 0
13 14 15 16 17 18 19 20 21 22
31 2
14 7
5642 6076 6510 6944 7378 252 266 280 294 308


23 24 25 26 27 28 29 30 31 0
12 22
3 1
828 864 900 936 972 616 638 660 682