High Fidelity Qubit Mapping for IBM Q

Shin Nishio[1] * Takahiko Satoh[2] † Rodney D. Van Meter[3] ‡

[1] *Faculty of Policy Management , Keio University, 5322 Endo, Fujisawa City, Kanagawa Japan*
[2] *Keio University Quantum Computing Center, 3-14-1 Hiyoshi, Kohoku-ku, Yokohama, Kanagawa Japan*
[3] *Faculty of Environment and Information Studies, Keio University, 5322 Endo, Fujisawa City, Kanagawa Japan*

Abstract. Existing quantum computer processors have topological limitations on the execution of CNOT gates. Error rates reduce the fidelity of execution results for the individual qubits and connection via CNOT. The problem of which qubit variable on the program is allocated to which qubit on the processor has a strong influence on the feasibility and fidelity on the current medium-sized and noise-unequal processors. In this research, we are creating software for QISKIT that assigns quantum bit variables to quantum bits of the processor to execute programs on existing IBM quantum processors.

In this study we are going to relax the limitation of processor's use of CNOT gate to some extent using swap gates. Also, we are going to improve the fidelity by decomposing the errors contained in the quantum circuit.

Keywords: QISKIT, QASM, IBM Q, Quantum Architecture, Graph Embedding, Compiler, Transpiler, Qubit Allocation, Qubit Mapping

1 Problems in Adapting Programs to Real Machines

1.1 Processor Topology

The number of qubits in the processor of a quantum computer is increasing day by day [1]. However, it is difficult to generate the entangled state in any physically non-adjacent qubits on the processor. In fact, any processor laid outnin 20 and without a common bus, including all processors created by IBM, are limited in the use of CNOT gates.

This graph of limitation of use of the CNOT gate is referred to as the processor topology. For example, Fig. 1 show the topologies of IBM Q20 Austin[2].

Also, as can be seen from this topology, the number of qubits that can use CNOT varies for each qubit. Right of Fig. 1 shows how many CNOTs can be used for qubits.

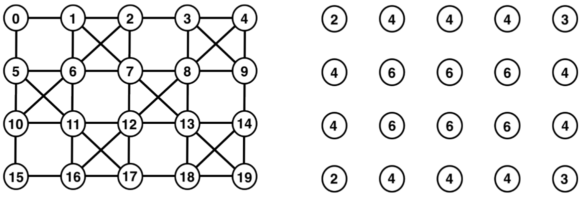


Figure 1: left: IBM Q20 Austin's topology. right: The number of qubits with which each qubit can execute a CNOT corresponding to the node degree.

1.2 Errors and Error Propagation

If you run a quantum circuit in the current IBM processor, the following errors will occur stochastically and the fidelity of your final state will go down.

1. Gate error
   Error occurring when unitary gate is executed for qubit.

2. Measurement error
   Errors that occur when observing qubits.

3. Bi-Qubit error
   Errors that occur when using a control gate such as a CNOT gate for 2 qubits.

2 Executing Long-Distance Operations

2.1 Choosing Sub-circuits

The swap gate exchanges the state of two qubits. Swap gates can be implemented by combining CNOT gates as shown in Fig. 2. On the IBM processors, this is the prefered approach.

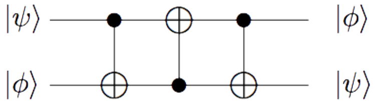


Figure 2: SWAP gate

By using the SWAP gate, it is possible to increase the effective range of CNOT.

For example, the 6th and 7th qubits in Figure 1 are connected to 6 qubits, respectively, but as shown in Fig. 3, CNOT can be considered to reach 9 qubits by inserting single SWAP gate. Of course, inserting more SWAP gates can in principle, extend the range across the chip. In many quantum compputations such as error correction, there are cases where CNOT gates are applied from one qubit to many qubits. Therefore, it is required to relax restrictions on CNOT owned by the processor by inserting SWAP gates.

*parton@sfc.wide.ad.jp

†satoh@sfc.wide.ad.jp

‡rdv@sfc.wide.ad.jp

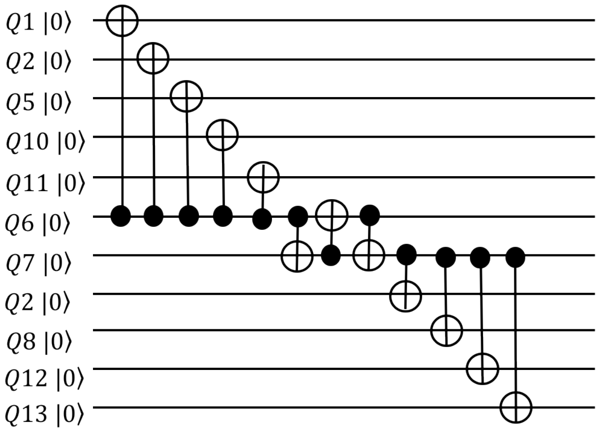


Figure 3: Quantum circuit with SWAP gate applied to 6th and 7th qubits

In quantum mapping, if we aim to improve fidelity despite limitations on the circuit, we consider as follows. If there is a qubit structure on the quantum processor as shown on the left side of Fig. 4, a CNOT gate can be executed directly as in circuit A on the right side of Fig. 4.

However, it cannot be executed in a structure where the 0th qubit and the 2nd qubit are not coupled as shown in Fig. 5. In such a case, circuits like circuits B, C and D in Fig. 6 can be substituted. At this time, the fidelity obtained by observing the qubit of each circuit is different. Also, which circuit's fidelity is high depends on the following values.

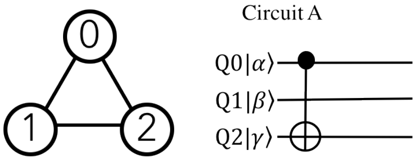


Figure 4: left: Three qubits in a completely connected graph right: Circuit A

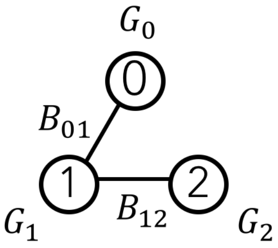


Figure 5: Most processors will have only a limited set of connections. G_i and B_{ij} are gate error rates.

1. Single-qubit gate error of Q0 and Q2 G_0, G_2

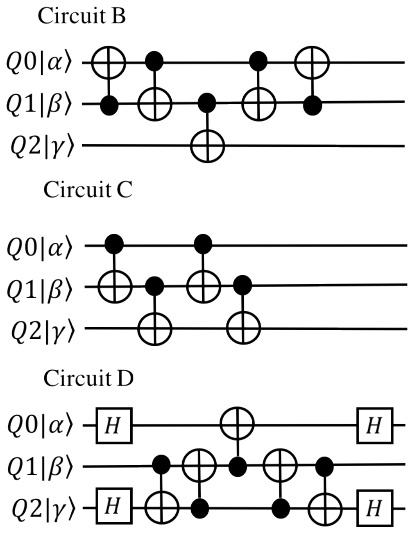


Figure 6: Circuits which can substitute for the CNOT in circuit A.

2. Bi-Qubit error of each connections between qubits B_{01}, B_{02}, B_{12}

In the current quantum circuit, the gate error tends to be smaller than the Bi-Qubit error, so mapping like circuit D is also effective.

Since the value of Bi-Qubit errors is differs by location in the current quantum processor, we are investigating which kinds of circuit can increase the fidelity by classifying in the following cases and applying this knowledge at the time of mapping .

- If $B_{01} \gg B_{12}$, Circuit B is the highest fidelity.
- If $B_{01} \simeq B_{12}$, Circuit C is the highest fidelity.
- If $B_{01} \ll B_{12}$, Circuit B is the highest fidelity.

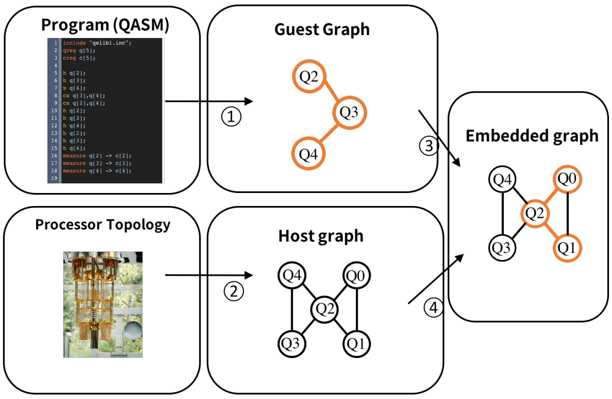
2.2 Variable Mapping and Graph Embedding

Therefore, in order for the programmer to allocate the variable used in the program to the qubit on the hardware, it is necessary to refer to the topology. In addition, in order to obtain a calculation result with high fidelity, it is necessary to consider the error rate of each qubit and the topology of the processor.

In order to deal with large code and increase the reusability of various programs on various hardware it is necessary to automate this process. Like the compiler on classical computers, automation is necessary to efficiently use resources.

This is called qubit mapping automation. Fig. 7 is an example of the qubit mapping process.

Qubit mapping can be regarded as a graph embedding problem. Graph embedding is widely used for analyzing the performance of different structures[5]. To embed one graph in another, each node of the guest graph is assigned to a node of the host graph, and each edge of the guest graph is assigned to a link or path on the host graph. In this research, we treat the processor's topology as a host graph, and the quantum circuit as a guest graph.



```
include "qelib1.inc";
qreg q[5];
creg c[5];

h q[2];
h q[3];
x q[4];
cx q[3],q[4];
cx q[2],q[4];
h q[2];
h q[3];
h q[4];
h q[2];
h q[3];
h q[4];
measure q[2] -> c[2];
measure q[3] -> c[3];
measure q[4] -> c[4];
```

Figure 7: qubit mapping

Our group has created tools for performing similar mapping in prior work [3][4]. Those studies introduced the idea of incorporating graphs into the allocation of qubits, but there was no consideration of the impact of the errors on quantum circuits.

3 Preliminary Results and Plans

In this research, we relax CNOT topology restriction by inserting SWAP gate or using a chain of CNOT gates as shown circuit C in Fig. 6 in addition to quantum bit allocation, and we are increasing the number of executable quantum circuits.

If you use Q6, Q11, Q12 of IBM Q 20 as Q0, Q1, Q2, the error rate is as shown in the Table 1, and the fidelities of Circuit B, C, and D is as follows.

Circuit B: $F = (1 - B_{01})^4 * (1 - B_{12}) = 0.487$

Table 1: Single gate errors and bi-qubit errors. IBM machine fidelity continues to evolve as researchers improve. This data is an analytical estimate using only the gate fidelity reported in 2018.6.9.

Qubit	Name	Error
Q6	G_0	$3.21 \times\ 10^{-3}$
Q11	G_1	$4.88 \times\ 10^{-3}$
Q12	G_2	$4.43 \times\ 10^{-3}$
Q_6— Q_{11}	B_{01}	$15.73 \times\ 10^{-2}$
Q_{11}— Q_{12}	B_{12}	$3.43 \times\ 10^{-2}$

Circuit C: $F = (1 - B_{01})^2 * (1 - B_{12})^2 = 0.662$

Circuit D: $F = (1 - B_{01}) * (1 - B_{12}) * (1 - G_0)^2 * (1 - G_2)^2 = 0.801$

In this case, circuit D's fidelity is the highest. For generalization, Ignoring the effect of a single gate error that is smaller than the bi-qubit error, circuit with high fidelity is required according to the value of bi-qubit error as Fig. 8. For getting higher fidelity, we need to estimate quantum states more accurate. For that, we need to know more detail of error of qubits by using process-tomography[6].

These considerations show that in order to obtain a high fidelity quantum circuit in the NISQ era when the processor error is inhomogeneous, it is important to flexibly change the way of mapping in one processor. By using the appropriate metrics, route optimization for high fidelity becomes possible. A path with a high infidelity is a poor choice, and so it is assigned a high cost in the mapping phase. Ultimately, with the right definition of path cost, we can apply a form of Dijkstra's algorithm on the host graph.

Our next steps are to confirm the basic approach through experiments on the IBM processors, to automate the process, then to expand the error model used in path selection beyond simple fidelity.

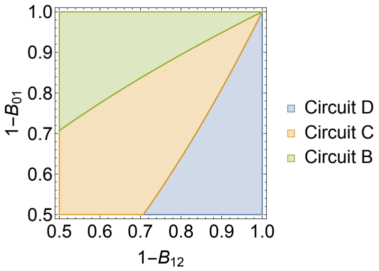


Figure 8: A circuit that can obtain high fidelity when B_{01} and B_{12} vary.

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