

High Fidelity Qubit Mapping for IBM Q

2nd International Workshop on
Quantum Compilation

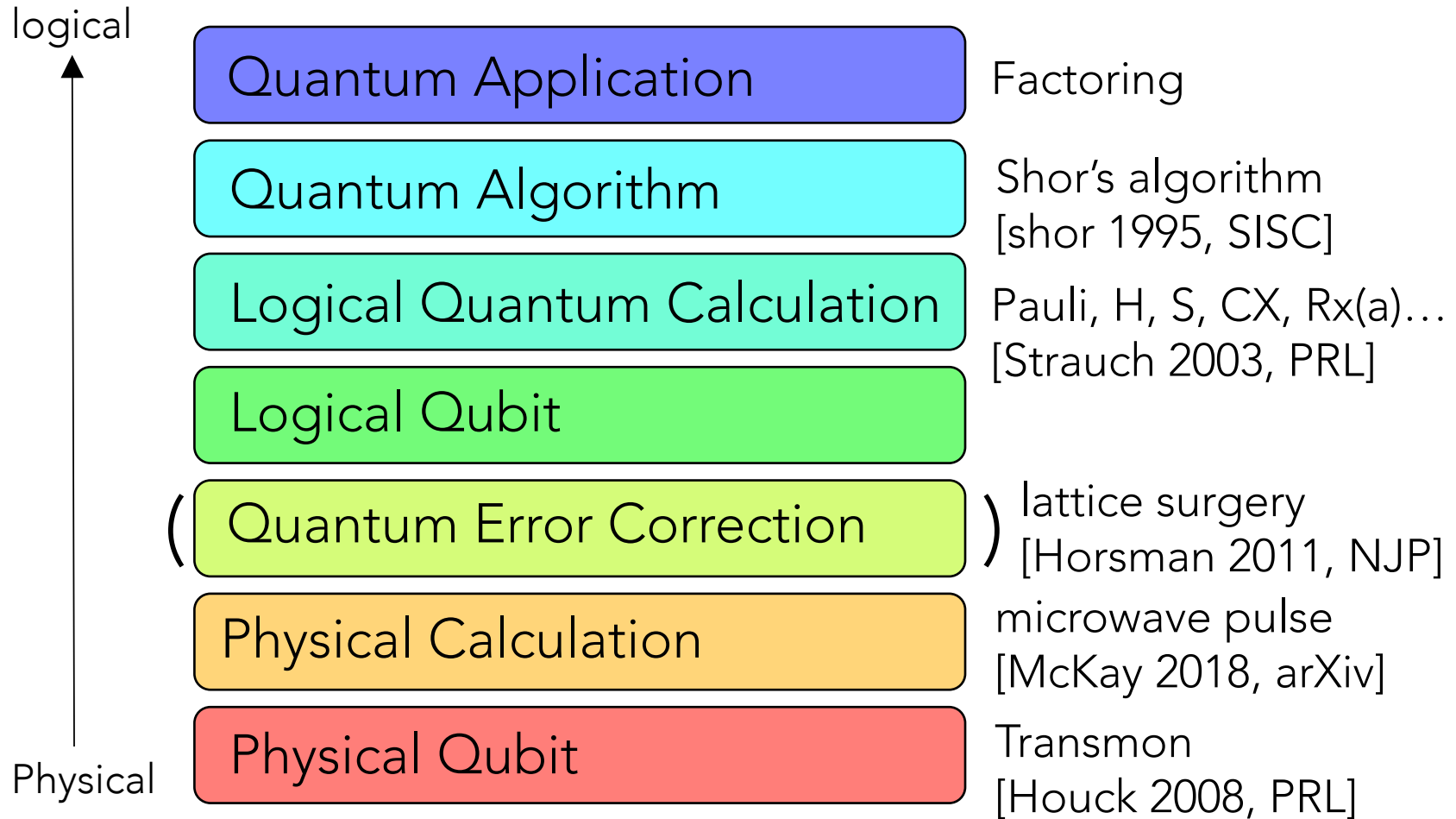
Keio University Quantum Computing Center

Shin Nishio, Yulu Pan,
Takahiko Satoh, Rodney Van Meter



Quantum Computer Architecture

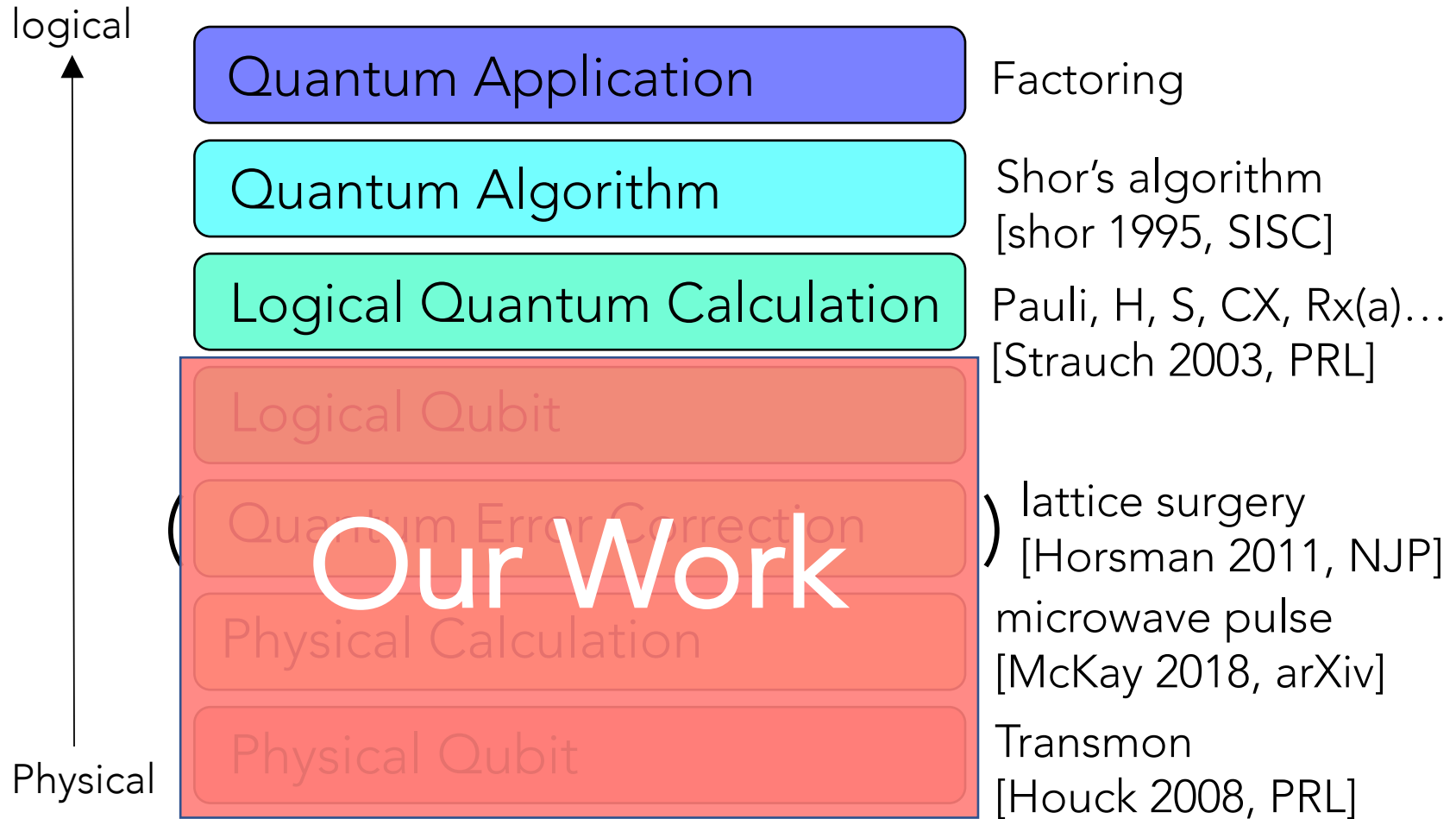
example



Quantum Computer Architecture

Quantum Computer Architecture

example

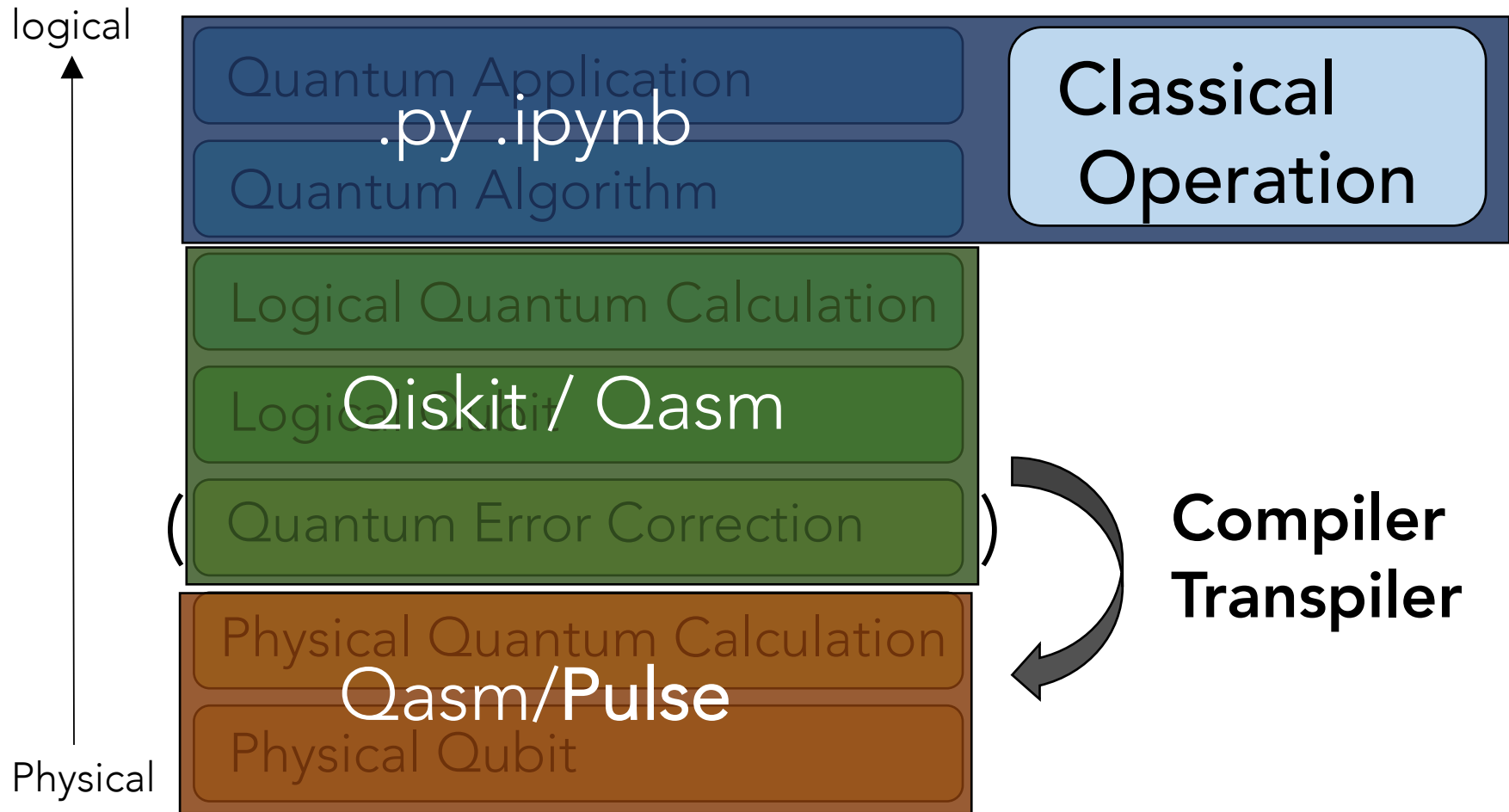


Quantum Computer Architecture

Function of Compilation

- **Optimize Quantum Circuit**
 - gate disassembly & assembly ex) Solovay-Kitaev [Dawson 2005, arXiv]
 - decrease T-Depth
- Quantum Error Correction (post NISQ?)
- Quantum Distributed Computation (post NISQ?)
- Convert logical quantum circuit into physical quantum circuit.
 - **Qubit Mapping**

Existing Architecture (IBMQ Qiskit)



Definition of NISQ

Noisy

- ibmq20_tokyo [IBMQ 2018]
 - Gate error(10^{-3}): 1.83
 - Bi-Qubit Gate error(10^{-2}): 8.06 (IBMQ16)
 - Readout error(10^{-2}): 8.58
- Error rate of each qubit is unequal

Intermediate-Scale

- # of Qubits in a processor: about $10 \sim 10^3$

Definition of problem

Compare analytic simple error model with the reality of the machine.

Enable error aware compilation.

The Story

1. Characterize the machine
2. Create an **estimation of circuit success probability**
3. Compare to the reality of the machine
4. (incorporate into compilation process; **Pan et al.**, later this morning)

Randomized Benchmarking (RB)

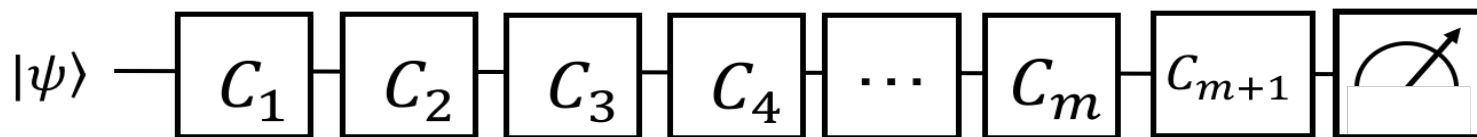
Get $\overline{F^{ave}}$ (Average Gate Set Fidelity)

[Knill 2007, PRA]

- Can be used as a cost function

Clifford gate : $C_n = \{U : UP_nU^\dagger = P_m\}$

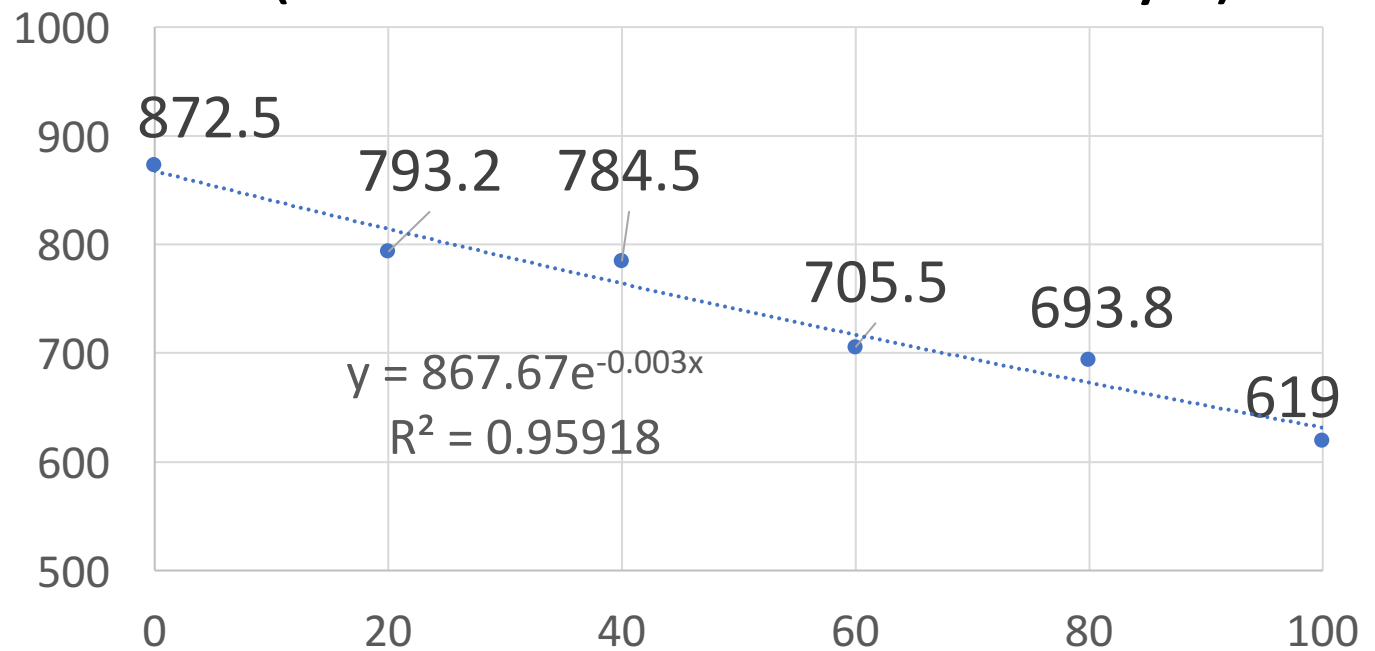
$$C_{m+1} = \left(\prod_{i=1}^m C_i \right)^\dagger$$



RB on IBMQ

Randomized Benchmarking (0th Qubit of IBMQ20 Tokyo)

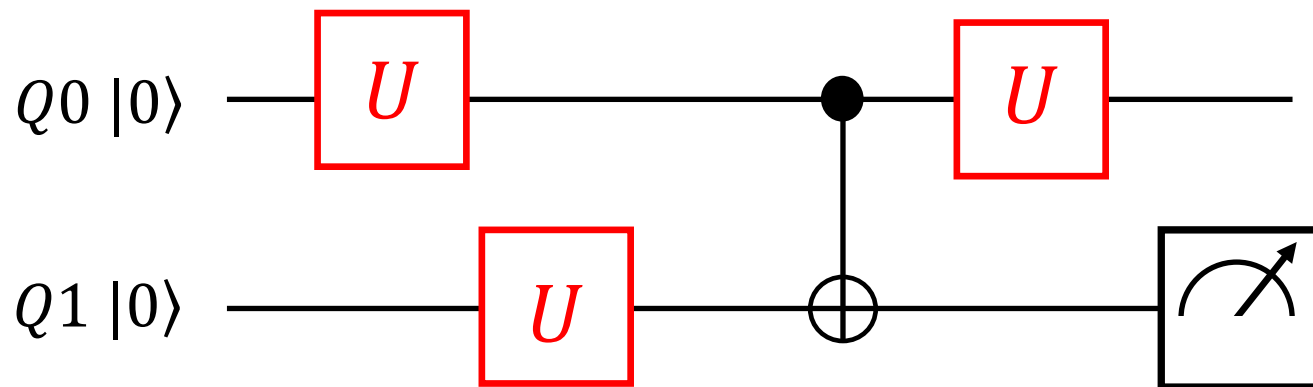
of
Success Shot
/1000shot



of single clifford gates

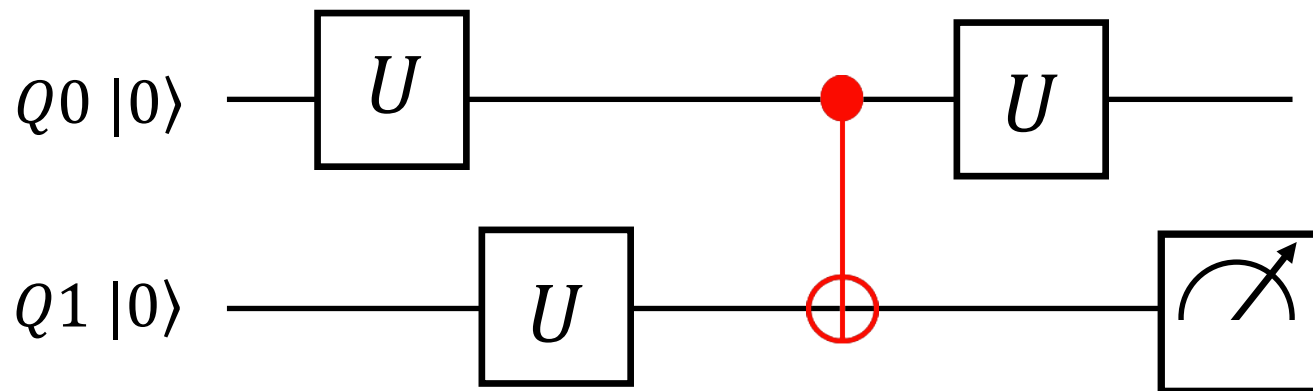
Error model

1. G(single qubit gate error)
2. B(bi-qubit gate error)
3. SPAM(state preparation and measurement)



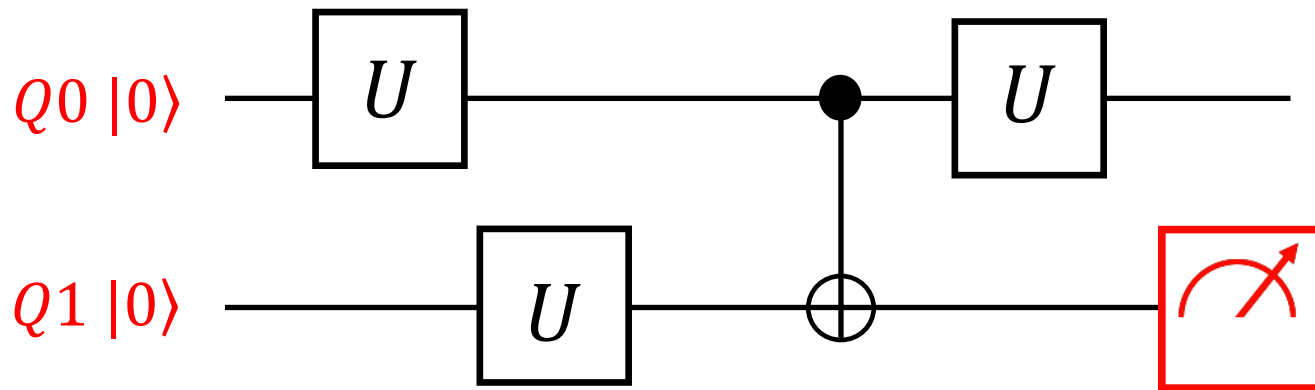
Error model

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Error model

1. G(single qubit gate error)
2. B(bi-qubit gate error)
3. SPAM(state preparation and measurement)



For IBMQ20 $G \ll B < \text{SPAM}$

Success Probability

$$S_{est} = \prod_i (1 - \varepsilon_i)$$

ε_i : the error rates(G, B, SPAM)

S_{act} (*Fidelity*)

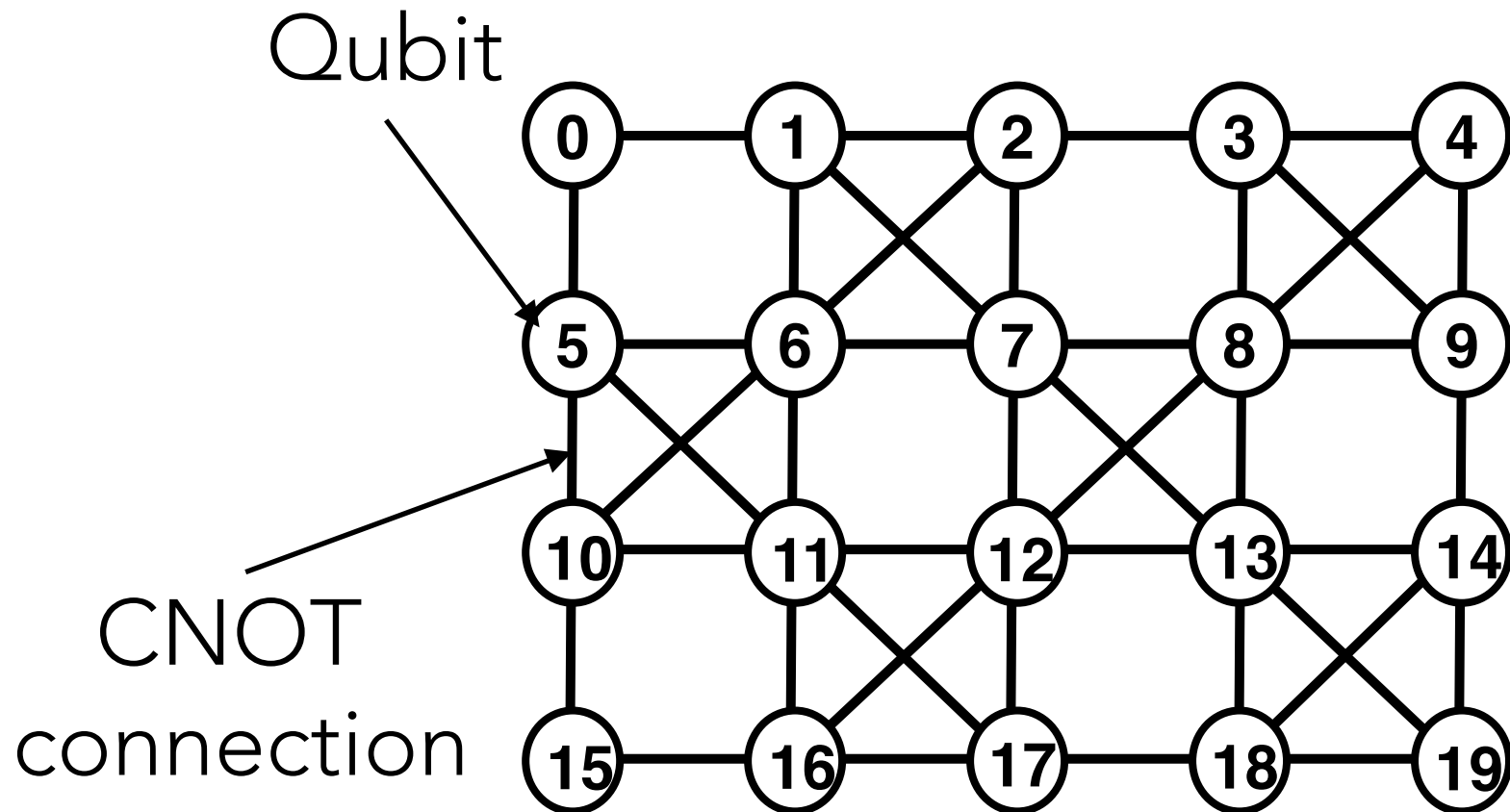
Compare!!



Problem 1 : Path Selection

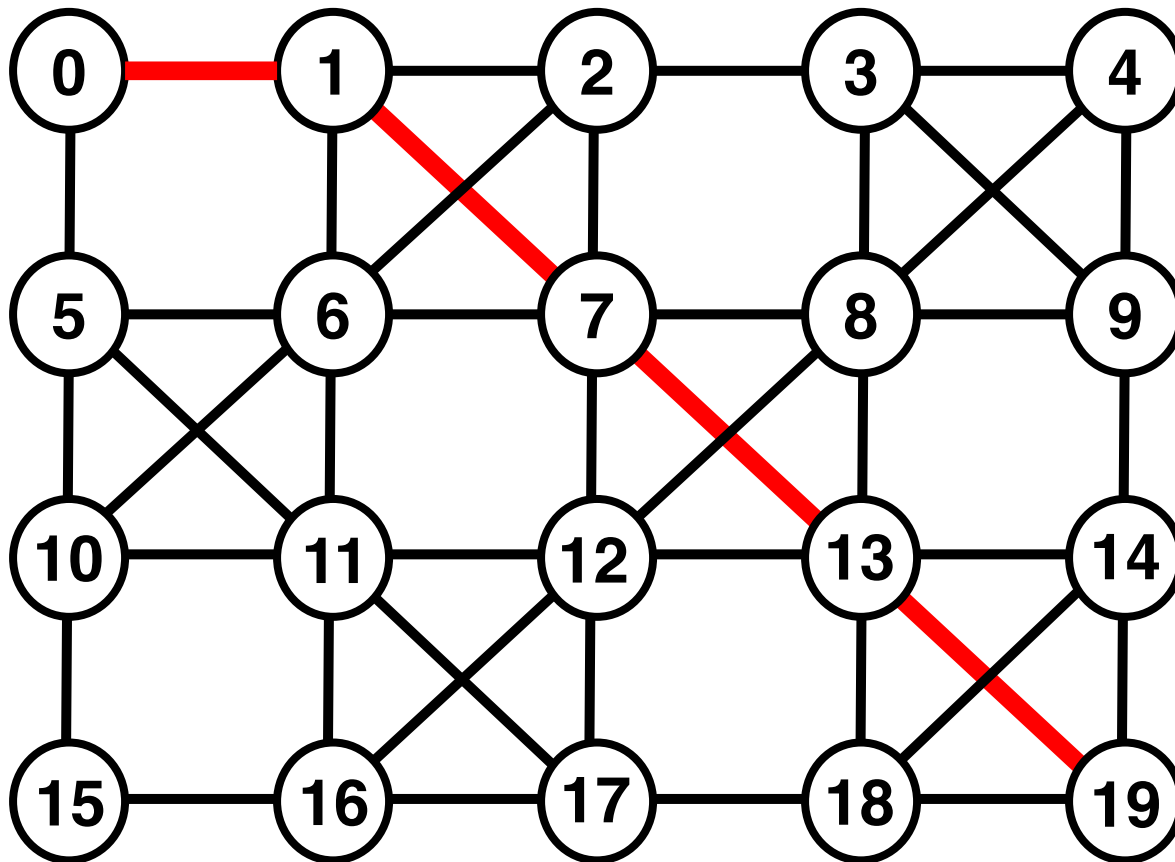
an example of grid architecture

IBMQ20 TOKYO



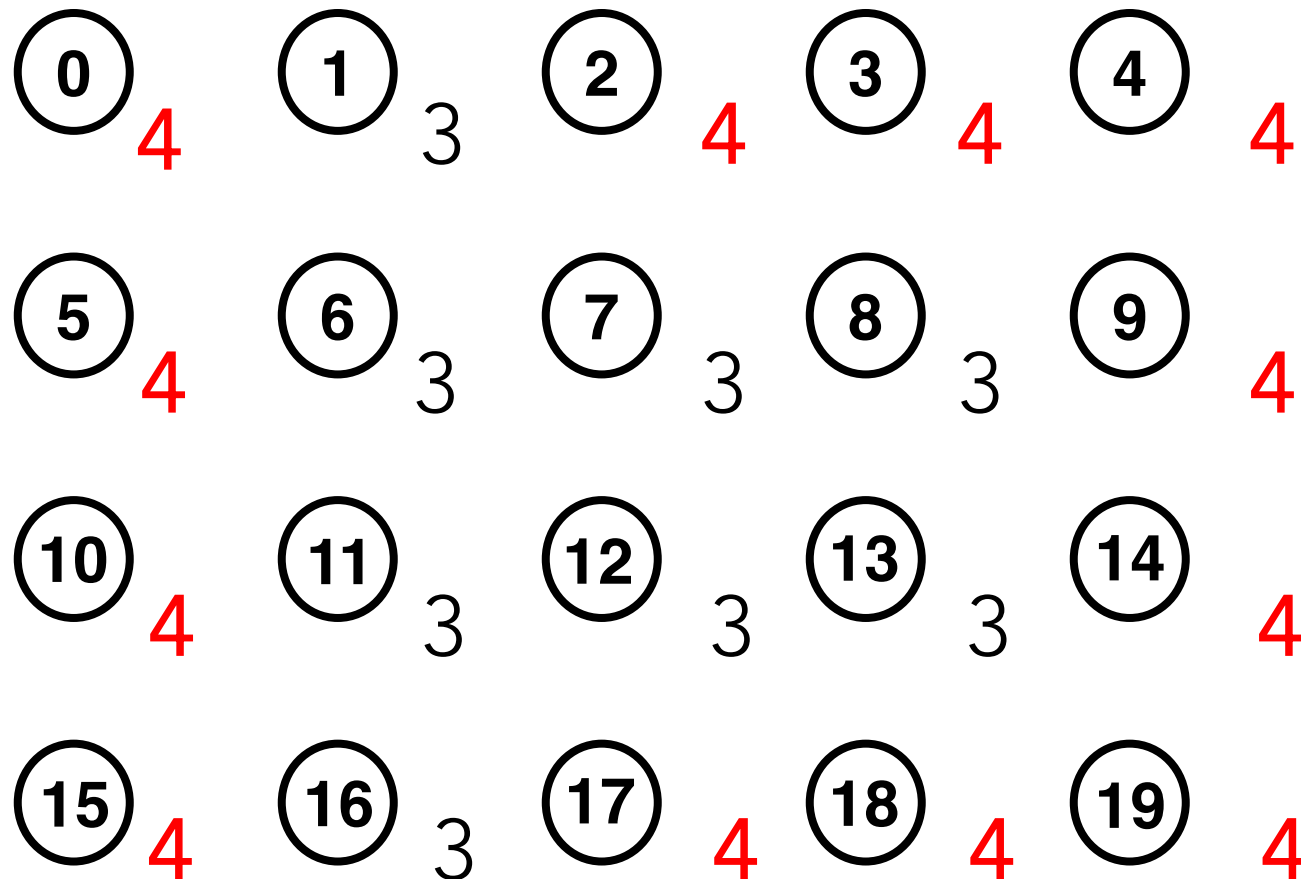
Scale of the Problem

one of the longest “shortest path”
in IBMQ20 TOKYO



Eccentricity

Max distance to another qubit

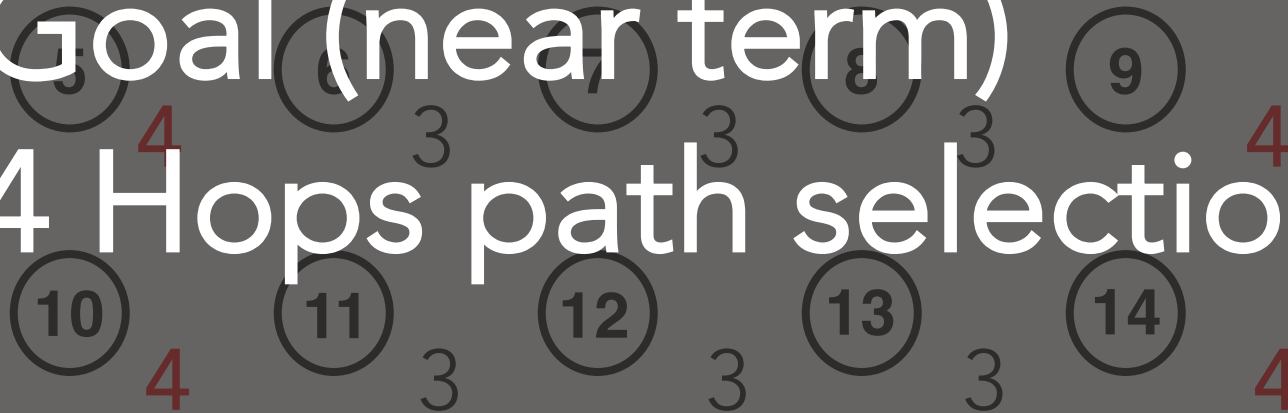


Eccentricity

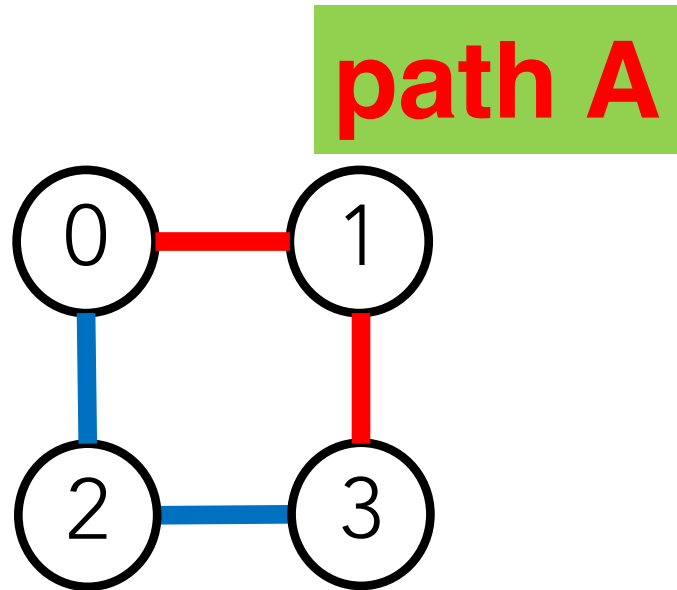
Max distance to another qubit



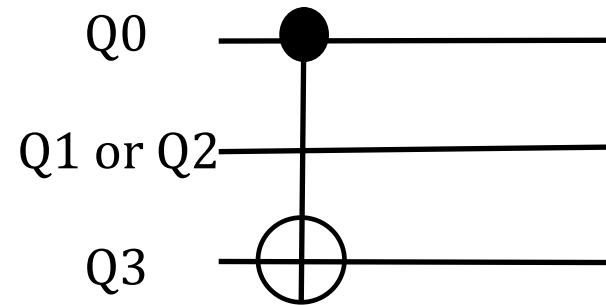
Goal (near term)
4 Hops path selection



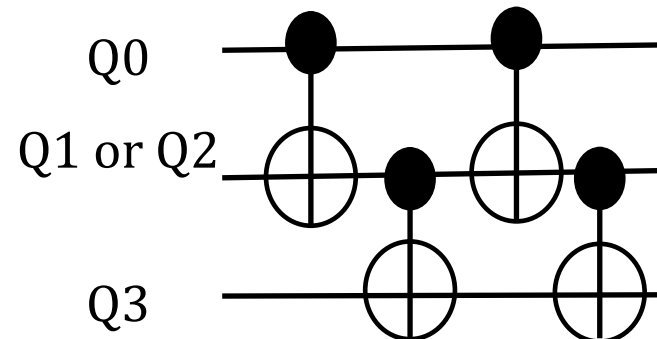
2 Hops Path Selection



Logical Circuit
(written by programmers)



Implementation

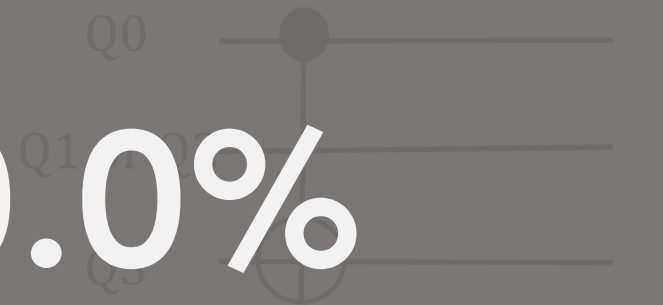
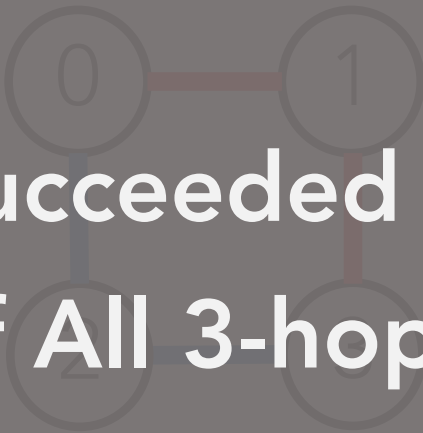


2 Hops Path Selection

Succeeded in **70.0%**
of All 3-hops paths in IBMQ20 Tokyo

Logical Circuit
(written by programmers)

path A

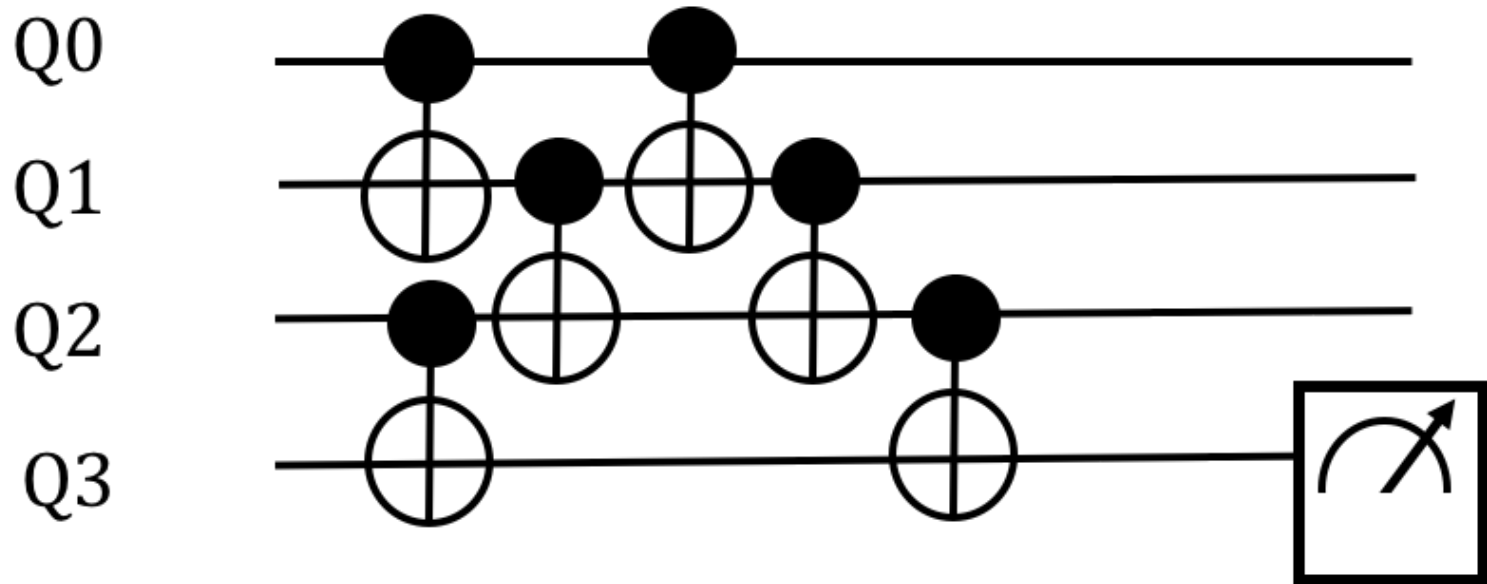


path B



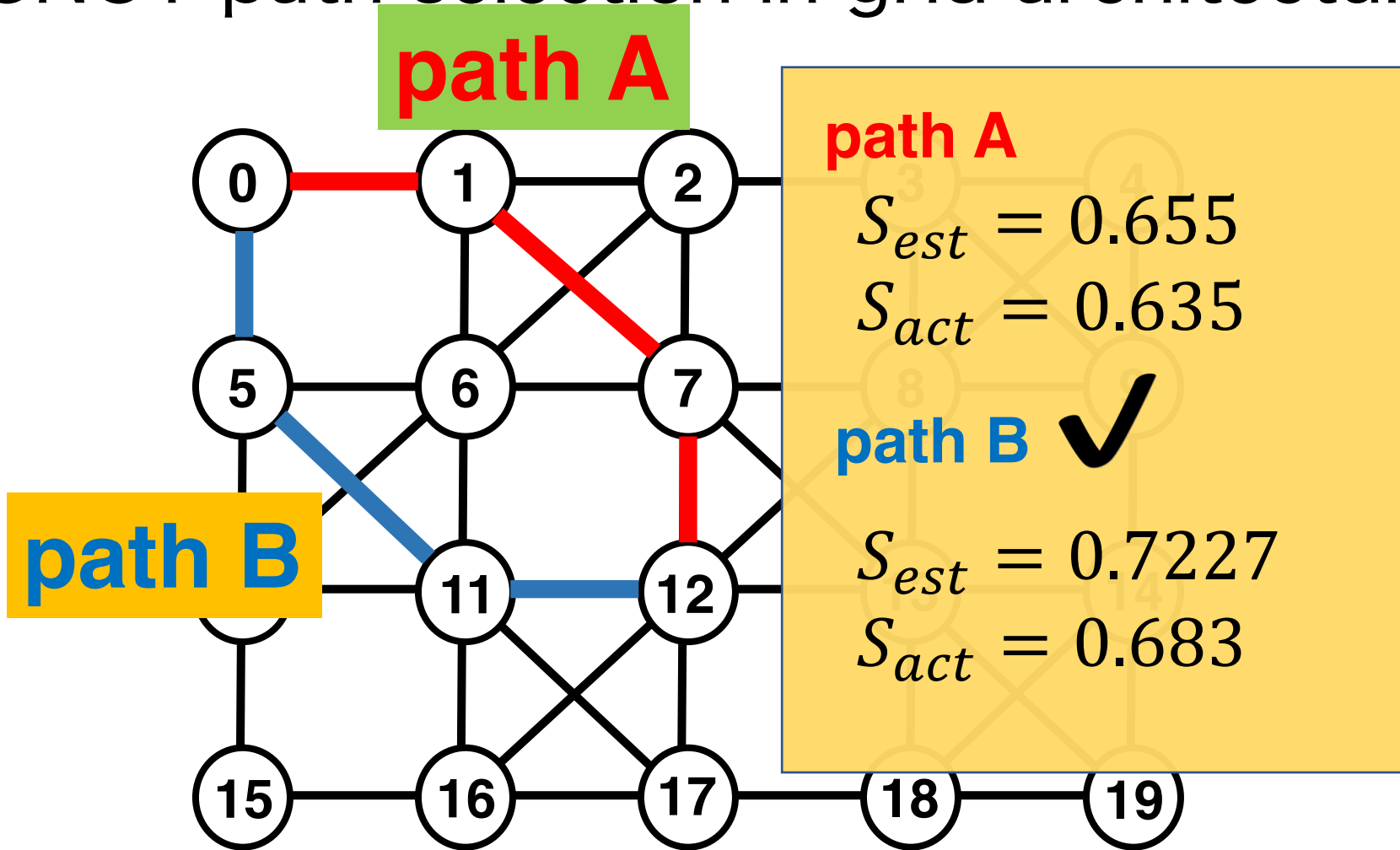
3 Hops Circuit

Circuit for the Benchmarking 3-hops path



3 Hops Circuit

CNOT path selection in grid architecture



3 Hops Path Selection

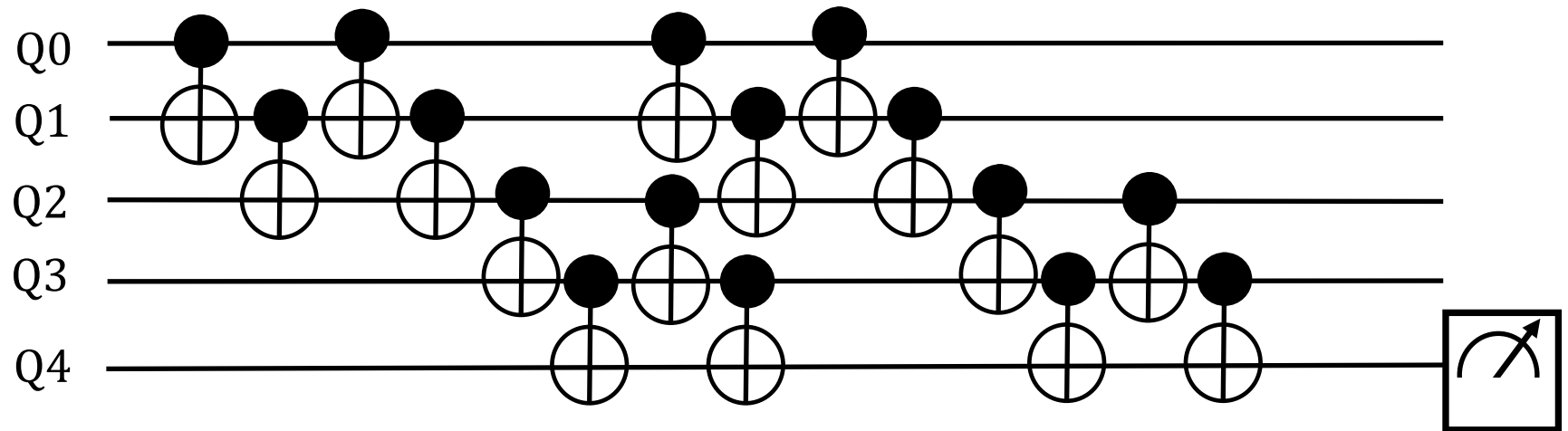
CNOT path selection in grid architecture

Succeeded in **66.6%**
of All 3-hops paths in IBMQ20 Tokyo



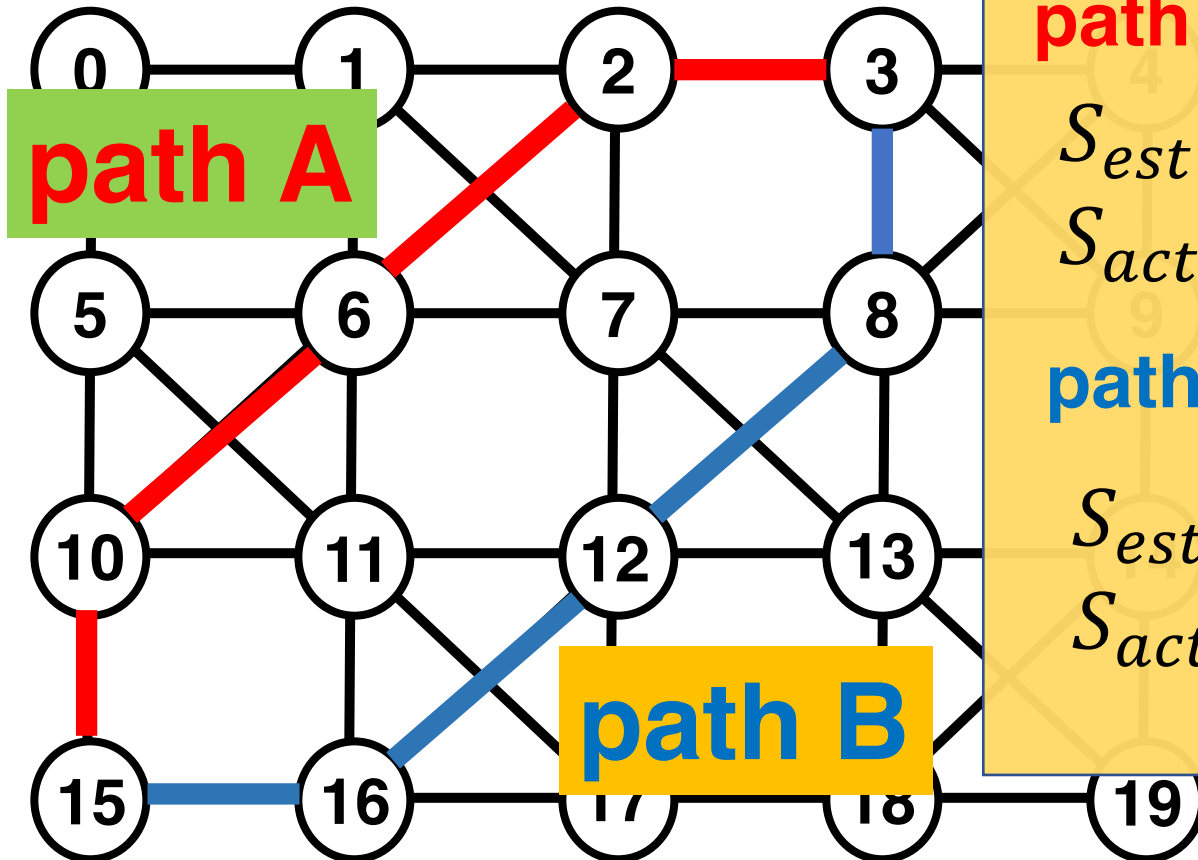
4 Hops Circuit

Circuit for the Benchmarking 4-hops path



4 Hops Path Selection

CNOT path selection in grid architecture



path A ✓

$$S_{est} = 0.5503$$

$$S_{act} = 0.850$$

path B

$$S_{est} = 0.497$$

$$S_{act} = 0.743$$

4 hops path

CNOT path selection in grid architecture



Succeeded in **62.5%**
of All 4-hops paths in IBMQ20 Tokyo

path A ✓

$$S_{est} = 0.5503$$

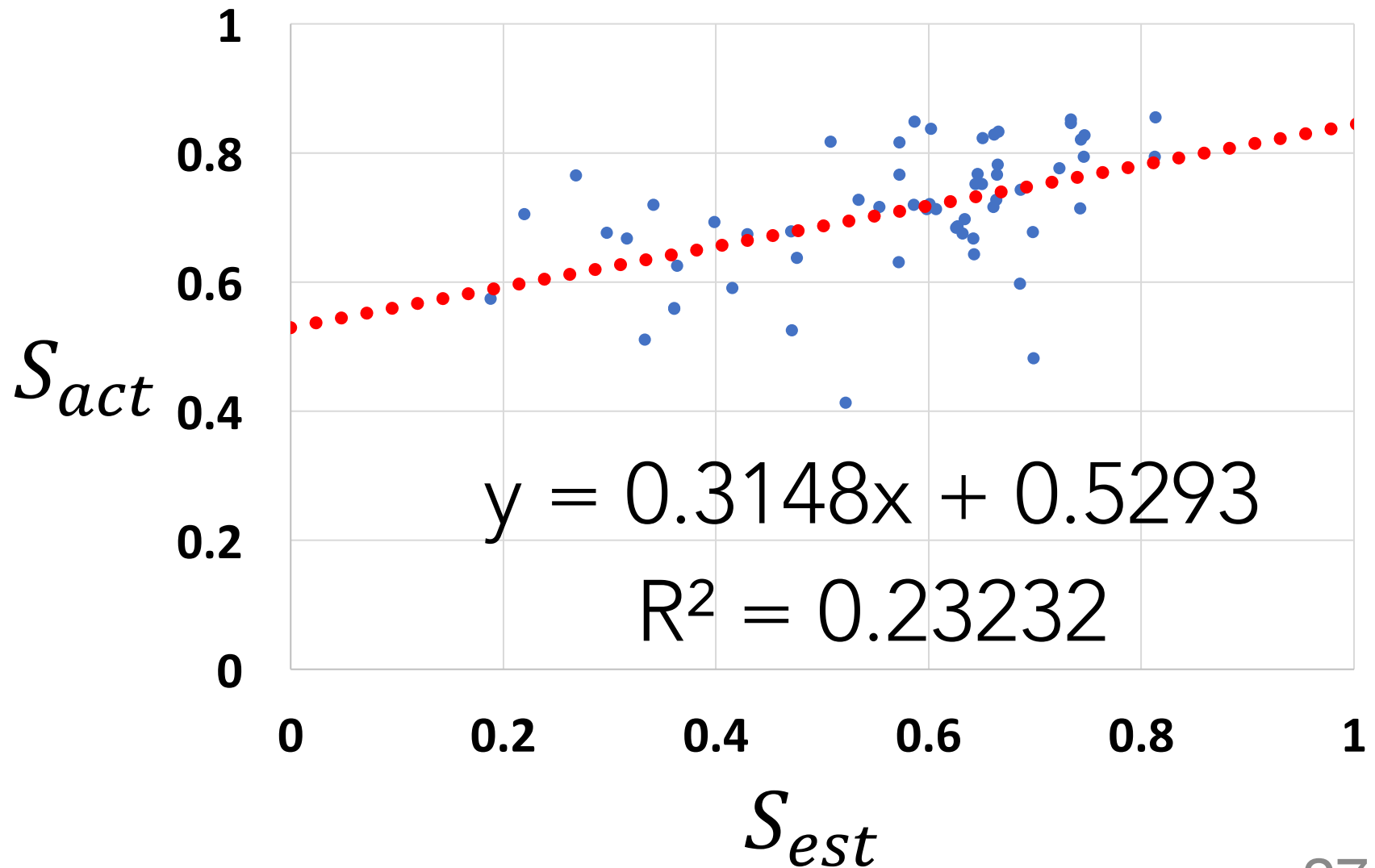
$$S_{act} = 0.850$$

path B

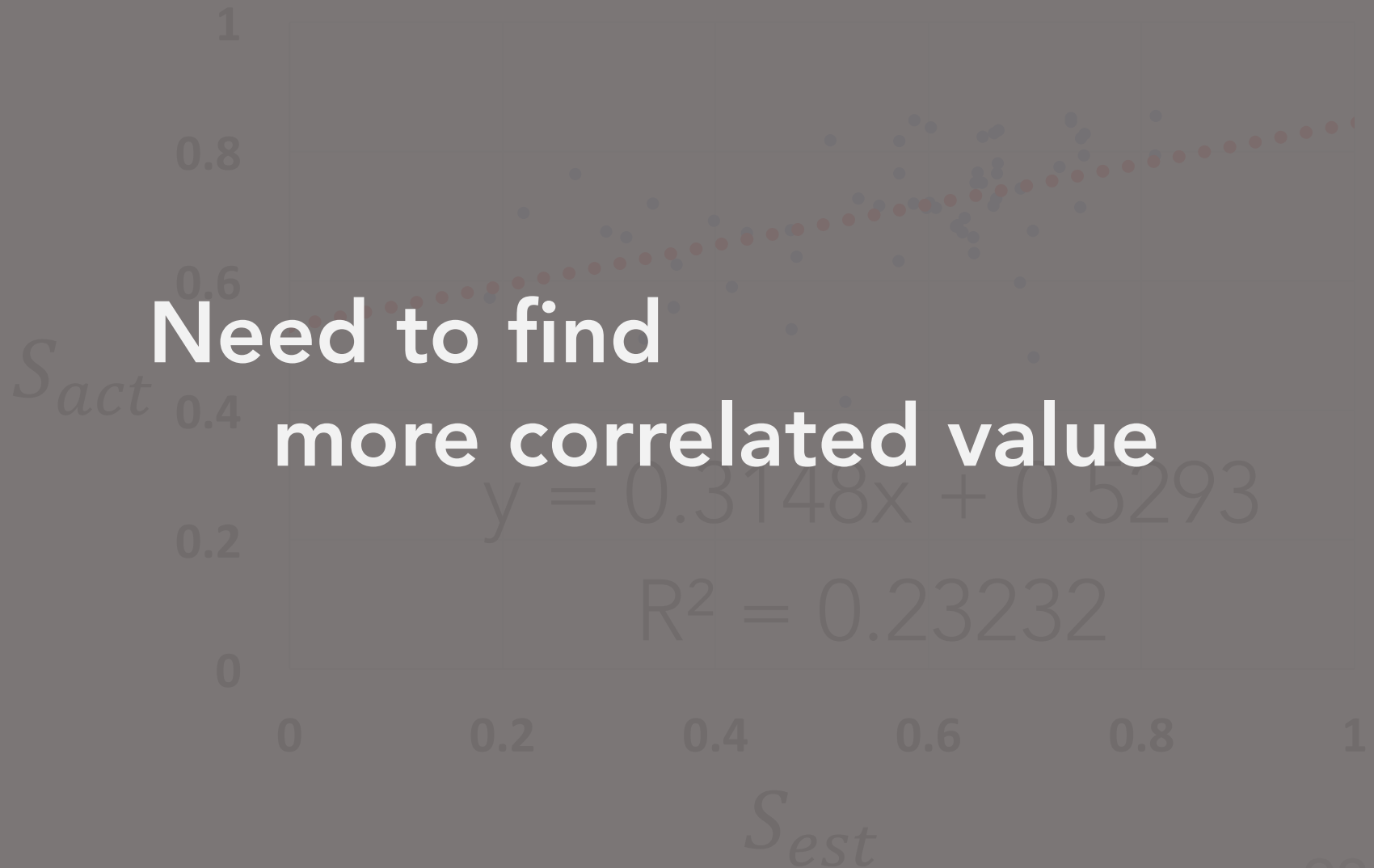
$$S_{est} = 0.497$$

$$S_{act} = 0.743$$

Correlation Between s_{est} and s_{act}

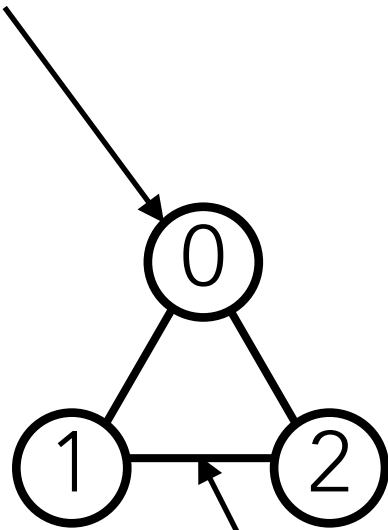


Correlation Between S_{est} and S_{act}

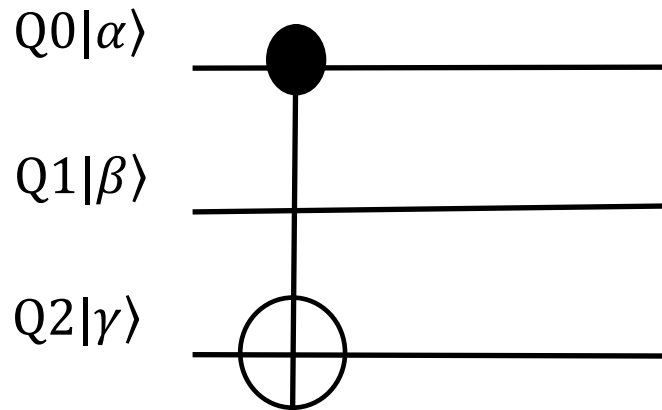


Problem2 : Three body Problem

Qubit



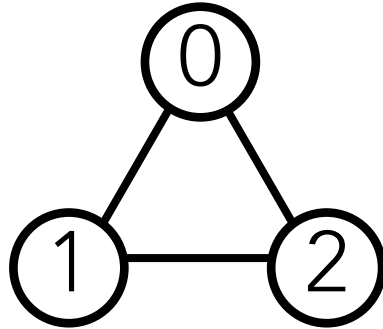
Circuit A



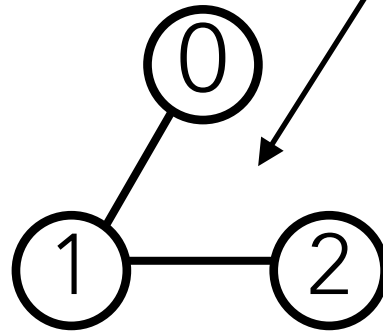
CNOT connection

Equivalent Circuits for Circuit A

ideal



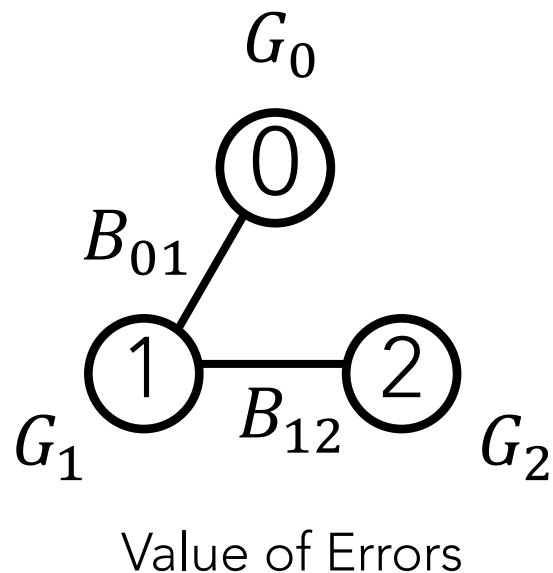
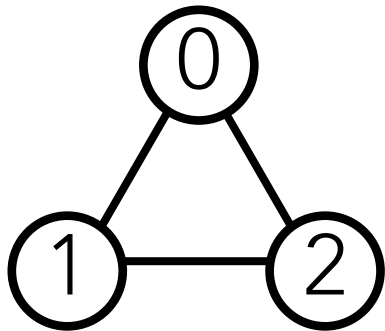
real



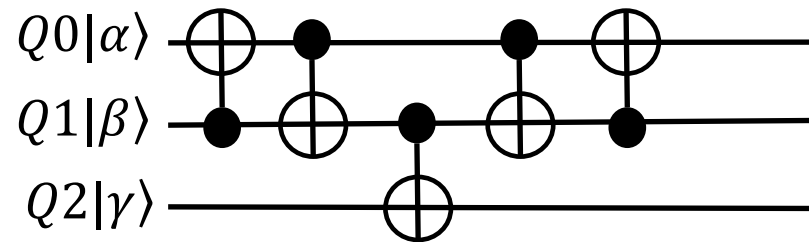
NO CNOT connection



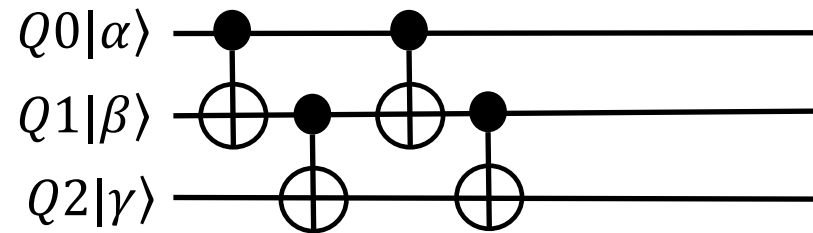
Equivalent Circuits for Circuit A



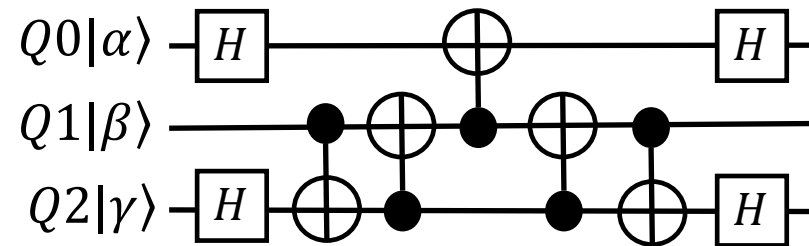
Circuit B



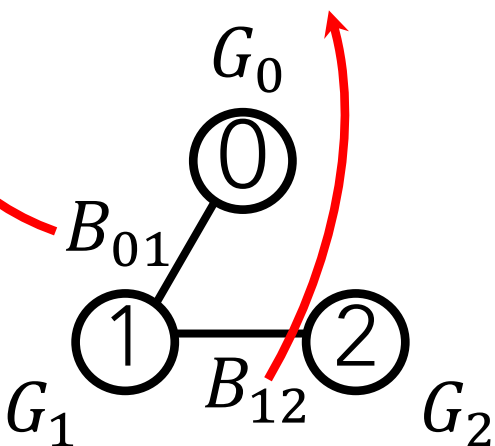
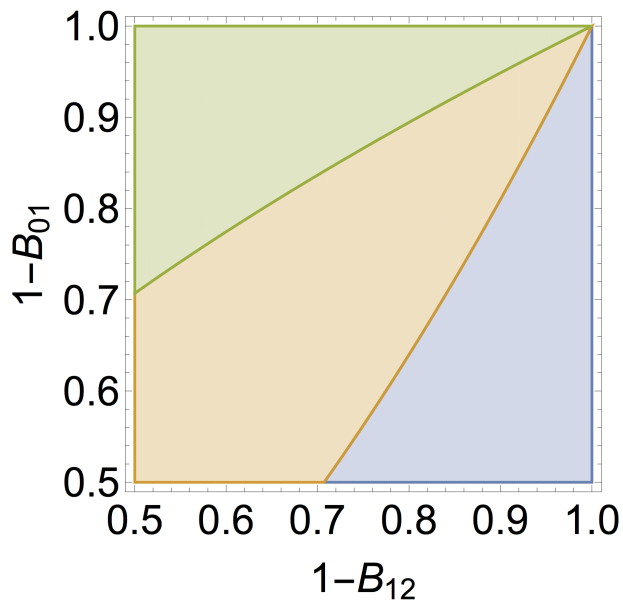
Circuit C



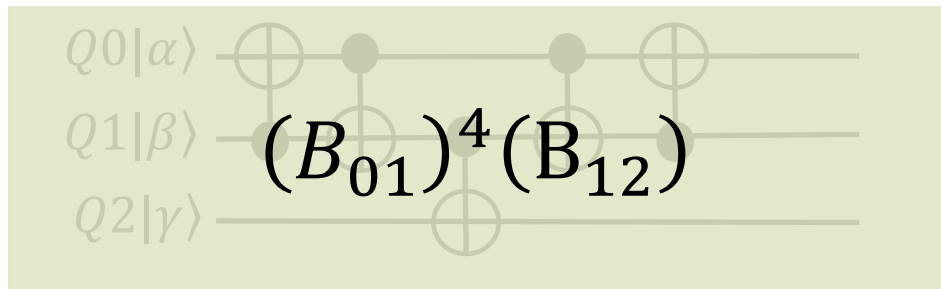
Circuit D



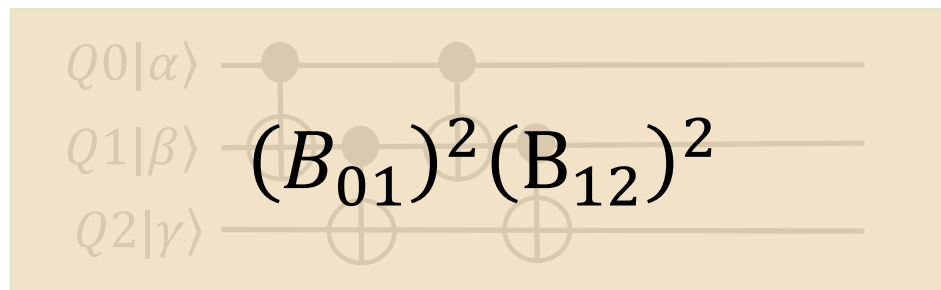
Error of each circuits



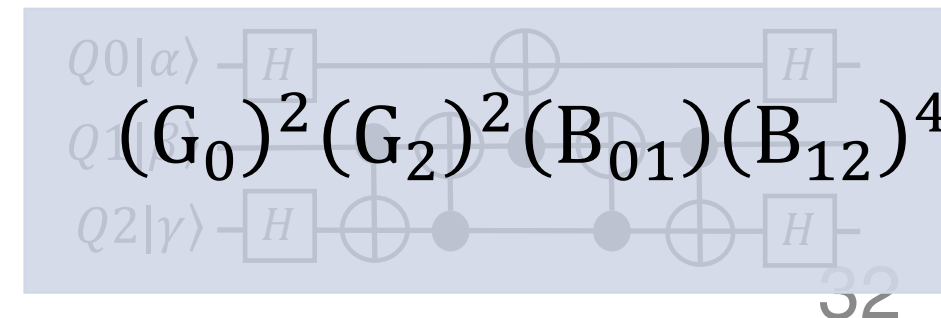
Circuit B



Circuit C

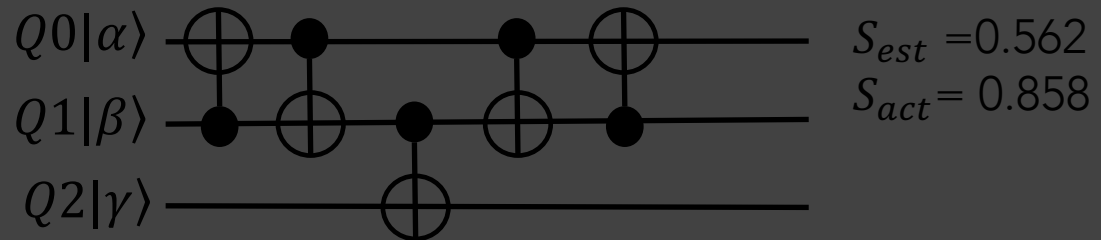


Circuit D



Three body problem

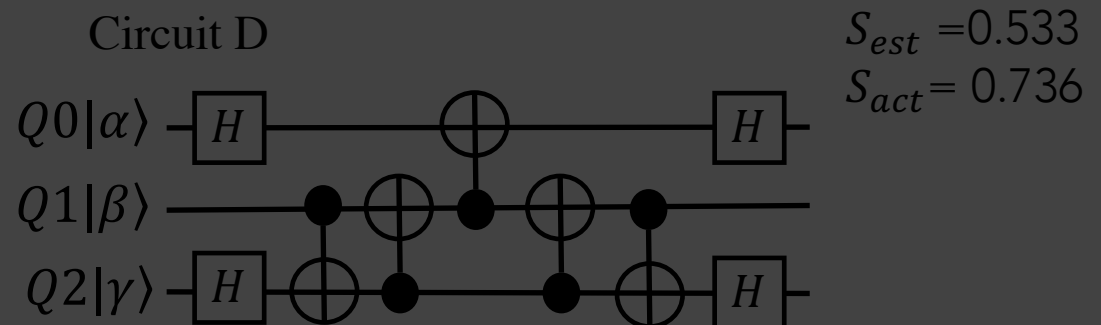
Circuit B



Circuit C



Circuit D



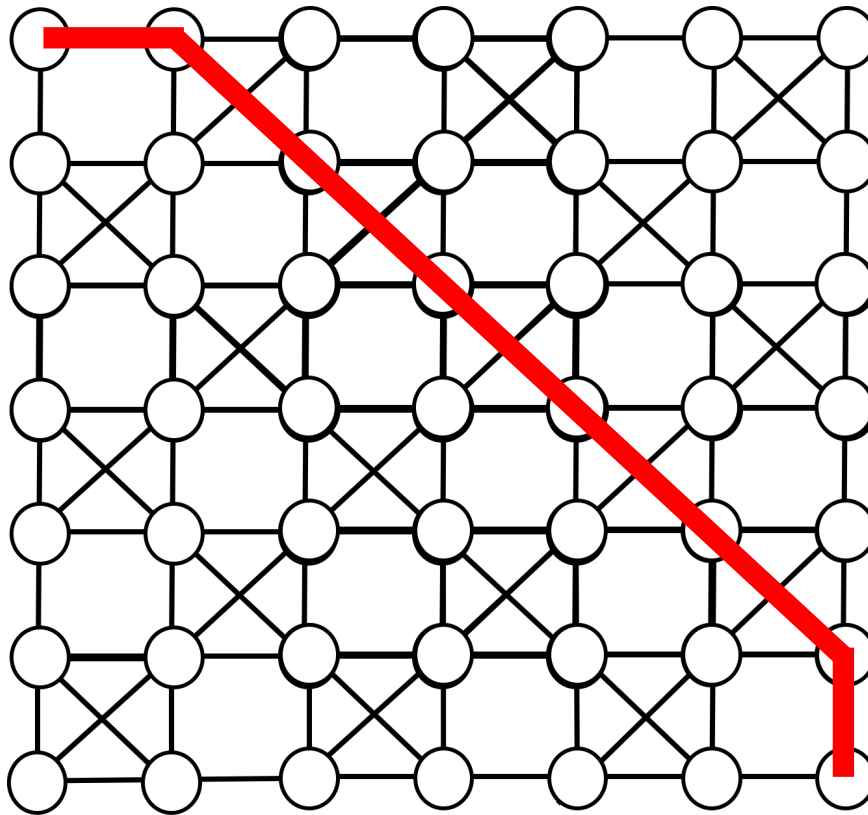
Succeeded in **40.0%**
of All 3-hops paths in IBMQ20 Tokyo

数式を入力します。

Conclusion

- S_{est} is useful for 2-4 hops path selection.
- Using single parameter (e.g. output of RB) is not good enough to estimate long CNOT path S_{est} of quantum circuit.
- We need more sophisticated error model.

Future work



7 hops path?

near 50 qubit device?

Future work

Use Other Error Model

- more physical
 - T1, T2 & time for execute gate
 - leakage
 - crosstalk
- Divide
 - Decoherence
 - Dephasing
 - Unitary

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Thanks for Listening !