Distributed Battery Management System (BMS) Design, Optimisation, and System Integration for an Electric Solar Vehicle

Research Paper - Final Year Research Project (ENG40001)

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***Abstract*—This paper proposes a battery management system that integrates an active balancing system in order to extend the lifetime time of an electric vehicle and minimise wasted energy. The system makes use of a central gateway that functions as the master, and a user configurable number of measurement taps in multiples of 12. Whilst there are many automotive grade BMS units available, very few include an active balancing system, it is the goal of this project to create a template for one that optimises cost, physical space requirements, complexity, performance, and safety. The design context for this system is for the purposes of an SPEV (Solar Powered Electric Vehicle) intended for entry into the World Solar Challenge, however the technology is not limited to this application. Being able to maximise the amount of energy that is wasted is especially beneficial - as current generation EV battery systems age, the delta between the highest and lowest cells will increase, and being able to quickly balance out the issue on the go will prove to be a groundbreaking leap in technology.**

***Index Terms*—SPEV, EV, BMS, Lithium Ion, Lithium Titanate, Electric Vehicles**

I. Introduction

A Battery Management System (BMS) is one of the most important components of a lithium powered electric vehicle. They function to ensure the safety of the pack, preventing dangerous under/over-voltage conditions, preventing component damage and hazardous fail modes. As lithium batteries degrade, their electrical properties change and will charge and discharge at different rates.

The difference between the highest and lowest cell voltage is termed the pack delta, and the aim of balancing is to reduce it as much as possible, typically within the range of tens of milivolts. Battery packs that do not balance contain excess energy that cannot be discharged because if so, the minimum cell voltage will be exceeded [1]. Likewise, the same is true of charging, if the maximum cell voltage will be exceeded, then charging must cease.

The most common method of cell balancing is passive balancing, where the energy from the highest cell is discharged as heat. This practice is inherently wasteful and if the BMS is stored within the accumulator, this also serves as an unwanted source of heat for the pack, wearing the cells out further. Another issue of this strategy is that one is still limited by the lowest cell voltage - all cells are bled down to the lowest cell voltage, a poorly performing cell cannot have energy put into it. Passive balancing is slow, and slower if the thermal limits are exceeded.

Active balancing differs from passive balancing in that is is able to redistribute energy about the pack; higher cells are able to charge lower cells. This process reduces wasted energy and heat in the accumulator. In the case where there is a cell with poor health, it is then possible to siphon energy from this highest cell to extended the life of the pack.

II. Background

The Swinburne Solar Team vehicle at present makes use of repurposed Lthium Titanate (LTO) cells acquired in 2018. Lithium Titanate cells have

a nominal cell voltage of 2.3V, well below the minimal cell voltage supported by most commercially available BMS units. Furthermore, these cells are from several different sources; they discharge at vastly different rates. Whilst the project would likely transition to LFP (Lithium Iron Phosphate) based cells at a later stage, in the pre-competition phase of the project, budgetary constraints are an ongoing issue; it is likely that large cell deltas will prove to be an issue for some years to come.

Cell measurement is not the only challenge in the scope of this design. The changing landscape of solar technology also provides quite a few issues for how to structure an architecture suitable for an extremely wide voltage range. At the moment, the most prevalent flexible cells have a low open cell voltage, around 5.6V [2]; these being connected in series to maximise their voltage output. The most successful cruiser class vehicles in the competition are medium voltage, around 90V to 220V. As this technology improves, it is likely that the voltage will increase rather than decrease to reduce mass [3], and as such, it is necessary to accommodate higher voltages, possibly as high as 400V or 800V. At this voltage, it is unlikely that LTO (Lithium Titanate) cells could be used, as the low nominal cell voltage would mean at least 285 cells would be required in series for 800V, with parallel units required for the extra current carrying and energy. It should be noted that LTO cells do typically support a higher cell current before experiencing failure, however it is unlikely this would not compensate for the extra capacity requirements.

A. Project Goals, Scope, and Research Questions

With this context in mind, the following goals were set to guide the design of the system:

- Cell voltage range of at least 0.8V to 4.5V to meet the requirements of most lithium chemistries.
- Accommodate a total pack voltage of up to 600V.
- There should be no unpopulated cell measurement taps; with fewer cells the BMS should be reduced in size.
- Able to manage cells in poor health as efficiently as possible; the reduction of energy waste in balancing.

With so few automotive grade BMS units offering active balancing, this project addresses the gap in research into the feasibility and practicalities of including an active cell balancing system. The primary questions are as follows:

- Is the amount of space required to include an active balancer suitable in such a weight optimised vehicle.
- Is it possible balance the vehicle on the go to extend the life of vehicle.
- How would one approach the design of such a BMS system, and ensure it meets ISO26262 requirements.
- What efficiency gains can this system provide over typical passive-only solution on the market currently?

III. Methodology

A. State of Charge Estimations

After initial research of existing ways to estimate state of charge early on in the project, it was decided to use a combination of cell voltage readings and coulomb counting [4].

Further research into the cell chemistry available to use for this project (LTO) demonstrated potential challenges with voltage-level based estimations. An LTO discharge graph shown in Figure 1. While the non-linearity is not of direct concern (creating a map of voltages to correspond to charge levels would be trivial), it does result in a large portion of the cell's discharge cycle occurring over a relatively small voltage delta. This itself can be mostly accounted for but the additional presence of voltage sag complicates this characteristic. A cell experiencing a high current draw that starts to lessen whilst in a shallow-sloped region of its discharge curve could read approximately the same voltage level for 10-20% of the cell's capacity. Accounting for voltage sag could be done formulaically by establishing a mathematical relationship between the amount of voltage sag occurring at a given capacity level and the amount of current being drawn through that cell [5]. Even accounting for voltage sag, using only instantaneous measurement based estimation will result in SoC readings fluctuating in a dynamic charging/discharging environment. Accurately accounting for voltage sag while current draw changes constantly is a much more difficult task.

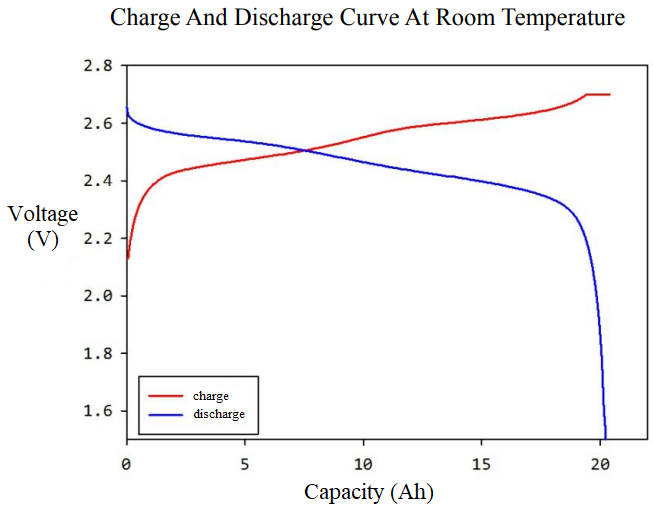

Fig. 1: Discharge graph of an LTO cell. Note the low cell voltage range. Sorce: data sheet for 16Ah LTO cells in use by the Swinburne Solar Team [6].

Coulomb counting can be achieved by attaching a current clamp to the output, measuring the instantaneous power discharged overtime, and integrating this to find how much energy has been consumed and compare to the pack's theoretical capacity. Coulomb counting can provide a stable SoC estimation over time, reading cell voltage and current draw multiple times a second and extrapolating energy used. Coulomb counting will result in far more meaningful SoC readouts during periods of high/fluctuating current draw. A drawback of this method is that it can drift over time, due to not being able to account for energy wasted as heat and a lack of absolute reference. In nautical terms, this method is analogous to dead reckoning.

With these two estimations of the packs health, a weighting can be applied to the validity of each estimation. With high current discharge, the effect of voltage sag can be mitigated by relating current discharge to the weighting of the coulomb counting method; During periods of high current draw the coulomb counting estimation will be weighted more.

After this methodology has been implemented in the BMS a formula will have been developed to represent stage of charge.

B. Modular Stack Design

In order to achieve the target of space optimisation, a distributed architecture was pursued to provide scalable device size across different battery configurations. This architecture abstracts away the functionality of the BMS chips, making it simpler to change out modules, iterate designs, and refine the project further.

A similar modular architecture is explored by Henar Cailang, Caliway, and Wanson, for a small form BMS for use in a Motorbike, using a master-slave system [7]. Similarly, the BMS concept of this project is to be designed is broken up into the same style of system, with a Central Management Unit (CMU) as the gateway that oversees many Local Measurement Units (LMU), which each attend to a particular group of cells. The main disadvantage of this scheme is that fault detection becomes inefficient, as communication becomes reliant on persistent updates between units, requiring a watchdog, and whilst the absence of a module may not mean a fault, one shall be triggered, and little more information can be gained [7].

C. Cell Measurement, Active vs. Passive Balancing, and ASICs

Passive balancing is conceptually quite simple; Whilst a battery is charging, the highest cell is discharged to match the lowest cell, and this process repeats until all are within a certain delta. This is achieved by simply discharging energy from the cell as heat, light, or kinetic energy, etc.

Active balance utilises the excess energy from the highest cell to charge the lowest cell. In this way, energy has been redistributed, not lost, thus minimising wasted energy. This is usually achieved with some form of coupling, to connect the highest to the lowest cell, and using that to equalise the two cells. This is usually done by isolating both cells from the stack, and connecting them in parallel, with circuitry that allows the control of current flowing between the cells to prevent large loads causing degradation for both cells involved. In addition to gains in energy conservation this method can also achieve more than double the effective rate of balancing, since the two most outlying cells are being equalised to an average cell voltage simultaneously,

rather than one cell being discharged all the way down to the lowest cell voltage at a time.

In order to simplify the complexity and overall size of the final output, it was decided very early into the project, that a pre-designed BMS IC would be used. These ASICs typically integrate various forms of cell measurement to autonomously perform balancing with little external input required. Two ICs were sought to solve this issue, based on research from an earlier literature review [4], the LTC6811, and the LTC3300. These two BMS ICs are designed to work together to achieve the passive and active balancing requirements outlined for this project [8].

IV. Discussion

Given cost and time restraints, the project was reduced in scope from it's original plans such that a only the LMU would be designed, and a single functional LMU be produced to serve as a proof of concept. The LMU is the most important part of this project, representing the most complex amount of circuitry and the largest portion of functionality (for both hardware and software). The CMU's functionality can be containerised in software; it can be simply a CANBUS gateway with some high side drivers to run the contactors, and simulating its functionality would be relatively trivial.

A. Active Balance Circuit Design

The active and passive circuits follow the design recommendations outlined by the manufacturer of the ASICs [9] [8], The passive circuit makes use of a small P-Channel FET that is able to handle around 100-500mA, and a small resistor. A LED circuit has been added to indicate which cells are balancing. The active balance circuit requires two high current switching FETs, with the secondary of each transformer being connected to a common charge rail(denoted as BOOST in the schematic). To help decrease the BOM, a dual channel N-FET with a low R_{DS}, and low gate capacitance was used. These FETs will switch at a frequency of 2kHz, with a typical charge current of 2-4A. The way in which this circuit operates, is that the primary side of the highest voltage cell's module will be coupled onto the secondary side. At the same time, the lowest cell's primary coil will be switched at high speed to enable current flow. The LTC3300 manages this control loop, and a small measurement tap is attached to a shunt resistor connected to the drain of each FET, closing the control loop and providing the required hysteresis. The port on the right extends to the active and passive cell measurement inputs, and makes use of a simple RC filter to the adjacent cell (Cell measurements are differential), and the ground reference.

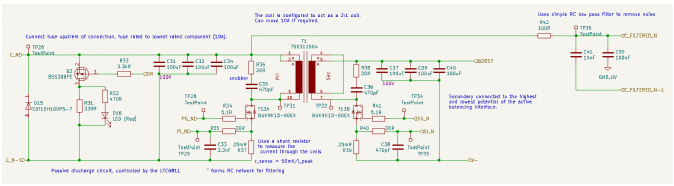

Fig. 2: The circuit used on each cell input, the left part includes reverse protection diode, and the passive balance circuit, a small SOT23 P-Channel FET, and a 330Ω resistor. The right half includes an isolated 2:1 10A transformer and N-Channel FETs with a connection to the boost rail.

B. PCB Design

The PCB for the LMU is significantly larger than original concepts for the design earlier in the project. The original idea was to create a daughterboard with a SODIMM form factor that would hold either 2(single-sided) or 4(double-sided) active balancing modules, that would connect to a backplane that would attach directly to the terminals of the cells [4]. in this way, should the active system be too large, modules could simply be removed.

C. Isolation, Safety, and Grounding

Grounds serve two main purposes, for protecting the integrity of signals, and protecting systems and users in case of a fault [10]. In the vehicle, an IMD (Isolation Monitoring Device) is used to ensure that no more than 2mA is able to pass from the high voltage system into the vehicles system. A device such as the ISOMETER IR155-3204 will be connected with the ability to break power to the main accumulators on fault [11]. This protects against the mechanical failure of various parts of the powertrain, where contact is made when insulation

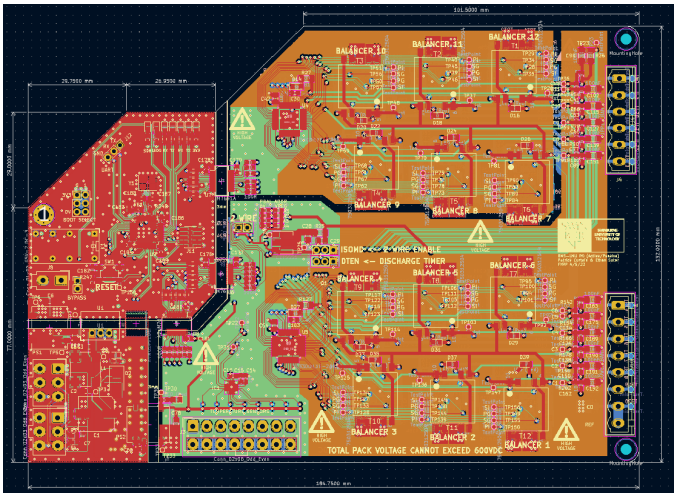

Fig. 3: The PCB designed to perform the functions described by the LMU.

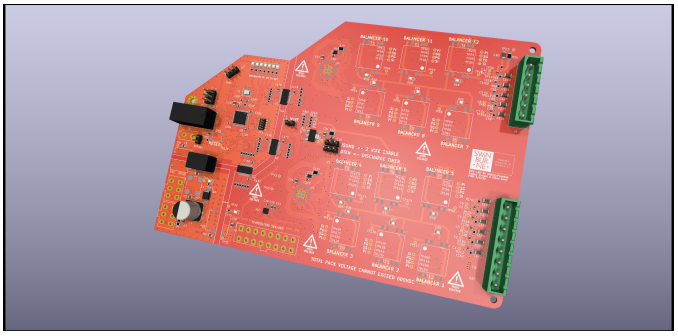

Fig. 4: Rendering of the top side of the LMU PCB.

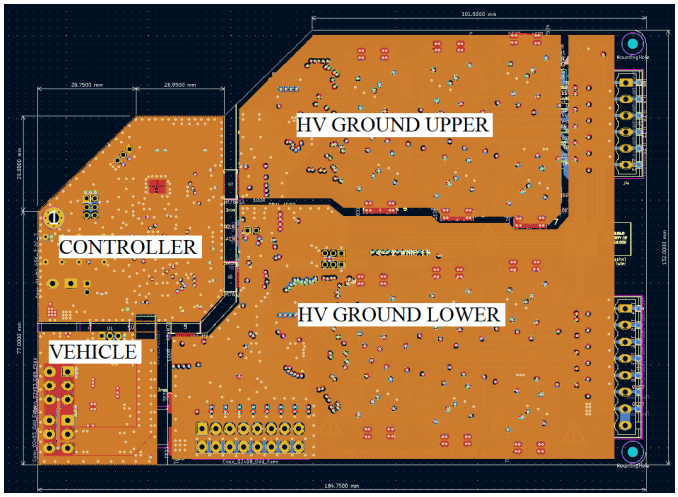

Fig. 5: The different ground planes used to break up the PCB. Note that each of these zones is galvanically isolated except for HV ground upper and lower, explained in Section IV-D.

is not present or has fatigued, as well as the electrical failure of the various ICs and DC-DC converters that are used to isolate the barrier.

Of great concern in the development of this BMS was its ability to handle high voltages. A safety isolation barrier of 3mm has been included to allow the device to meet the IPC2221B high voltage clearance requirements [12].

In order to simplify the architecture and avoid being locked into using Linear Technology's proprietary interpretation of SPI, isoSPI, a simple series of simple high speed digital isolators is to be use. The primary advantage of this scheme is that inter stack connections do not need to be adjacent since the communication interface is connected to the same ground as the vehicle. As such, the pack can be split across the vehicle without much additional wiring.

There is some danger associated with extending the ground planes used for high voltage. A large plane is a huge physical target and risks the operator or assembler making contact with the high voltage plane. Of course, during assembly, high voltage gloves must always be warn and ample warnings are listed on both sides of the board, however additionally, these planes have been restricted to the internal layers of the PCB. Therefore the risk is reduced to only traces and components.

D. EMC Considerations

There are several issues that face the design of the HV system; balancing cost, physical size, and ensuring board maintains good electromagnetic immunity. The active balancers switch high currents at a relatively high frequency, as such they pose a risk to the other ICs as they will be the primary source of noise affecting cell measurement. The emissions of the device will directly affect the immunity of the other ground. The standard defence against this issue is to increase the size of the return path, and place that as close as possible to the signal. All signal layers are directly adjacent to a ground layer to minimise issues [3].

A small RC filter is utilised on the board. Due to space constraints, this was placed at the input of each voltage tap to the board, however the way to best optimise the strength of the filter would be to

place it as close as possible to the input of the cell measurement IC.

The highest six cells of the stack are referenced relative to two points. The first reference is for the cell measurement the lowest potential of the stack. Whilst measurements are performed in a differential manner, the passive balance IC itself is grounded to the lower potential ground, and as such lines to the point, must be shielded to that ground. The second ground is relative to the reference of the sixth cell in the stack.

A proposed alternative strategy was to make use of a six layer stackup, with the cell signal layer being adjacent to a layer for the active ground, and another layer dedicated to only the HV ground. This was dismissed to reduce cost.

There is an additional ground included on each LMU that is galvanically isolated from the vehicle ground and the HV ground, that contains the microcontroller and logic. This is done to provide an extra level of immunity for the mission critical microcontroller. This practice is well endorsed by SAE design guidelines as it provides a good way to break up critical areas of the vehicle [3]. Even in the case of a communication failure with the rest of the vehicle, the microcontrollers integrity must be maintained. Given the high amount of switching noise generated by the powertrain, one should expect immunity to be an issue. CISPR 25 is the typical automotive standard that is used to quantify how much the device radiates, and its immunity [13], and as testing progresses, some parts of this regime may be tested to gain insight into the performance of the design.

V. Conclusion

With the testing of the LMU commencing in the next week on a live battery stack, it will be interesting to begin qualifying and quantifying the proposed solution. The challenges to reach this point have been great, with an underestimation of the space required for the additional active balancing circuitry being the primary issue, and causing the most delay. As discussed earlier, a good proposal would be to build a system where it is possible to remove the active balancing circuitry where not required. This has several advantages, such as minimising the width and length of the PCB, in exchange for better using the height, a usually under utilised part of the volume.

Various logistical issues have greatly affected component selection on the PCB, and as such, many parts have been interchanged since the initial schematic conception in late 2021. In its current state however, this project is close to producing a system that is able to outperform many of the automotive BMS that are available, and maximise the running time of the solar powered electric vehicle it which it will be used.

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