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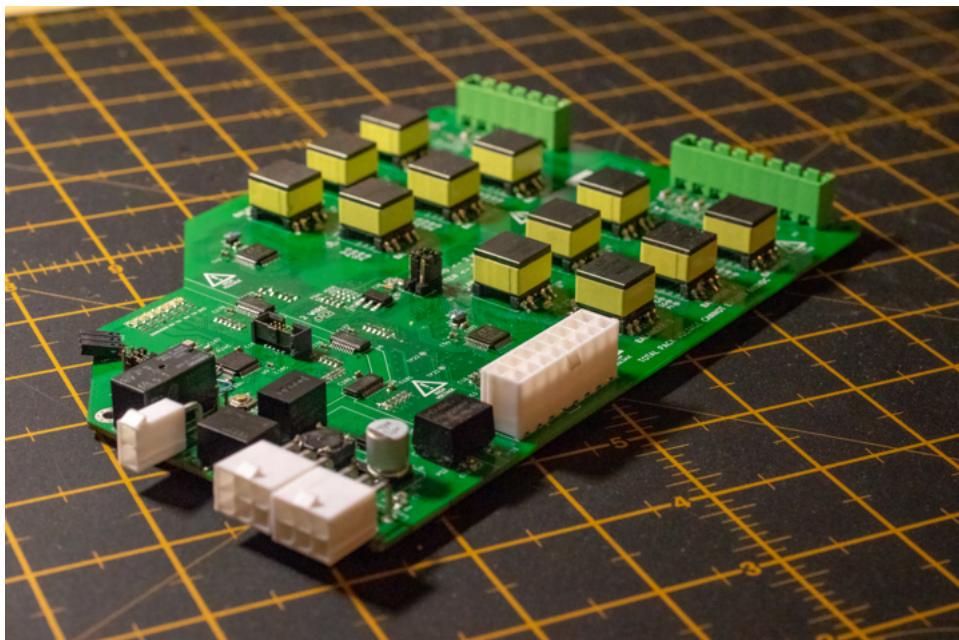
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Distributed Battery Management System (BMS) Design, Optimisation, and System Integration for an Electric Solar Vehicle

Final Report - Final Year Research Project (ENG40002)

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Abstract

Battery Management Systems are critical to the operation of any kind of electric vehicle, taking care of its most vital and fragile component: the battery. The high requirement for energy conservation, low heat generation, and high speed charging in an electric solar vehicle demands that every system be as efficient as possible; but many existing off the shelf BMS solutions do not take this into consideration with their design.

Cell balancing is the most important function of a BMS, wherein the individual cell groups of a battery assembly are kept at similar voltage levels to each other, ensuring the battery stays healthy and can be used to its fullest extent.

In this project, research was conducted on the methods through which a BMS can balance a battery. Passive balancing discharges excess energy as heat, whereas active balancing provides a means to redistribute excess energy across the accumulator. Methods of active balancing were found to be beneficial to efficiency gains for a solar electric vehicle, at the cost of increased logical complexity and external circuitry. To compare the two methods and test on the solar vehicle, a PCB was developed with the presence of an active and passive balancer.

This design focuses on efficiency and has a form factor compatible with Swinburne University's electric solar vehicle project. It is designed to be scalable with the use of more units for larger battery stacks, makes use of a central gateway for monitoring and interacting with the rest of the vehicle, and can provide a wealth of diagnostic information and feedback to the rest of the vehicle over CANBUS. It is fully compliant with the World Solar Challenge rule-set,

Index Terms

BMS, Lithium, Lithium Titanate, SPEV, Electric Vehicles, Passive Balancing, Active Balancing

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II. INTRODUCTION

The development of Electric Vehicles (EVs) and Solar Powered Electric Vehicles (SPEVs) has rapidly advanced over the past twenty years, due to the widespread adoption of lithium battery technology. Lithium cells present a challenge for safe EV design because of their volatile nature. Lithium Iron Phosphate (LFP) batteries are typically limited to 4.2V, and if exceeded will combust. Similarly, draining the cell below 2.8V promotes internal crystalline growth which will eventually pierce the cell when they are charged again, causing a short circuit and leading to a thermal runaway event [6]. Once Lithium Cells exceed their maximum rated temperature, typically around 80°C , they will begin the process of thermal runaway, which poses a grave safety hazard, especially for an electric vehicle and its occupants.

To mitigate such risks, lithium cells must be protected with a monitoring device called a Battery Management System (BMS). While these devices range in complexity, all must at least monitor series cell voltages and provide a mechanism to stop discharge in the case of a fault [7]. More fully-featured units will typically include some way of relaying data to external systems or to a user, measuring cell temperatures, and estimating state of charge, but the most useful feature they provide is balancing. Balancing is the process of equalising all series cell voltages to increase the state of charge of the battery.

There are two ways of balancing cells, passive balancing, and active balancing. Passive balancing discharges the excess energy from the highest cell of the pack and discards it as heat or light. The process is inherently wasteful, and thus only performed during charging to maximise the voltage, and subsequently the capacity, of every cell in the accumulator. Passive Balancing is typically employed when charging from a source such as the mains grid, whereby the energy wasted from balancing does not result in the battery being unable to reach maximum charge. By contrast, active balancing is the process of redistributing this excess energy from the highest charged cell into adjacent cells [8]. This can be performed even when the vehicle is stationary, preventing the lowest cell from over-discharge, extending the life of the pack.

Individual cells in an accumulator should be selected such that they are of equal health and will discharge at equivalent rates, however over time their internal resistances will drift, causing the delta between cells to increase, requiring additional time balancing. Passive cell balancing through large resistors generates great amounts of heat, and as such can typically not be performed for prolonged periods of time without damaging the battery [9]. Active balancing can be done mechanically with the use of switches or relays to place these cells in parallel. More often is the solid state approach, usually done with the use of a DC-DC converter. This functions more as a DC-AC-DC process, whereby the charging cell is coupled to an AC rail which is itself AC coupled to the cell that is to be charged. Active balancing circuits require many additional components compared to passive circuits which are simply some kind of switch and a resistor.

BMS typically come in two different architectures, centralised and distributed. With a centralised BMS, all series cells are connected to a single unit. This requires long wires, creating signal integrity and isolation issues. A distributed BMS delegates measurement and balancing to multiple smaller units, spread throughout the accumulator. Provided that the additional volume required for each measurement unit is minimal, this provides huge benefits to the design of an accumulator. Sub-units of this larger accumulator can be safely spread throughout the vehicle, with minimal connections required between stacks.

The significant cost increase, large physical overhead, and additional complexity of an active balancing BMS has limited its use in electric vehicles, however the energy saving requirements of electric vehicles provides a good platform to test such a system. Swinburne's Solar Team has struggled for years with the challenge of using heavily cycled lithium titanate cells with a large pack delta. As such, this prototype vehicle functions as a good test bed for such a BMS design.

III. BACKGROUND

A. World Solar Car Challenge Background

Since 1987, the World Solar Challenge (WSC) has provided a platform for universities and corporations to fuel the development of solar vehicles. The competition runs over seven days, with vehicles crossing the 3022 kilometre long road between Darwin and Adelaide [10].

There are two competitive classes of vehicles in the competition; Challenger Class; small lightweight single pilot vehicles which evoke the typical image of the solar challenge, and the Cruiser Class; a more practical, consumer focused offering, for vehicles with 2-4 seats. There is a third non-competitive class, Adventurer, offered for entries that meet safety requirements, however not the constraints of the Challenger or Cruiser class, as a non-scored event. The Swinburne Solar Team (SST) aimed to produce a vehicle in the Cruiser class, and as such, this project will focus on the regulations surrounding this requirement.

The cruiser class allows for the use of Type 2 vehicle chargers at controlled points on the road between Darwin and Adelaide (Currently at Tennant Creek, NT, and Coober Pedy, SA), with regulations as to what hours the vehicles may charge. The chemistry of these packs affects the total points penalty incurred by the accumulator size, a smaller accumulator being favourable. *There is no such restriction on the size of the accumulator in the Cruiser class.* Additionally, the more energy that

is fed into the pack by means of these stationary chargers rather than solar, the greater the penalty at the end of the race, thus energy conservation is a priority.

The rules for the competition are available from the following URL: <https://www.worldsolarchallenge.org/the-challenge/regulations> [11].

B. Statement of Problem

The issues are as follows:

- The voltage range of the measurement interface of most existing BMS solutions do not support the required cell chemistry available during testing.
- The use of a passive balancing system does not meet the desired energy conservation principles of an electric solar vehicle.
- Most available active balance interfaces are external, intended for stationary use, and very few are suitable for use in electric vehicles.
- There is a desire to provide a highly scaleable solution and potentially distribute the accumulator safely throughout the vehicle; no exposed high voltages tap wires are to be strewn through the vehicle.

C. Project Goals

With this context in mind, the following goals were set to guide the design of the system:

- Cell voltage range of at least 0.8V to 4.5V to meet the requirements of most lithium chemistries.
- Accommodate a total pack voltage of up to 600V.
- There should be no unpopulated cell measurement taps; with fewer cells the BMS should be reduced in size.
- Able to manage cells in poor health as efficiently as possible; the reduction of energy waste in balancing.

With so few automotive grade BMS units offering active balancing, this project can address the gap in research into the feasibility and practicalities of including an active cell balancing system. The primary questions are as follows:

- Is the amount of space required to include an active balancer suitable in such a weight optimised vehicle?
- Is it possible to balance the vehicle on the go to extend the life of vehicle?
- How would one approach the design of such a BMS system, and ensure it meets ISO26262 requirements?
- What efficiency gains can this system provide over typical passive-only solution on the market currently?

The project aims to design both a BMS with capability for active and passive balancing, and a complementary electrical architecture for a solar car vehicle potentially to be developed by Swinburne University for the Cruiser Class of the World Solar Challenge. The BMS will feature a distributed architecture, whereby more BMS modules can be added with a single interface to a centralised ECU. In order to optimise capacity of the pack for, the design and implementation of an active balancing system shall be explored. The BMS design must also accommodate the use of a MPPT (Maximum Power Point Tracking) charger, a standard Type 2 electric vehicle charger, be able to negotiate the maximum discharge current with the throttle and motor controller system, and provide a discharge and precharge mechanism to avoid damage to the inverter. All of these features must be able to integrate into the vehicle's control and management systems.

IV. LITERATURE REVIEW

A. Conventional Cell Monitoring Methodologies

The main functions of a BMS is dependant on its ability to monitor certain characteristics of the cell under its care. Given the measured capacity and discharge characteristics of a cell, a State of Charge (SoC) plot can be draw to determine the maximum desired level of charge and the lowest desired depth of discharge that the cell will experience. As explained in the introduction, poorly maintained lithium-based cells that are allowed to overcharge or over-discharge beyond their typical operating range can cause irreversible chemical damage and affect the capacity, performance, reliability and safety of the cell [7] [9].

Different types of cells/chemistries offer different methods of monitoring and calculation of properties such as State of Charge. The most accurate method possible for cells with a liquid electrolyte (e.g. Lithium variants, Lead Acid) is to measure the pH of the electrolyte since that is directly linked to the amount of potential energy present in the cell. Unfortunately lithium chemistries are too delicate and volatile to allow for such an invasive method of monitoring. More robust chemistries such as Lead Acid that can be left unsealed prove more conducive to this method. As such, non-invasive methods of cell monitoring have to be employed.

Conventional methods of monitoring lithium cells utilise the electrically measurable characteristics of the cell. The internal resistance of the cell can help determine its overall health, as well as its ability to supply high amounts of current. The open circuit voltage across the cell's terminals can be used as a crude method of estimating SoC. The voltage across the cell while under load can be used to infer how well the cell is coping with the given load and whether it should normally operate under those conditions. The current being drawn from the cell can be used to determine how much load the cell is under.

Monitoring the temperature of the cell is of particular importance. The electrolyte inside a lithium cell is quite sensitive to temperature. Too cold and the electrolyte starts to become viscous, lowering its chemical reactivity and affecting its output ability [12]. Too hot and many chemical changes can occur in the electrolyte that cause degradation in performance over time, such as an increase in internal resistance which makes the cell less efficient. Using a heating and cooling system to maintain a window of optimal operating temperature for lithium cells is critical to their safe, effective use and their longevity.

B. State of Charge Calculation

There are various ways to calculate the state of charge of the accumulator. The simplest method that is fairly ubiquitous across many low power BMS designs is voltage monitoring. The voltage measured across a lithium cell's terminals can be described as a function of the state of charge. Figure 1 illustrates what that relationship looks like.

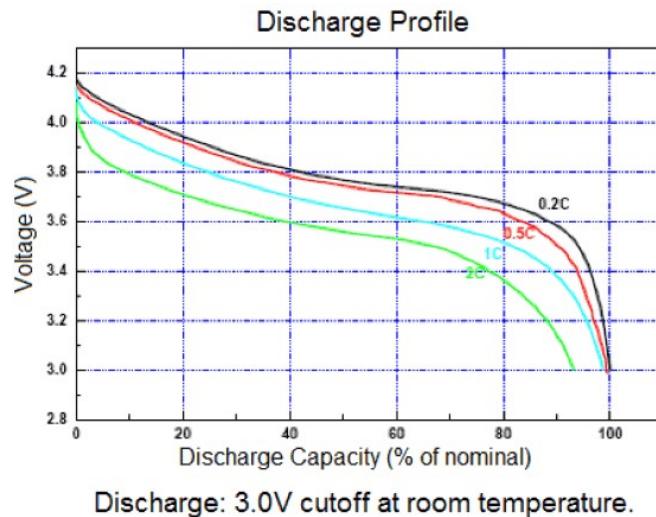


Fig. 1: The voltage versus SoC graph aka Discharge Curve for a typical Li-Ion cell [1].

The main problem with this approach is that the voltage of a cell at any given SoC can vary greatly from what has been measured on its discharge curve. Factors such as cell temperature and the current being drawn from the cell (the different curves on the above graph are for different discharge currents) can cause the voltage to dip below what would normally be measured - a phenomenon known as *Voltage Sag*. For small scale and very low power draw scenarios, this problem is a nonissue and plenty of small scale, battery-powered embedded systems use voltage monitoring for tracking SoC.

The second conventional method to calculate state of charge is current integration, also know as coulomb counting. The current being delivered to or supplied by the cell is measured, and integrating that over time gives the total amount of charge remaining

in the cell in amp-hours or coulombs. This is a more complex approach than voltage monitoring since it requires some kind of system with memory to store and update the charge level of the cell on an ongoing basis.

There are two downsides to this method. The first one is that there is no absolute reference point for such a system. Over time, a pure coulomb counting system will drift above or below the cell's actual SoC and could lead to problems for the BMS. The second problem is that this system cannot account for inefficiencies in the cell. For example, if a cell is experiencing a high current draw and has a higher internal resistance, it will discharge more power as heat, no quantifiable. Coulomb counting is only monitoring the charge that ends up being delivered to the power sink, and does not see the energy/charge lost from heat. So if a cell experiences high power draw and heats up, it's losing more charge than a coulomb counting BMS recognises, possibly leading to the BMS allowing a lower depth of discharge than should otherwise be permitted in normal operating conditions.

In practice it is frequently seen that a combination and/or variation of these two methods is employed in many BMS designs. While using multiple methods in tandem further increases complexity it also addresses most of the shortcomings of both systems. The utilisation of these balancing methods in the design of the BMS controller will be considered, as well as the exploration of non-conventional and/or emerging methods of monitoring.

C. BMS Architecture and Scalability

There are two traditional ways that a BMS is structured; centralised, whereby leads run between cells and a centralised measurement unit, and decentralised, where the BMS units are individualised to each stack. A subcategory of this decentralised unit is the modular architecture, whereby only measurement is segregated is distributed throughout the pack, a communication system linking these to a centralised management unit (CMU) [2]. Devices such as the well regarded and common Orion BMS series of BMS by Ewert are an example of a centralised BMS [13].

1) Modular Stacks

For safety reasons, a well designed accumulator will break up the accumulator into *stacks*, smaller series units that will be connected with a removable interconnect. This is done for several reasons; it allows for the isolation of faults, should a fault be detected in a stack, it can be disconnect quickly and potentially bypassed; it also ensures that those servicing the accumulator are exposed to less lethal voltages, with stacks typically having a maximum voltage under 60V. This can also be done for storage reasons, it may be necessary to stow cells in unusual places throughout the vehicle.

We can see a good example of a custom battery management solution developed for an electric motor bike that makes use of a system similar to the proposed architecture, see Figure 2. This report proposes using multiple LMU (Local Measurement Units) connected via an isolated interface to the CMU (Centralised Management Unit). This simplifies the complexity of the control interface, and allows the accumulator to be split throughout the small form factor required.

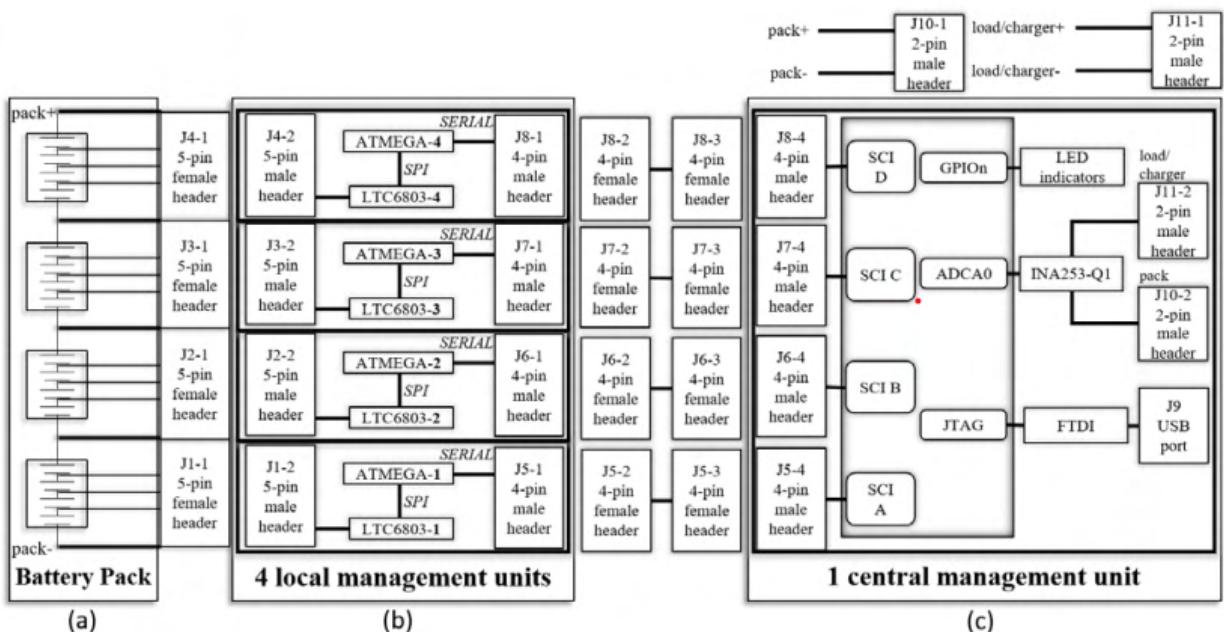


Fig. 2: The BMS system Designed by Henar, Cailang, Caliwag, and Wansu [2].

2) BMS ASICs

Large IC development companies design ASIC (Application Specific Integrated Circuits) for many different cell measurement purposes. One of the most popular of these is the LTC68xx series by linear technologies. These typically feature multiple cell measurement inputs, a way to control the discharge system, and a communication interface. Alternatives to the LTC68xx series include the ATA6870 by Atmel, AD7280A by Analog (Parent Company of Linear Technologies), or the MAX11068 (Maxim now being a child company of Analog Devices) [14].

To focus on the LTC6811 IC, this ASIC makes use of an integrated ISO-SPI interface; a serialised, differential pair, version of SPI that uses galvanically isolated transformers to bridge the gap between stacks [15]. This is important as within the accumulator, there are high voltage potentials that pose a risk to life. This also features a daisy chain interface that allows for multiple ICs to behave as a single unit.

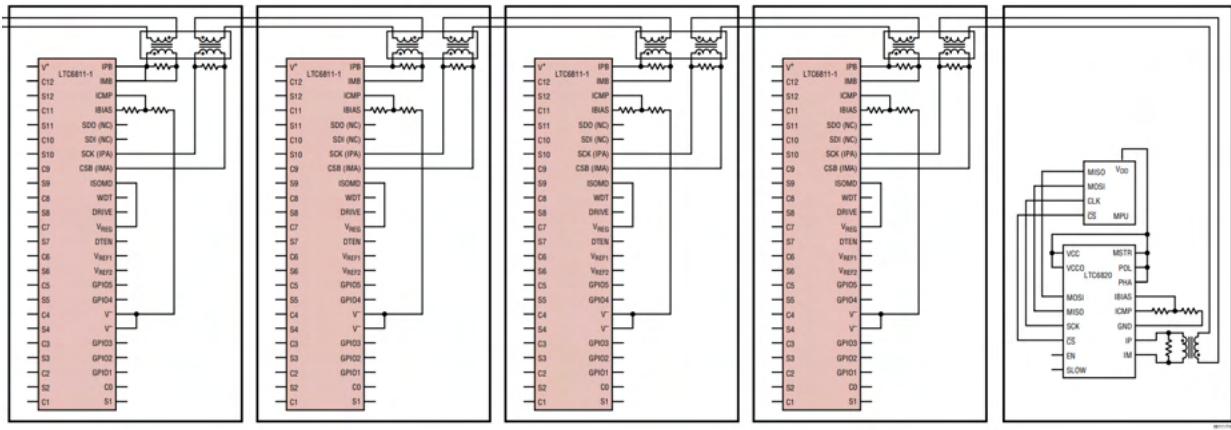


Fig. 3: The suggested daisy chain (Series) network of an LTC6811 BMS ASIC.

Using an ASIC BMS has several key advantages and disadvantages:

- They provide an integrated solution to the issue at hand, and offer a single interface with minimal external circuitry [14].
- As they are ASIC, there should not be a need to program these devices.
- They are typically more complex than using an ADC based or analogue BMS. With unusually usually poorly documented communication protocols usually reserved for B2B (Business to Business) projects [15], [14].

In order to meet the design scalability and distribution versatility requirements of this project, it is proposed to use an architecture similar to the system described in Figure 3.

D. Solar and EV Charger Integration

The battery this BMS will be fitted to will have three independent charging sources; the EVSE conventional charger, the solar charging array and MPPT, and the active balancing system, a form of charging. Each of these function exclusive to each other; the flow of current this must be controlled.

Some vehicles on the market such as PHEV (Plug-in Hybrid Electric Vehicle) make sure of further energy buffering system. A 2017 project by Toyota to develop a solar assisted hybrid Prius integrated a secondary battery that would be charged during phases where the hybrid power-train was active, preventing the additional waste made by DC-DC converter further in the power-train system. A simple relay being used to disconnect this mechanism [16].

1) Vehicle Charge System (EVSE)

EVSE (Electric Vehicle Supply Equipment) is the technical term for what many consider to be a conventional EV "charger". These are in fact not actually a charger, but rather the charger and rectifier are kept internal to the vehicle and this station simply provides a source of electricity for this charger [17]. The newer generation of these EVSE do include an additional DC charger,

The competition rules (Section 2.5.19) require that all Cruiser Class vehicles fit the following:

"...an on-board ac charger with an IEC 62196-2 Type 2 (male) charging inlet and be capable of charging from a single-phase ac supply (230 Vac, +10%, -6%, 50 Hz). The ac current draw must not exceed the limit indicated by the J1772 pilot signal generated by the event organiser's Electric Vehicle supply Equipment (EVSE), which will allow charging rates up to 30 A."

There are several things to unpack from this requirement.

- IEC 62196 Type 2 (Male) is the requirement for the socket and pin-out. Developed by the International Electrotechnical Commission, this features 7 contacts, 2 for signalling, a protective earth, a neutral pin, and three live contacts, pictured in Figure 4.
- J1772 is a signalling system that is used to control the most EV chargers. It uses a simple two wire system to indicate how much current the system can accept, and if there is a vehicle present.
- A type 2 charger is any that is able to support multiple phases, Type 2 being more common in Europe and Australia [18], however as noted, this should also support a single phase connection.

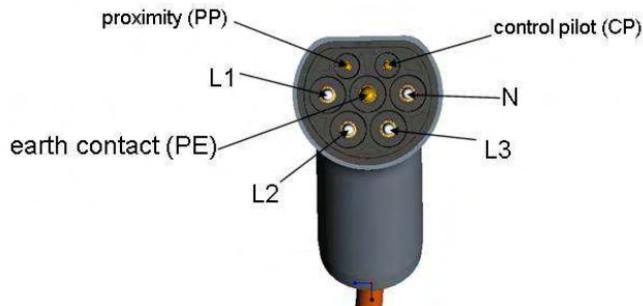


Fig. 4: Pinout of the IEC 62196 Type 2 Connector [3].

The J1772 is an SAE standard, and one of the most common signalling systems used to control the charging system in electric vehicles [18]. There are other standards defined by the SAE, that allow the connection of an off board DC charger such as J2847/2, and some that allow the vehicle to function as an off grid energy reserve such as J2847/3 [17].

There are two pins used in a J1772 system; the control pilot, and proximity pilot. The proximity pilot is a passive circuit that acts as the safety interlock for the vehicle, using a simple resistor as the feedback mechanism to tell if a vehicle is attached. The control pilot uses a PWM signal to direct the charger as to what is available. The proximity pilot is designed to act as the physical interlock for the vehicle, usually locking the vehicle in "Park" if detected, preventing damage to the outlet [4] [17].

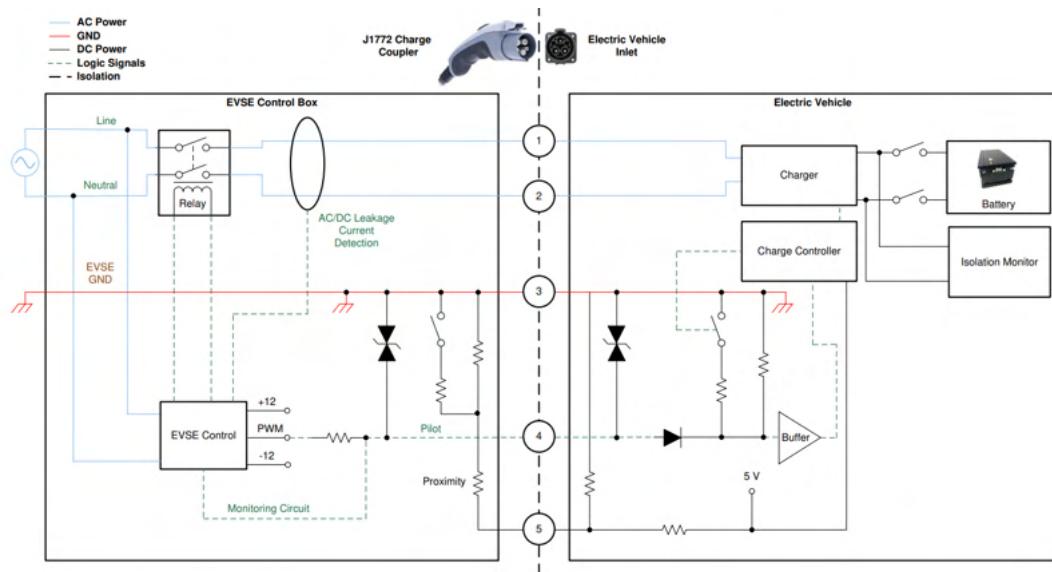


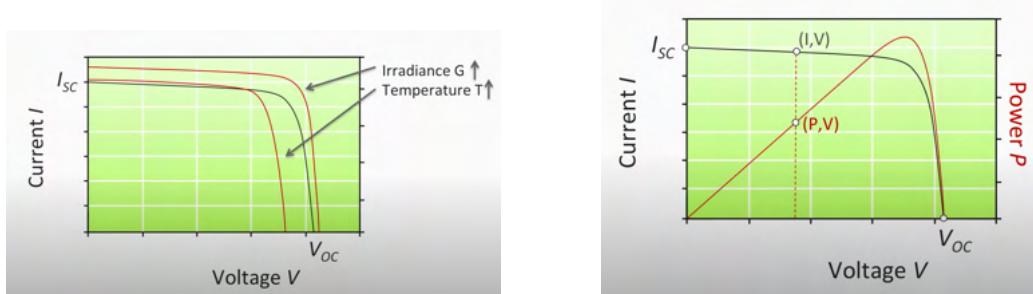
Fig. 5: A circuit diagram of the SAE J1772 interface requirement. The right half of this diagram is the most relevant to this project and must be implemented per the specifications [4].

2) Solar Charge System

Photovoltaic cells do not produce a consistent power output, the output of which varying based on the configuration of the cells (Series and parallel units), the temperature of the cell (Which may also be influenced by any cooling effects from air flow and shaded regions), the solar intensity, and countless other factors. There must be done form of regulation in order to achieve a usable output. There are typically two methods to achieve this, a simple solar regulator, usually using some form of PWM control for the output and MPPT.

MPPT (Maximum Power Point Tracking) is a technology used to maximise the output of a solar array; it is a form of DC-DC converter, that relates voltage and current to maximise power. It is able to track the optimal voltage and current relationship in order to extract the highest possible power level from the solar array.

Solar cells has a high open cell voltage, and this will reduce dramatically under load. To expand on this concept; they have a typical cell voltage, however one should note that the open circuit voltage will always be higher than one under load; in this way they behave like a non-Ohmic current source. Stringing together PV cells in series increases the maximum voltage array voltage, and in parallel, the maximum discharge current. In very simple terms, An MPPT relates the voltage and current, adjusting the output voltage of the DC-DC converter relative to the required charge voltage, such that it is always drawing the highest amount of power from the panel.



(a) A standard IV curve changes depending on the environment [5].

(b) A PV curve, calculated by multiply the current and voltage, based on the IV curve [5].

Fig. 6: A power curve (Also called a PV Curve) can be super imposed over the I-V curve by using the power relationship $P = VI$. Any point on the IV curve can be found on the PV curve. An MPPT algorithm finds the point of inflection of the PV curve, and uses this value to find the required discharge current by varying the output voltage. Images sourced from TU Delft [5].

If we consider the anatomy of a solar vehicle, the solar cells will be affected by various conditions; cells on the front of the vehicle are subject to greater air flow, and will typically be cooler than those in the rear. In the case of a solar car travelling north-south, one half of the vehicle will be in shade for many hours of the day. This affects the way in which the MPPT system will behave, and as such there are many SPEVs that utilise multiple MPPT, managed by a centralised control plane. These feature a buck-boost DC-DC converter to control the output, such that they can be part of the same system [19]. This multi MPPT system has two advantages, the MPPT does not need to have as high of a current rating since this load is shared, and the output power can be better managed.

Much of how these MPPT behaves is invisible to the operator; it is a black box. These controllers track this point of inflection typically by using some form of fuzzy logic or analogue means to perform the required calculation [20].

It may be necessary to use a DC-DC converter after the MPPT to boost the output MPPT voltage to the DC-DC converter, depending on which MPPT unit is selected.

E. Active versus Passive Cell Balancing

Cell Balancing is the most vital aspect of maintaining the health and performance of an accumulator. An accumulator will consist of an array of multiple cells making up a parallel pack, with a number of those packs connected in series. These parallel packs will be simply referred to as *cells* in this section due to there being no functional difference in the amount of cells you have connected in a parallel pack. Balancing involves having a connection to each point between all the cells, so that each cell can be monitored without having to account for other cells in the stack.

1) Passive Balancing

The most ubiquitous form of balancing found in BMS solutions currently is passive balancing, which employs the use of a bleed resistor in line with each cell. Typically a passively balanced BMS will perform balancing while it is charging the

battery. The charger connects to the top and bottom of the stack and delivers current. The voltages of each cell are monitored and if an individual cell's voltage rises above the average cell voltage of the whole stack, its bleed resistor is connected via a transistor to drain a small amount of current and dissipate the energy until the cell's voltage is brought down to match the average cell voltage level.

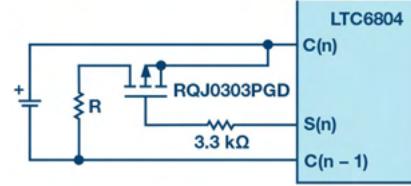


Fig. 7: The layout of a passive balancing circuit, focused on one cell, using an *LTC6804* as a balancing controller.

This is the simplest approach to balancing, both in structure and in the required amount of hardware. Only a single resistor and transistor is required per cell to enable balancing. The major downside to this approach is that it is inherently inefficient. Any balancing that needs to be done is power that gets wasted in the form of excess heat, which can prove problematic in the environment of an enclosed vehicle chassis where the cells are quite sensitive to temperature. The main advantage that this approach could provide in a solar powered vehicle is that balancing can take place no matter whether the accumulator is being charged, discharged, or experiencing no power draw.

2) Active Balancing

This form of balancing is not as common as passive balancing, due to its higher complexity, but it does find itself commonly used in electric vehicles due to the electric automotive industry's focus on gaining efficiencies wherever possible. Instead of passively dissipating excess energy from higher charged cells, that cell dissipates energy back into the other cells in the stack, ensuring little energy is wasted. [8]

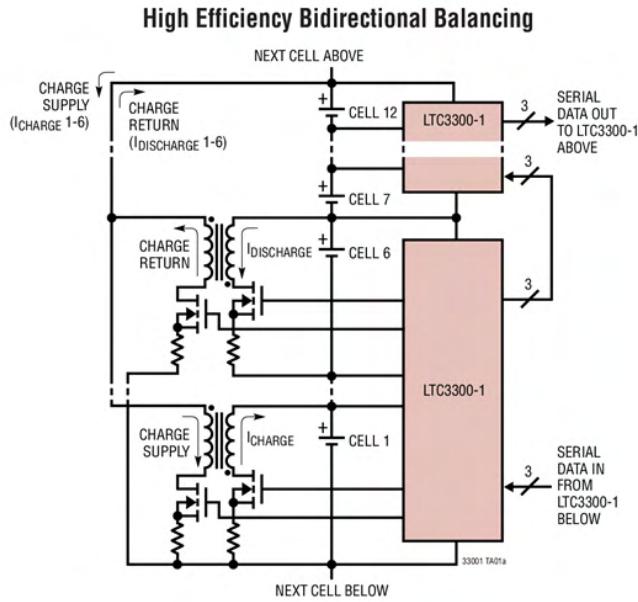


Fig. 8: The layout of an active balancing circuit using an *LTC3300-1* as a balancing controller. This ASIC is able to interconnect the active balancers on a single differential-pair bus.

One possible difficulty with all high power balancing technologies, and in particular active balancing is that, balancing may only be able to occur when the battery is not being charged. Charging with a balancer must occur in a loop; charge, then balance, etc. In a vehicle where there is a constant yet varying power source - solar panels - this could prove to be problematic as trying to have a cell supply excess power to the rest of the battery stack whilst the whole stack is being charged by solar panels may not be possible (one should not try to connect two power supplies together in parallel). Active balancing is the ideal method we would like to implement in our BMS design, and this is a problem that will need to be addressed, either through the circuit layout of our active balancing, or through the design of the power distribution system in the vehicle.

F. Driver and Vehicle Feedback Mechanisms

One of the most important aspects of ensuring a vehicle is kept operating in optimal fashion is ensuring the driver is provided relevant information about the state of various systems in the vehicle. The power-train and power management systems are of particular interest here, given that the World Solar Car Challenge focuses on a competition that demands high performance (a vehicle race) while being severely limited by your source of energy (relative to a typical consumer combustion or electric road vehicle). This type of environment demands that every aspect of efficiency be utilised whenever possible and providing useful information on real-time relevant variables to the driver allows them to be more informed about changing the operating behaviour of the vehicle on the fly, seeking the best operation in varying conditions.

Whilst the development of a dashboard and user interface is beyond the scope of this project, the monitoring of various power systems and computation of statistics representing their behaviour should be handled by a module like the BMS, with only the final results delivered to the dashboard or other devices that relay that information to the driver. By confining the main workload to the BMS it allows for more flexibility later in the design process should it be decided that some aspects of power management would be better suited to manual control by the driver, or automatic control by the BMS. Listed in the following sections are various pieces of information that should be made available to the driver as well as other peripheral systems in the vehicle.

1) State of Charge History and Projections

At the very least, a State of Charge should be shown to the driver, much like a fuel gauge on a combustion vehicle. An area this can be improved upon over typical consumer vehicles is in providing a visual graph of the SoC over time, with both the history of the SoC, and a rough projection line of future usage, which conveys the rate of charge/discharge for a given period in an intuitive manner. This alleviates the necessity for a driver to be constantly watching the SoC to determine how fast power is being used and/or estimate important variables like time until empty. For example, there can be periods of time in the solar car challenge race where sunlight is quite intense, providing more charging power than normal. If the driver is made aware of exactly how much extra charging is being provided, they can safely know that this window can be used for a quick sprint of additional speed without sacrificing long-term range.

2) Peripheral Power Usage Overview

Modern vehicles often contain many small systems that use power and exchange information over the vehicle's CANBUS network. Giving the driver an overview of the power usage of each of these systems can allow them to better understand and adapt to the power needs of the vehicle and assist in decisions that may involve switching certain systems on or off, or adjusting the behaviour of a system, at any given time.

3) Power-Train Overview

The biggest user of energy in a vehicle is the powertrain. Here the disadvantage of batteries' lower energy density is offset somewhat by the higher energy efficiency electric motors can provide over combustion engines. That said, electric vehicles still require a lot more effort in the efficiency department to make them practical. Providing the driver with real-time calculation on aspects like current operating efficiency (vehicle speed or output torque vs power-train energy consumption) will allow them to make better judgments about driving behaviour and how to react to different driving conditions.

For example, wind resistance has an exponential relationship to vehicle speed. Lower speeds result in better efficiency and longer range, but in a race you need to be trying to go as fast as possible whilst still maintaining good enough efficiency so you can reach the finish. Being able to track the power-train's efficiency assists greatly in finding the "sweet-spot" of operation.

V. SAFETY

Much of the vehicle's safety is stipulated by the competition rules, however not limited to these requirements. Given the danger to life possible from the failure of the accumulator, additional practices and standards must be well understood and followed. Section 2.28 of the WSC rules, Electrical Safety, defines a high voltage system as any system containing more than 60V.

Several Design Standards are relevant to the application and should be kept in mind in addition to **ISO26262** Functional Requirements include [7]:

IPC2221B Generic Standard on Printed Board Design (High Voltage Clearance)

AS3001/IEEE 100 Double Insulation Requirements.

UL94-V0 Inflammable Material Self Extinguishment

UL1741 Standard for Inverters, Converters, Controllers, and Interconnection System Equipment for Use with Distributed Energy Resources

IEEE 1547 Standard for Interconnecting Distributed Resources with Electric Power Systems.

A. Galvanic Isolation

In an electric vehicle, the high voltage system must be kept away from vehicle occupants, however if battery shared a ground with buttons, this would mean there is always a potential risk to vehicle occupants. As such, it is typical for there be a segregation of the low voltage system and the high voltage system.

Galvanic isolation is the principle that two circuits are not connected by the same ground reference; they are two isolated circuits. These circuits may only be coupled optically, magnetically, capacitively, or by some form of electro-mechanical interface. This is usually done to decouple electrical noise, however, if correct spacing is maintained, this can be used as a form of high voltage electrical safety. Galvanic isolation is employed both between discrete systems within the vehicle and within the design of system PCBs

B. Isolation Monitoring

Section 2.28.9 of the rules stipulate that a device be included to monitor that the galvanic isolation barrier is being maintained. In the case of failure, the vehicle should shutoff and return to a fail-safe state. These devices function by providing a controlled leak path. This current leak is monitored and if there is a leak of more than around 2 mA is detected, a fault flag is detected.

Whilst many off the shelf BMS devices include a leak monitoring device, an IMD designed by German organisation Bender should be used, as it is a well tested device [21]. Similar competitions such as Formula Student mandate use of this specific device and in fact provide these free of charge to all teams to avoid any troubles.

C. Fusing and Current Protection

Each terminal of the accumulator that connects to the BMS must be fused. Additionally a large fuse will be placed between the last series bus of the battery pack, and before the positive isolation relay.

The current clamp used to assist in state of charge calculation can be used as a way to detect over-current. There are two software based protection mechanisms that should be built in, both of which triggering an accumulator fault condition, and opening the accumulator isolation relays. They are; a hard over-current limit, a high current exceeding the current limit of the minimum rated component, aimed at preventing the main fuse from blowing, and a feedback system whereby if the discharge current limit forwarded to the motor controller is exceeded for an extended period of time, a fault condition will be triggered to prevent damage to the pack.

D. Over-Voltage, Under-Voltage, and Over Temperature Protection

The battery management system will be monitoring the voltage of each cell. For each chemistry which which the BMS can support, a range must be established for the voltage which each cell is considered safe; when out of range of this range, the accumulator

E. Safety Loops and Interlocks

The power for the accumulator isolation relays must be fail safe, as such, it is sensible that the current for the AIRs pass through all interlocks within the vehicle; including the IMD, the BMS, a Emergency Stop available within reach of the driver, and the key switch, as well as any manual service disconnects for the HV. In this way, if a fault occurs at any point within the vehicle, the accumulator will be closed and power disconnected from the system.

VI. SYSTEM DESIGN METHODOLOGY

In order to accommodate the presence of this BMS, there should be modifications made to the vehicle's electrical architecture with the overall system looking much like Figure 9. This conversion is a necessary step before the BMS can be implemented, as the current state of the vehicle's electrical architecture breaches many competition safety rules and is a collection of efforts by separate individuals that modified each others work. A complete overhaul of the architecture is necessary to provide a reliable and safe platform that accommodates and compliments the new BMS system.

A. Design Assumptions

The exact vehicle parameters are out of scope for this project, since the platform currently available for the Swinburne solar challenge team is meant purely for prototyping and is not viable for competition use. As such, any given vehicle parameters are likely to change depending on future projects, so a scalable design should be used in order to create the most versatile solution, however several assumptions can be made to simplify the process:

- A maximum voltage ranging between 70 V and 144 V, with the possibility of expanding up to 600V
- A cell voltage ranging between 0.8 and 5V.
- A medium speed CANBUS 2.0B interface as the primary vehicle communication method.
- Individual stacks may be positioned at multiple points of the vehicle, with a stack voltage ranging from 20 V to 60 V.

These assumptions are based on the limitation of the motor controller available, the Curtis 1238-E available for use has a maximum voltage of 72V - 96V, with a 60V under-voltage limit [22]. Even if the inverter were to change, there is still the practical limitation of the solar panels; modern cells with the appropriate area and efficiency typically have a usable open cell voltage of 5 V [23] and must be placed in series in order to reach the high voltage required. For an 80V system, 160 unique cells would therefore have to be used. This voltage should be as close as possible to the battery voltage in order to remove the undesirable inefficiencies of a boost converter.

We can also benchmark these design specifications against existing solar vehicle entries. A great example of a competitive challenger solar car vehicle is the 2017 Sunswift eVe, developed by UNSW. This WSC entry included a 129.6 V_{NOM} , 151.2 V_{MAX} accumulator. This is comprised of NCR18650BF cells 36S,34P with a Tritium distributed BMS. Each series unit is comprised of a spot welded unit with multiple cells in parallel [24] [25].

B. System Integration and Vehicle Control Architecture

SPEVs feature a system architecture similar to most other electric vehicles; they require a connection to the power-train usually in the form of an inverter for AC induction motors, a charger, a human interface for feedback and control. This report proposes the use of the following system architecture. A CANBUS network is used to link up each discrete module of the vehicle.

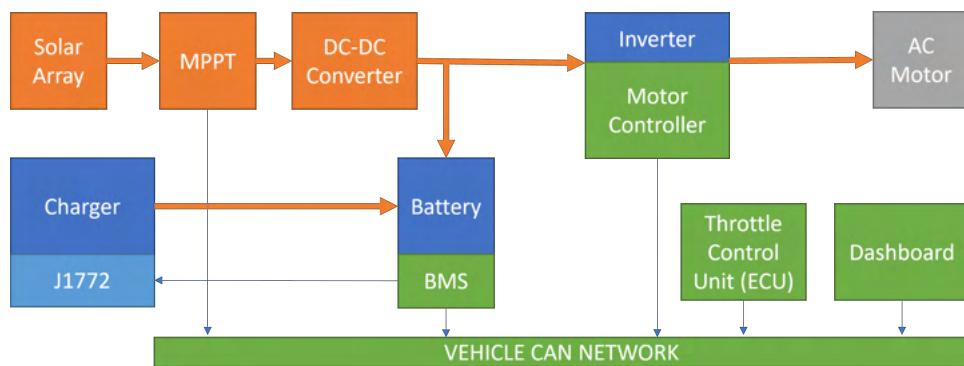


Fig. 9: The proposed high level system diagram for the Solar Car being developed.

If the high voltage bus is made common between Solar DC-DC converter, the inverter, the accumulator and the charger, this greatly simplifies high voltage power distribution. Feeding the the Solar DC-DC Converter, we are able to connect multiple MPPT modules and solar arrays in parallel. This DC-DC converter should also be current limited on the HV-DC-Bus side to prevent over-discharge issues.

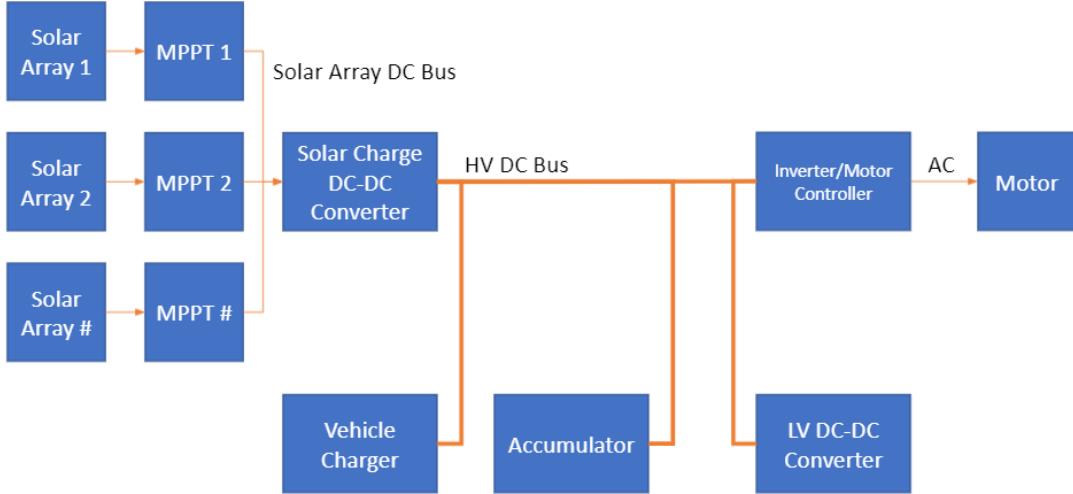


Fig. 10: Design concept for the HV system design.

C. Overall BMS Architecture

Based on the research from Section IV-C, this design aims to pursue a master and slave system, borrowing a similar notation with the BMS-CMU (Central Management Unit) and BMS-LMU (Local Measurement Unit). The Central Management unit functions as a gateway interface to the vehicle's public CAN network, and uses a private CAN network to communicate between the LMUs.

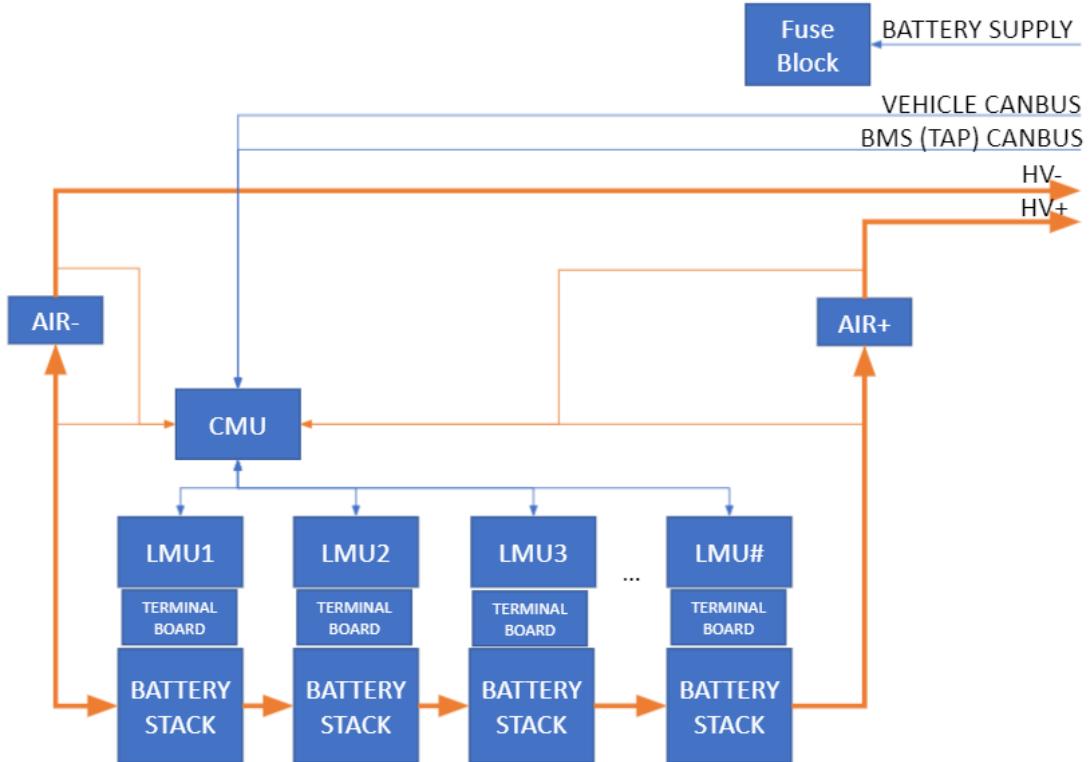


Fig. 11: Design concept for the BMS system design. For each stack there will be a single Local Measurement Unit relaying information back to the CMU. The central management unit is also responsible for sequencing the Accumulator Isolation Relays (AIR) that isolate the pack in the case of a fault.

As shown in Figure 11, this design will make use of an individual fuse block for each of the LMUs. This greatly simplifies the fusing strategy of the vehicle, making the accumulator able to be powered externally, behaving as a self contained unit. This

has the concession of meaning that individual issues relating to fusing will be harder to diagnose (Since they are downstream of another fuse), however it is the most appropriate technique for this application. As time progresses, it may be possible to include an intelligent power distribution manager on the CMU, or do away with fusing if the safe operating current is significantly below the lowest rated component. One should always appreciate the acronym of KISS, and this individually fused system strikes a good balance between fault detection and prevention.

The pin-out for the accumulator is described by the following table. This pin-out may grow, however the intention is to keep this connection list to a minimum and hide the complexity of the interface in the CAN communication protocol. This allows for a more dynamic and adaptable software system, more appropriate for the modifications that may be required as the project progresses.

Port Type/Direction	Name	Description
Power	Supply +VE	9-36V Input for the accumulators logic system.
Power	Supply -VE	Grounded to the vehicle
Input	Safety In	The input side of the vehicle wide shutdown loop.
Output	Safety Out	The output side of the vehicle wide shutdown loop
Bus	CAN_H Vehicle	Differential Pair to VEHICLE CANBUS.
Bus	CAN_L Vehicle	Differential Pair to VEHICLE CANBUS.
Bus	CAN_H BMS (TAP)	Differential Pair tap for private BMS CANBUS.
Bus	CAN_L BMS (TAP)	Differential Pair tap for private BMS CANBUS.
Power	AIR Power Return	Activated by external relay driven by the vehicle shut down loop. Activated when safe.
Input	GND_REF1	Reference point to external point of chassis for galvanic isolation monitoring.
Input/Output	J1772 Pilot	Required for J1772 Signalling, controls charger operational mode and maximum current limits.
Input/Output	J1772 Detect	Required for J1772 Signalling, alerts if charger detected.

D. Software System Requirements

The server on the CMU will be comprised of multiple daemons and programs. For each of these applications, a set of requirements has been constructed and documented in the following sections.

1) Balancer State Machine

This is the application for controlling what mode the system should be in, it follows a simple three stage check. This is called whenever a balance cycle is allowed. The balance limits are then passed down to the LMU, which handles each step of the process.

- 1) Check cell delta, if delta above threshold, balance, otherwise charge/discharge.
- 2) Active balance to cell groups with highest delta.
- 3) Passive balance the remaining difference.

2) Vehicle Charge Control

This application is started when the J1772 Pilot signal is detected, and begins the vehicle charging sequence. The steps, in no order, are as follows:

- Disconnects external load.
- Disconnects charger when balancing.
- Sets voltage and current from charger
- Weighs up when to passive balance and active balance in charge/active/passive cycle.
- Ensures that charging is maintained within limits.
- Toggles and reads the pins responsible for the J1772 sequencing.

3) Solar Charge Routine & Continuous Balancing

This procedure runs whenever solar charging is enabled. The requirements are as follows:

- Sets inverter DCL to that of the DC-DC converter, and disconnects battery pack to balance.
- Weighs up when to passive balance and active balance in charge/active/passive cycle.

4) Discharge Current Limit Calculation

In order for the inverter to function within limits and not over-draw power from the accumulator, a maximum discharge value may be set. This application needs to meet the following functional requirements:

- If balancing, set to charge current.
- Relate voltage and current to maximum discharge power, and check not above minimum current limits.
- Derate as temperature rises.
- Derate based on range required.

5) Cell Monitoring

The cell monitoring system is the most important part of this project. It must read the data from each stack from the CANBUS, and determine how to act. The input steps are as follows:

- Applies FIR (Likely Moving Average) Filter to Input signals.
- Check temperatures do not exceed maximum, otherwise set AMS relay open.
- Check cell voltages within range, otherwise set AMS relay open.
- Check cell delta not too high, otherwise start balancing.
- Check for disconnected cell.

6) Vehicle Start Sequence

Simple function to signal to the microcontroller to begin the precharging sequence.

7) State of Charge Calculator

Calculates the state of charge. A more advanced algorithm is still to be determined, however for simplicity's sake, the following steps are taken.

- Measures the output current, tracks how much has been used, relates to expected lifespan.
- Benchmarks this against estimation using open cell voltage values.
- Relays discharge current de-rating limits.

8) Stack ordering procedure

Simple routine to relate the Serial ID of a given microcontroller to the stack for which it is responsible. Each LMU only has a relative measurement of the pack, therefore, these must be set manually. Essentially linking a physical characteristic of the stack to a logical value, analogous to MAC-IP address resolution in the TCP-IP stack.

9) Human Interface (Web Server)

- Allows for Stack IDs to be changed.
- Displays individual cell voltage measurements.
- Displays cell temperature measurements
- Displays pack health information.

E. BMS-CMU Design and Requirements

The Central Management Unit functions as the gateway between the BMS and the vehicle. It is responsible for the final safety critical control of the vehicle, as well as providing intelligence to the rest of the vehicle. Due to cost and time constraints, it was decided to design the CMU only conceptually, leaving a template for how one should be designed.

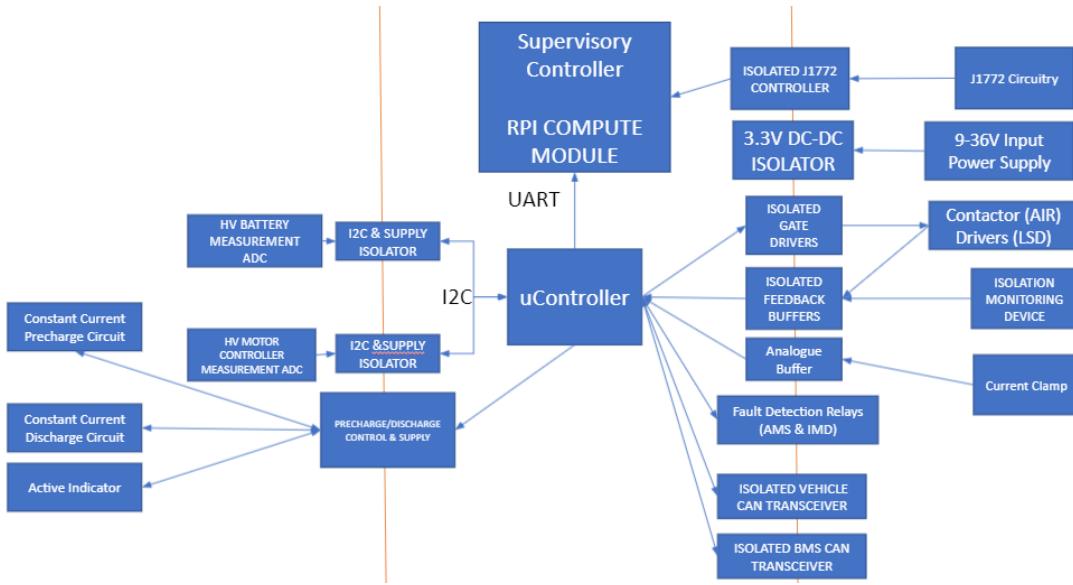


Fig. 12: The proposed BMS-CMU Architecture

The CMU is comprised of a microcontroller for mission-critical functionality with a supervisory controller to oversee all BMS operations. The microcontroller of the CMU is used to sequence the precharge, take measurements of the BMS, control the fault relays, and act as a CAN transceiver. Responsible for the entire pack is a supervisor controller, making use of a Debian (Linux) based microcomputer, most likely a Raspberry Pi Compute Module or equivalent. This interfaces with the micro controller through the use of a simple UART Interface.

The microcontroller interfaces with the ADCs responsible for the measuring the voltage on each side of the contactor by using an isolated I2C interface. This also has the advantage of using a significantly more accurate external ADC like the ADS1115. An alternate solution to this is to use an isolating op-amp like the ISO124, however these are expensive, highly sensitive to ESD, and require a second isolated DC-DC converter to power the secondary side. The requirement of the second DC-DC converter for the I2C based solution is to use an I2C isoalated with an integrated DC-DC converter, like the ADM3260.

The microcontroller that has been proposed for use is an STM32F446, a lightweight 48 pin, 32-bit microcontroller, with support for two CANBUS channels. This microcontroller is also well supported by various frameworks, including Arduino, ST_HAL, and ARM MBED. Good framework support means that there will be many existing libraries to enable use of the various low-level hardware features of this controller without having to write support for them from scratch, speeding up development time. This microcontroller also includes various internal timers, making it possible to apply real time logic to the system.

VII. LMU DESIGN METHODOLOGY

The local measurement unit is the most complex part of this project to manage, despite the relatively simple appearance. The main difficulty of this project comes from the balancing and measurement system, which must be carefully designed to avoid issues with large voltage differences, and complex ASICs. Due to this it was decided to focus the practical element of this research project on the design and testing of only the LMU as a proof of concept.

A. Sub-System Design

The input side of the LMU is constructed of a discrete 9-40V SMPS that steps down the battery voltage to 5V. This logic level voltage powers one side of the isolated CAN transceiver, and powers an isolating DC-DC converter. This is done to reduce the effects of high voltage switching transients being coupled to the LV system, and protects the microcontroller. Note that this is not for safety purposes, but the safety barrier to the HV system must be equivalent. The microcontroller is another lightweight variant of the microcontroller in use on the master; the STM32F103C8T6. This is then galvanically isolated with a 1000kV spec. isolation barrier to the high voltage components including the balance system, cell measurement system, and the temperature measurement system. The micro-controller also controls a small relay that can disable the vehicle's shutdown network if a preliminary fault is detected.

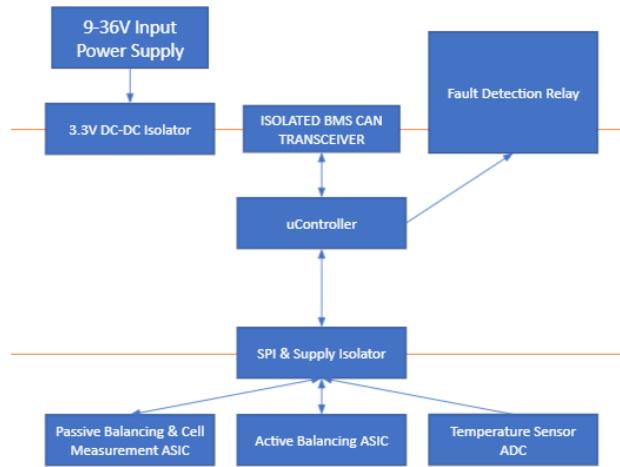


Fig. 13: The BMS-LMU Architecture. The bottom third of this forms the measurement and balance interface.

The design of the balance system is based on the reference design provided by Linear Technology, the DC2100B-C [26]. This example provides a good reference point to start with, however this makes use of an LTC3300-1 which makes use of an ISO-SPI interface, rather than the floating reference.

Importantly, this design is to make use of a transformer based active balancing method, with a backup passive balance system if the active balance system becomes too complex. The transformer is a simple 2:1 transformer, capable of driving 10A. This is switched at high frequencies by two P-Channel FETs. The LTC3300-2 requires a current sense resistor on each side for proper hysteresis, and this is provided in the form of a current shunt. There is also some input protection in the form of a 5.6V Zener, and a fuse.

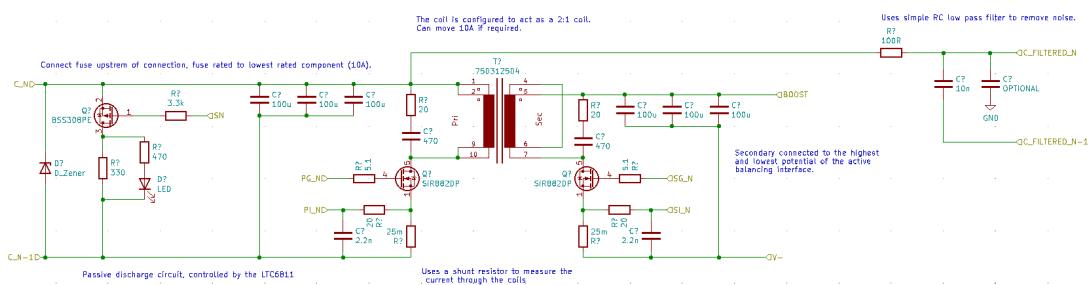


Fig. 14: The design of the cell balancer and measurement interface. Note this includes both an active and a passive cell balancing interface.

B. Initial PCB Drafts

Initial concepts for the physical design of the board involved the use of plug-in daughter-boards on the LMU to make the physical size of the unit scale with its cell capacity. With the balancing module circuits representing the largest amount of complexity and space on the board the initial decision to separate them from the rest of the LMU would have served the scalability aspect of the project very well. The design of the daughter-boards was based on a DDR3 SODIMM memory module, since concept exploration proved that 4 balancing modules would fit on one memory module. SODIMM is a standardised form-factor for Random Access Memory modules typically utilised in laptops [27].

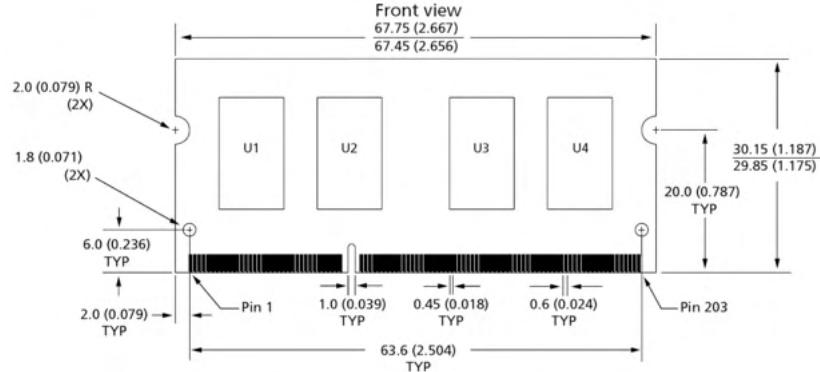


Fig. 15: The mechanical specifications for a DDR3 SODIMM memory board.

Of course this would only utilise the physical standard of SODIMM and not the pinout or protocols used by actual SODIMM memory modules. This simply provided a way to utilise daughter-boards with a connector type that was already commonly available from electronic part suppliers.

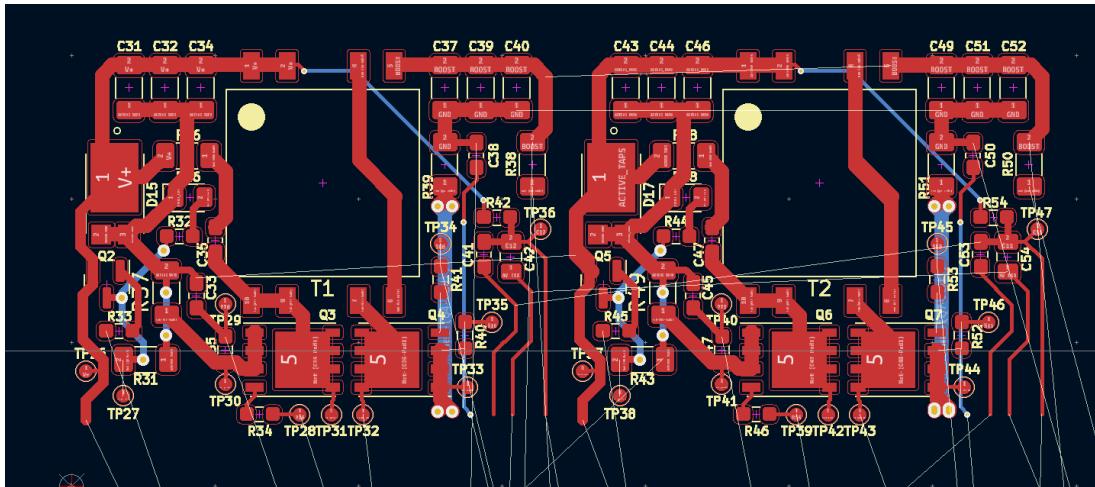


Fig. 16: Original concept for the balancing modules. Within each module is the entirety of the active and passive balancing circuit for one cell. Shown is 2 Modules laid out to fit on a SODIMM form-factor board. Each side only utilised 2 layers, so a 4-layer board allowed for 2 additional modules mirrored on the back side of the board.

Further along into developing this design, it was decided due to several constraints that this modularity would have to be scrapped in favour of a single-board LMU design. Reasons included:

- Added complexity trying to design multiple boards for one unit. The software package used for circuit and board design was KiCad which is a very capable program but is limited in many ways to single-board designs. Trying to create a design across two KiCad projects and manually perform design checks between them would have increased the time needed for design and the chance of a fatal design error making its way into fabricated boards.

Other existing software solutions such as Altium support multi-board projects but they are highly commercialised software and thus too it was expensive to obtain a paid license for this project.

- The space-saving aspect of the removable modules was not as beneficial as initially believed. To optimise the footprint of the LMU the modules would have been mounted vertically which drastically increased the volume that the LMU would

occupy. Given that most of the components used on the LMU are low in profile (perhaps a few centimeters in height maximum) a monolithic flat design was decided on going forward.

This would reduce the scalability of the design somewhat, but given that each LMU only services 12 series cell groups, this compromise did not sacrifice that too much given the need for multiple LMUs in any practically-sized vehicle battery pack. Besides that, a single-board LMU design could likely achieve a smaller size compared to a fully populated modular LMU given that it would not need any additional connectors

- Further research into the datasheets of some components selected for the design, such as the LTC3300 and the LTC6811 balancing chips, raised concerns about signal integrity requirements. The environment this design is intended for will likely encounter a high level of electrical noise from nearby systems, and crucial signals between the balancing module and the balancing chips would need to be sufficiently isolated from possible interference to ensure accurate readings of parameters such as cell voltages.

A modular design would increase the distance these crucial signals would need to travel and introduce additional interference factors such as the electrical characteristics of the SODIMM connectors. A single board provides the best basis for good signal trace design.

- Each LTC3300 chip was designed for 6 cells. On an LMU servicing 12 cells this would have resulted in 3 balancing daughter-boards, with the middle board having two modules being serviced by each chip, which could introduce problems with separate grounds having rather high voltage differences travelling through a connector with such fine contact pitch.

The second major design version (foregoing modularity) took the balancing module layout from the first version and attempted to integrate everything into a single board (refer to figure 17)



Fig. 17: The high-level layout proposed for the second design version. The numbered red and blue blocks are the cell balancing modules, and the numbered gold blocks along the bottom are the cell terminals

This proposed design also had a number of design constraints outlined:

- The active balancer, passive balancer and temperature modules should be placed in close proximity to the LV zone for the SPI signal traces to cross the isolation line.
- Balancing Module 6 needs to be adjacent to balancing module 7 given that each sequential cell needs to be connected directly.
- The active balancing chips must be placed equidistant from each module in its balance group for signal integrity reasons.
- The temperature module should be coupled to the ground that is copper poured under the passive balance module and the first active balance module (lower ground)
- Along the vertical axis across the board layout, each module should be in sequential order.

Work continued on the board with this new layout. But as layout progressed and routing commenced it became clear that reusing the balancing module layout initially intended for a SODIMM board was detrimentally affecting the design. They were created so that most of the module's traces entered and exited out of one side, and while this suited the initial concept where the daughter-board connections were all along the bottom of the SODIMM board, this was making layout difficult as the

modules did not fit well together and did not route well with the proposed layout above. An attempt was made to design the board with a far more ortholinear layout compared to the proposal to try and work around the balancing module's drawbacks. Work continued in an attempt to save this design but ultimately it was realised that a major rework was required, since the size of the LMU had increased to almost the size of an A4 piece of paper, which was far larger than originally envisioned and it was clear that the design had potential to be smaller with better design principles in respect to isolating different grounds and other design aspects.

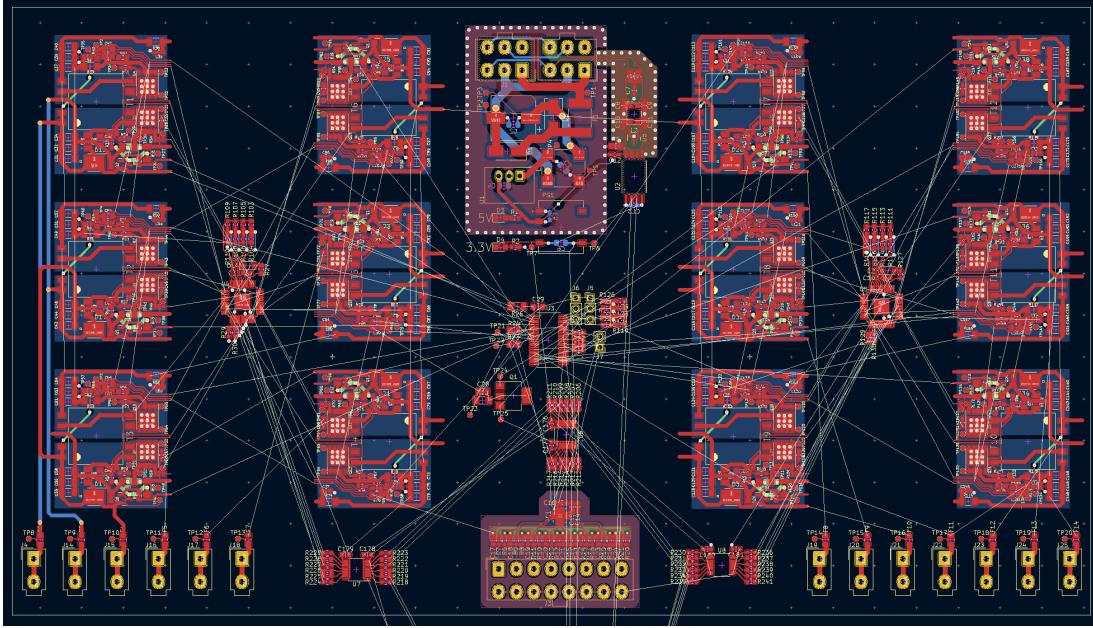


Fig. 18: The final progress of version 2, early into routing. The space around each cluster is spacing allowance for routing. This design ended up being so unwieldy that there were even components that had not been placed on this board yet simply because there was no place to put them

The design was taken back to the drawing board to make everything more compact and allow better layout principles. The balancing modules were majorly reduced in size by moving a large number of components to the back side of the board. This allowed for a large number of the version 2 design constraints to finally be realised in a board.

Given time constraints, these two initial designs were scrapped, after no progress had been made, and a simpler design, with clear direction and dedicated layers used.

Briefly explored also was the use of six layers to speed up time and assist with EMC performance, however cost constraints limited this proposition. The requirement of modules being equidistant was relaxed, partially due to the more compact design reducing the length of the balancing chips from their farthest balancing modules, and partially due to the need for more breathing room with regards to layout flexibility. The modules were placed in sequential order for clarity (along the vertical axis this time instead of horizontal). All the major ICs on the board are close to or inside the LV zone to ensure signal integrity for the SPI signal lines. However out of all these design aspects, the biggest achieve for this version was the size. Version 2 of the board in its most progressed state totalled an area of 375.7 cm^2 . Version 3 of the board in its final state totalled an area of 221.3 cm^2 . This represents a reduction in size of 41% between boards which is very significant.

C. Final PCB Design

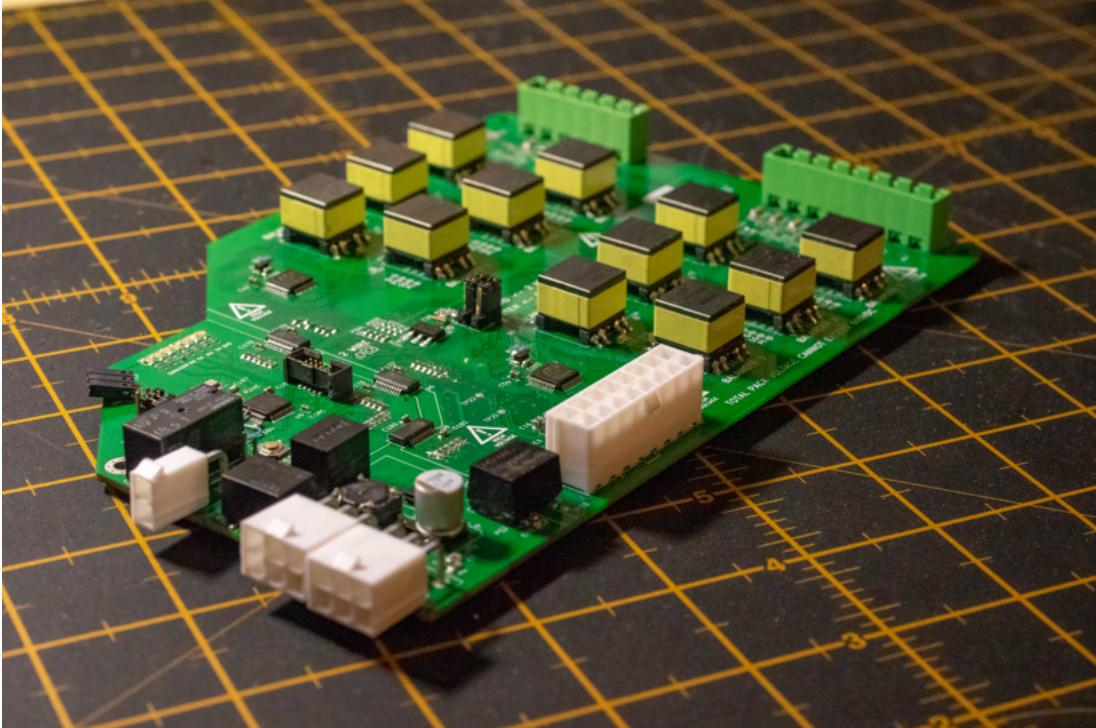
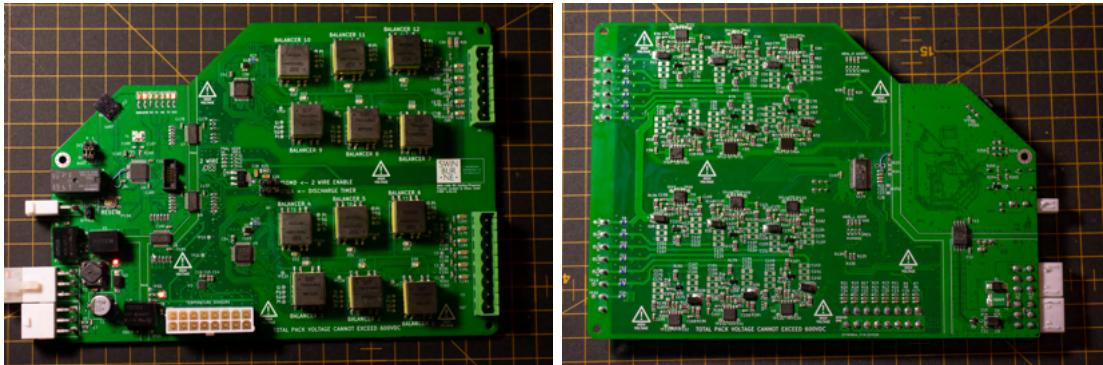


Fig. 19: The completed PCB.



(a) Top side.

(b) Bottom side.

As stated earlier, the PCB for the LMU is significantly larger than original concepts for the design earlier in the project, however more compact than later drafts, making it a good size and form factor to hide in the existing battery management containers.

1) Isolation, Safety, and Grounding

Grounds serve two main purposes, for protecting the integrity of signals, and protecting systems and users in case of a fault [28]. In the vehicle, an IMD (Isolation Monitoring Device) is used to ensure that no more than 2mA is able to pass from the high voltage system into the vehicles system. A device such as the ISOMETER IR155-3204 will be connected with the ability to break power to the main accumulators on fault [21]. This protects against the mechanical failure of various parts of the powertrain, where contact is made when insulation is not present or has fatigued, as well as the electrical failure of the various ICs and DC-DC converters that are used to isolate the barrier.

Of great concern in the development of this BMS was its ability to handle high voltages. A safety isolation barrier of 3mm has been included to allow the device to meet the IPC2221B high voltage clearance requirements [29].

In order to simplify the architecture and avoid being locked into using Linear Technology's proprietary interpretation of SPI, isoSPI, a simple series of simple high speed digital isolators is to be use. The primary advantage of this scheme is that inter

stack connections do not need to be adjacent since the communication interface is connected to the same ground as the vehicle. As such, the pack can be split across the vehicle without much additional wiring.

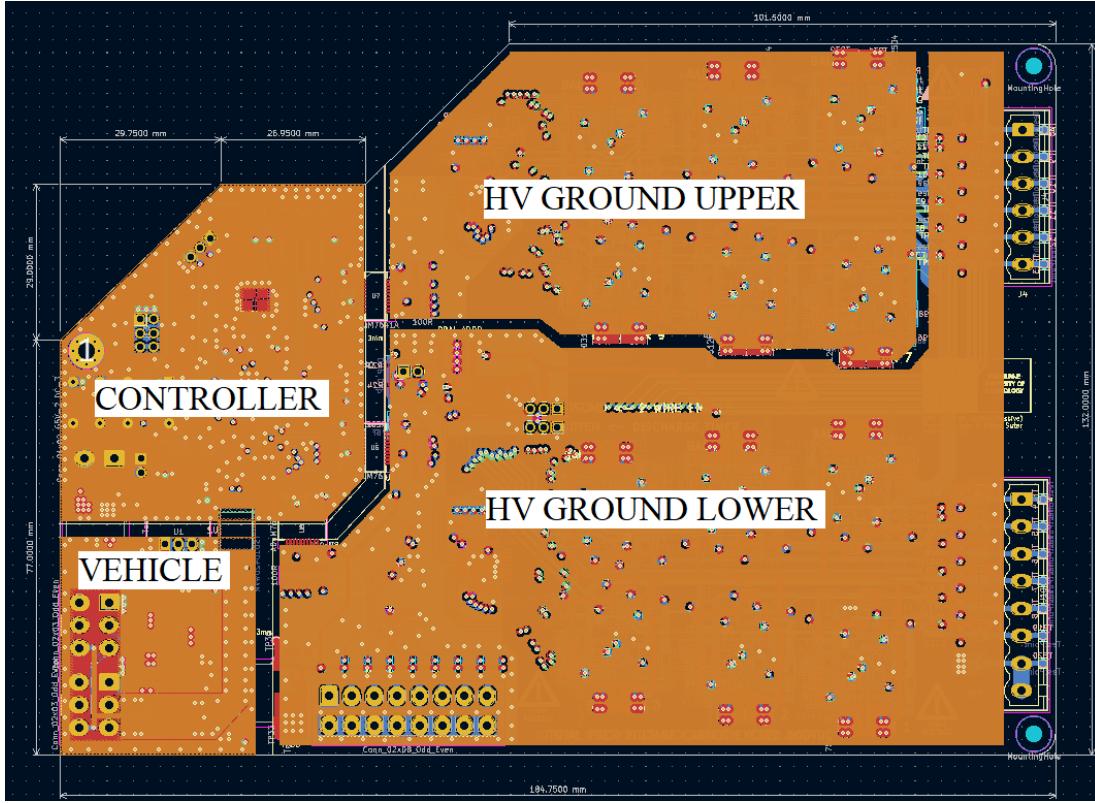


Fig. 21: The different ground planes used to break up the PCB. Note that each of these zones is galvanically isolated except for HV ground upper and lower, explained in Section VII-C2.

There is some danger associated with extending the ground planes used for high voltage. A large plane is a huge physical target and risks the operator or assembler making contact with the high voltage plane. Of course, during assembly, high voltage gloves must always be worn and ample warnings are listed on both sides of the board, however additionally, these planes have been restricted to the internal layers of the PCB. Therefore the risk is reduced to only traces and components. An analysis of this performance is included in Section VIII-B.

2) EMC Analysis and Considerations

There are several issues that face the design of the HV system; balancing cost, physical size, and ensuring board maintains good electromagnetic immunity. The active balancers switch high currents at a relatively high frequency, as such they pose a risk to the other ICs as they will be the primary source of noise affecting cell measurement. The emissions of the device will directly affect the immunity of the other ground. The standard defence against this issue is to increase the size of the return path, and place that as close as possible to the signal. All signal layers are directly adjacent to a ground layer to minimise issues [30].

A small RC filter is utilised on the board. Due to space constraints, this was placed at the input of each voltage tap to the board, however the way to best optimise the strength of the filter would be to place it as close as possible to the input of the cell measurement IC.

The highest six cells of the stack are referenced relative to two points. The first reference is for the cell measurement the lowest potential of the stack. Whilst measurements are performed in a differential manner, the passive balance IC itself is grounded to the lower potential ground, and as such lines to the point, must be shielded to that ground. The second ground is relative to the reference of the sixth cell in the stack.

A proposed alternative strategy was to make use of a six layer stackup, with the cell signal layer being adjacent to a layer for the active ground, and another layer dedicated to only the HV ground. This was dismissed to reduce cost.

There is an additional ground included on each LMU that is galvanically isolated from the vehicle ground and the HV ground, that contains the microcontroller and logic. This is done to provide an extra level of immunity for the mission critical

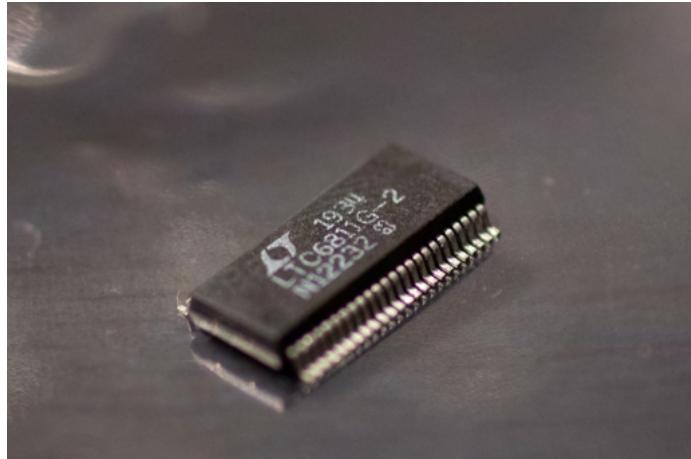


Fig. 22: The BMS ASIC, LTC6811-2, sourced from an alternate supplier. Note the subtle wear marks as this appears to have already been used.

microcontroller. This practice is well endorsed by SAE design guidelines as it provides a good way to break up critical areas of the vehicle [30]. Even in the case of a communication failure with the rest of the vehicle, the microcontrollers integrity must be maintained. Given the high amount of switching noise generated by the powertrain, one should expect immunity to be an issue. CISPR 25 is the typical automotive standard that is used to quantify how much the device radiates, and its immunity [31]. The intention is that by the final presentation, there will be a test done in a CISPR 25 approved chamber to test the emissions of the PCB and if it falls over when radiated.

D. Alternate Part Sourcing due to the Coronavirus Pandemic

One issue that greatly affected this project was component sourcing. Due to the Coronavirus pandemic, and various market forces, automotive grade chips are in short supply. This is due to a silicon shortage, mixed with a waning, and then sudden increased demand of automotive grade ICs, fueled by fears around the pandemic's economic effects [32]. Compared to early revisions of the schematic, there were great BOM changes that had to be made. Additional to this, some parts, such as the BMS ASICs were simply not available, or had to be back-ordered until 2023. As such, it was decided to attempt part sourcing from alternate suppliers. The LTC6811-2 was sourced from Ali-Express at an inflated price. The chips purchased are functional, but appear to have some degree of wear on the top of the casing. The current theory as to why this is the case is that they are reclaimed from an existing product that has failed, and the pins re-tinned.

One practice in which irreputable sellers have engaged is the use of blank or empty cases. These cases are functionally useless, with no bonding wires connecting the legs and no integrated circuit, and the part number is fraudulently laser etched into the top of the case. This is thankfully not the state of this IC, however, additional issues regarding this part in later testing may be attributed to the state of the IC.

Several notable small volume automotive aftermarket sellers have had to engage with these grey market sellers [33]. There is an entire research project that could be done analysing the performance of these grey market sourced parts; the quantity that are defective, where they originally come from, and the supply chain that leads them to these sellers.

E. Code

The code for this sample is designed to react in a real time way, and makes use of Object Oriented programming practices to increase modularity, and allow for common parts of the CMU and LMU to be directly compatible.

A small 1.27mm JTAG connector is included on the sample, and a breakout of the UART connection can be attached to an FTDI to monitor the samples serial link. Pictured in Figure 23.

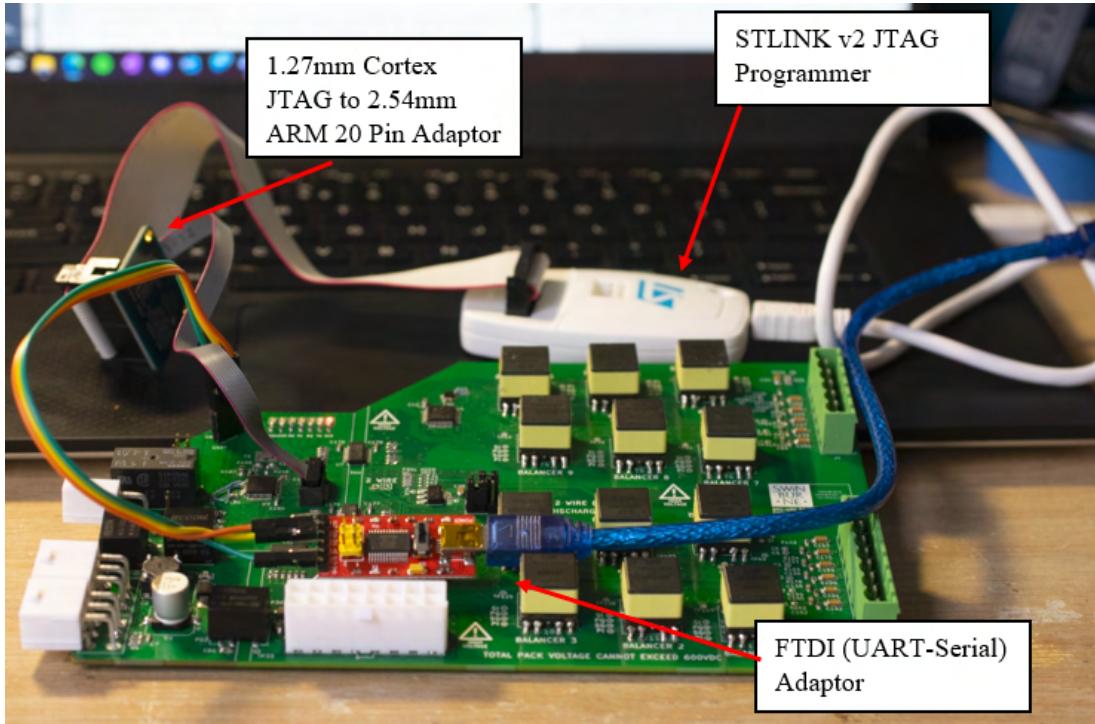


Fig. 23: The programming setup used to flash the LMU.

A 1 second Programmable Interrupt Timer (PIT), available from the TIM module of the STM32F103 is used to drive the heartbeat. The heartbeat is a self check that is performed at regular intervals. It stores the state of the microcontroller, the state of the relay, a counter that ticks with each heartbeat call, and stores the error code.



Fig. 24: UML Diagrams depicting the objects created to manage the safety features of the BMS-LMU.

The BMS-LMU functionality is controlled by a simple state machine. The LMU, after commencing setup, starts in a fault state, before it can be cleared in the idle state. Once in the idle state, the system can then be advanced into the idle state, or the balance state. Measurements of the cells are performed by another interrupt timer. The LMU can be requested to enter either ACTIVE_BALANCE, which will always end with the PASSIVE_BALANCE state, or skip active, and just do passive. Once these modes are completed, they can then be reverted. If a fault is detected at any point, then the device will return to the fault state, and wait for the code to clear.

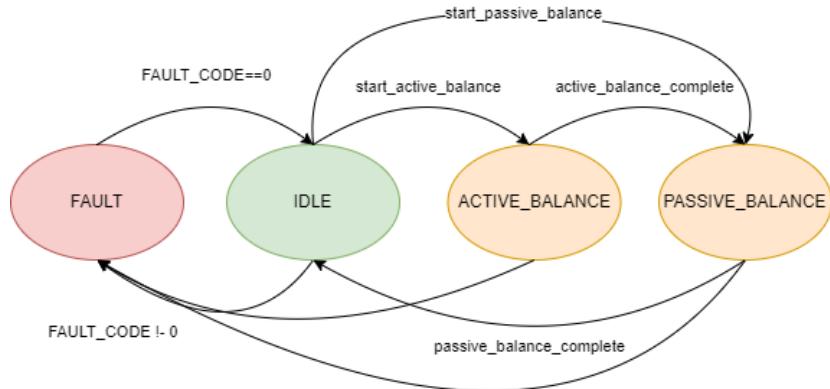


Fig. 25: State machine (FSP) used to drive the LMU.

Unfortunately, at the time of writing this report, the functionality of the SPI communication to the LTC6811-2 and the LTC3300-2s is not finished. However Linear technology provide sample code for a development board with a similar, though with far more unnecessary and proprietary features, characteristics. To work around this issue, this sample code was adapted and used for testing, described in Section VIII-A.

F. Modifications to Current Solar Car Batteries

The lithium titanate packs currently in possession of the Swinburne Solar Car Team are sourced from a home Solar PV installation. They make use of a small printed circuit board to connect each cell, 10 AWG wire, and a small circuit breaker, connected to an MC4 connector used to daily chain the connection. Unfortunately none of these parts are suitable for the hundreds of amps required to drive the Solar Beatle and the Curtis 1238E motor controller. These must be refitted with copper bus bars and 50mm^2 connections to the other cells.

The BMS-LMU does however fit perfectly into the existing battery pack enclosures. These can be attached to the phoenix connectors of the LMU.

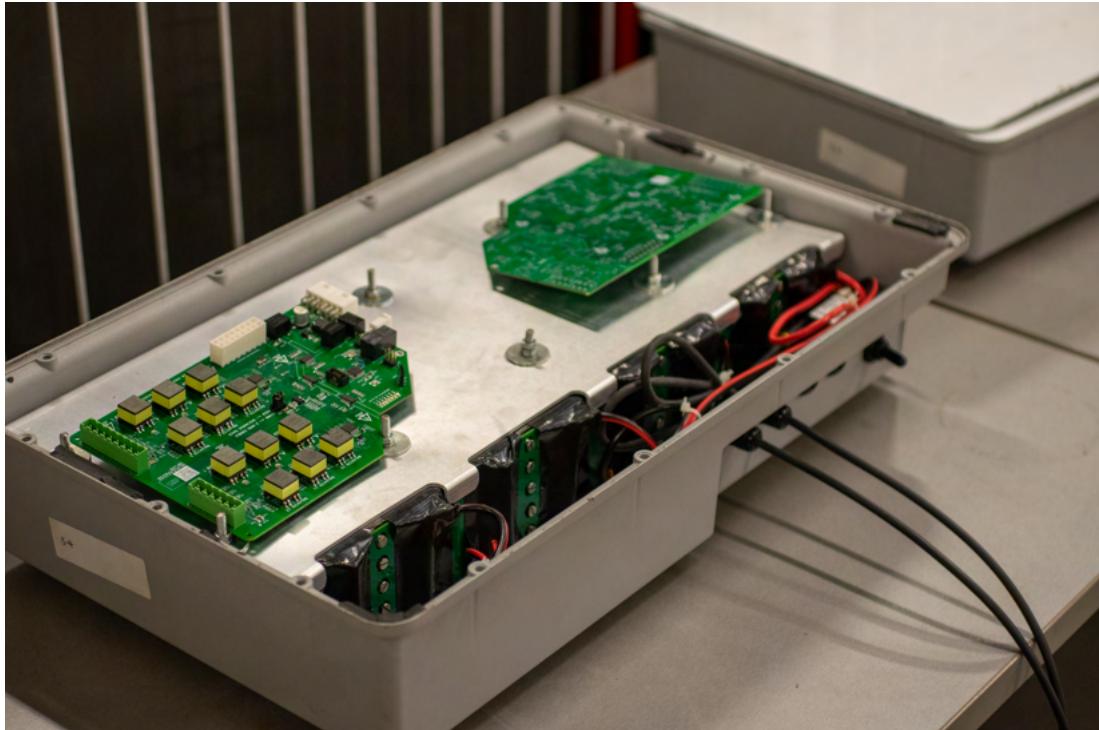


Fig. 26: The BMS housed within an existing battery module, requires refit to run wires to the cell taps.

VIII. TESTING AND RESULTS

The intention of this project was to perform a balancing session with the BMS attached directly to the cells of the accumulator to be used. Unfortunately, at the time of writing this report, there has not been any activities performed to balance cells. In the coming week as semester concludes and the boards firmware is settled and safe, a balance on the lithium titanate cells within the lab can be performed.

A. Initial LMU Bring-Up and Corrections

The sample is able to boot, report activity on the CANBUS, and perform basic SPI calls. There are two modifications required to correct errors that are present on the PCB, as shown in Figure 27.



(a) A $5k\Omega$ pull-up resistor had to be added as the SDO pin of the LTC6811 works as an open collector, noted pins on the micro have been lifted and wires soldered to the fine-print of an application note.
(b) MISO and MOSI pins are inverted to the micro. The pin of the LTC6811 is noted pins on the micro have been lifted and wires soldered to the vias.

Fig. 27: SPI issues that required corrective soldering to resolve.

Additionally, the series resistance of 100Ω was too high and causing transmission errors. This was reduced to 10Ω . C0 is also not directly connected to V-, which is an error that arises in several of the application notes in the documentations, however this is trivial to resolve.

With these issues fixed, it was then possible to communicate with the BMS. For the initial testing, the demo firmware for LT's DC2259A product could be used. This software works using Linear's proprietary interpretation of an Arduino Uno, Linduino, however modifying it to instead work using the STM32F103C8T6 proved simple enough. Several other features, such as the external SPI and I2C had to be removed in order to make this test function, as they are Linduino specific. The SPI speed was also reduced; due to the two modifications made in Figure 27, there proved to be stability issues; the clock divider was set to 128, the highest supported division, in order to make this work. With the 16MHz clock of the sample board, the SPI is functioning, just around 125kHz, and still having some stability issues.

B. Isolation Testing

To test the strength of the HV isolation, a Mega-Ohm Tester was used. These testers work by injecting a high voltage across two probes which must be placed on the planes that are isolated from each other.

The 3mm gap should be suitable for the 1000V source to not detect any leakage; the breakdown voltage of air is $3kV/mm$. The following isolation tests were performed, with no leakage detected.

- HV- to Vehicle Ground
- HV- to Vehicle Battery
- HV- to Microcontroller Ground
- HV- to Microcontroller VCC
- HV+ to Vehicle Ground
- HV+ to Vehicle Battery
- HV+ to Microcontroller Ground
- HV+ to Microcontroller VCC



Fig. 28: The Mega-Ohm isolation tester tests the conductance of the fibreglass insulation.

Additional to these tests, a general sweep was performed on pads close to the barrier to make sure no contact would be made. Tests need not be performed on the barrier to the vehicle as this gap is to prevent noise coupling; thus is the barrier between the microcontroller and the HV area is maintained, then the barrier would subsequently protect the vehicle.

C. Cell Measurement Testing

To safely test the cell measurement functionality of the BMS, a voltage divider circuit was used. This was made of 12 33Ω 1W carbon resistors in series. Each end of this would then be connected to a power supply capable of applying the correct voltage across the divider, in this case, 33V, simulating the maximum voltage (2.8V) of a lithium titanate cell.

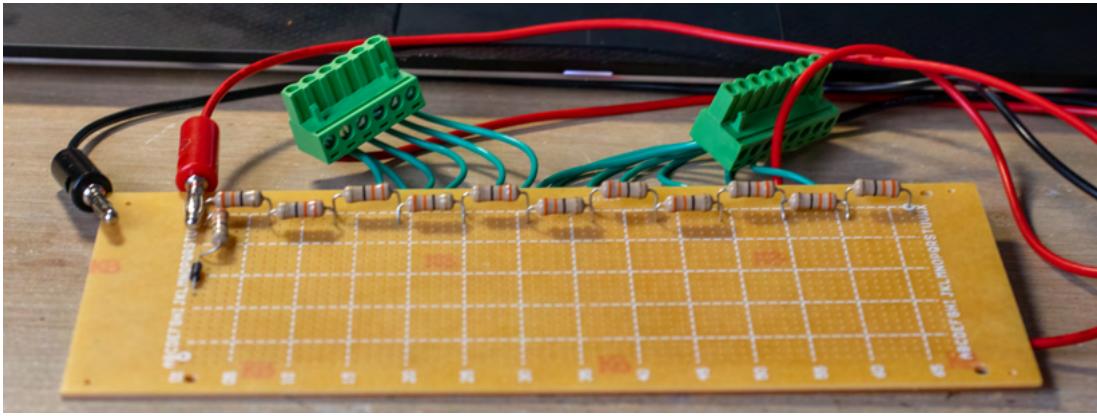


Fig. 29: The resistor bridge used to test the BMS-LMU. Each 33Ω resistor represents a cell. Note the presence of the small 1N4001 diode used as forward protection for the whole stack.

The rest of the setup made use of a small lead acid battery, and an FTDI connection to a battery powered laptop. Since the power supply must be isolated for the most accurate scenario, the LMU must be battery powered, and the PC that is reading the data must not be connected to the same circuit - otherwise the isolation between high and low voltage is broken.

By running the 6811-2's multiplexer read, and then taking the values from the registers, we can see that the device reads the cells and returns them via serial.

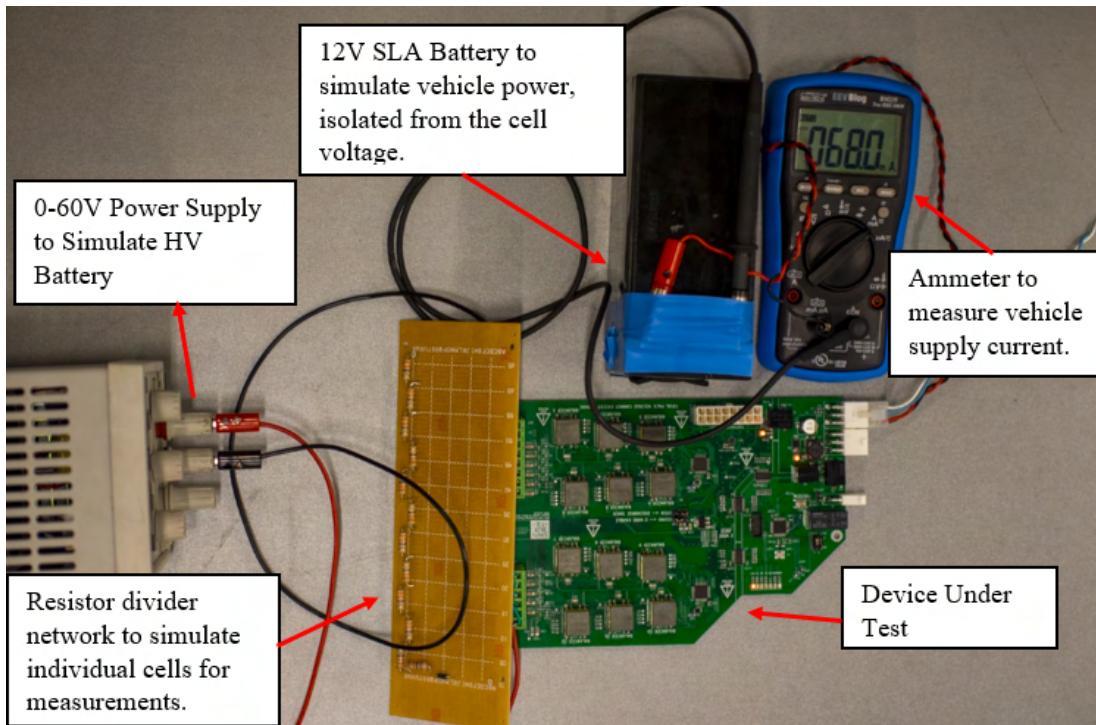


Fig. 30: The test setup used, note that the sample only draws 68mA in idle.

³
Cell conversion completed in:0.8ms

⁴
IC 1: C1:2.7591, C2:2.7478, C3:2.7501, C4:2.7480, C5:2.7518, C6:2.7406, C7:2.7499, C8:2.7511, C9:2.7313, C10:2.7397, C11:2.7092, C12:1.5964,

Fig. 31: Testing results of the cell measurement. Whilst most of the cells appear to be measuring correctly, still to resolve at the point of writing this report, is the measurement of the highest cell voltage.

Testing the voltage range of the input, we are limited by the way in which the LTC6811-2 self powers; the 5V rail is not generated until 6.61V is measured across the resistor divider bridge, meaning each cell is at 0.5V.

By sweeping the voltage of the supply, logging then, and then requesting a read of the cells, we can see the following measurements. Note that for the calculated voltage, the diode is considered negligible.

Voltage	Calculated	Cell Voltages											
		C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
6.61	0.55	2.18	0.47	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
8.16	0.68	0.70	0.73	0.74	0.74	0.74	0.74	0.70	0.73	0.74	0.74	0.61	0.01
10.04	0.84	0.84	0.83	0.83	0.83	0.84	0.83	0.84	0.84	0.83	0.83	0.66	0.00
15.07	1.26	1.26	1.25	1.26	1.25	1.26	1.25	1.26	1.26	1.25	1.25	1.26	0.12
20.05	1.67	1.67	1.67	1.67	1.67	1.67	1.66	1.67	1.67	1.66	1.66	1.67	0.53
25.17	2.10	2.10	2.09	2.10	2.09	2.10	2.09	2.10	2.10	2.09	2.09	2.09	0.96
29.92	2.49	2.52	2.51	2.51	2.51	2.51	2.50	2.51	2.51	2.47	2.34	2.45	1.37
35.16	2.93	3.06	3.04	3.05	3.04	3.05	3.03	3.05	3.05	2.69	2.49	2.65	1.77
39.91	3.33	3.62	3.60	3.60	3.60	3.60	3.59	3.60	3.60	2.80	2.51	2.71	1.89
45.24	3.77	4.26	4.24	4.24	4.23	4.24	4.22	4.24	4.24	2.86	2.56	2.76	1.94
50.76	4.23	4.93	4.90	4.90	4.90	4.91	4.89	4.91	4.91	2.87	2.62	2.74	1.99
55.16	4.60	5.48	5.44	5.44	5.44	5.45	5.42	5.45	5.46	2.81	2.69	2.74	2.02
60.49	5.04	5.74	5.73	5.73	5.73	5.73	5.73	5.73	5.73	2.87	2.77	2.74	2.07

This can then be extrapolated into the following table of errors:

Error Calculation ([Calculated-Recorded]/Calculated)%													
Voltage	Calculated	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
6.61	0.55	296%	15%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
8.16	0.68	3%	7%	9%	9%	9%	8%	3%	7%	8%	8%	10%	98%
10.04	0.84	0%	0%	0%	0%	0%	1%	0%	0%	1%	1%	21%	100%
15.07	1.26	0%	0%	0%	0%	0%	0%	0%	0%	1%	0%	0%	90%
20.05	1.67	0%	0%	0%	0%	0%	1%	0%	0%	1%	0%	0%	68%
25.17	2.10	0%	0%	0%	0%	0%	0%	0%	0%	1%	0%	0%	54%
29.92	2.49	1%	1%	1%	1%	1%	0%	1%	1%	1%	6%	2%	45%
35.16	2.93	4%	4%	4%	4%	4%	4%	4%	4%	8%	15%	9%	40%
39.91	3.33	9%	8%	8%	8%	8%	8%	8%	8%	16%	24%	18%	43%
45.24	3.77	13%	12%	12%	12%	12%	12%	12%	13%	24%	32%	27%	48%
50.76	4.23	17%	16%	16%	16%	16%	16%	16%	16%	32%	38%	35%	53%
55.16	4.60	19%	18%	18%	18%	18%	18%	19%	19%	39%	41%	40%	56%
60.49	5.04	14%	14%	14%	14%	14%	14%	14%	14%	43%	45%	46%	59%

As can be seen in this heat map, we have more measurement errors past the 2.93V mark, ignoring the known issue with C12's measurement interface. This measurement range is perfect for the range of the lithium titanate cells. By turning the input circuitry to improve the performance at higher voltages, this BMS will be suitable for LFP and other lithium chemistries.

D. Cell Balancing Performance

Unfortunately, due to time constraints, no tests have been able to be performed on the balancing routine, however with the use of the linear sample code, we can activate all the passive switches of the BMS. This is a great outcome, because it will allow for the testing of the balancing routine once it is completed. Once the cell measurement issue noted in Section VIII-C is resolved, it is the intention that the code for the active balancer will be completed such that the BMS will be able to run the DC-DC converter logic. The way to do this is relatively simple, with the BMS making a single SPI call to the LTC3300-2. The LTC3300-2 then decides which cells must act as the source and the sink and manages the coupling logic internally. This is done to avoid problems with the

IX. CONCLUSION, FINDINGS, AND RECOMMENDATIONS FOR FUTURE WORK

With time, it is hoped that successive members of the Swinburne Solar Team will be able to build upon this BMS design and make subsequent changes, and reduce the footprint, or adapt the form factor to apply the technology to later accumulator designs. There is much flexibility with the way in which this system can be integrated. The gateway can be changed to simply be a virtual gateway, rather than having a dedicated microcomputer and associated circuitry attached.

Whilst this project has suffered from a large scope, an undersized budget, and limited testing time, the outcomes have been mostly positive. The PCB for the BMS-LMU what was designed is significantly more complex than originally anticipated. It is possible to integrate an active balancing system into a form factor suitable for a SPEV, however those designing such a system should be wary of several constraints; the large number of parallel cells in a low voltage system provide an opportunity to include such a circuit. The proof of concept of this BMS system's measurement component appears to be functional and perform basic balancing tasks.

Without the balancing routine in a functional state, it is very difficult to quantify the performance of this BMS, especially with respect to the active balancer. Past the conclusion of this project, the aim is to perform a pack balancing, and measure the time taken to do such a move.

As stated throughout this report, the presence of an active balancer is hugely beneficial to the functionality of a solar car that is maximising its energy efficiency. We can expect to see savings over the life of the vehicle only around 3-4%. With this in mind, the gains to the efficiency of the accumulator can be better qualified by looking at the extension to the life of the vehicle with age. The active balancer is allowed to run after the charging, and as such has the ability to allow a vehicle to finish in the case of the drop of parallel unit's internal resistance. This additional performance advantage is extremely difficult to quantify, however, this issue has plagued many electric vehicle competitions before. Other additional benefits of an active balancing system include the lack of heat generation, and the incredibly fast balancing times. Most current automotive BMS, including the Orion BMS, and the BMS used in the Porche Taycan are limited to a few hundred milamps, however, with the inclusion of an active balancer, up to 4 Amps can be shifted quickly across a stack.

A functionality that would be required for a later hardware version would be the inclusion of a stack level discharge resistor. As this system stands at the moment, balancing between stacks is difficult to manage large discharge currents. This could possibly be done by including a high side driver that could power a relay in series with a resistor connected across the stack to quickly perform a discharge; however this use case of such a resistor would be few and far between.

In terms of the future work for this project, more research should be done into state of charge estimation for the vehicle, and integrating this with the aforementioned BMS-CMU, and creating a human interface for the gateway.

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X. APPENDIX

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B. Bill of Materials (BMS-LMU)

Index	Reference(s)	Value	Manufacturer
1	C1	220uF	Vishay
2	C2	10uF	-
3	C3	10uF	-
4	C4	22uF	-
5	C5	100nF	-
6	C6	22uF	-
7	C7	10nF	-
8	C8	DNP 10pF	-
9	C9	DNP 10pF	-
10	C10	DNP 10pF	-
11	C11	DNP 10pF	-
12	C12	100nF	-
13	C13	100nF	-
14	C14	1uF	-
15	C15	1uF	-
16	C16	1uF	-
17	C17	10nF	-
18	C18	10nF	-
19	C19	10nF	-
20	C20	10nF	-
21	C21	10nF	-
22	C22	10nF	-
23	C23	10nF	-
24	C24	10nF	-
25	C25	100nF	-
26	C26	100nF	-
27	C27	100nF	-
28	C28	100nF	-
29	C29	100nF	-
30	C30	100nF	-
31	C31	100uF	Walsin
32	C32	100uF	Walsin
33	C33	2.2nF	-
34	C34	100uF	Walsin
35	C35	470pF	-
36	C36	470pF	-
37	C37	100uF	Walsin
38	C38	470pF	-
39	C39	100uF	Walsin
40	C40	100uF	Walsin
41	C41	10nF	-

Index	Reference(s)	Value	Manufacturer
42	C42	1uF	-
43	C43	100uF	Walsin
44	C44	100uF	Walsin
45	C45	2.2nF	-
46	C46	100uF	Walsin
47	C47	470pF	-
48	C48	470pF	-
49	C49	100uF	Walsin
50	C50	470pF	-
51	C51	100uF	Walsin
52	C52	100uF	Walsin
53	C53	10nF	-
54	C54	1uF	-
55	C55	100uF	Walsin
56	C56	100uF	Walsin
57	C57	2.2nF	-
58	C58	100uF	Walsin
59	C59	470pF	-
60	C60	470pF	-
61	C61	100uF	Walsin
62	C62	470pF	-
63	C63	100uF	Walsin
64	C64	100uF	Walsin
65	C65	10nF	-
66	C66	100nF	-
67	C67	100uF	Walsin
68	C68	100uF	Walsin
69	C69	2.2nF	-
70	C70	100uF	Walsin
71	C71	470pF	-
72	C72	470pF	-
73	C73	100uF	Walsin
74	C74	470pF	-
75	C75	100uF	Walsin
76	C76	100uF	Walsin
77	C77	10nF	-
78	C78	22uF	-
79	C79	100uF	Walsin
80	C80	100uF	Walsin
81	C81	2.2nF	-
82	C82	100uF	Walsin
83	C83	470pF	-
84	C84	470pF	-
85	C85	100uF	Walsin
86	C86	470pF	-
87	C87	100uF	Walsin
88	C88	100uF	Walsin
89	C89	10nF	-
90	C90	100nF	-
91	C91	100uF	Walsin
92	C92	100uF	Walsin
93	C93	2.2nF	-
94	C94	100uF	Walsin
95	C95	470pF	-
96	C96	470pF	-

Index	Reference(s)	Value	Manufacturer
97	C97	100uF	Walsin
98	C98	470pF	-
99	C99	100uF	Walsin
100	C100	100uF	Walsin
101	C101	10nF	-
102	C102	100nF	-
103	C103	100nF	-
104	C104	100uF	Walsin
105	C105	100uF	Walsin
106	C106	2.2nF	-
107	C107	100uF	Walsin
108	C108	470pF	-
109	C109	470pF	-
110	C110	100uF	Walsin
111	C111	470pF	-
112	C112	100uF	Walsin
113	C113	100uF	Walsin
114	C114	10nF	-
115	C115	100nF	-
116	C116	100uF	Walsin
117	C117	100uF	Walsin
118	C118	2.2nF	-
119	C119	100uF	Walsin
120	C120	470pF	-
121	C121	470pF	-
122	C122	100uF	Walsin
123	C123	470pF	-
124	C124	100uF	Walsin
125	C125	100uF	Walsin
126	C126	10nF	-
127	C127	100nF	-
128	C128	100uF	Walsin
129	C129	100uF	Walsin
130	C130	2.2nF	-
131	C131	100uF	Walsin
132	C132	470pF	-
133	C133	470pF	-
134	C134	100uF	Walsin
135	C135	470pF	-
136	C136	100uF	Walsin
137	C137	100uF	Walsin
138	C138	10nF	-
139	C139	100nF	-
140	C140	100uF	Walsin
141	C141	100uF	Walsin
142	C142	2.2nF	-
143	C143	100uF	Walsin
144	C144	470pF	-
145	C145	470pF	-
146	C146	100uF	Walsin
147	C147	470pF	-
148	C148	100uF	Walsin
149	C149	100uF	Walsin
150	C150	10nF	-
151	C151	100nF	-

Index	Reference(s)	Value	Manufacturer
152	C152	100uF	Walsin
153	C153	100uF	Walsin
154	C154	2.2nF	-
155	C155	100uF	Walsin
156	C156	470pF	-
157	C157	470pF	-
158	C158	100uF	Walsin
159	C159	470pF	-
160	C160	100uF	Walsin
161	C161	100uF	Walsin
162	C162	10nF	-
163	C163	100nF	-
164	C164	100uF	Walsin
165	C165	100uF	Walsin
166	C166	2.2nF	-
167	C167	100uF	Walsin
168	C168	470pF	-
169	C169	470pF	-
170	C170	100uF	Walsin
171	C171	470pF	-
172	C172	100uF	Walsin
173	C173	100uF	Walsin
174	C174	10nF	-
175	C175	100nF	-
176	C176	100nF	-
177	C177	100nF	-
178	C178	100nF	-
179	C179	100nF	-
180	C180	100nF	-
181	C181	100nF	-
182	C182	10nF	-
183	C183	1uF	-
184	C184	100nF	-
185	C185	100nF	-
186	C186	100nF	-
187	C187	22p	-
188	C188	22p	-
189	C189	100nF	-
190	C190	100nF	-
191	C191	100nF	-
192	C192	100nF	-
193	D1	1SMB5942B-13	Diodes Inc
194	D2	SD560BTR	SMC Diode Solutions
195	D3	LED (Red)	AMS OSRAM
196	D4	LED (Red)	AMS OSRAM
197	D5	NUP2105L	ON Semiconductor
198	D6	LED (Red)	AMS OSRAM
199	D7	LED (Green)	AMS OSRAM
200	D14	CMMHS2-40	Central Semiconductor
201	D15	SDT15H100P5-7	Diodes Inc
202	D16	LED (Red)	AMS OSRAM
203	D17	SDT15H100P5-7	Diodes Inc
204	D18	LED (Red)	AMS OSRAM
205	D19	SDT15H100P5-7	Diodes Inc
206	D20	LED (Red)	AMS OSRAM

Index	Reference(s)	Value	Manufacturer
207	D21	SDT15H100P5-7	Diodes Inc
208	D22	LED (Red)	AMS OSRAM
209	D23	SDT15H100P5-7	Diodes Inc
210	D24	LED (Red)	AMS OSRAM
211	D25	SDT15H100P5-7	Diodes Inc
212	D26	LED (Red)	AMS OSRAM
213	D27	CMMHS2-40	Central Semiconductor
214	D28	SDT15H100P5-7	Diodes Inc
215	D29	LED (Red)	AMS OSRAM
216	D30	SDT15H100P5-7	Diodes Inc
217	D31	LED (Red)	AMS OSRAM
218	D32	SDT15H100P5-7	Diodes Inc
219	D33	LED (Red)	AMS OSRAM
220	D34	SDT15H100P5-7	Diodes Inc
221	D35	LED (Red)	AMS OSRAM
222	D36	SDT15H100P5-7	Diodes Inc
223	D37	LED (Red)	AMS OSRAM
224	D38	SDT15H100P5-7	Diodes Inc
225	D39	LED (Red)	AMS OSRAM
226	D40	LED (Blue)	Lumex
227	D41	LED (Red)	AMS OSRAM
228	D42	LED (Blue)	Lumex
229	D43	LED (Orange)	AMS OSRAM
230	D44	LED (Orange)	AMS OSRAM
231	F1	Polyfuse 1A	Littelfuse
232	F2	Fuse	Vishay
233	F3	Fuse	Vishay
234	F4	Fuse	Vishay
235	F5	Fuse	Vishay
236	F6	Fuse	Vishay
237	F7	Fuse	Vishay
238	F8	Fuse	Vishay
239	F9	Fuse	Vishay
240	F10	Fuse	Vishay
241	F11	Fuse	Vishay
242	F12	Fuse	Vishay
243	F13	Fuse	Vishay
244	F14	Fuse	Vishay
245	FB1	Ferrite Bead	TDK
246	IC1	ADS7028QRTERQ1	Texas Instruments
260	K1	G5V-2 DC-3	Omron
261	L1	7.44E+08	Wurth
262	L2	0ZCF0100AF2A	EPCOS - TDK
263	PS1	R2S-053.3	RECOM
264	PS2	R2S-0505	-
265	Q1	CZT5551	Central Semiconductor
266	Q2	BSS308PE	Infineon Technologies
267	Q5	BSS308PE	Infineon Technologies
268	Q8	BSS308PE	Infineon Technologies
269	Q11	BSS308PE	Infineon Technologies
270	Q14	BSS308PE	Infineon Technologies
271	Q17	BSS308PE	Infineon Technologies
272	Q20	BSS308PE	Infineon Technologies
273	Q23	BSS308PE	Infineon Technologies
274	Q26	BSS308PE	Infineon Technologies

Index	Reference(s)	Value	Manufacturer
275	Q29	BSS308PE	Infineon Technologies
276	Q32	BSS308PE	Infineon Technologies
277	Q35	BSS308PE	Infineon Technologies
278	Q38	BC817	Nexperia
279	R1	2.2kR	-
280	R2	2.2kR	-
281	R3	60R	-
282	R4	60R	-
283	R5	0R	-
284	R6	10kR	-
285	R7	51kR	-
286	R8	10kR	-
287	R9	51kR	-
288	R10	10kR	-
289	R11	51kR	-
290	R12	10kR	-
291	R13	51kR	-
292	R14	10kR	-
293	R15	51kR	-
294	R16	10kR	-
295	R17	51kR	-
296	R18	10kR	-
297	R19	51kR	-
298	R20	10kR	-
299	R21	51kR	-
300	R22	1MR	-
301	R23	DNP	-
302	R24	DNP	-
303	R25	100R	-
304	R26	100R	-
305	R27	6.81R	-
306	R28	1MR	-
307	R29	23.7kR	-
308	R30	33.2kR	-
309	R31	330R	-
310	R32	470R	-
311	R33	3.3kR	-
312	R34	5.1R	-
313	R35	20R	-
314	R36	20R	-
315	R37	25mR	-
316	R38	20R	-
317	R39	25mR	-
318	R40	20R	-
319	R41	5.1R	-
320	R42	100R	-
321	R43	330R	-
322	R44	470R	-
323	R45	3.3kR	-
324	R46	5.1R	-
325	R47	20R	-
326	R48	20R	-
327	R49	25mR	-
328	R50	20R	-
329	R51	25mR	-

Index	Reference(s)	Value	Manufacturer
330	R52	20R	-
331	R53	5.1R	-
332	R54	100R	-
333	R55	330R	-
334	R56	470R	-
335	R57	3.3kR	-
336	R58	5.1R	-
337	R59	20R	-
338	R60	20R	-
339	R61	25mR	-
340	R62	20R	-
341	R63	25mR	-
342	R64	20R	-
343	R65	5.1R	-
344	R66	100R	-
345	R67	330R	-
346	R68	470R	-
347	R69	3.3kR	-
348	R70	5.1R	-
349	R71	20R	-
350	R72	20R	-
351	R73	25mR	-
352	R74	20R	-
353	R75	25mR	-
354	R76	20R	-
355	R77	5.1R	-
356	R78	100R	-
357	R79	330R	-
358	R80	470R	-
359	R81	3.3kR	-
360	R82	5.1R	-
361	R83	20R	-
362	R84	20R	-
363	R85	25mR	-
364	R86	20R	-
365	R87	25mR	-
366	R88	20R	-
367	R89	5.1R	-
368	R90	100R	-
369	R91	330R	-
370	R92	470R	-
371	R93	3.3kR	-
372	R94	5.1R	-
373	R95	20R	-
374	R96	20R	-
375	R97	25mR	-
376	R98	20R	-
377	R99	25mR	-
378	R100	20R	-
379	R101	5.1R	-
380	R102	100R	-
381	R103	50k DNP	-
382	R104	50k DNP	-
383	R105	50k DNP	-
384	R106	50k DNP	-

Index	Reference(s)	Value	Manufacturer
385	R107	50k DNP	-
386	R108	50k DNP	-
387	R109	50k DNP	-
388	R110	50k DNP	-
389	R111	50k DNP	-
390	R112	50k DNP	-
391	R113	50k DNP	-
392	R114	50k DNP	-
393	R115	50k DNP	-
394	R116	50k DNP	-
395	R117	50k DNP	-
396	R118	50k DNP	-
397	R119	50k DNP	-
398	R120	50k DNP	-
399	R121	50k DNP	-
400	R122	50k DNP	-
401	R123	50k DNP	-
402	R124	50k DNP	-
403	R125	50k DNP	-
404	R126	50k DNP	-
405	R127	6.81R	-
406	R128	1MR	-
407	R129	23.7kR	-
408	R130	33.2kR	-
409	R131	330R	-
410	R132	470R	-
411	R133	3.3kR	-
412	R134	5.1R	-
413	R135	20R	-
414	R136	20R	-
415	R137	25mR	-
416	R138	20R	-
417	R139	25mR	-
418	R140	20R	-
419	R141	5.1R	-
420	R142	100R	-
421	R143	330R	-
422	R144	470R	-
423	R145	3.3kR	-
424	R146	5.1R	-
425	R147	20R	-
426	R148	20R	-
427	R149	25mR	-
428	R150	20R	-
429	R151	25mR	-
430	R152	20R	-
431	R153	5.1R	-
432	R154	100R	-
433	R155	330R	-
434	R156	470R	-
435	R157	3.3kR	-
436	R158	5.1R	-
437	R159	20R	-
438	R160	20R	-
439	R161	25mR	-

Index	Reference(s)	Value	Manufacturer
440	R162	20R	-
441	R163	25mR	-
442	R164	20R	-
443	R165	5.1R	-
444	R166	100R	-
445	R167	330R	-
446	R168	470R	-
447	R169	3.3kR	-
448	R170	5.1R	-
449	R171	20R	-
450	R172	20R	-
451	R173	25mR	-
452	R174	20R	-
453	R175	25mR	-
454	R176	20R	-
455	R177	5.1R	-
456	R178	100R	-
457	R179	330R	-
458	R180	470R	-
459	R181	3.3kR	-
460	R182	5.1R	-
461	R183	20R	-
462	R184	20R	-
463	R185	25mR	-
464	R186	20R	-
465	R187	25mR	-
466	R188	20R	-
467	R189	5.1R	-
468	R190	100R	-
469	R191	330R	-
470	R192	470R	-
471	R193	3.3kR	-
472	R194	5.1R	-
473	R195	20R	-
474	R196	20R	-
475	R197	25mR	-
476	R198	20R	-
477	R199	25mR	-
478	R200	20R	-
479	R201	5.1R	-
480	R202	100R	-
481	R203	51kR	-
482	R204	10kR	-
483	R205	51kR	-
484	R206	100R	-
485	R207	100R	-
486	R208	100R	-
487	R209	100R	-
488	R210	100R	-
489	R211	100R	-
490	R212	100R	-
491	R213	100R	-
492	R214	100R	-
493	R215	100R	-
494	R216	100R	-

Index	Reference(s)	Value	Manufacturer
495	R217	100R	-
496	R218	100R	-
497	R219	100R	-
498	R220	100R	-
499	R221	100R	-
500	R222	100R	-
501	R223	100R	-
502	R224	100R	-
503	R225	100R	-
504	R226	100R	-
505	R227	100R	-
506	R228	100R	-
507	R229	100R	-
508	R230	100R	-
509	R231	100R	-
510	R232	100R	-
511	R233	100R	-
512	R234	100R	-
513	R235	100R	-
514	R236	100R	-
515	R237	100R	-
516	R238	100R	-
517	R239	100R	-
518	R240	100R	-
519	R241	100R	-
520	R242	2.2kR	-
521	R243	2.2kR	-
522	R244	2.2kR	-
523	R245	2.2kR	-
524	R246	2.2kR	-
525	R247	51kR	-
526	R248	0R	-
527	R249	51kR	-
528	R250	51kR	-
529	R251	2.2kR	-
530	R252	0R DNP	-
531	R253	2.2kR	-
532	SW1	SW_Push	XKB
533	T1	7.5E+08	Wurth
534	T2	7.5E+08	Wurth
535	T3	7.5E+08	Wurth
536	T4	7.5E+08	Wurth
537	T5	7.5E+08	Wurth
538	T6	7.5E+08	Wurth
539	T7	7.5E+08	Wurth
540	T8	7.5E+08	Wurth
541	T9	7.5E+08	Wurth
542	T10	7.5E+08	Wurth
543	T11	7.5E+08	Wurth
544	T12	7.5E+08	Wurth
545	T13	BUK9K13-60EX	-
546	T14	BUK9K13-60EX	-
547	T15	BUK9K13-60EX	-
548	T16	BUK9K13-60EX	-
549	T17	BUK9K13-60EX	-

Index	Reference(s)	Value	Manufacturer
550	T18	BUK9K13-60EX	-
551	T19	BUK9K13-60EX	-
552	T20	BUK9K13-60EX	-
553	T21	BUK9K13-60EX	-
554	T22	BUK9K13-60EX	-
555	T23	BUK9K13-60EX	-
556	T24	BUK9K13-60EX	-
557	U1	R-78C5.0-1.0	RECOM
558	U2	ISO1042DWVR	Texas Instruments
559	U3	LTC6811HG-2#PBF	Linear Technology
560	U4	LTC3300ILXE-2#PBF	Linear Technology
561	U5	LTC3300ILXE-2#PBF	Linear Technology
562	U6	ADuM7641A	-
563	U7	ADuM7641A	-
564	U8	ADuM7641A	-
565	U9	STM32F103C8Tx	ST Microelectronics
566	Y1	16MHz	ABRACON

C. Code

1) main.cpp

```

1  #include <Arduino.h>
2  #include "bms_lmu.h"
3  #include "SPI.h"
4  #include <eXoCAN.h>
5  #include "TickerInterrupt.h"
6  #include "PBalancer.h"

7
8  /*****
9   * BMS_LMU - HARDWARE REVISION 0
10  * Patrick Curtain & Ethan Suter
11  *
12  * Battery Management System - Local Measurement Unit
13  *
14  * An active balancer created for FYRP by Patrick Curtain and Ethan Suter,
15  * Semester 2 2021 and Semester 1 2022, at Swinburne University of Technology.
16  *
17  * Code base derived from Team Swinburne FSAE
18  * Available: https://github.com/Team-Swinburne/ts\_20-code-development
19  *
20  * Revision      Date      Comments
21  * -----        -----    -----
22  * 0.0          28/5/2022  Patrick Curtain Initial Code Base
23  *
24  *
25  *****/
26
27 #define HW_REV "0"
28 #define SW_REV "0.0"

29
30 // PINOUT
31 #define LED0 PC13
32 #define CAN_TX_LED PB5
33 #define CAN_RX_LED PB6
34 #define SPI_TX_LED PB7
35 #define SPI_RX_LED PB8
36 #define FAULT_RELAY PA9
37 #define FAULT_RELAY_FEEDBACK PA10

38
39 // NOT SAFETY PARAMETERS
40 #define DISCHARGE_TIMER_LIMIT 1000
41 #define HEART_RATE 1000
42 #define CAN_INTERVAL 800

```

```

43 #define CANBUS_FREQUENCY 250000
44
45 #define TX_ADDRESS 0x481
46
47 // led pins
48 DigitalOut can_tx_led(CAN_TX_LED);
49 DigitalOut can_rx_led(CAN_RX_LED);
50 DigitalOut spi_tx_led(CAN_TX_LED);
51 DigitalOut spi_rx_led(CAN_RX_LED);
52
53 // Globals
54 Heartbeat heartbeat(FAULT_RELAY, FAULT_RELAY_FEEDBACK, LED0);
55 Stack stack;
56 PBalancer passive_balancer(stack, DISCHARGE_TIMER_LIMIT);
57
58 DigitalOut temp_sensor_ss(PA0);
59 DigitalOut active_balance_upper_ss(PB0);
60 DigitalOut active_balance_lower_ss(PB4);
61 DigitalOut passive_balance_ss(PA1);
62
63 // Interfaces
64 eXOCAN can;
65
66 // Timers
67 TickerInterrupt ticker(TIM2, 1);
68
69 struct msg_frame
70 {
71     uint8_t len = 8;
72     uint8_t bytes[8] = {0};
73 };
74
75 static msg_frame heart_frame {.len = 3},
76                 bms_lower_bank {.len = 6},
77                             bms_upper_bank {.len = 6},
78                 temperature {.len = 8};
79
80 uint8_t rxData[8];
81
82 void can_tx() {
83     can.transmit(TX_ADDRESS, heart_frame.bytes, heart_frame.len);
84     can.transmit(TX_ADDRESS + 1, bms_lower_bank.bytes, bms_lower_bank.len);
85     can.transmit(TX_ADDRESS + 2, bms_upper_bank.bytes, bms_upper_bank.len);
86     can.transmit(TX_ADDRESS + 3, temperature.bytes, temperature.len);
87
88     can_tx_led = !can_tx_led;
89 }
90
91 // Can receive interrupt service routine
92 void canISR() {
93     can.rxMsgLen = can.receive(can.id, can.flIdx, can.rxData.bytes);
94 }
95
96
97 void can_rx() {
98     if (can.rxMsgLen > -1) {
99         can_rx_led = !can_rx_led;
100    }
101 }
102
103 uint8_t array_to_uint8(bool arr[], int count) {
104     int ret = 0;
105     int tmp;
106     for (int i = 0; i < count; i++) {
107         tmp = arr[i];
108         ret |= tmp << (count - i - 1);
109     }
110     return ret;
111 }

```

```

112
113 uint16_t check_errors() {
114     bool error_code[8];
115
116     error_code[ERROR_OV_FAULT] = stack.ov_fault();
117     error_code[ERROR_UV_FAULT] = stack.uv_fault();
118     // error_code[ERROR_OT_FAULT] = !imd.get_IMD_ok();
119     error_code[ERROR_RELAY_FAULT] = heartbeat.relay_fault();
120
121     // error_code[ERROR_ORION_LOW_VOLTAGE]      = orion.check_low_voltage();
122     // error_code[ERROR_ORION_HIGH_VOLTAGE]       = orion.check_high_voltage();
123     // error_code[ERROR_ORION_OVERTEMPERATURE] = orion.check_overtemperature();
124     // error_code[ERROR_PERIPHERALS] = 0;
125
126     return array_to_uint8(error_code, 8);
127 }
128
129 void update_can_frames() {
130     heart_frame.bytes[0] = heartbeat.state();
131     heart_frame.bytes[0] = heartbeat.counter();
132     heart_frame.bytes[1] = heartbeat.fault_code();
133
134     for (int i = 0; i < 6; i++) {
135         bms_lower_bank.bytes[i] = stack.cell_voltage(i);
136     }
137
138     for (int i = 6; i < 12; i++) {
139         bms_upper_bank.bytes[i] = stack.cell_voltage(i);
140     }
141
142     // add in the temp measurement thing.
143 }
144
145 void state_d() {
146
147     update_can_frames();
148     heartbeat.fault_code(check_error());
149
150     switch(heartbeat.state()) {
151
152         case (FAULT):
153             // do nothing, clear the error as quickly
154             // as possible.
155             if (check_errors() == 0) {
156                 heartbeat.state(IDLE);
157             }
158             break;
159
160         case (IDLE):
161             // literally do nothing!
162             break;
163
164         case (ACTIVE_BALANCING):
165             // not sure yet!
166             // push into passive state once done
167             break;
168
169         case (PASSIVE_BALANCING):
170             passive_balancer.start_balance();
171             break;
172
173     }
174 }
175
176 void start_up_lights() {
177     pinMode(PB5, OUTPUT);
178     pinMode(PB6, OUTPUT);
179     pinMode(PB7, OUTPUT);
180     pinMode(PB8, OUTPUT);

```

```

181
182     int scroller_time = 100;
183     digitalWrite(PB5, HIGH);
184     delay(scroller_time);
185     digitalWrite(PB6, HIGH);
186     delay(scroller_time);
187     digitalWrite(PB7, HIGH);
188     delay(scroller_time);
189     digitalWrite(PB8, HIGH);
190     delay(scroller_time);
191
192     digitalWrite(PB5, LOW);
193     delay(scroller_time);
194     digitalWrite(PB6, LOW);
195     delay(scroller_time);
196     digitalWrite(PB7, LOW);
197     delay(scroller_time);
198     digitalWrite(PB8, LOW);
199     delay(scroller_time);
200 }
201
202
203 // timer functions
204 void heartbeat_cb() {
205     heartbeat.tick(check_errors());
206 }
207
208 void setup() {
209
210     // setup the serial.
211     Serial.begin(9600);
212     Serial.print("Starting BMS-LMU \n");
213     Serial.print(" HARDWARE REVISION - 0\n");
214     Serial.print(" SOFTWARE REVISION - 0.0\n\n");
215     Serial.print("Swinburne University of Technology
216 - FYRP40002\n Patrick Curtain & Ethan Suter\n");
217
218     // setup the can
219     can.begin(STD_ID_LEN, CANBUS_FREQUENCY, PORTA_11_12_WIRE_PULLUP);      //11 Bit Id, 500Kbps
220     // can.filterMask16Init(0, 0x600, 0x7ff);
221     can.attachInterrupt(canISR);
222
223     // setup heartbeat tickers.
224     ticker.start();
225     ticker.attach(heartbeat_cb, HEART_RATE);
226
227     // start up the pbalance
228     passive_balancer.setup();
229
230     ticker.attach(can_tx, CAN_INTERVAL);
231
232     // finished boot, flash the lights to confirm startup!
233     start_up_lights();
234     Serial.print("Finished boot! Starting\n");
235
236     Serial.begin(9600);
237
238     #define adSS PA0
239     pinMode(adSS, OUTPUT);
240     digitalWrite(adSS, HIGH);
241
242     SPI.begin();
243 }
244
245
246 void loop() {
247     state_d();
248 }
```

2) bms-lmu.h

```
1 #include <stdint.h>
2 #include "Linduino.h"
3 #include "SPI.h"
4 #include "LT_SPI.h"
5 #include "LTC6811.h"
6 #include "LTC681x.h"
7
8 #define STACK_SIZE 12
9
10 // SAFETY PARAMETERS!
11 #define MAX_VOLTAGE 4.2
12 #define MIN_VOLTAGE 2.8
13 #define MAX_TEMPERATURE 60
14
15
16 class Stack {
17     private:
18         uint16_t cells[STACK_SIZE];
19
20     public:
21         bool update_cell(int pos, uint16_t cell_voltage) {
22             if (pos >= STACK_SIZE || pos < 0) {
23                 return false;
24             } else {
25                 cells[pos] = cell_voltage;
26                 return true;
27             }
28         }
29
30         uint16_t min() {
31             uint16_t lowest_cell = cells[0];
32             for (int i = 0; i < STACK_SIZE; i++) {
33                 if (lowest_cell > cells[i]) {
34                     lowest_cell = cells[i];
35                 }
36             }
37             return lowest_cell;
38         }
39
40         uint16_t max() {
41             uint16_t highest_cell = cells[0];
42             for (int i = 0; i < STACK_SIZE; i++) {
43                 if (highest_cell < cells[i]) {
44                     highest_cell = cells[i];
45                 }
46             }
47             return highest_cell;
48         }
49
50         float average() {
51             return (float)sum_stack_voltage() / STACK_SIZE;
52         }
53
54         int sum_stack_voltage() {
55             int sum = 0;
56             for (int i = 0; i < STACK_SIZE; i++) {
57                 sum = sum + cells[i];
58             }
59             return sum;
60         }
61
62         bool ov_fault() {
63             return (max() > MAX_VOLTAGE);
64         }
65
66         bool uv_fault() {
67             return (min() < MIN_VOLTAGE);
```

```

68     }
69
70     uint16_t cell_voltage(int cell_number){
71         return cells[cell_number];
72     }
73 }

```

3) *pbalancer.h*

```

1  // Ethan Suter
2  #ifndef PBALANCER_H
3  #define PBALANCER_H
4
5  #include "Stack.h"
6  #include <Arduino.h>
7
8  class PBalancer
9  {
10     private:
11     Stack _stack;
12     uint16_t over_v_cell_limit;
13     uint16_t under_v_cell_limit;
14     uint16_t discharge_time_limit;
15
16     public:
17     PBalancer();
18     PBalancer(Stack _stk, uint16_t ov, uint16_t uv, uint16_t dtl);
19     void start_balance(int cell);
20     void end_balance();
21     Stack measure();
22     bool pbalance_ok();
23 }
24
25
26 #endif

```

4) *pbalancer.cpp*

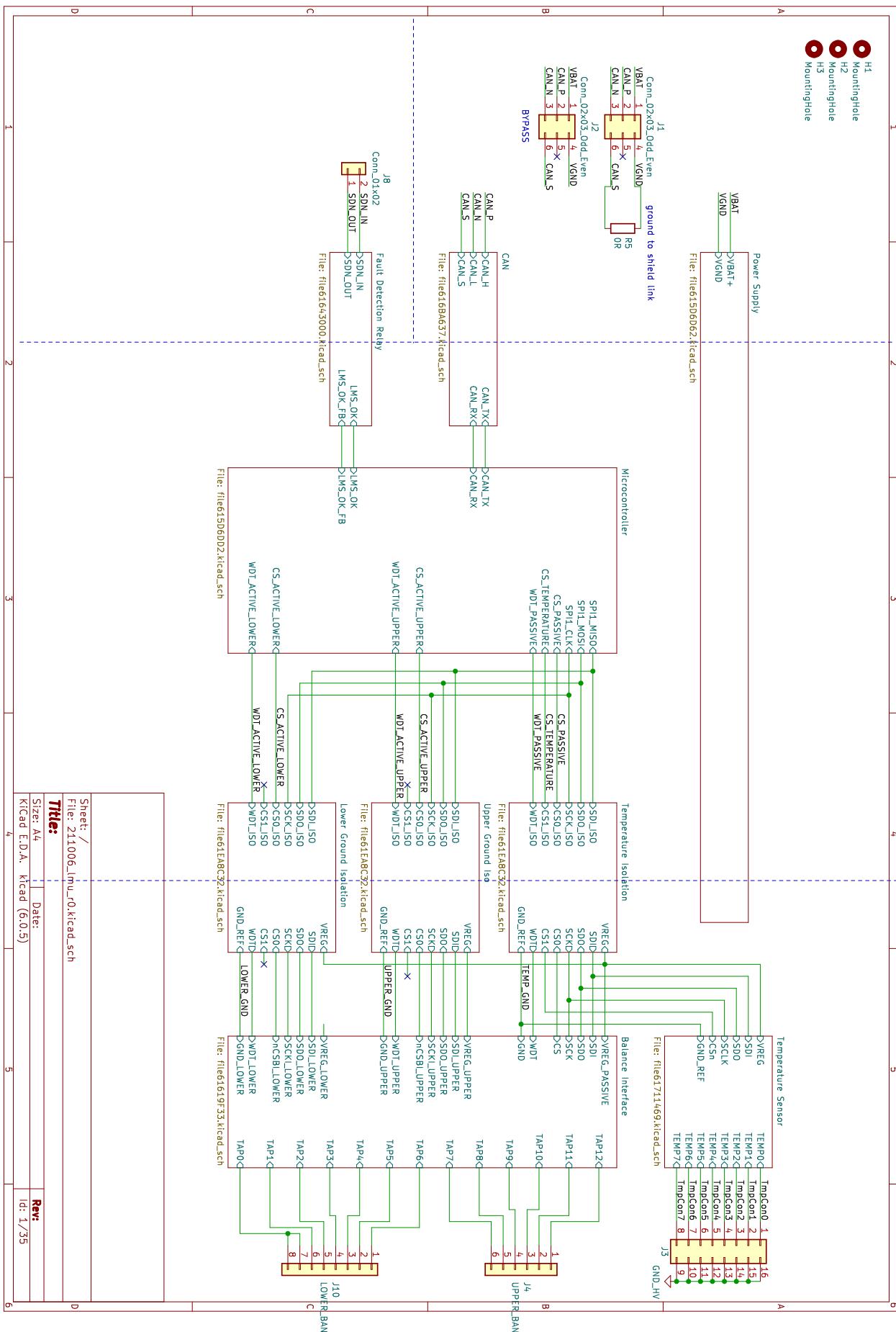
```

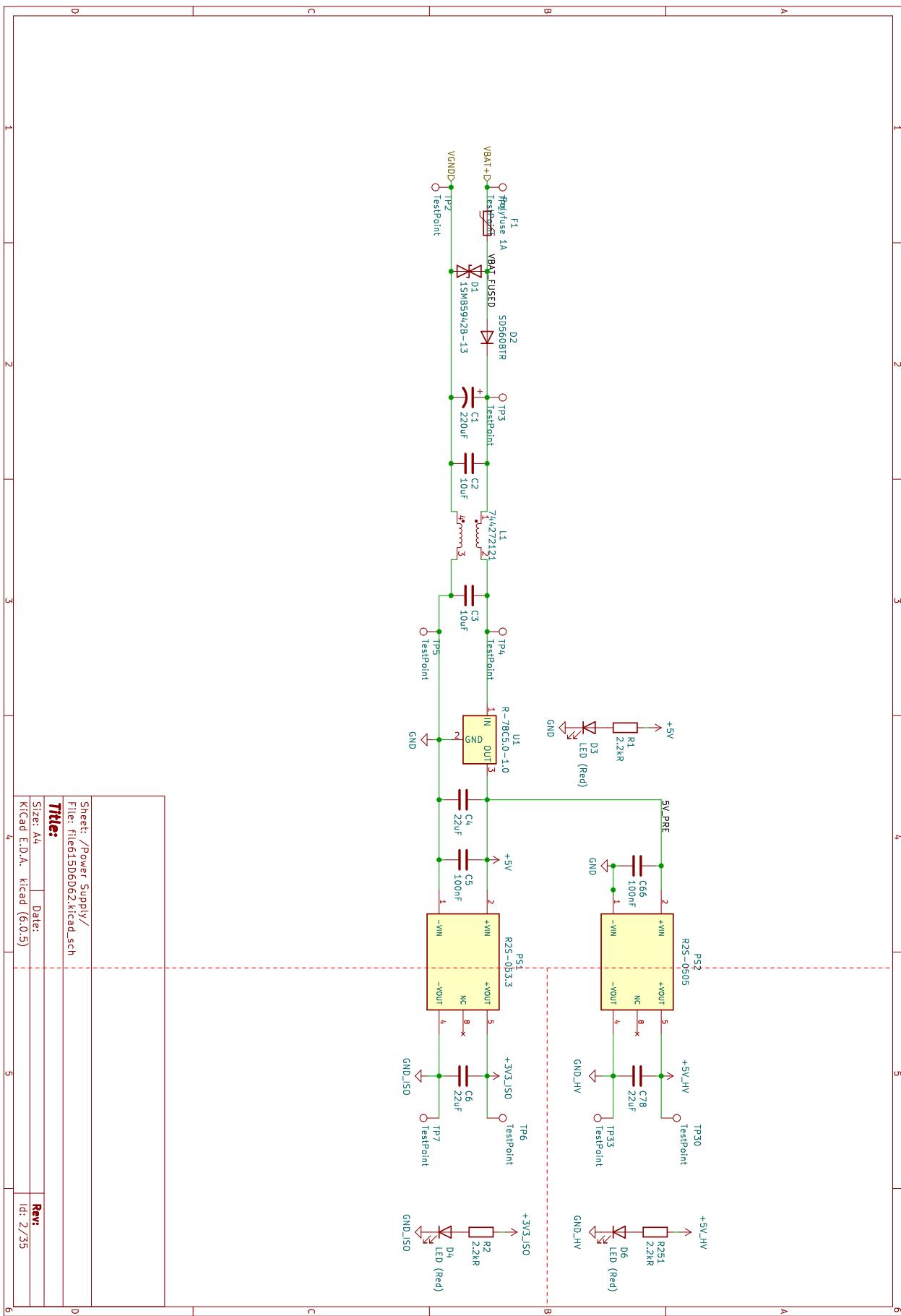
1  #include "PBalancer.h"
2  // Ethan Suter
3
4
5  // Default Constructor
6  PBalancer::PBalancer() {}
7
8  // Constructor Override
9  PBalancer::PBalancer(Stack _stk, uint16_t ov, uint16_t uv, uint16_t dtl){
10    _stack = _stk;
11    over_v_cell_limit = ov;
12    under_v_cell_limit = uv;
13    discharge_time_limit = dtl;
14 }
15
16 void PBalancer::start_balance(int cell)
17 {
18
19    // Enable a discharge transistor
20    Serial.print(F("Discharging cell: "));
21    readIC = cell;
22    Serial.println(readIC);
23    wakeup_sleep(TOTAL_IC);
24    LTC6811_set_discharge(readIC, TOTAL_IC, bms_ic);
25    LTC6811_wrcfg(TOTAL_IC, bms_ic);
26    print_config();
27    wakeup_idle(TOTAL_IC);
28    error = LTC6811_rdcfg(TOTAL_IC, bms_ic);
29    check_error(error);
30    print_rxconfig();

```

```
31     }
32
33 void PBalancer::end_balance()
34 {
35     // Clear all discharge transistors
36     wakeup_sleep(TOTAL_IC);
37     LTC6811_clear_discharge(TOTAL_IC,bms_ic);
38     LTC6811_wrcfg(TOTAL_IC,bms_ic);
39     print_config();
40     wakeup_idle(TOTAL_IC);
41     error = LTC6811_rdcfg(TOTAL_IC,bms_ic);
42     check_error(error);
43     print_rxconfig();
44 }
45
46 Stack PBalancer::measure()
47 {
48     _stk.update_stack();
49     return _stk;
50 }
51
52 bool PBalancer::pbalance_ok()
53 {
54     // Uses same format as OV_THRESHOLD and UV_THRESHOLD in LTC Code
55     const uint16_t BAL_THRESHOLD = 50; //!< ADC Code. LSB = 0.0001 -> So 50 represents 5mV
56     if (_stk.max() - _stk.min() <= BAL_THRESHOLD)
57     {
58         return true;
59     }
60     else
61     {
62         return false;
63     }
64 }
```

D. Schematics





Sheet: /Power_Supply/
File: file615D062.kicad_sch

Title:

Size: A4 Date:

Rev:

Kicad E.DA, kicad (6.0.5)

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