Trinity College Dublin

The University of Dublin

Assignment 2

Submitted To:

Prof. Shreejith Shankar

Digital System Design 3C7

Submitted By:

Parul Kumari

TCD ID: 21356575

Details:

Board No.: Basys3101

Width: 17

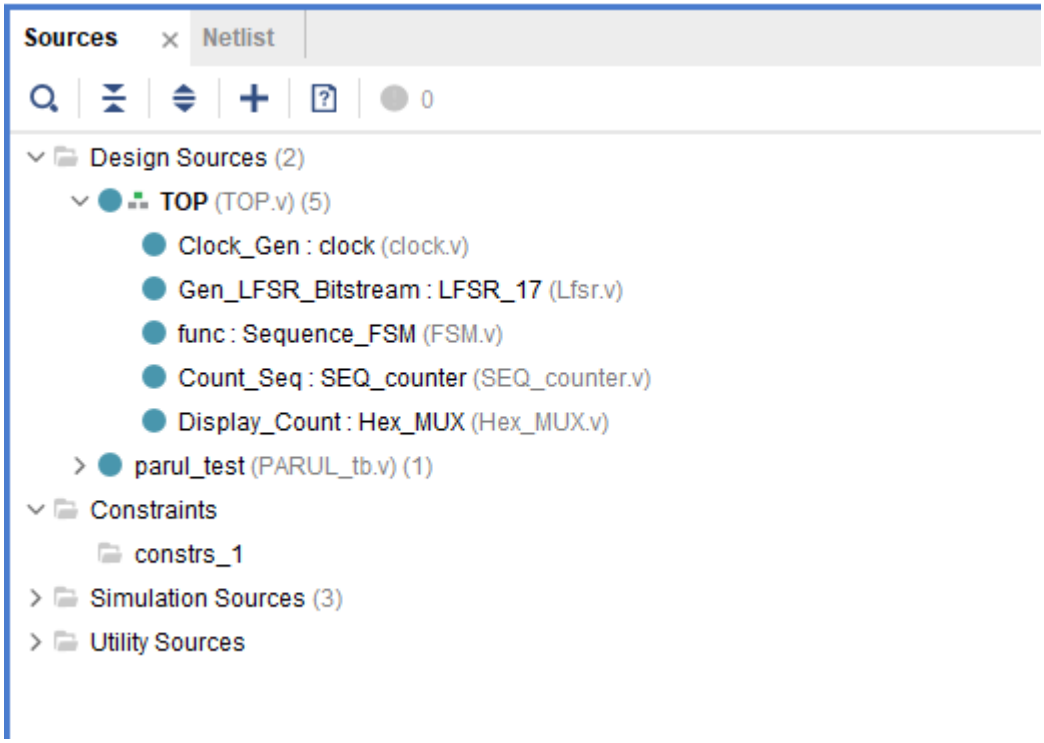
Feedback: XNOR

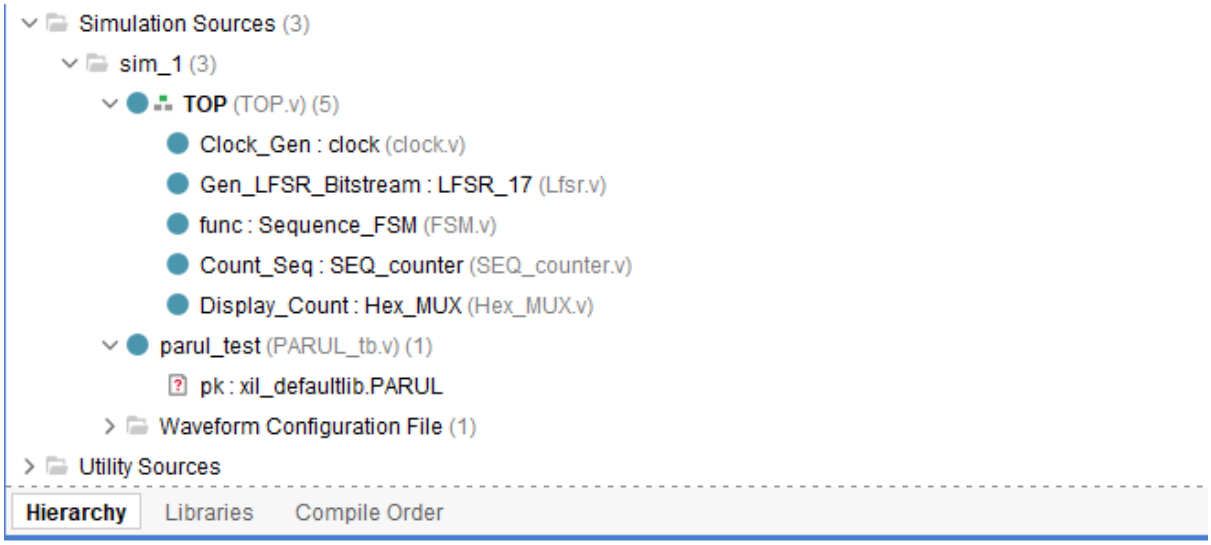
FSM Pattern: 100010000111

LFSR SEED: 1101100011110010

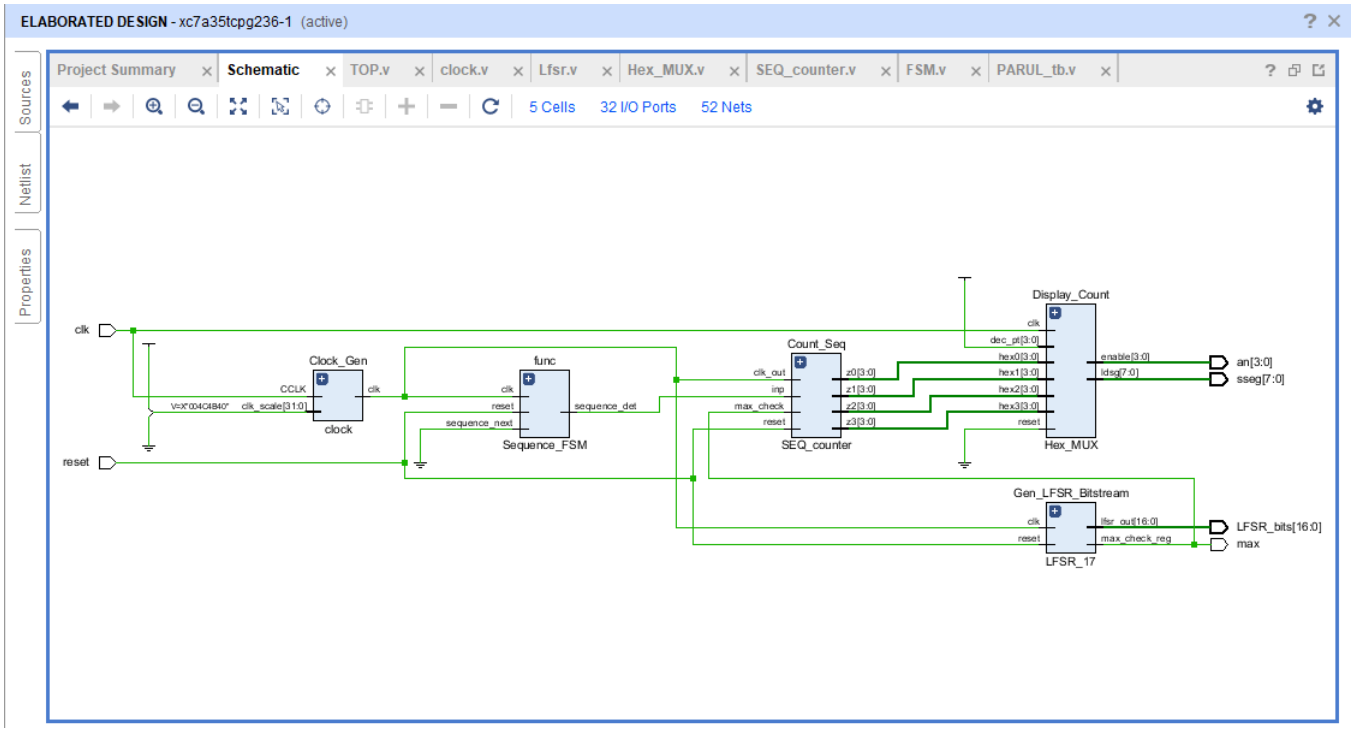
AIM: The purpose of this session is to bring together elements from all your Labs, but particularly Lab F-G, and give you experience with developing and testing a larger sequential design and targeting it to the FPGA board.

Sources:

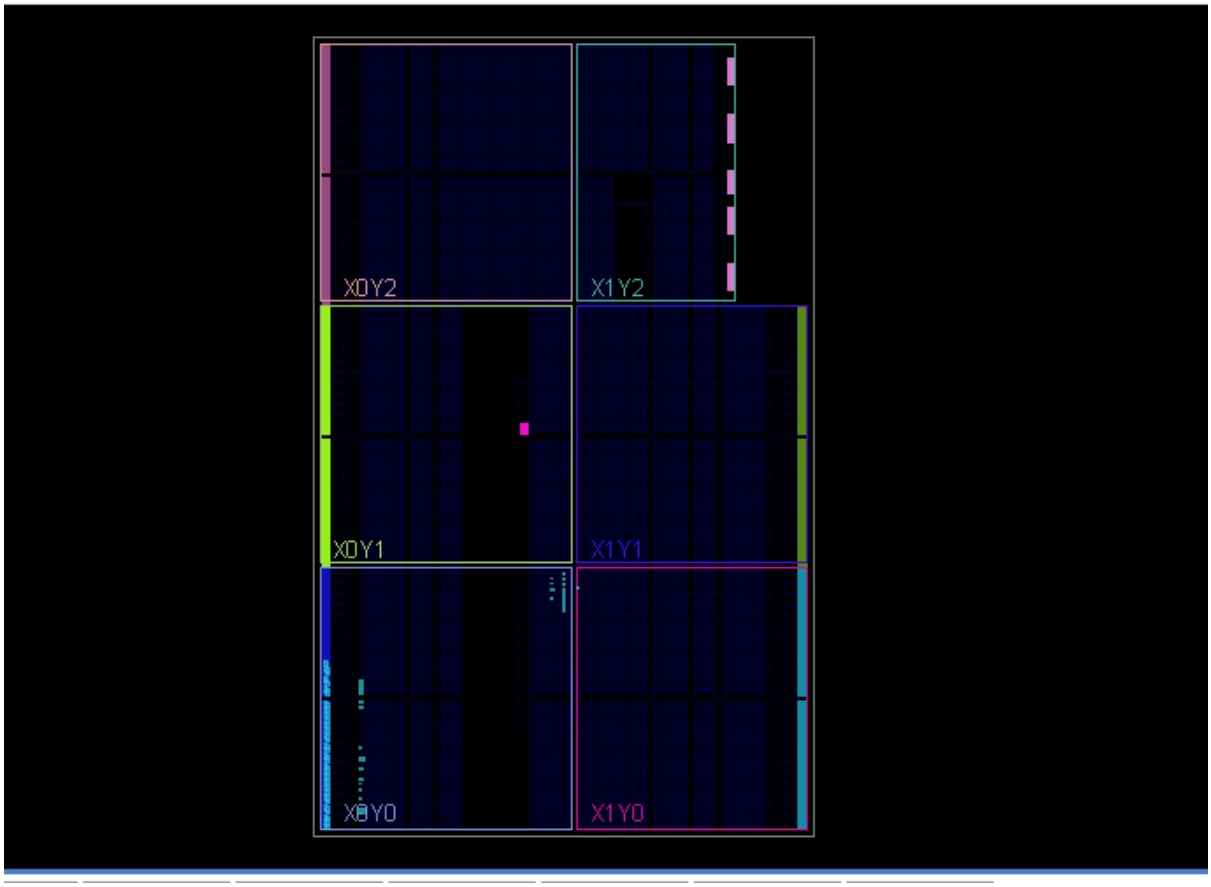




Schematic diagram:

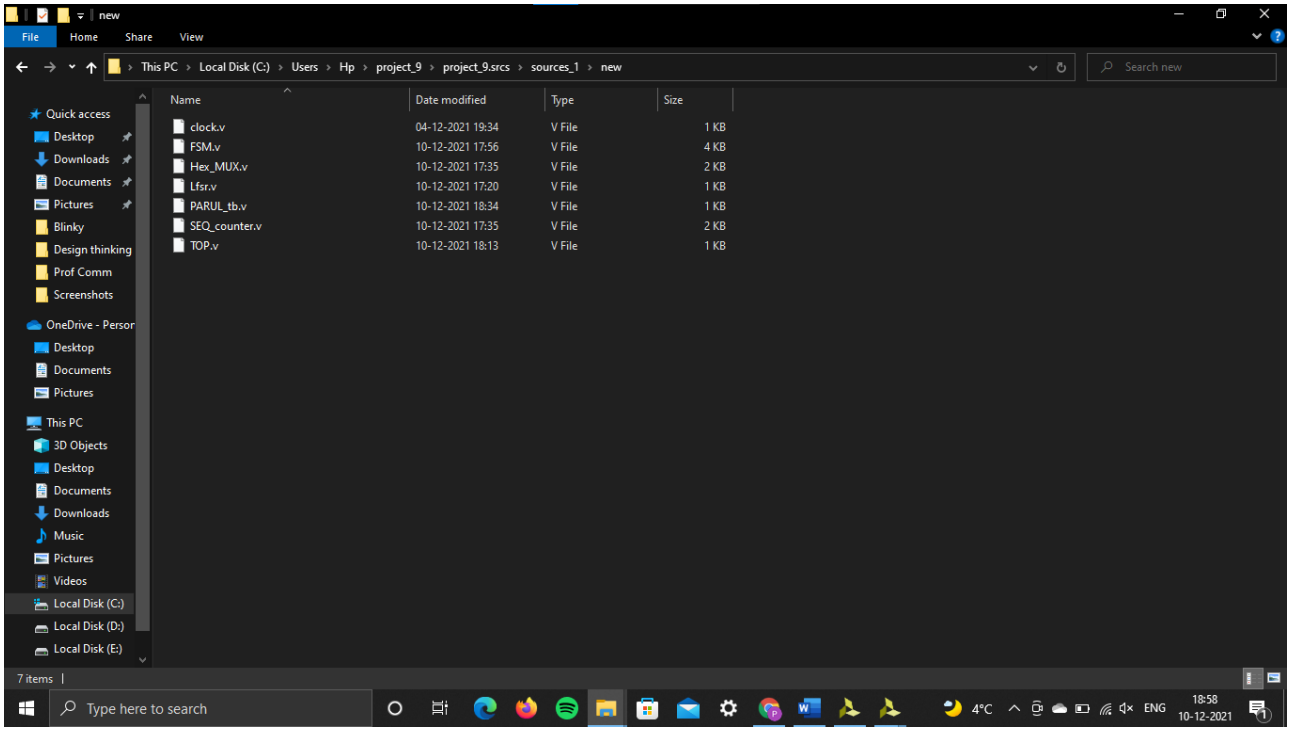


Elaborated design

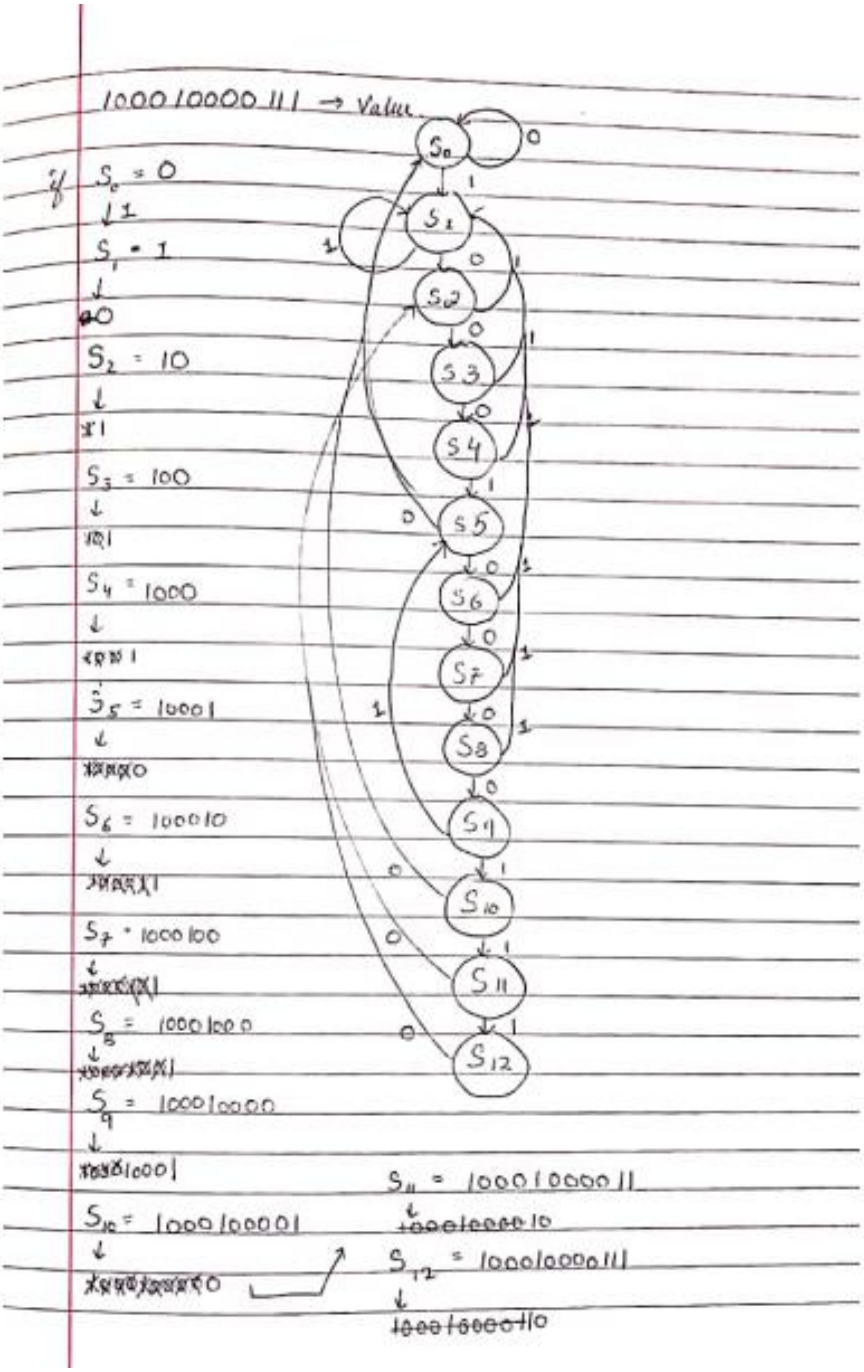


Synthesized design

FILES:


new
File
Home
Share
View
This PC › Local Disk (C:) › Users › Hp › project_9 › project_9.srcs › sources_1 › new
Search new
Quick access
Desktop
Downloads
Documents
Pictures
Blinky
Design thinking
Prof Comm
Screenshots
OneDrive - Persor
Desktop
Documents
Pictures
This PC
3D Objects
Desktop
Documents
Downloads
Music
Pictures
Videos
Local Disk (C:)
Local Disk (D:)
Local Disk (E:)
Name
Date modified
Type
Size
clock.v 04-12-2021 19:34 V File 1 KB
FSM.v 10-12-2021 17:56 V File 4 KB
Hex_MUX.v 10-12-2021 17:35 V File 2 KB
Lfsr.v 10-12-2021 17:20 V File 1 KB
PARUL_tb.v 10-12-2021 18:34 V File 1 KB
SEQ_counter.v 10-12-2021 17:35 V File 2 KB
TOP.v 10-12-2021 18:13 V File 1 KB
7 items
Type here to search
4°C
ENG
18:58
10-12-2021

FSM Diagram:


1000100000111 → Value.
If S0 = 0
↓ 1
S1 = 1
↓
10
S2 = 10
↓
101
S3 = 100
↓
1001
S4 = 1000
↓
10001
S5 = 10001
↓
100010
S6 = 100010
↓
1000101
S7 = 1000100
↓
10001001
S8 = 10001000
↓
100010001
S9 = 100010000
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S10 = 1000100001
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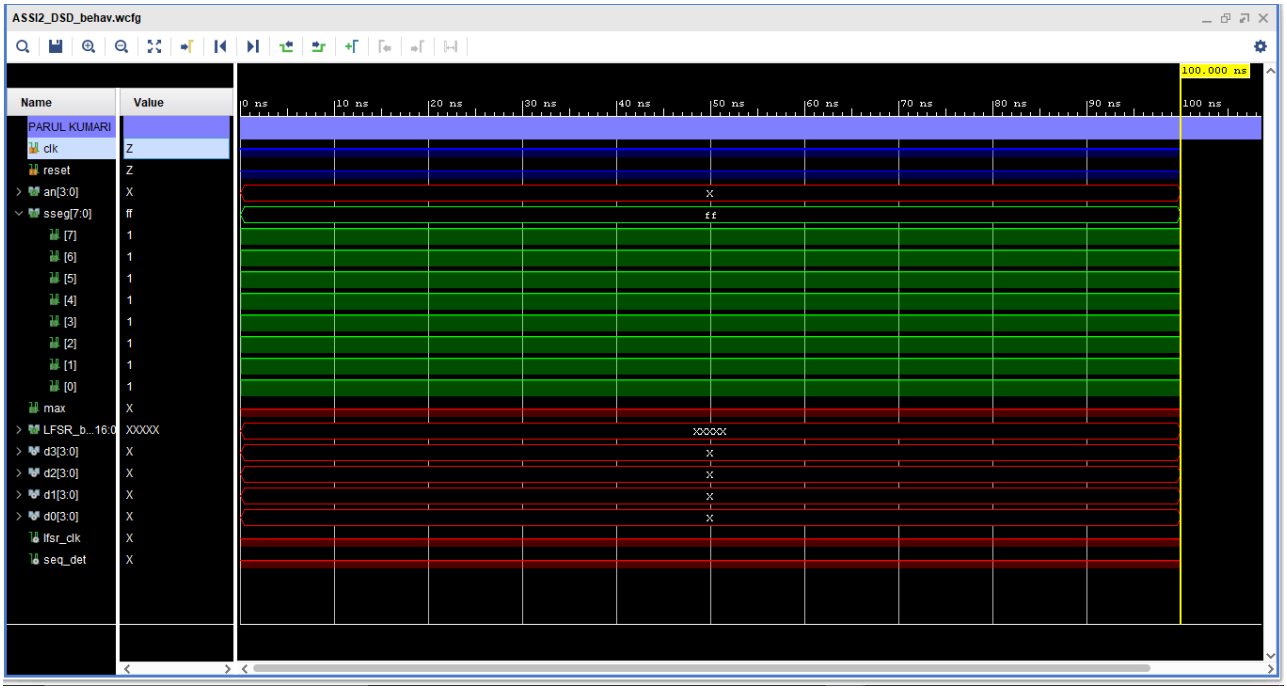
10001000010
S11 = 10001000011
↓
100010000110
S12 = 10001000011
↓
100010000110
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12

WAVEform:



Testbench:

PARUL_tb.v

C:/Users/Hp/project_9/project_9.srcs/sources_1/new/PARUL_tb.v

```
1  `timescale 1ns/1ps
2
3  module parul_test(
4  );
5  wire[16:0] out;
6  reg clk, reset;
7  wire max;
8  wire seq_det;
9  wire [3:0] b3, b2,b1,b0;
10
11 PARUL pk (.clk(clk),.reset(reset),.LFSR_bits(out),.max(max),.d3(b3),.d2(b2),.d1(b1),.d0(b0));
12
13
14 always
15     begin
16         clk = 1'b1;
17         #50;
18         clk = 1'b0;
19         #50;
20     end
21
22     initial
23     begin
24         reset = 1'b1;
25         #100
26          reset = 1'b0;
27     end
28 endmodule
```