Instruction_fetch.v

This Verilog module implements the Instruction Fetch (IF) stage of a MIPS pipeline processor. Its main responsibilities are:

- Maintaining the Program Counter (PC), which holds the address of the next instruction to fetch.
- Fetching the instruction from instruction memory (ROM) using the current PC value.
- Incrementing the PC by 4 (for word-aligned instructions) or updating it with a new value (for jumps/branches).
- Providing the fetched instruction and current PC to the next pipeline stage.
- The module is parameterized for address width, instruction width, and memory depth, making it flexible for different designs. It also supports loading instructions from a hex file for simulation or FPGA initialization.

If_id_pipeline_reg.v

This Verilog module implements the IF/ID pipeline register, which is a key component in pipelined processor architectures. Its main responsibilities are:

- Latching (storing) the instruction and PC fetched during the IF stage.
- Passing the latched instruction and PC to the Instruction Decode (ID) stage on the next clock cycle.

Supporting pipeline control signals:

- if_id_write to enable/disable updates (for stalling).
- flush to clear the register (for handling hazards or mispredicted branches).
- reset to initialize the register to zero.

This register ensures smooth and correct data flow between the IF and ID stages, enabling pipelined execution.