Static Circuits

Neuromorphic Engineering I

Giacomo Indiveri

Institute of Neuroinformatics
University of Zurich and ETH Zurich

Zurich, October 18, 2021

Outline

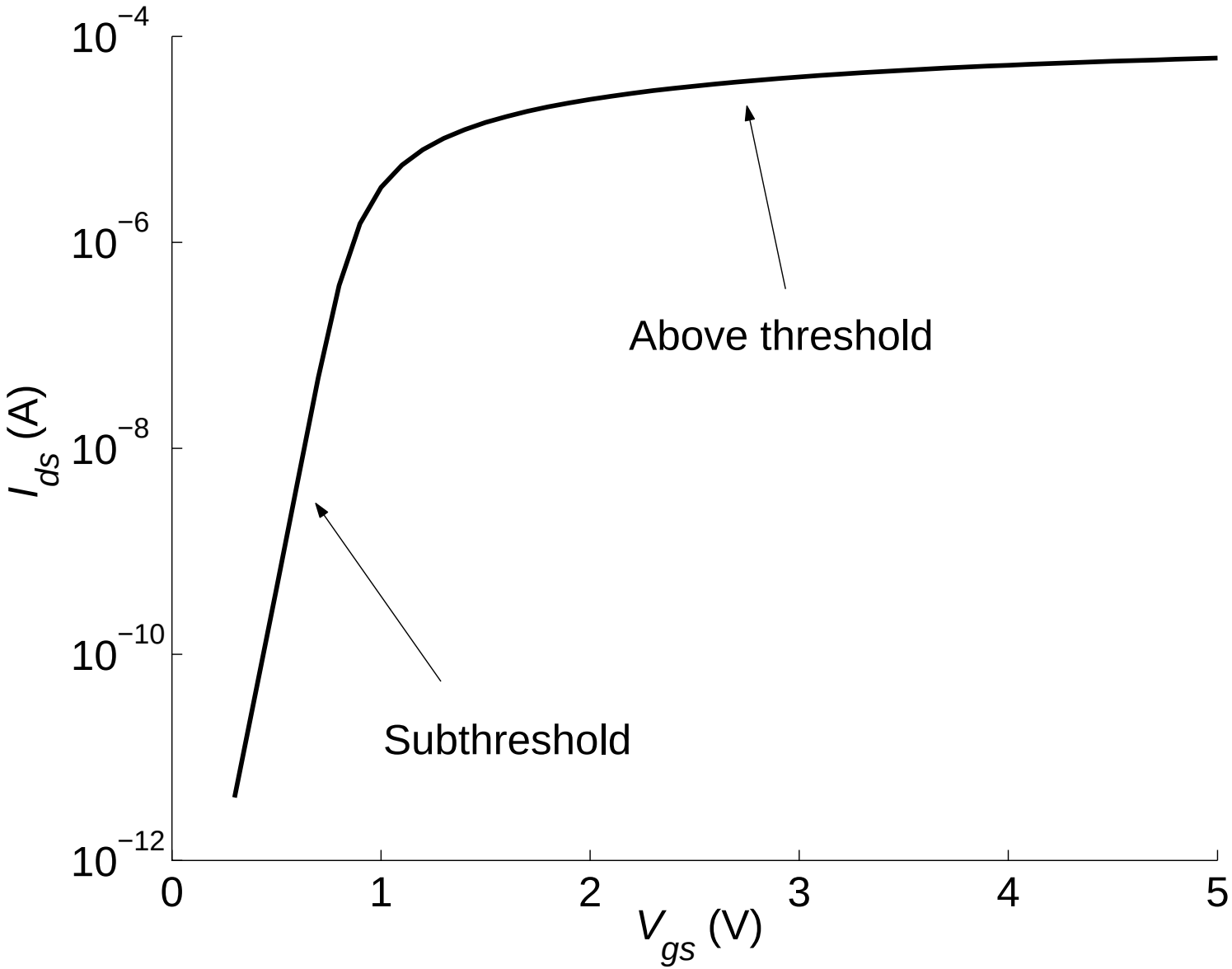
Outline

Outline

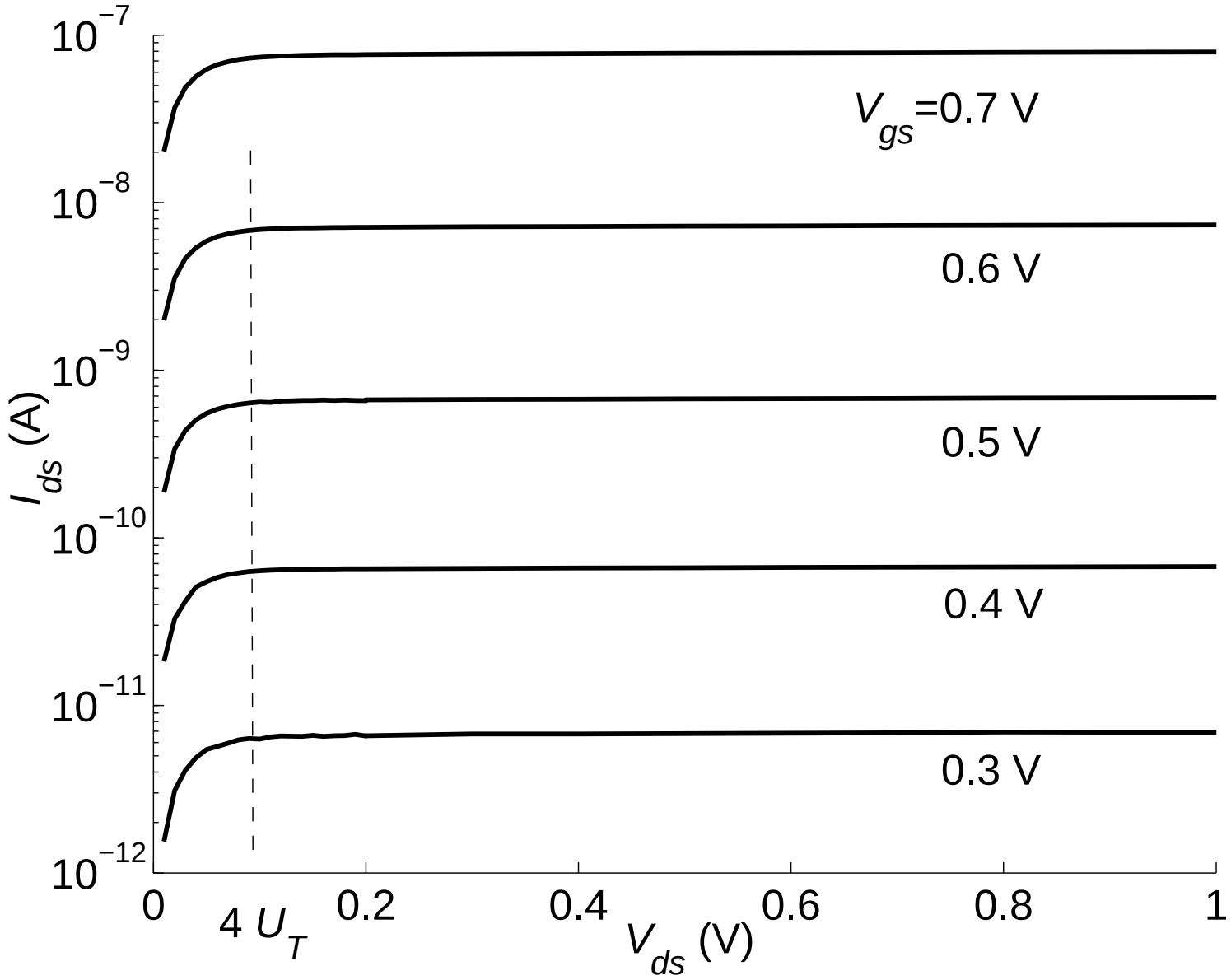
Outline

Outline

I_d vs V_{gs}


10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
I_{ds} (A)
0
1
2
3
4
5
V_{gs} (V)
Above threshold
Subthreshold

I_d vs V_{ds}


10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
I_{ds} (A)
V_{gs}=0.7 V
0.6 V
0.5 V
0.4 V
0.3 V
0
4 U_T
0.2
0.4
0.6
0.8
1
V_{ds} (V)

Body Effect

What is body effect?

Subthreshold

In subthreshold, for a constant I, a ΔV change in the source voltage means that the gate voltage has to increase by $\kappa \Delta V$ and not just ΔV.

Above threshold

In above threshold, this effect is often taken to mean that the threshold voltage of the transistor increases with the source voltage.

$$\kappa = \frac{C_{OX}}{C_{OX} + C_{dep}}$$

Transistor Subthreshold Equations

nFET

$$I = I_{n0} e^{\kappa_n V_g / U_T} \left(e^{-V_s / U_T} - e^{-V_d / U_T} \right)$$

pFET

$$I = I_{p0} e^{\kappa_p (V_{dd} - V_g) / U_T} \left(e^{-(V_{dd} - V_s) / U_T} - e^{-(V_{dd} - V_d) / U_T} \right)$$

where

- I_{n0} and I_{p0} denote the nFET/pFET current-scaling parameter
- κ_n and κ_p denote the nFET/pFET subthreshold slope factor
- U_T the thermal voltage
- V_g the gate voltage, V_s the source voltage, and V_d the drain voltage.

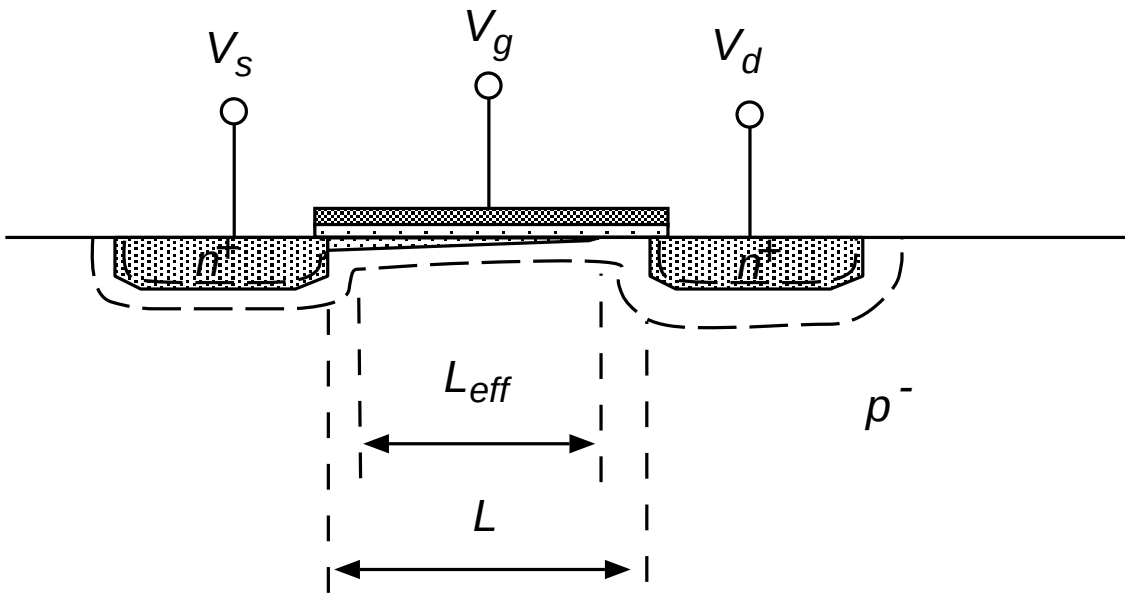
The current is defined to be positive if it flows from the drain to the source.

Early Effect

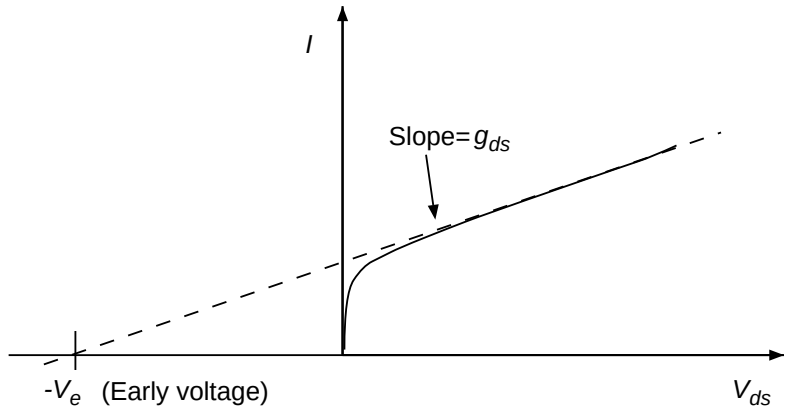
When deriving the I–V characteristics of the nFET we assumed that the current is constant in the saturation regime. This assumption is not sufficient, particularly for short-length MOSFETs. The drain voltage can modulate the channel current even in saturation.

Early Effect

When deriving the I–V characteristics of the nFET we assumed that the current is constant in the saturation regime. This assumption is not sufficient, particularly for short-length MOSFETs. The drain voltage can modulate the channel current even in saturation.



Early Voltage

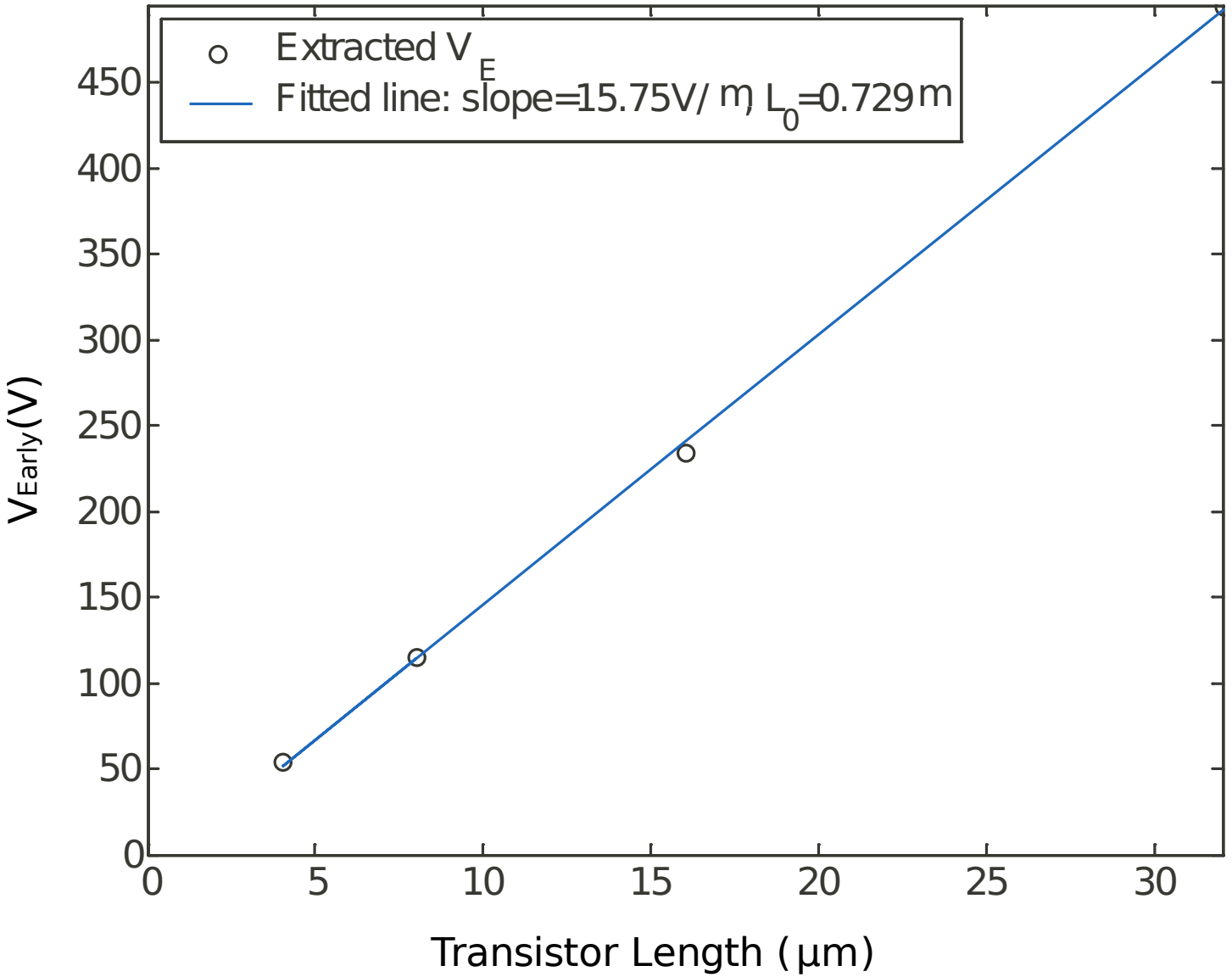


The Early voltage is defined as the absolute value of the voltage at which the slope intersects the voltage axis on this curve.

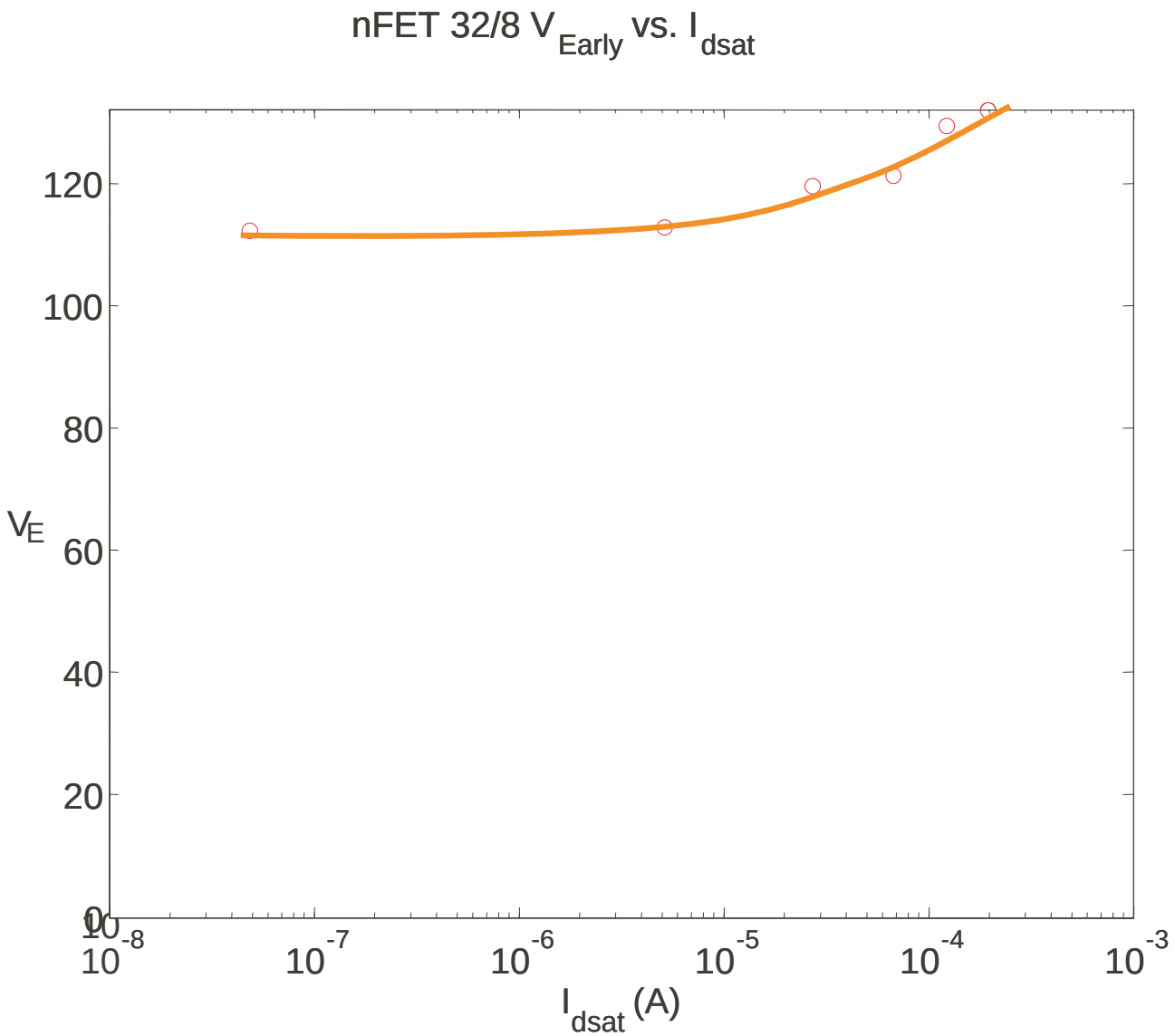
$$V_e = -L_{eff} \frac{\partial V_{ds}}{\partial L_{eff}}$$

V_e is named after *Jim Early* who first analyzed this effect in BJTs.

How does the Early voltage change with L?



Is V_E constant with I_{dsat}?



nFET Conductances

$$I = I_{n0} e^{\kappa_n V_g / U_T} \left(e^{-V_s / U_T} - e^{-V_d / U_T} \right)$$

Gate transconductance

$$g_m = \frac{\partial I}{\partial V_g} = \frac{\kappa I}{U_T}$$

Drain conductance

$$g_d = \frac{\partial I}{\partial V_d} = -\frac{I}{L_{eff}} \frac{\partial L_{eff}}{\partial V_{ds}} = \frac{I}{V_E}$$

In subthreshold, the output current can be expressed as

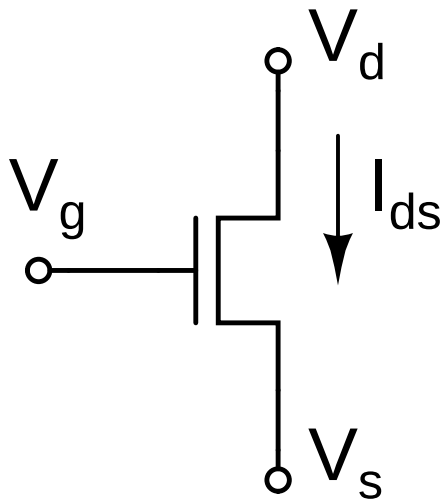
$$\boxed{I = I_{sat} + g_{ds} V_{ds} = I_{sat}(1 + \frac{V_{ds}}{V_e})}$$

where $I_{sat} = I_0 e^{\kappa V_g / U_T - V_s / U_T}$

Outline

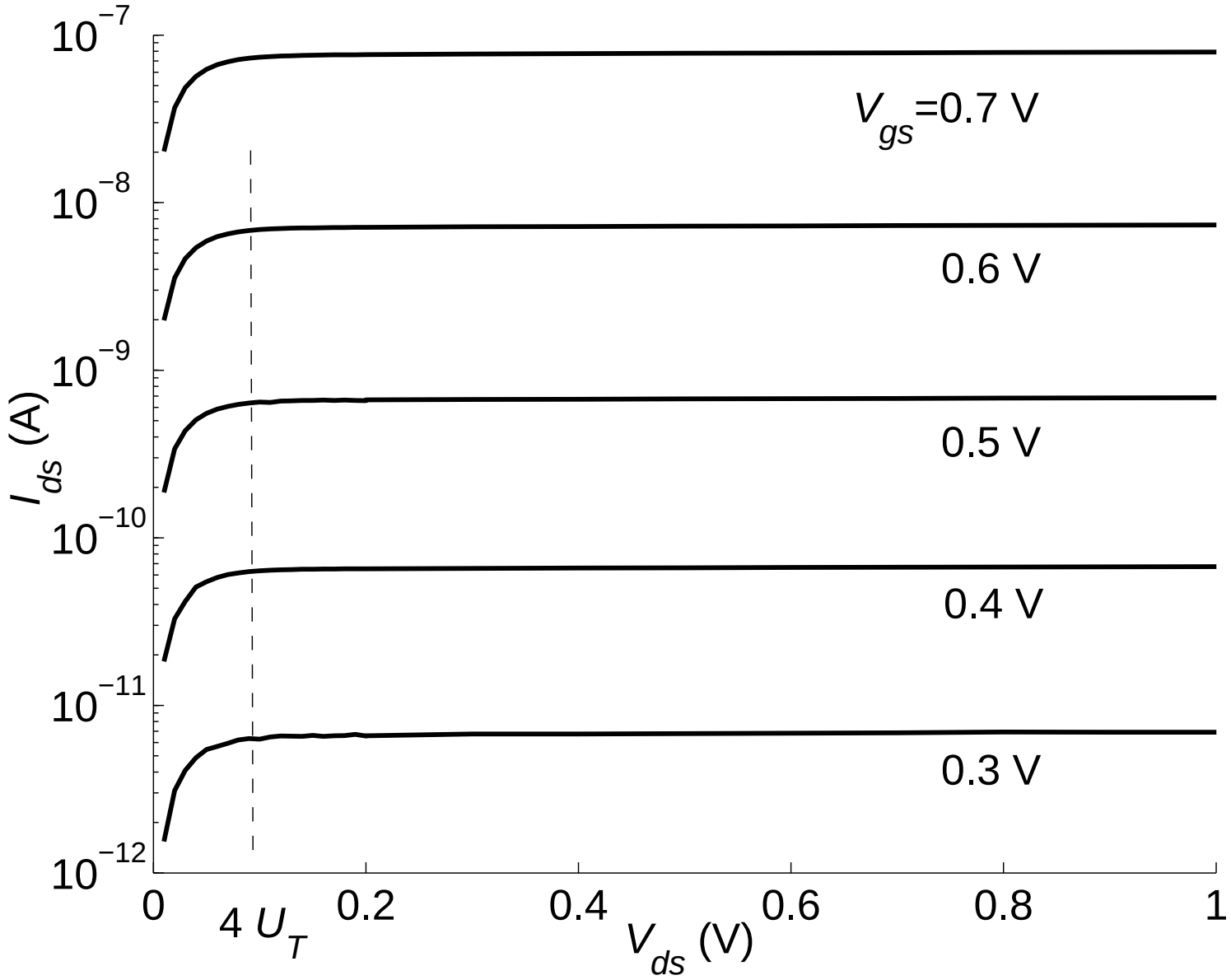
Current Source

If we can neglect the Early effect (use long transistors)



$$\boxed{I = I_{n0} e^{(\kappa_n V_g - V_s)/U_T}} \text{ for } |V_d - V_s| \geq 100mV$$

I_d vs V_{ds}


10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
I_{ds} (A)
V_{gs}=0.7 V
0.6 V
0.5 V
0.4 V
0.3 V
0
4 U_T
0.2
0.4
0.6
0.8
1
V_{ds} (V)

Linear Resistor

The drain current I in the triode regime depends on the relative values V_s and V_d.

$$\begin{aligned} I &= I_0 e^{\kappa V_g/U_T - (V_d+V_s)/2U_T} \left(e^{(V_d-V_s)/2U_T} - e^{-(V_d-V_s)/2U_T} \right) \\ &= 2I_0 e^{\kappa V_g/U_T - (V_d+V_s)/2U_T} \sinh\left(\frac{V_d - V_s}{2U_T} \right) . \end{aligned}$$

If $V_d - V_s$ is small enough to neglect third and higher order terms, a Taylor series expansion yields

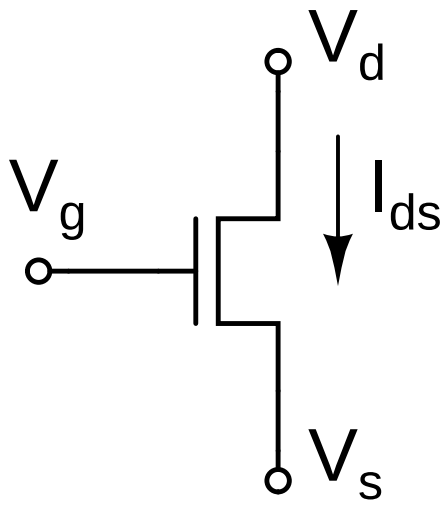
$$I \approx I_0 e^{\kappa V_g/U_T - (V_d+V_s)/2U_T} \frac{V_d - V_s}{U_T} .$$

For a given $(V_d + V_s)/2$ and a given V_g, a MOSFET acts as a *linear resistor* with resistance:

$$\boxed{R = \frac{U_T}{I_0} e^{(V_d+V_s)/2U_T - \kappa V_g/U_T} .} \tag{1}$$

Logarithmc I/V converter

In subthreshold the MOSFET acts as a logarithmic I/V converter if I is the input and either V_g or V_s is the output.



The I/V conversion function in subthreshold can be derive by solving for the output voltage:

$$V_s = \kappa V_g - U_T \log\left(\frac{I}{I_0}\right)$$

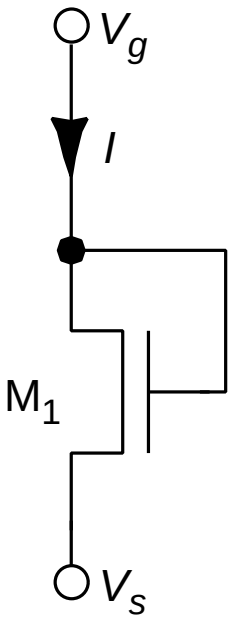
if the source is the output terminal and

$$V_g = \kappa_n^{-1}\left(V_s + U_T \log\left(\frac{I}{I_{n0}}\right)\right)$$

if the gate is the output terminal.

Diode connected transistors

V_g is determined by the gate charge, which can't be directly influenced by the input current due to the infinite impedance between channel and gate. To make the circuit work, the input node and the gate have to be in a negative feedback loop that controls the gate charge and keeps the MOSFET in saturation. The MOSFET is then reduced to a two-terminal device with similar characteristics to a diode, and said to be *diode-connected*.



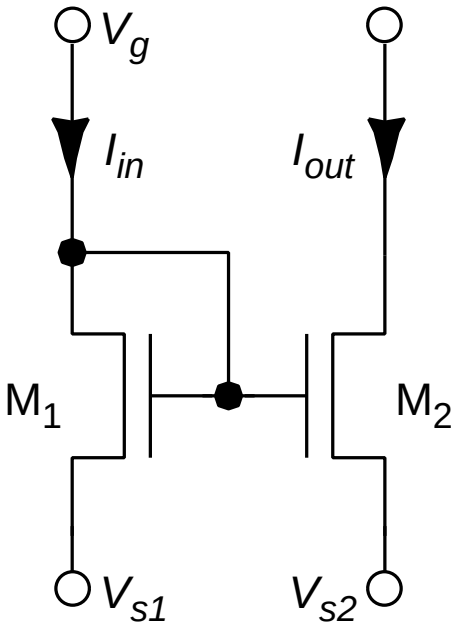
$$
\begin{aligned}
I = & \quad I_0 e^{\frac{\kappa V_g - V_s}{U_T}} \left(1 - e^{-\frac{V_d - V_s}{U_T}}\right) \\
= & \quad I_0 e^{\frac{\kappa V_g - V_s}{U_T}} \left(1 - e^{-\frac{V_g - V_s}{U_T}}\right) \\
= & \quad I_0 e^{\frac{\kappa V_g - V_s}{U_T}} - I_0 e^{-\frac{(1-\kappa) V_g}{U_T}}
\end{aligned}
$$

$$
\boxed{I = I_0 e^{\frac{\kappa V_g - V_s}{U_T}}}
$$

Outline

Current Mirror

The output current is a *mirrored* copy of the input current.



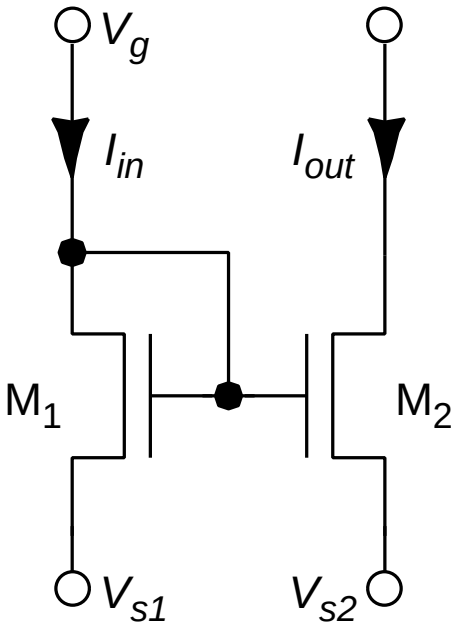
If both MOSFETs are of the same size and have the same source voltage, they source the same current, which is why the device is called a *current mirror*. The input current I_{in} through the diode-connected transistor M_1 sets the common gate voltage V_g and hence the output current I_{out} of the second transistor M_2.

The output current can be scaled by choosing different transistor sizes, or by choosing different source potentials V_{s1} and V_{s2} for the two MOSFETs.
If M_2 is in saturation:

$$I_{out} = e^{(V_{s1}-V_{s2})/U_T} I_{in}.$$

Current Mirror

The output current is a *mirrored* copy of the input current.



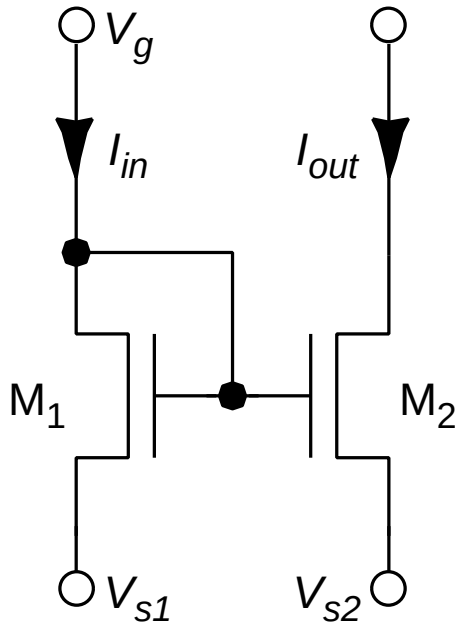
If both MOSFETs are of the same size and have the same source voltage, they source the same current, which is why the device is called a *current mirror*. The input current I_{in} through the diode-connected transistor M_1 sets the common gate voltage V_g and hence the output current I_{out} of the second transistor M_2.

The output current can be scaled by choosing different transistor sizes, or by choosing different source potentials V_{s1} and V_{s2} for the two MOSFETs.
If M_2 is in saturation:

$$I_{out} = e^{(V_{s1}-V_{s2})/U_T} I_{in}.$$

Current Mirror

The output current is a *mirrored* copy of the input current.

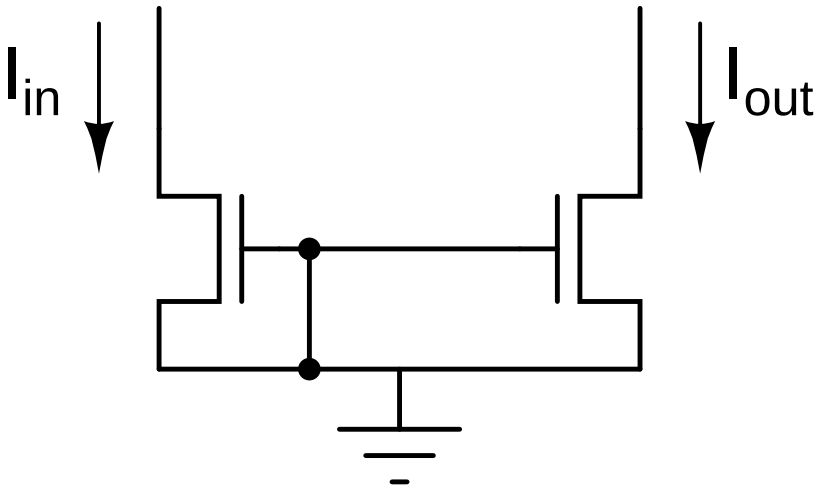


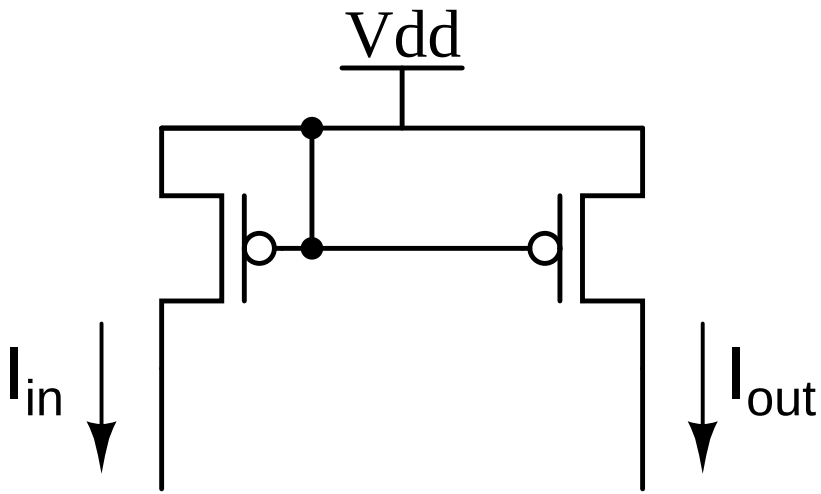
If both MOSFETs are of the same size and have the same source voltage, they source the same current, which is why the device is called a *current mirror*. The input current I_{in} through the diode-connected transistor M_1 sets the common gate voltage V_g and hence the output current I_{out} of the second transistor M_2.

The output current can be scaled by choosing different transistor sizes, or by choosing different source potentials V_{s1} and V_{s2} for the two MOSFETs.
If M_2 is in saturation:

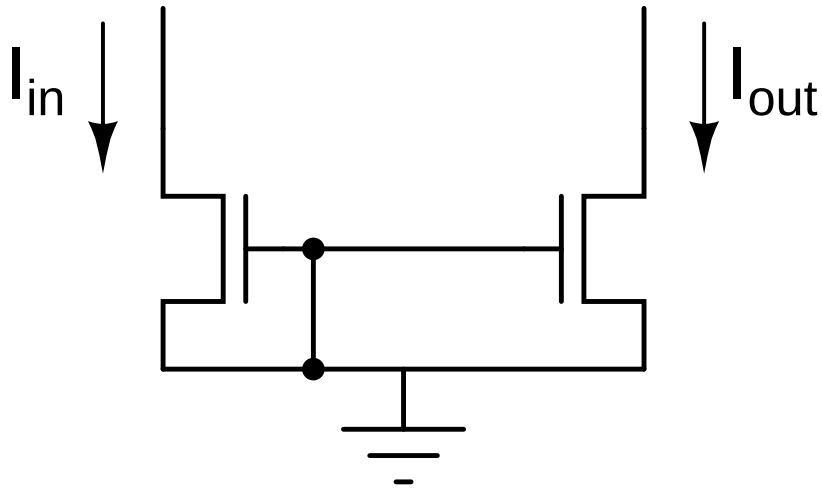
$$I_{out} = e^{(V_{s1} - V_{s2})/U_T} I_{in}.$$

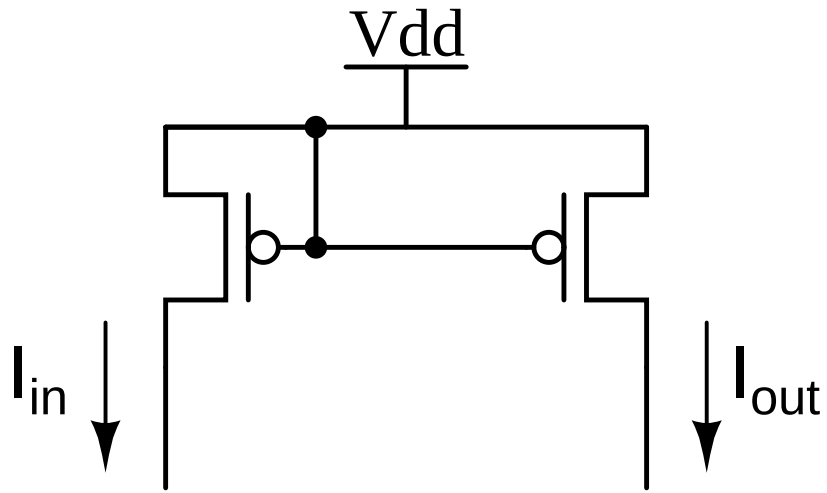
How about these configurations?





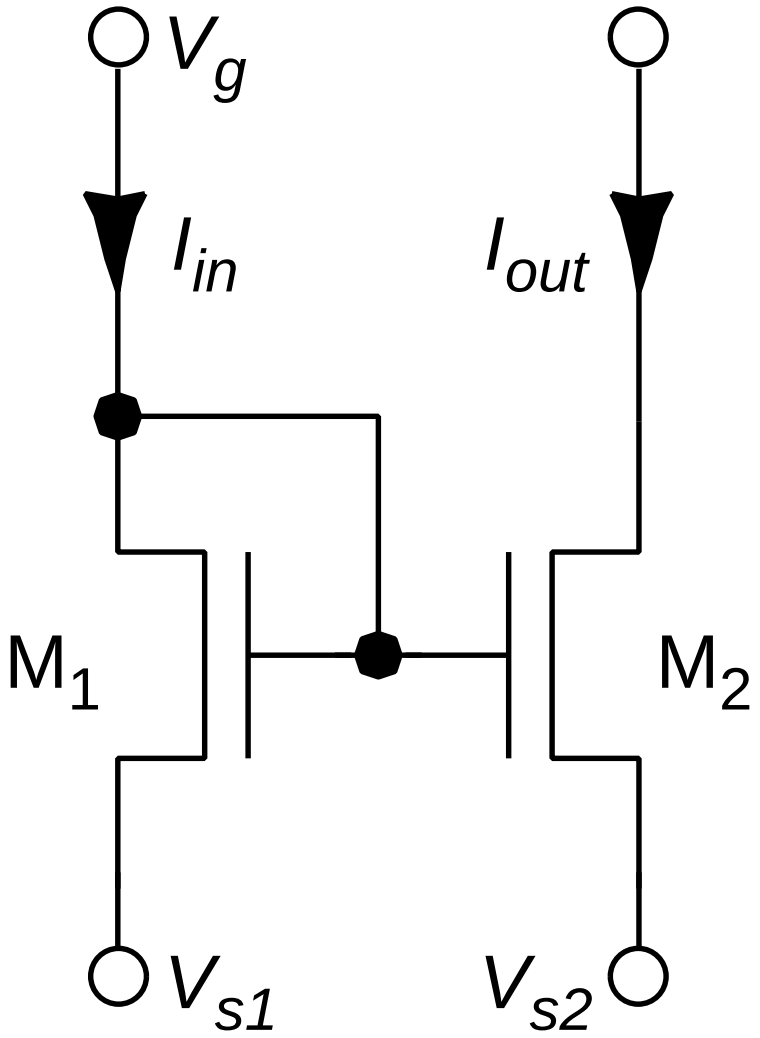
How about these configurations?





$$V_{gs} = 0, \text{ so } I_{ds} = 0$$

Current mirror with gain (I)

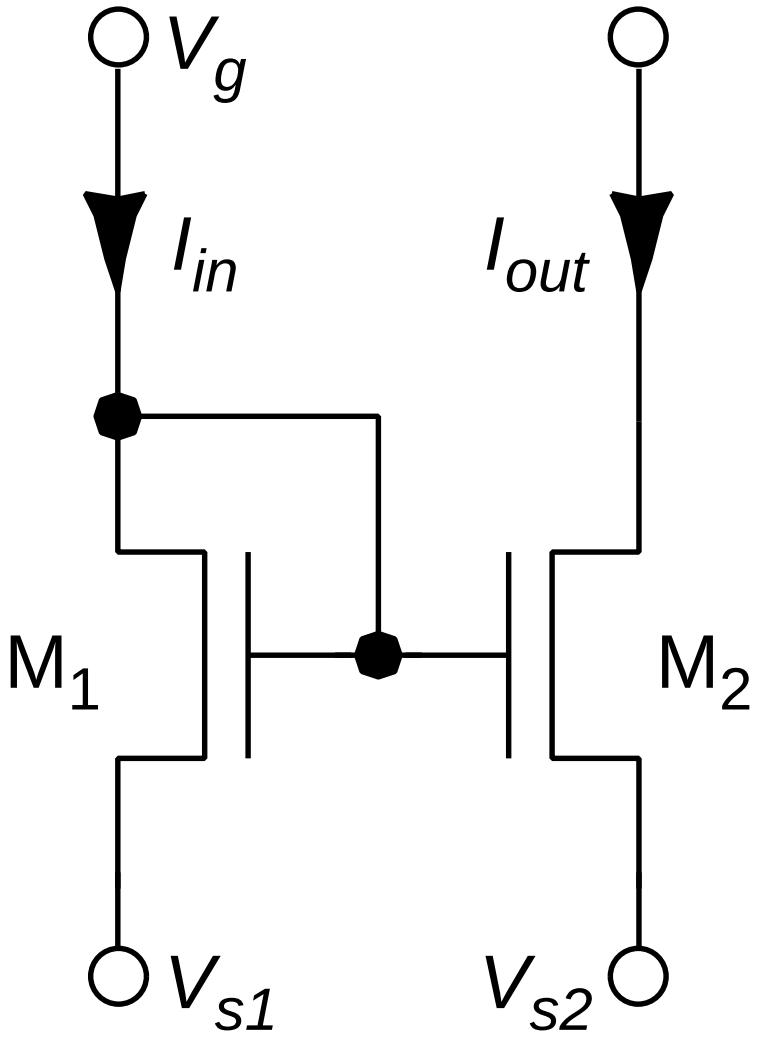


$$V_{s1} = V_{s2}$$

$$I_{out} = M \cdot I_{in}$$

$$\text{Gain } M = \frac{W_2/L_2}{W_1/L_1}$$

Current mirror with gain (II)



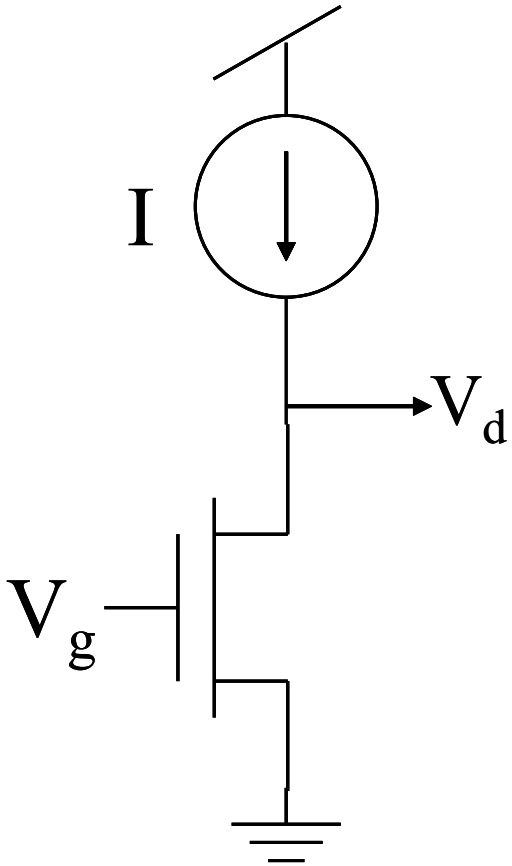
$$V_{s1} \neq V_{s2}$$

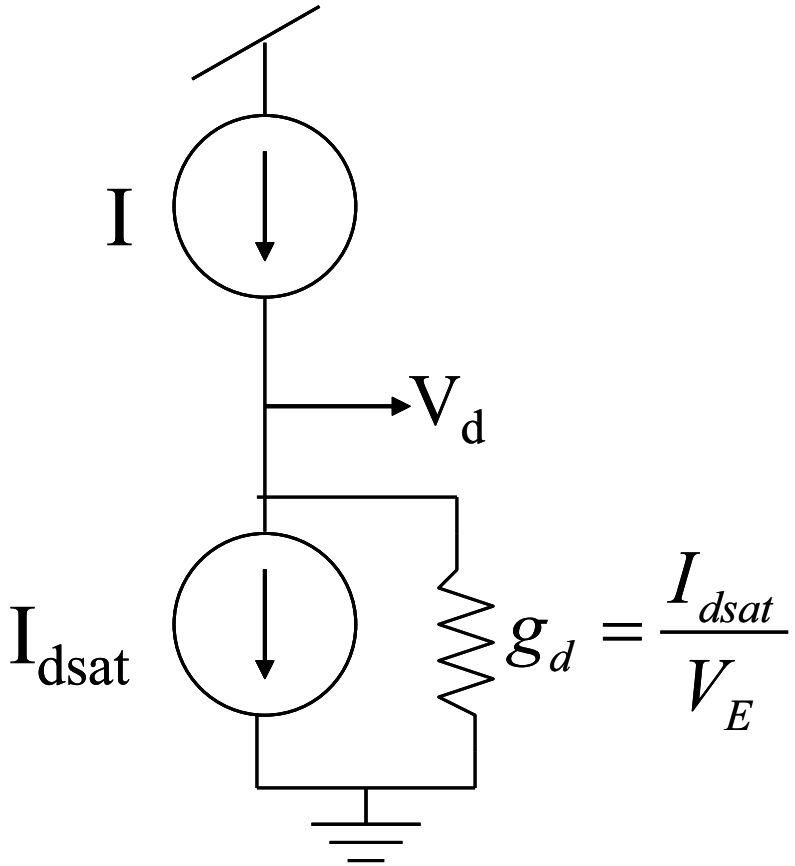
$$I_{out} = M \cdot I_{in}$$

$$\text{Gain } M = e^{\frac{V_{s1} - V_{s2}}{U_T}}$$

Voltage Gain

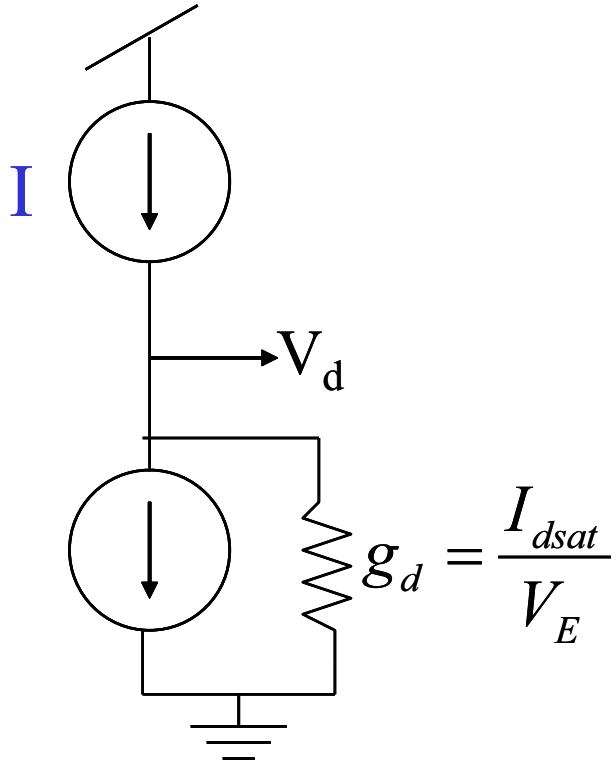
Intrinsic transistor voltage gain:

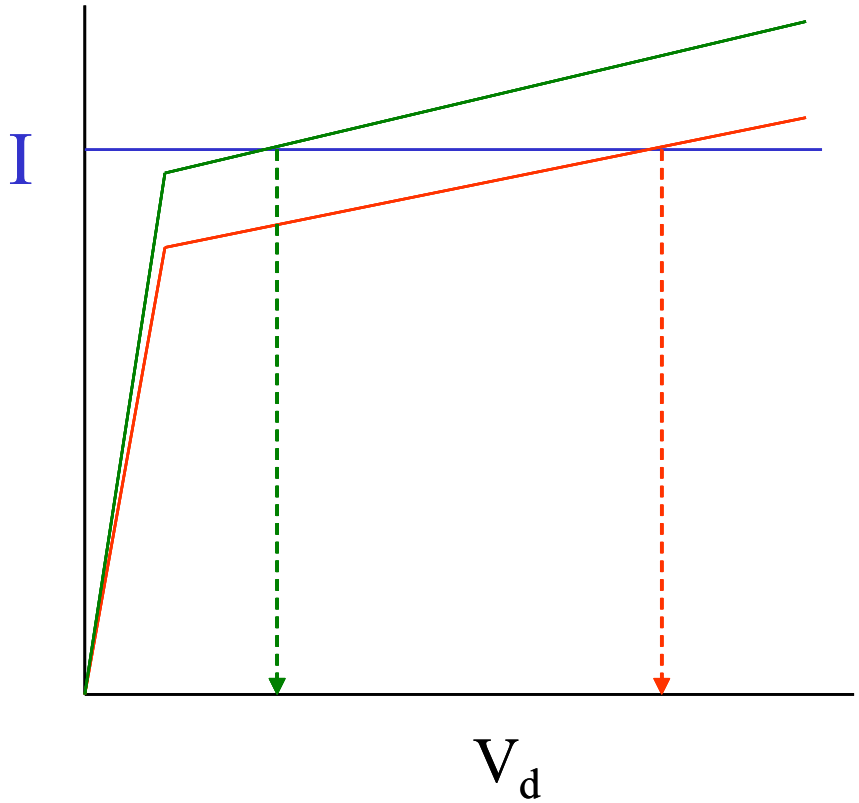




Voltage Gain

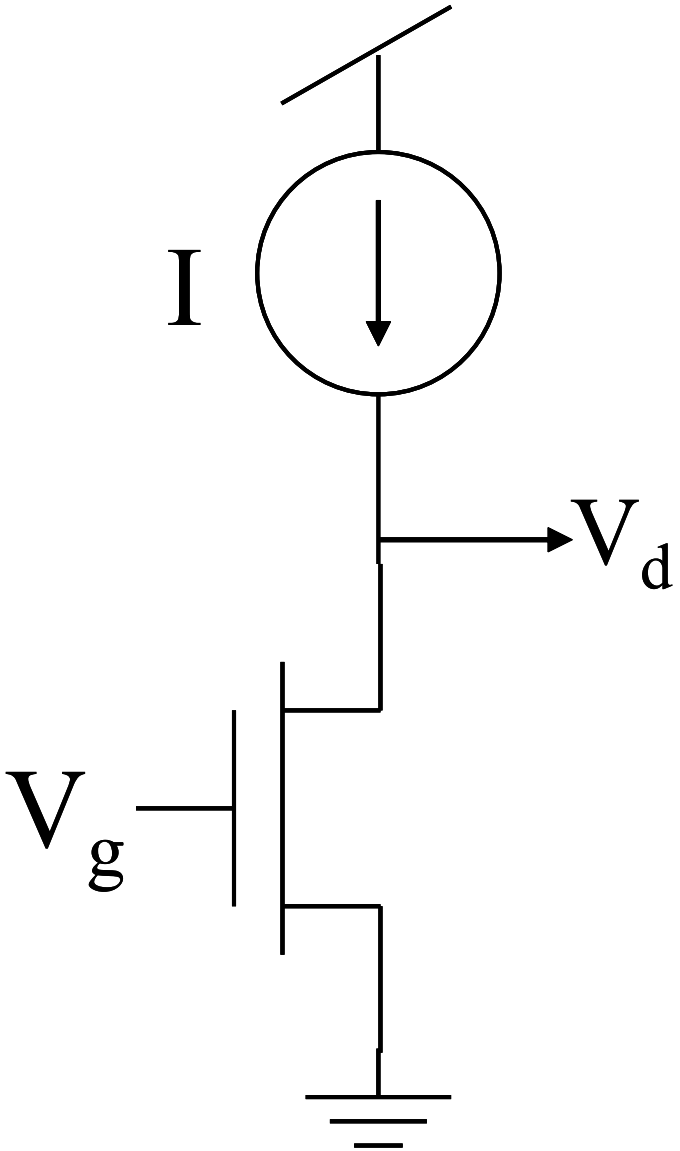
Intrinsic transistor voltage gain:





Voltage Gain

Intrinsic transistor voltage gain:



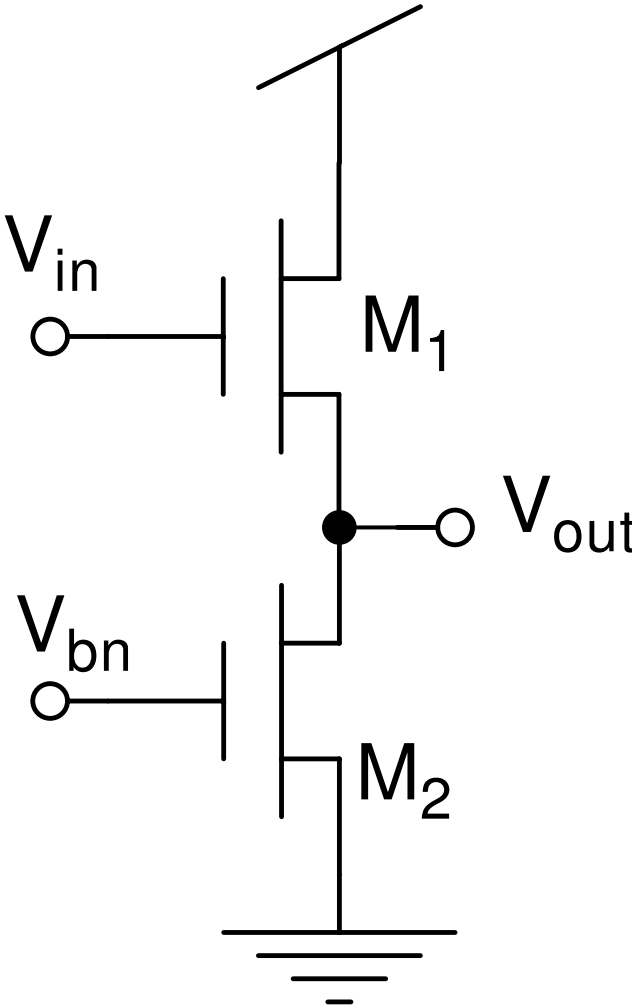
$$\text{Gain } A = \frac{\partial V_d}{\partial V_g} = \frac{\partial I}{\partial V_g}\frac{\partial V_d}{\partial I} = \frac{g_m}{g_d}$$

$$\boxed{A = \frac{\kappa V_E}{U_T}}$$

(in subthreshold)

The Source Follower

n-type



$$I_{M1} = I_0 e^{\kappa V_{in}/U_T - V_{out}/U_T}$$

$$I_{M2} = I_0 e^{\kappa V_{bn}/U_T}$$

$$I_{M1} = I_{M2}$$

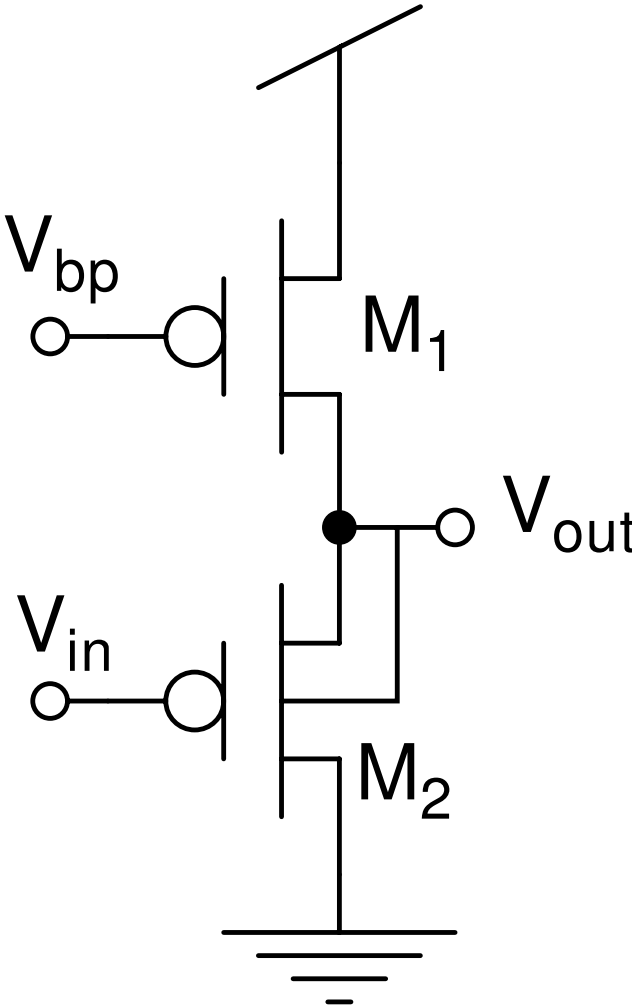
$$\boxed{V_{out} = \kappa(V_{in} - V_{bn})}$$

Saturation condition for `M2`:

$$V_{out} > 4U_T$$

The Source Follower

p-type



$$I_{M1} = I_0 e^{-\kappa(V_{bp}-V_{dd})/U_T}$$

$$I_{M2} = I_0 e^{-\kappa(V_{in}-V_{out})/U_T}$$

$$I_{M1} = I_{M2}$$

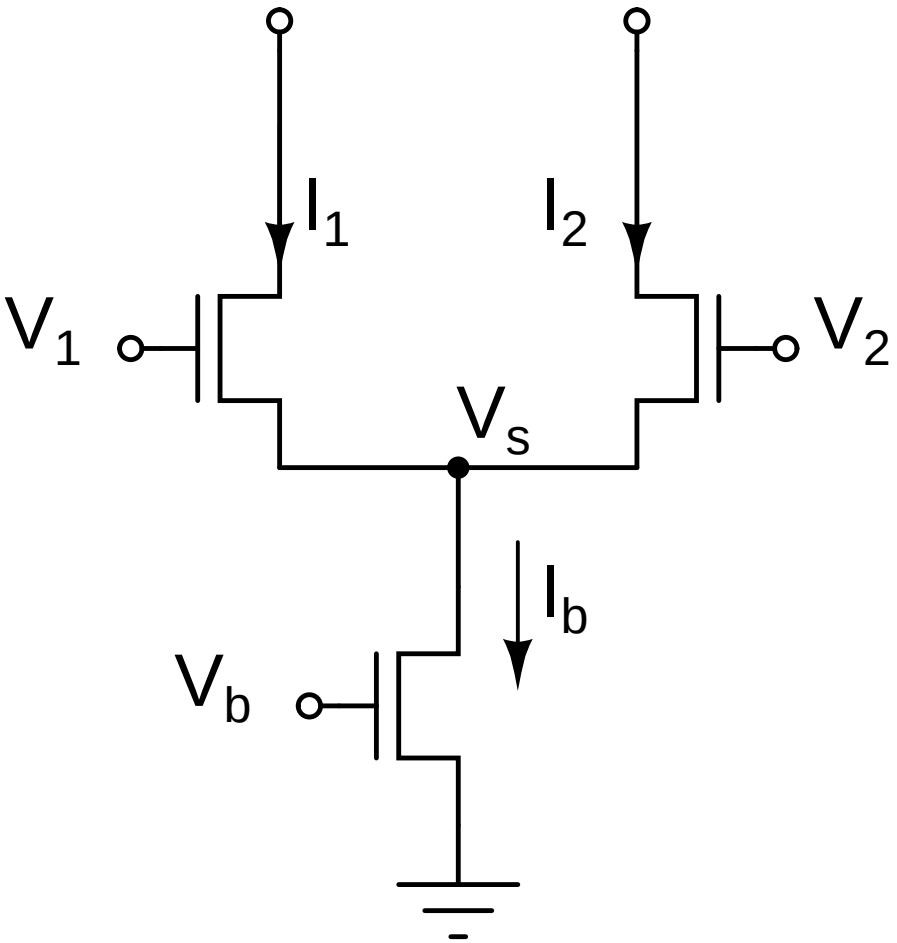
$$\boxed{V_{out} = (V_{dd} - V_{bp}) + V_{in}}$$

Saturation condition for `M1`:

$$V_{out} < V_{dd} - 4U_T$$

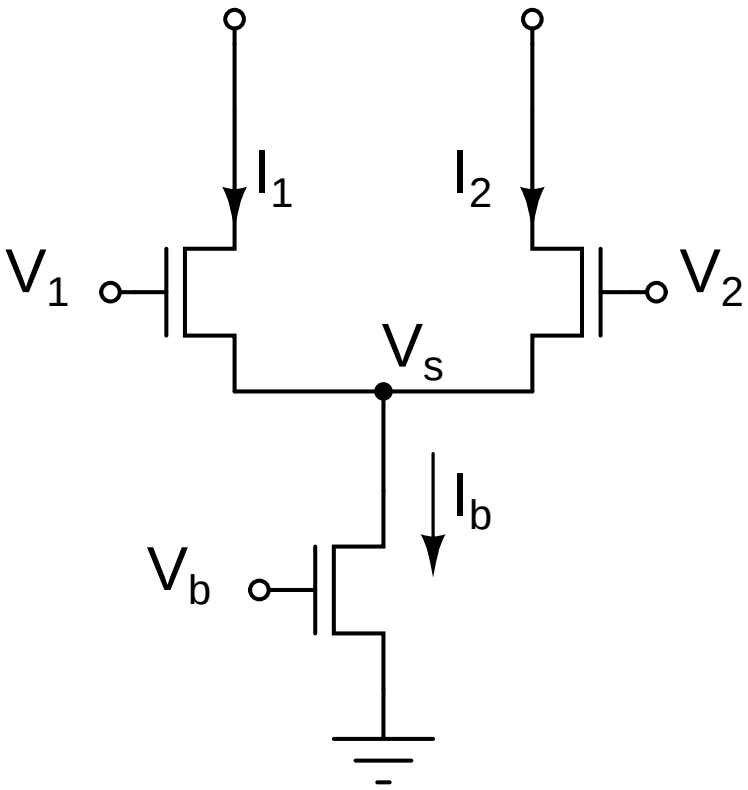
Outline

The differential pair

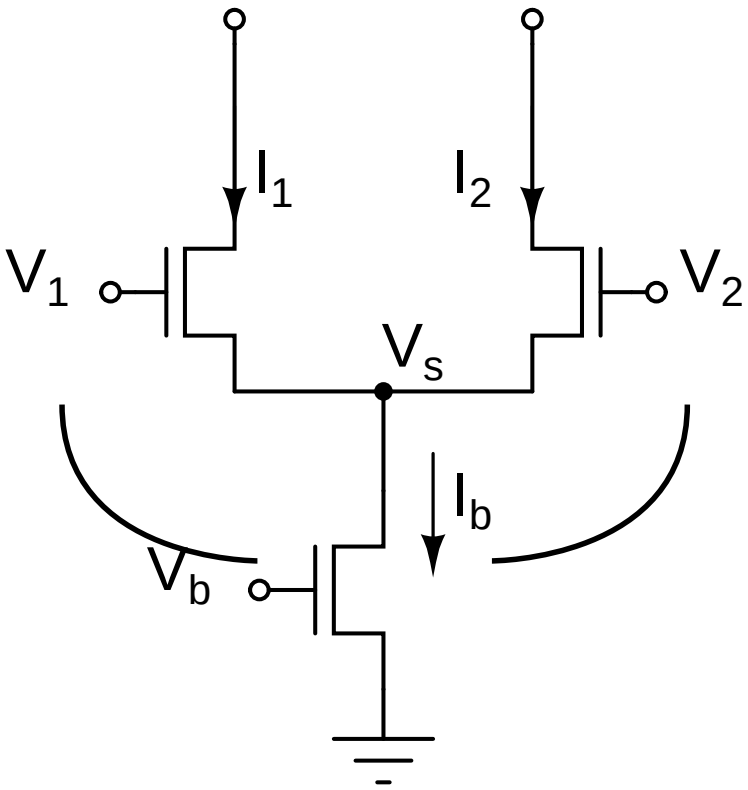


- Input signal: $\Delta V = V_1 - V_2$
- Output signals: I_1 and I_2, if saturated.
- Bias parameter: V_b

The diff-pair



The diff-pair

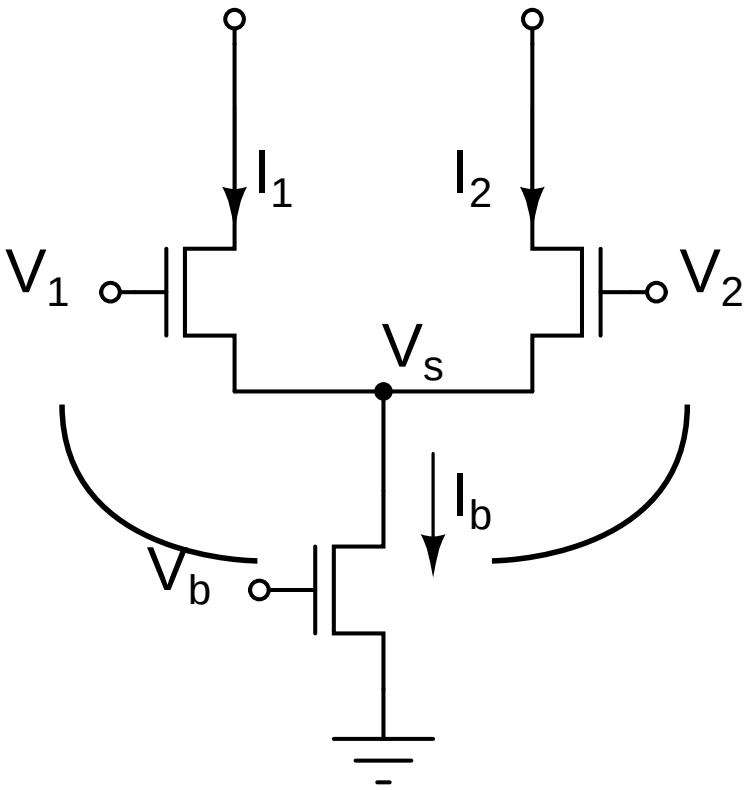


$$I_1 = I_0 e^{\frac{\kappa V_1 - V_s}{U_T}}$$

$$I_2 = I_0 e^{\frac{\kappa V_2 - V_s}{U_T}}$$

$$I_b = I_1 + I_2 = I_0 e^{\frac{\kappa V_b}{U_T}}$$

The diff-pair



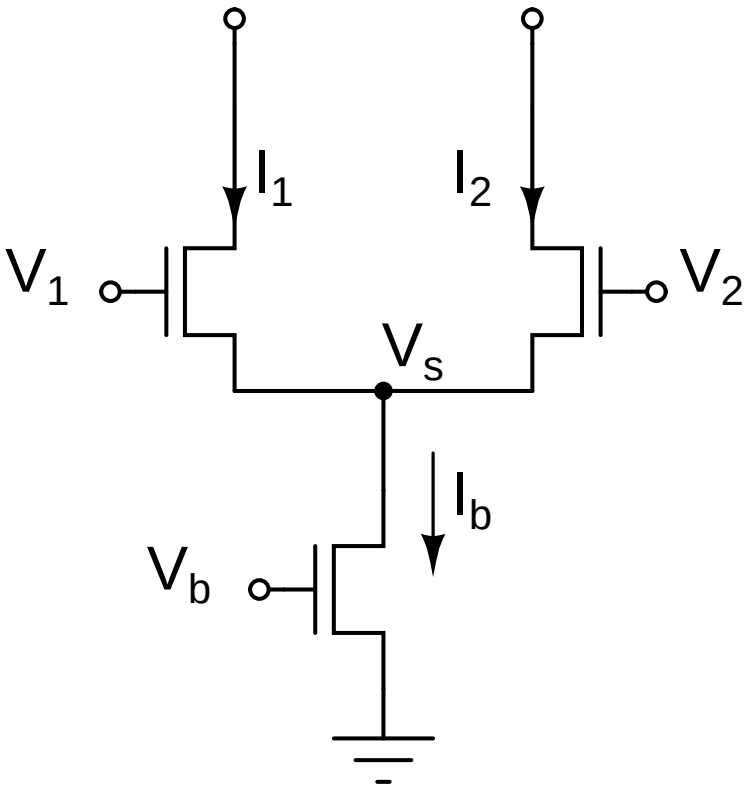
$$I_1 = I_0 e^{\frac{\kappa V_1 - V_s}{U_T}}$$

$$I_2 = I_0 e^{\frac{\kappa V_2 - V_s}{U_T}}$$

$$I_b = I_1 + I_2 = I_0 e^{\frac{\kappa V_b}{U_T}}$$

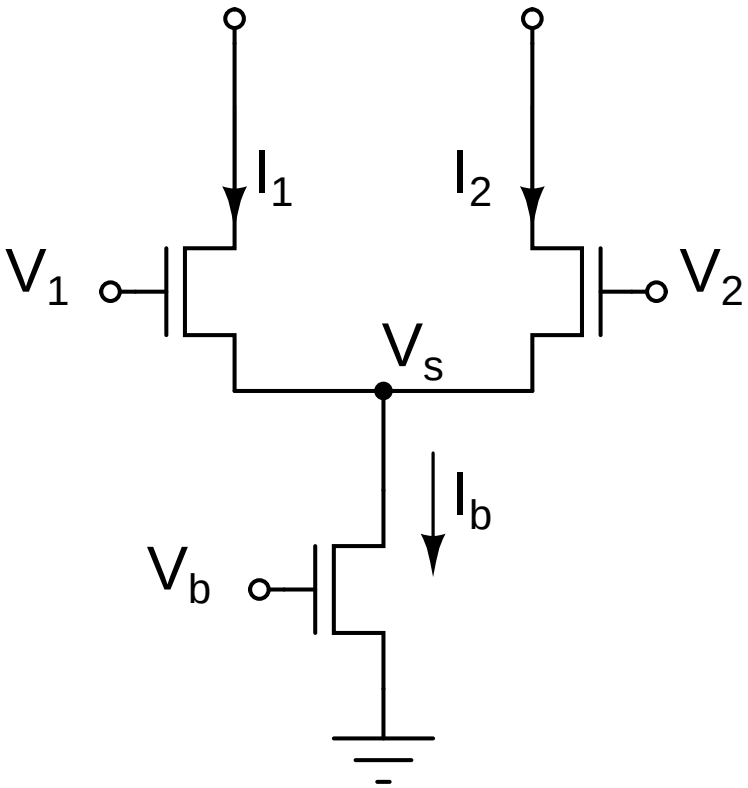
$$\boxed{I_b = I_0 e^{-\frac{V_s}{U_T}} \left(e^{\frac{\kappa V_1}{U_T}} + e^{\frac{\kappa V_2}{U_T}} \right)}$$

The diff-pair - contd.



$$e^{-\frac{V_s}{U_T}} = \frac{I_b}{I_0} \frac{1}{e^{\frac{\kappa V_1}{U_T}} + e^{\frac{\kappa V_2}{U_T}}}$$

The diff-pair - contd.



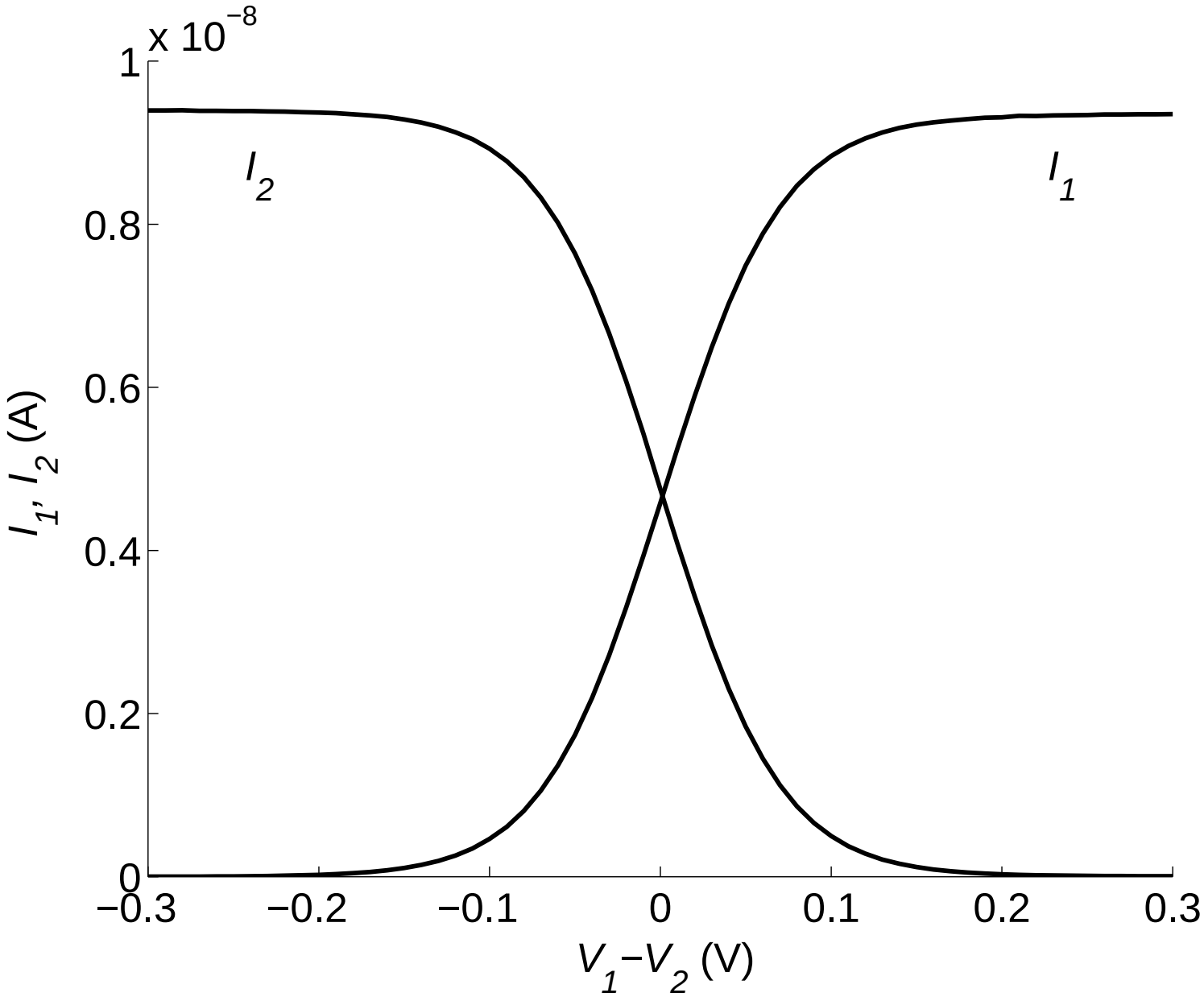
$$e^{-\frac{V_s}{U_T}} = \frac{I_b}{I_0} \frac{1}{e^{\frac{\kappa V_1}{U_T}} + e^{\frac{\kappa V_2}{U_T}}}$$

$$I_1 = I_b \frac{e^{\frac{\kappa V_1}{U_T}}}{e^{\frac{\kappa V_1}{U_T}} + e^{\frac{\kappa V_2}{U_T}}}$$

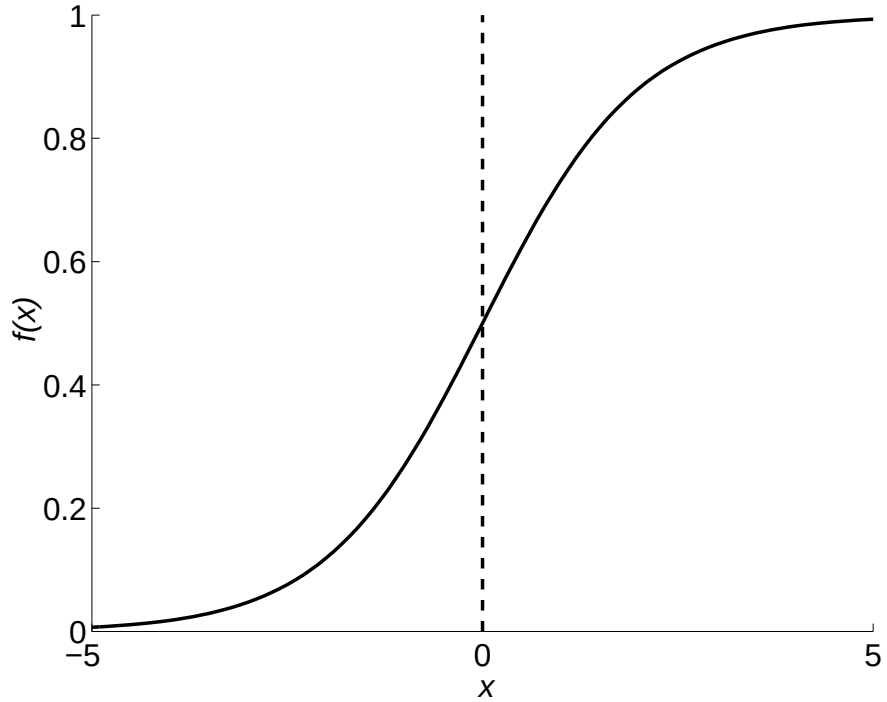
$$I_2 = I_b \frac{e^{\frac{\kappa V_2}{U_T}}}{e^{\frac{\kappa V_1}{U_T}} + e^{\frac{\kappa V_2}{U_T}}}$$

Fermi Functions

The diff-pair



Sigmoids



The term sigmoid means “S-shaped”. Sigmoid functions are typically used in the (conventional) neural network research community.
They are smooth, saturating, monotonic activation functions, that map the interval $(-\infty, \infty)$ onto $(0, 1)$. The canonical *logistic* sigmoid is defined as

$$f(x) = \frac{1}{1 + exp(-\alpha x)}$$

Sigmoids

The output currents of the diff-pair can be rewritten in the canonical sigmoid form:

$$I_1 = I_b \frac{e^{\frac{\kappa V_1}{U_T}}}{e^{\frac{\kappa V_1}{U_T}} + e^{\frac{\kappa V_2}{U_T}}}$$

$$I_2 = I_b \frac{e^{\frac{\kappa V_2}{U_T}}}{e^{\frac{\kappa V_1}{U_T}} + e^{\frac{\kappa V_2}{U_T}}}$$

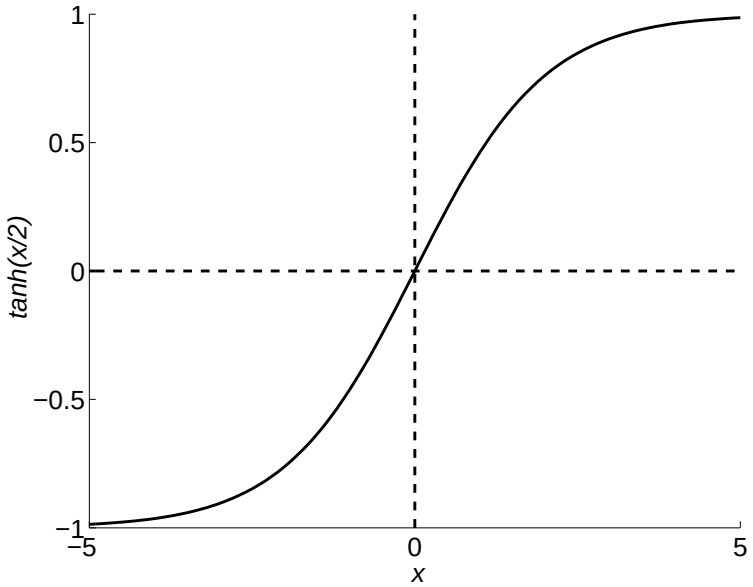
$$I_1 = I_b \frac{1}{1 + e^{\frac{\kappa}{U_T}(V_2 - V_1)}}$$

$$I_2 = I_b \frac{1}{1 + e^{\frac{\kappa}{U_T}(V_1 - V_2)}}$$

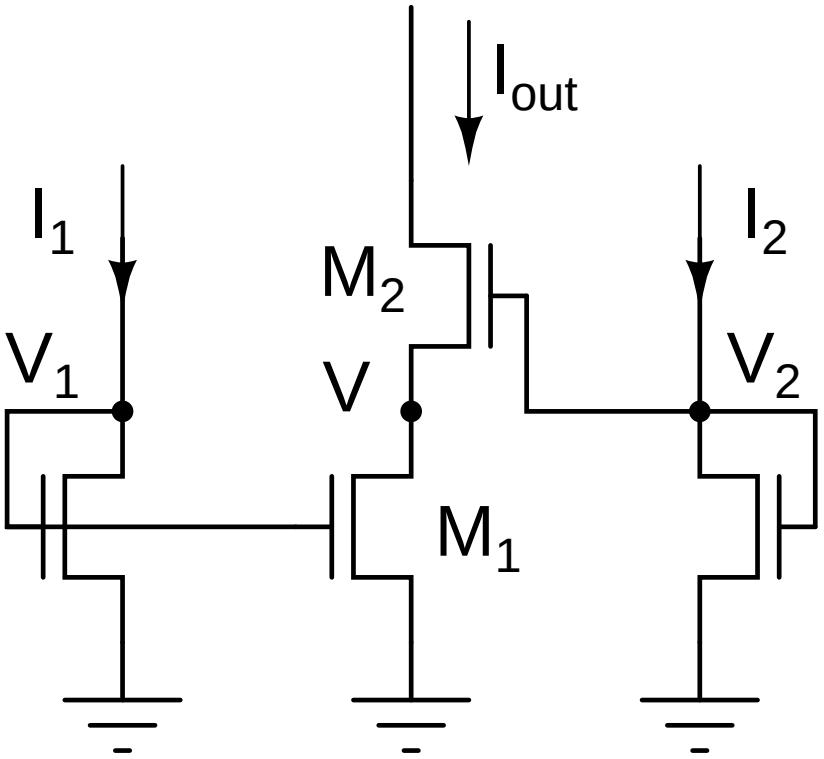
Difference of sigmoids

$$I_1 - I_2 = I_b \frac{e^{\frac{\kappa V_1}{U_T}} - e^{\frac{\kappa V_2}{U_T}}}{e^{\frac{\kappa V_1}{U_T}} + e^{\frac{\kappa V_2}{U_T}}}$$

$$\boxed{I_1 - I_2 = I_b \tanh\left(\frac{\kappa}{2U_T}(V_1 - V_2)\right)}$$



Current Correlator



Transistor M_1 is in *ohmic* region, transistor M_2 is in saturation:

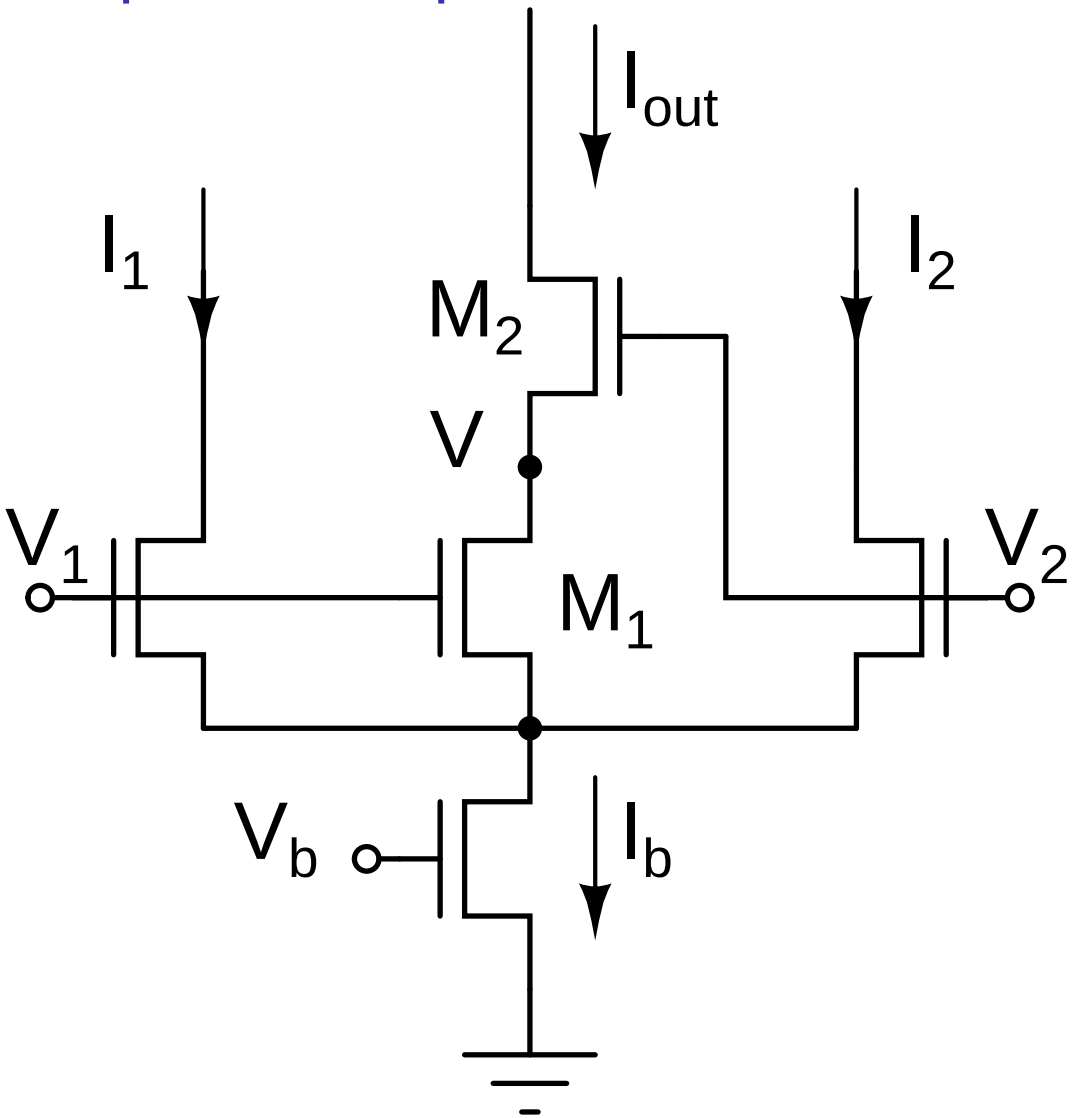
$$\begin{aligned} I_{out} &= I_0 e^{\kappa V_1}\left(1 - e^{-V}\right) \\ I_{out} &= I_0 e^{\kappa V_2 - V} \\ e^{V} &= \frac{I_0 e^{\kappa V_2}}{I_{out}} \end{aligned}$$

(with [V]=[U_T])

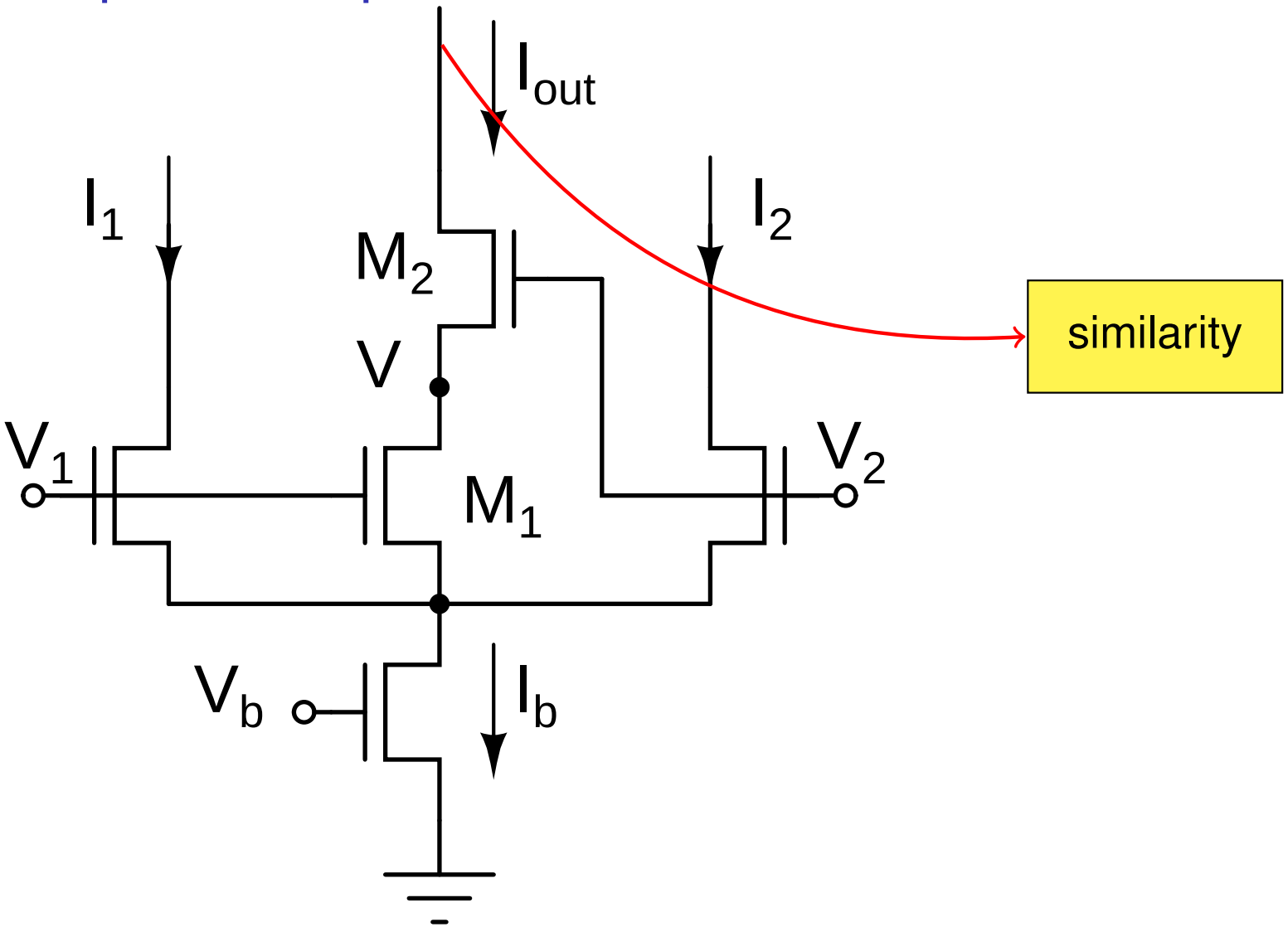
$$I_1 = I_0 e^{\kappa V_1};\ I_2 = I_0 e^{\kappa V_2}$$

$$\Longrightarrow \boxed{I_{out} = \frac{I_1 I_2}{I_1 + I_2}}$$

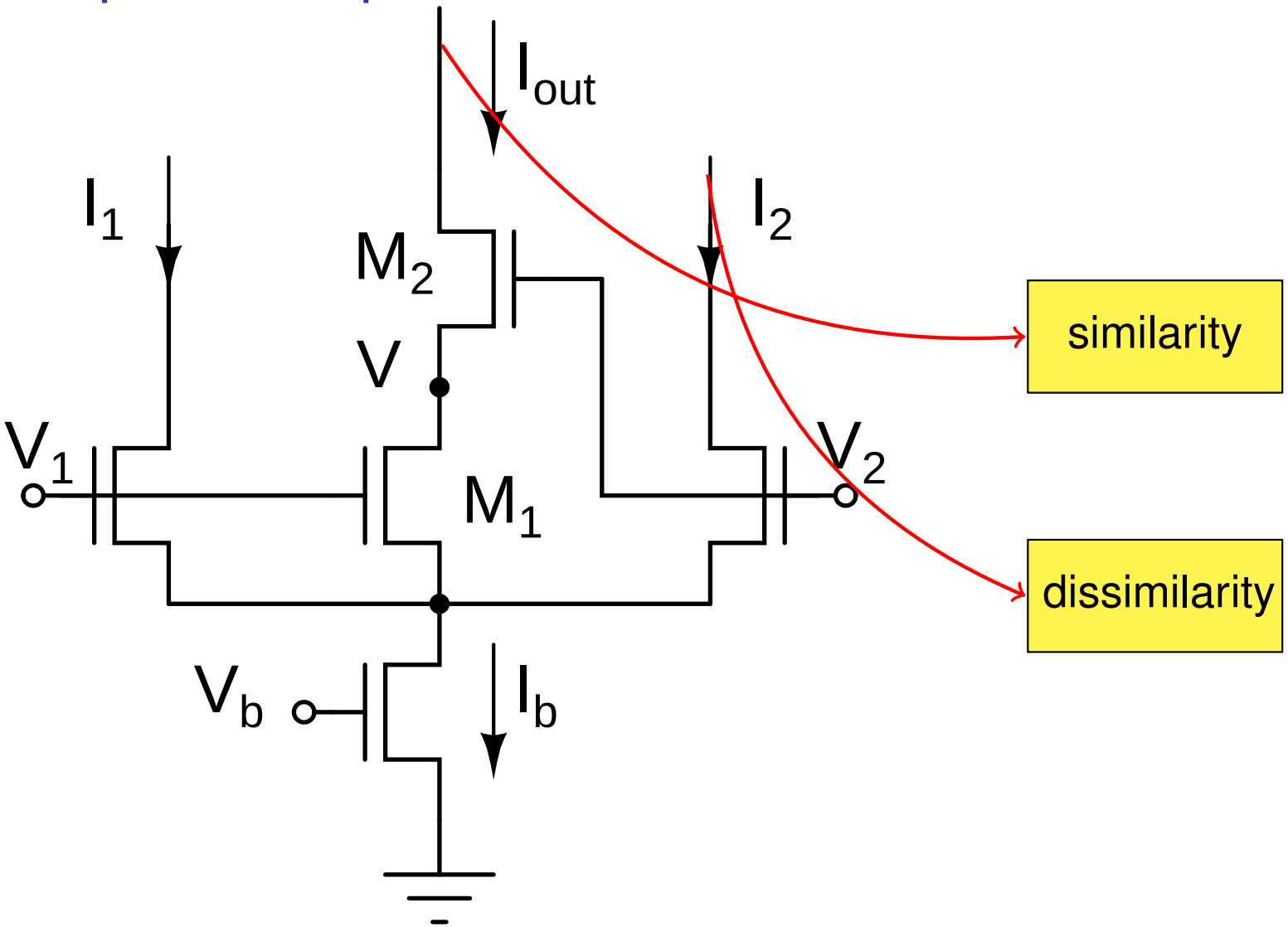
Bump-antibump circuit



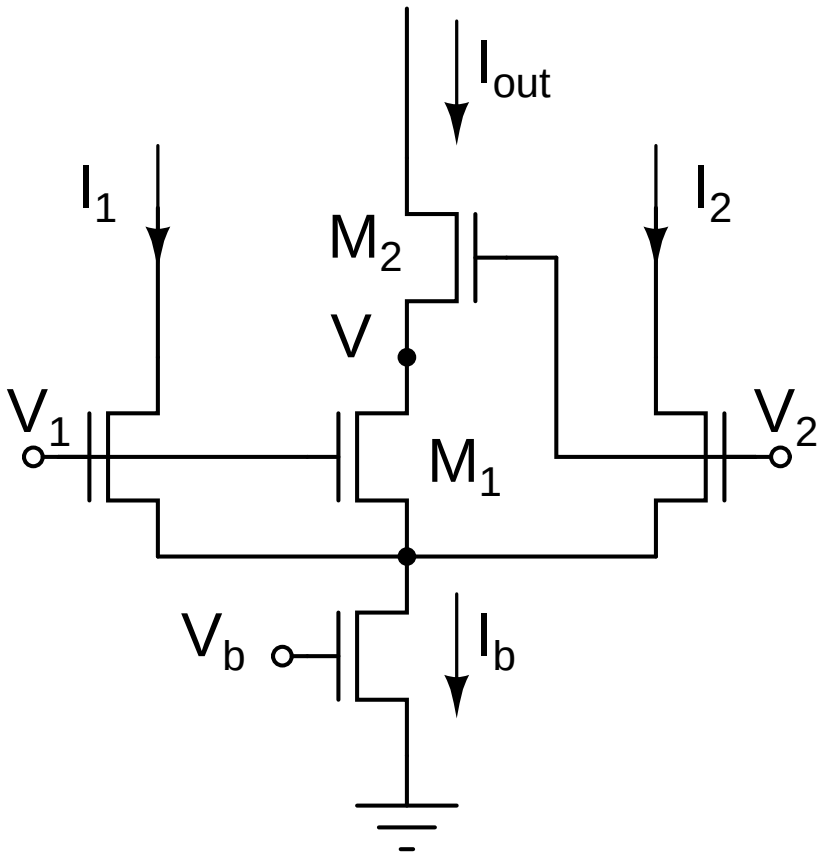
Bump-antibump circuit



Bump-antibump circuit



Bump circuit



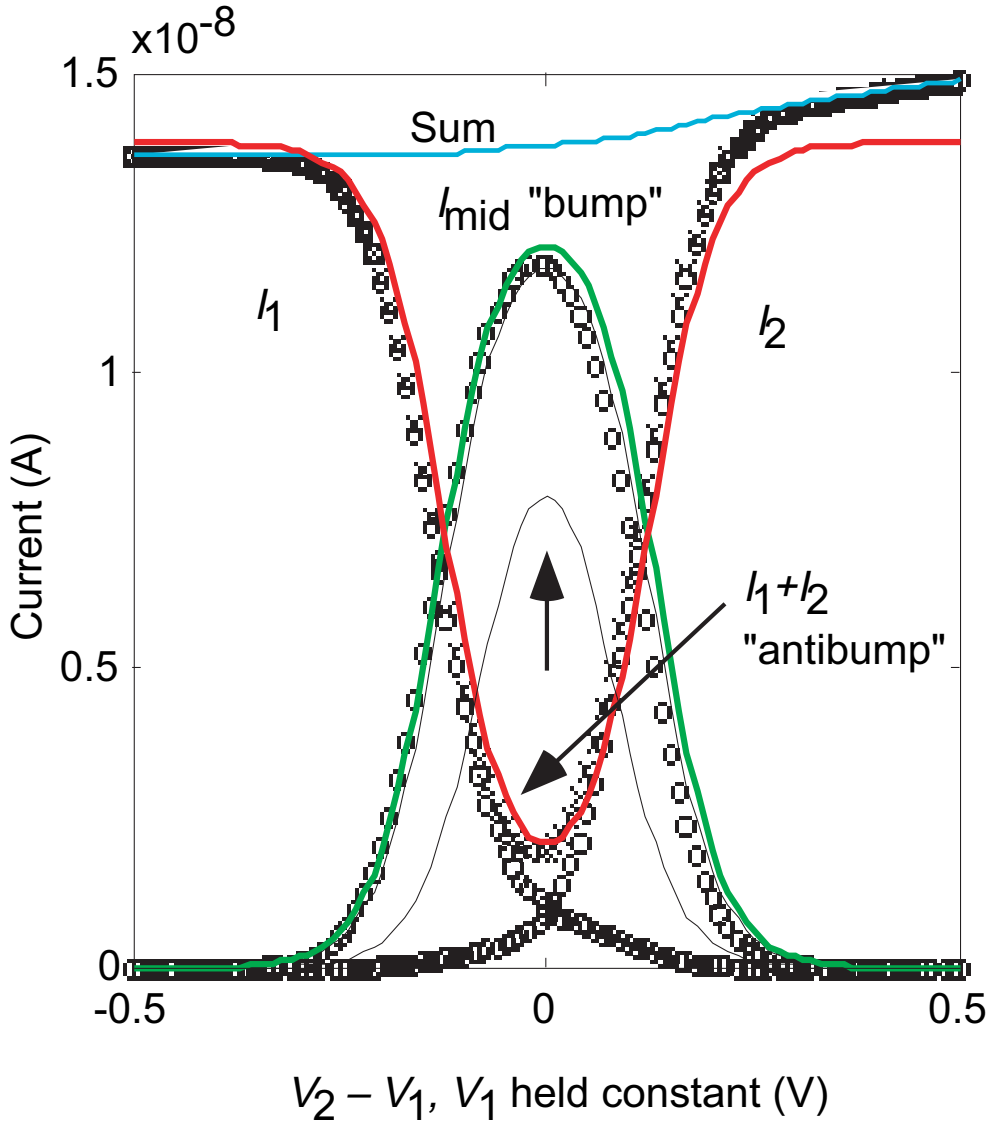
$$S = \frac{(W/L)_{middle}}{(W/L)_{outer}}$$

$$I_{out} = \frac{I_b}{1 + \frac{4}{S}\cosh^2\left(\frac{\kappa \Delta V}{2U_T}\right)}$$

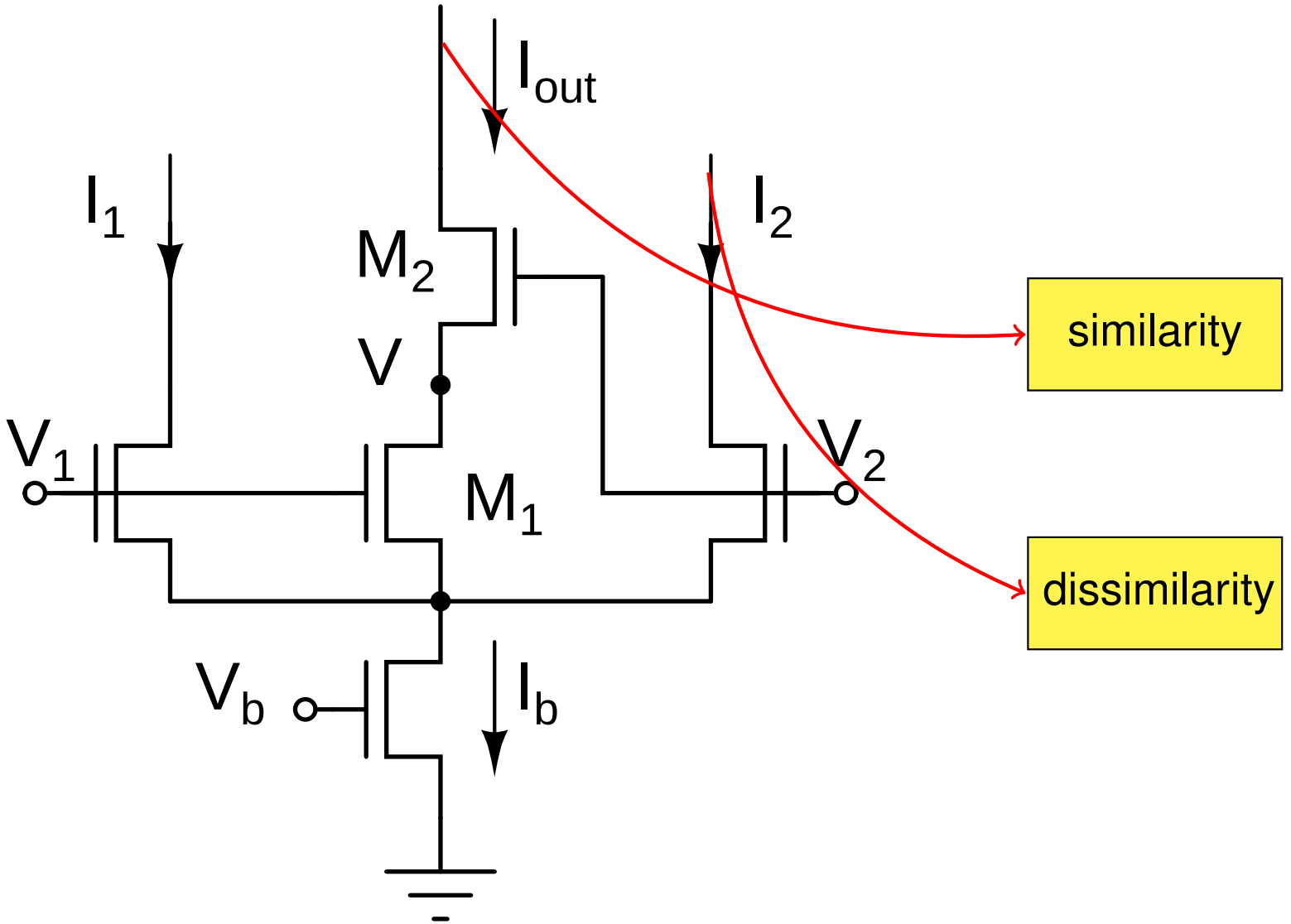
$$I_1 + I_2 = I_b - I_{out} = \frac{I_b}{1 + \frac{S}{4}\cosh^{-2}\left(\frac{\kappa \Delta V}{2U_T}\right)}$$

$$(I_1 + I_2)_{min} = \frac{I_b}{1 + \frac{S}{4}}$$

Bump circuit data



Bump-antibump circuit



Further info: `http://www.ini.uzh.ch/~tobi/anaprose/bump/`