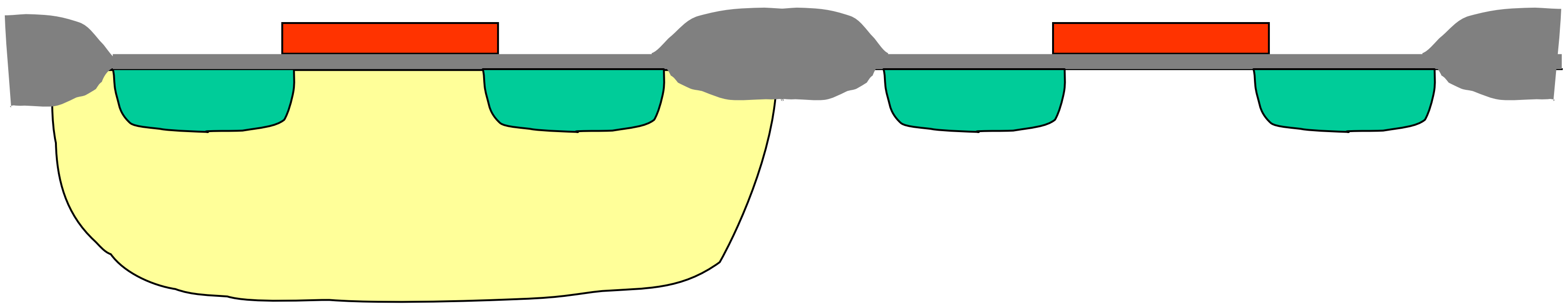
MOS transistors (in subthreshold)

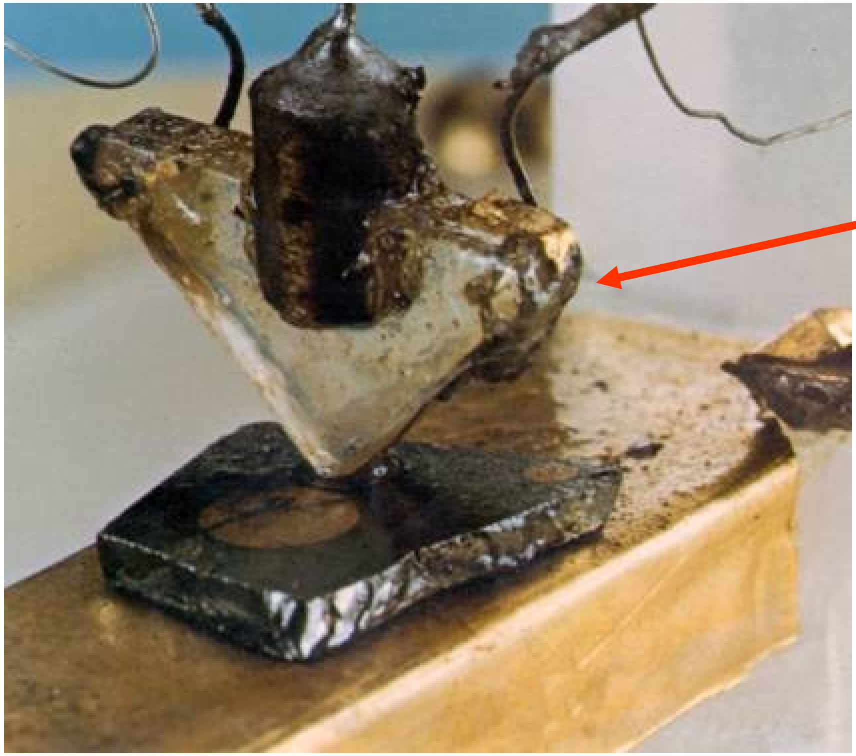


- History of MOSFET
- Review of Semiconductors
- What is a MOSFET? CMOS?
- How physics of transistors and voltage-sensitive nerve membrane channels are related
- MOS capacitor structure
- Surface: accumulation, depletion, inversion
- Capacitive dividers: The back-gate/body effect parameter kappa
- MOS transistor in subthreshold

History of the Transistor

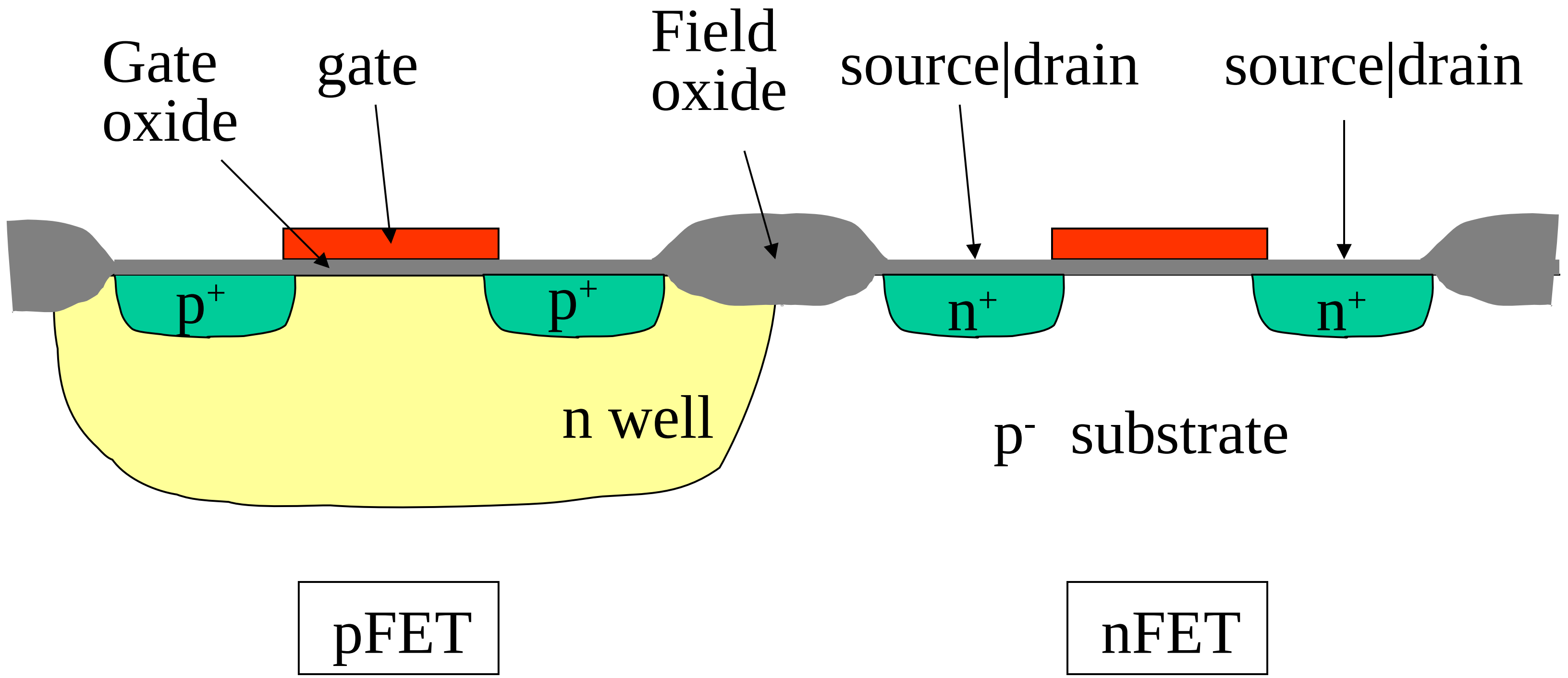
The term "transistor" is a generic name for a solid-state device with 3 or more terminals.

The field-effect transistor structure was first described in a patent by J. Lilienfeld in the 1930s! It took about 40 years before MOS transistors were in mass production.

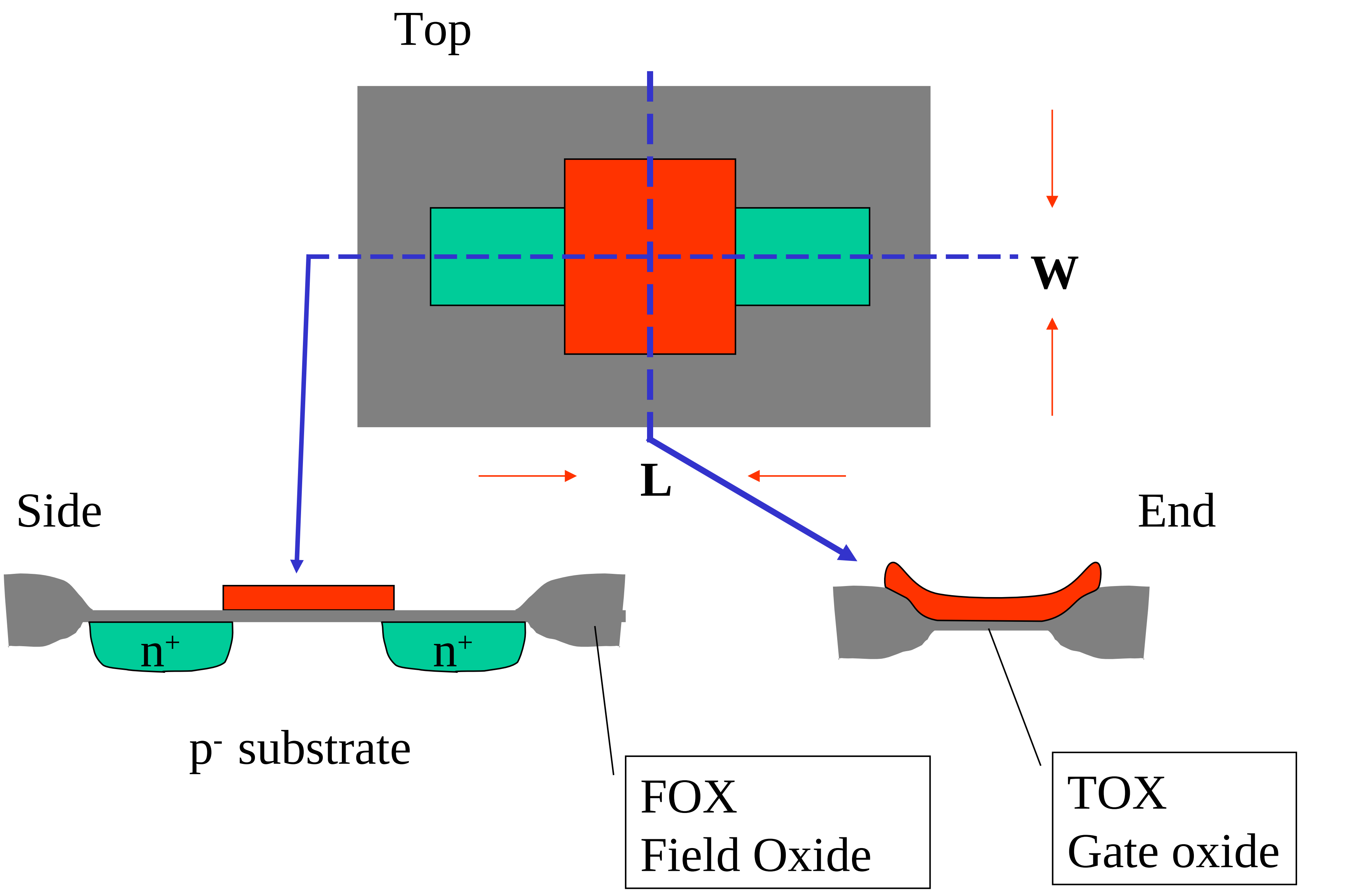


The first transistor (point-contact bipolar) fabricated at Bell Labs in 1947 (Bardeen, Brattain, Shockley). MOS transistors were not commericalized until mid 1970's.

Cross-section of a complementary pair of Field-Effect Transistor (FET)

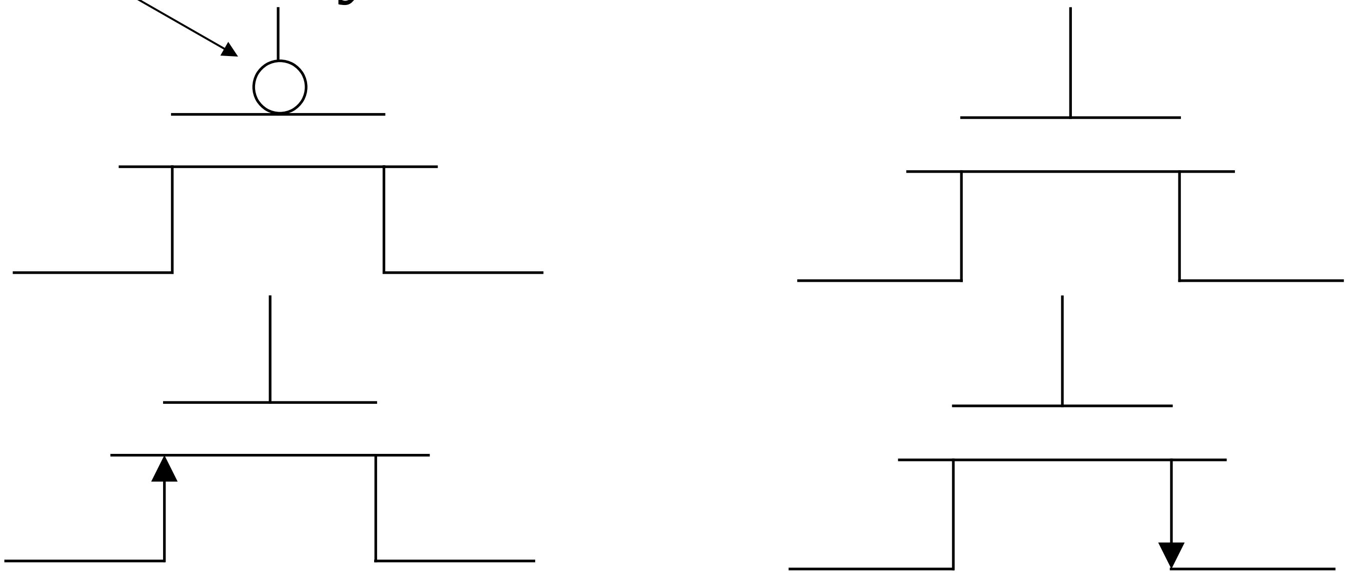


Top and Side Views of Field-Effect Transistor (FET)



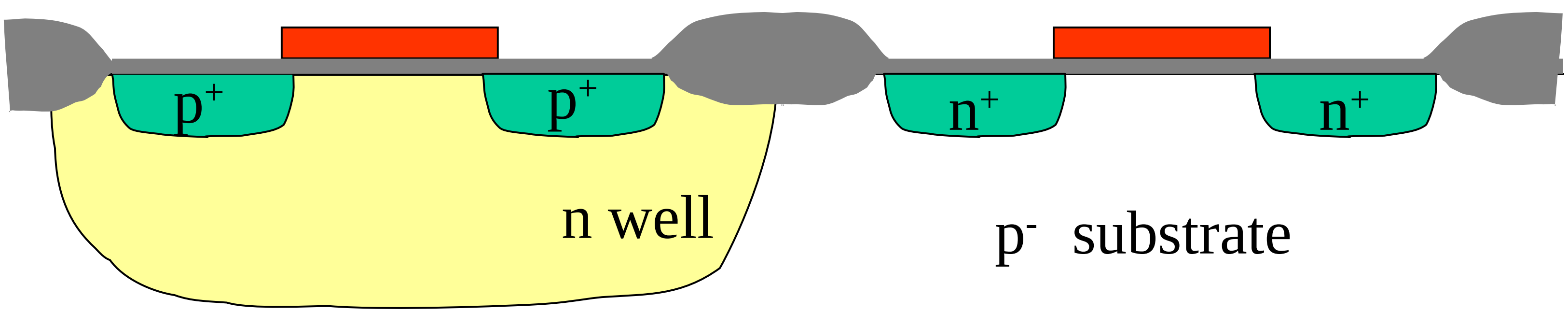
Symbols for transistors

hole carriers



pn junction & source

pn junction and source



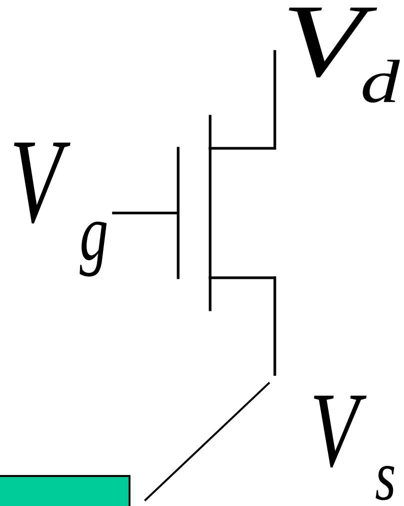
pFET

nFET

nFET terminology

Drain
(of electrons)
At higher voltage

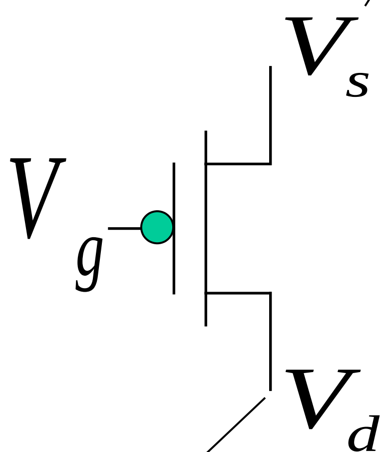
Gate
Putting positive charge here attracts electrons



Source
(of electrons)
At lower voltage

pFET terminology

Gate
Putting negative charge here attracts holes



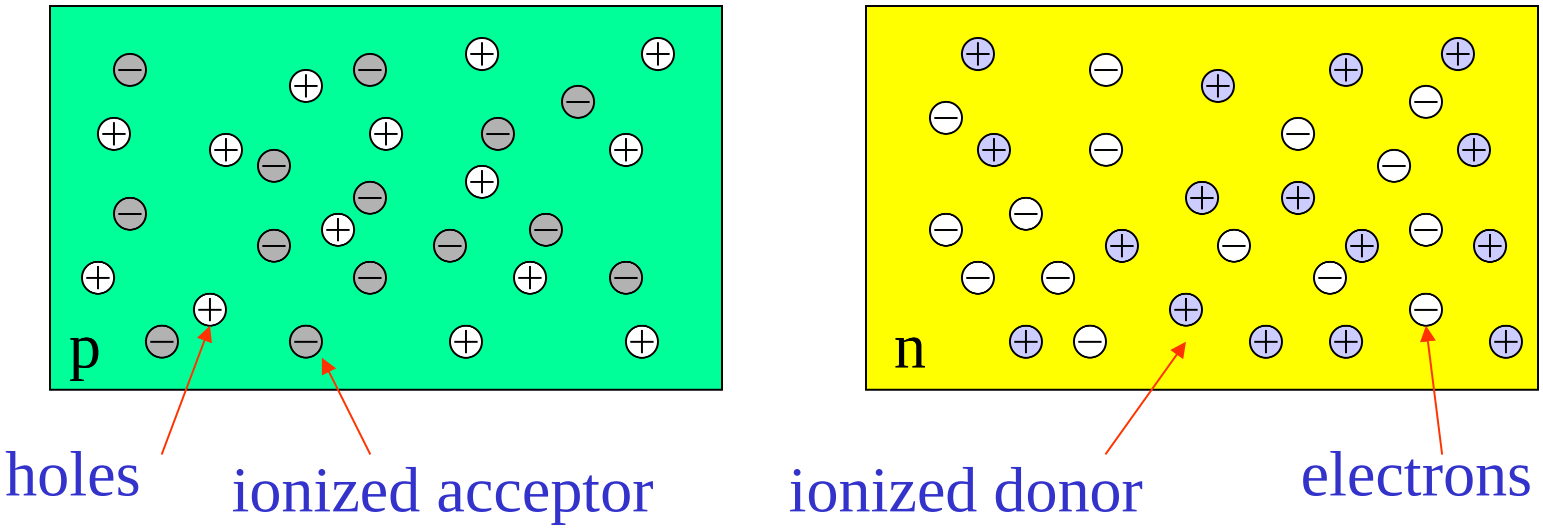
Source
(of holes)
At higher voltage

Drain
(of holes)
At lower voltage

Review on Semiconductors

Intrinsic silicon is undoped

Extrinsic silicon is doped



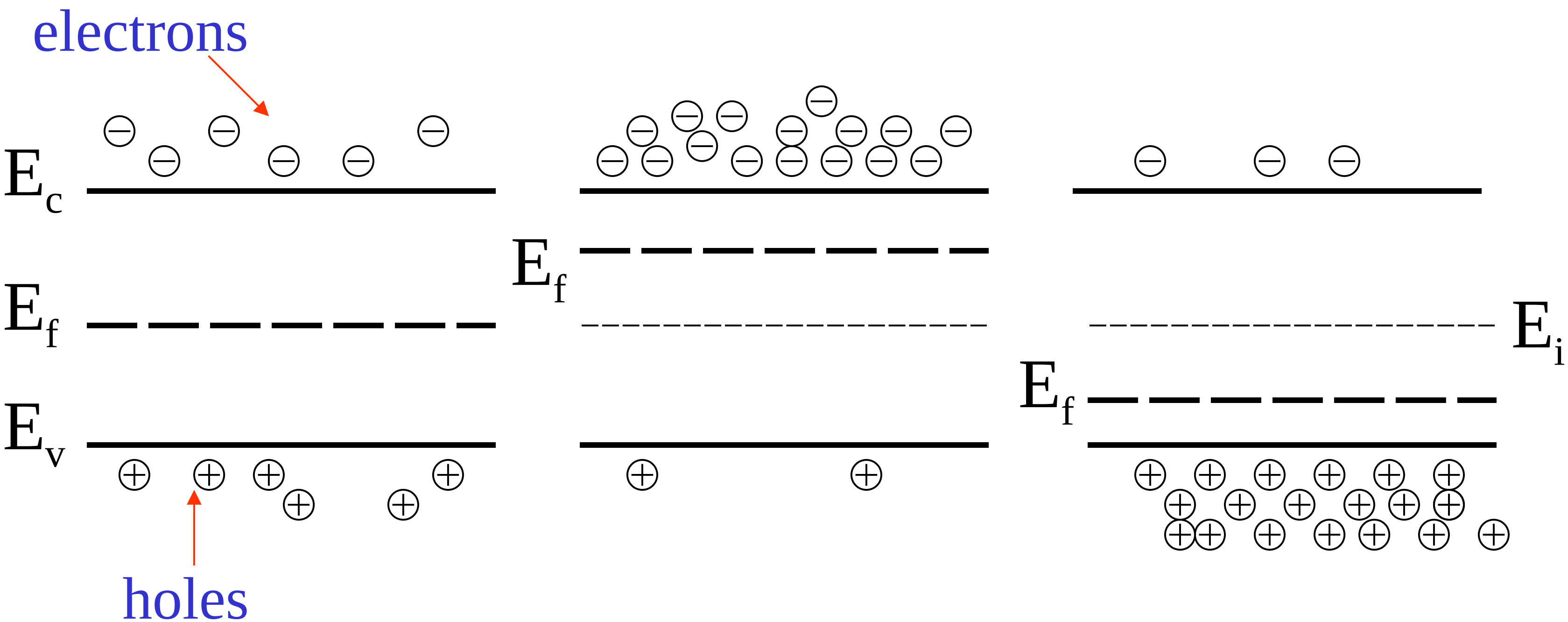
Majority carriers are holes

Minority carriers are electrons

Majority carriers are electrons

Minority carriers are holes

Review on Energy Band Diagrams



Intrinsic silicon

n-type silicon

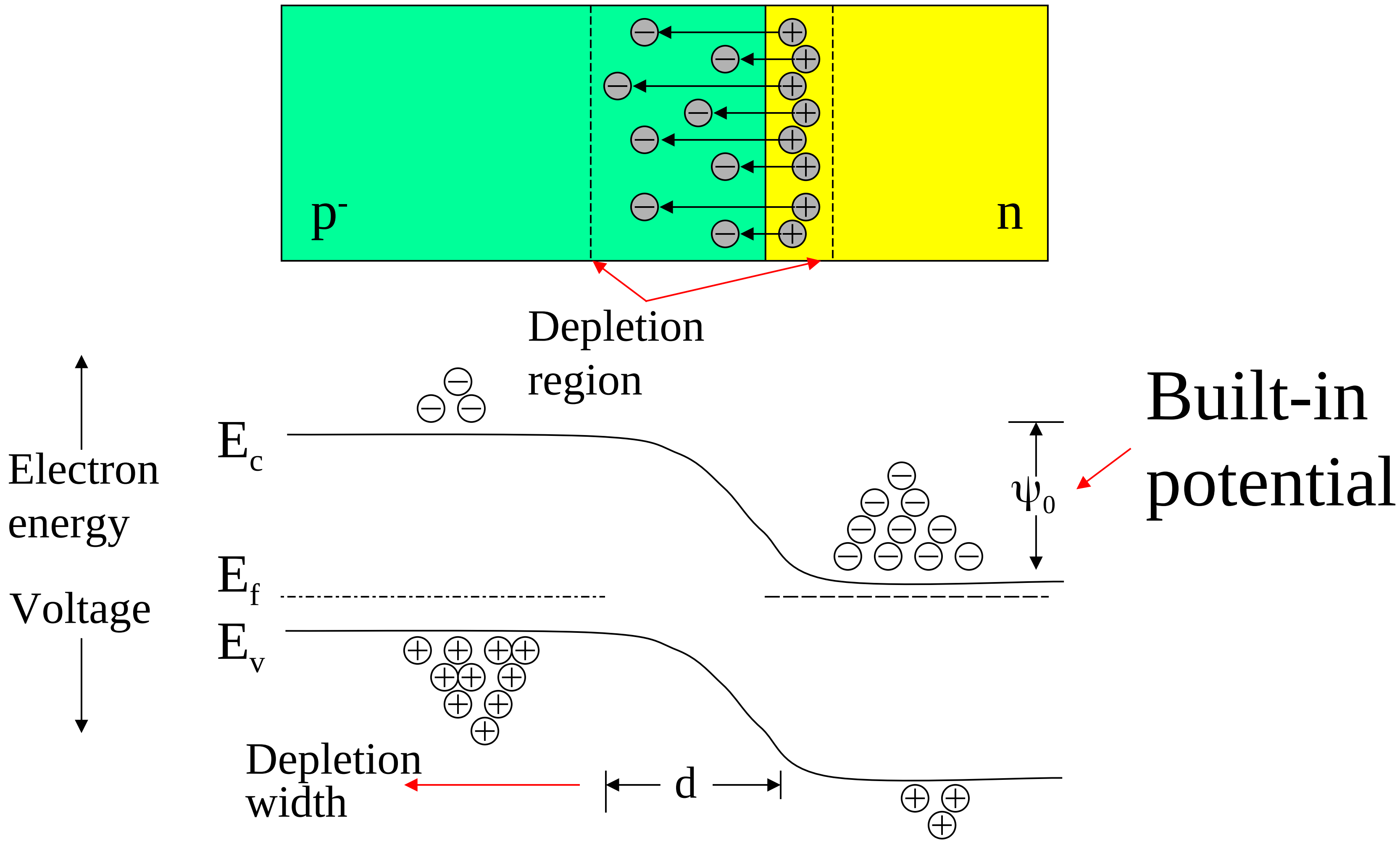
p-type silicon

$$np = n_i^2$$

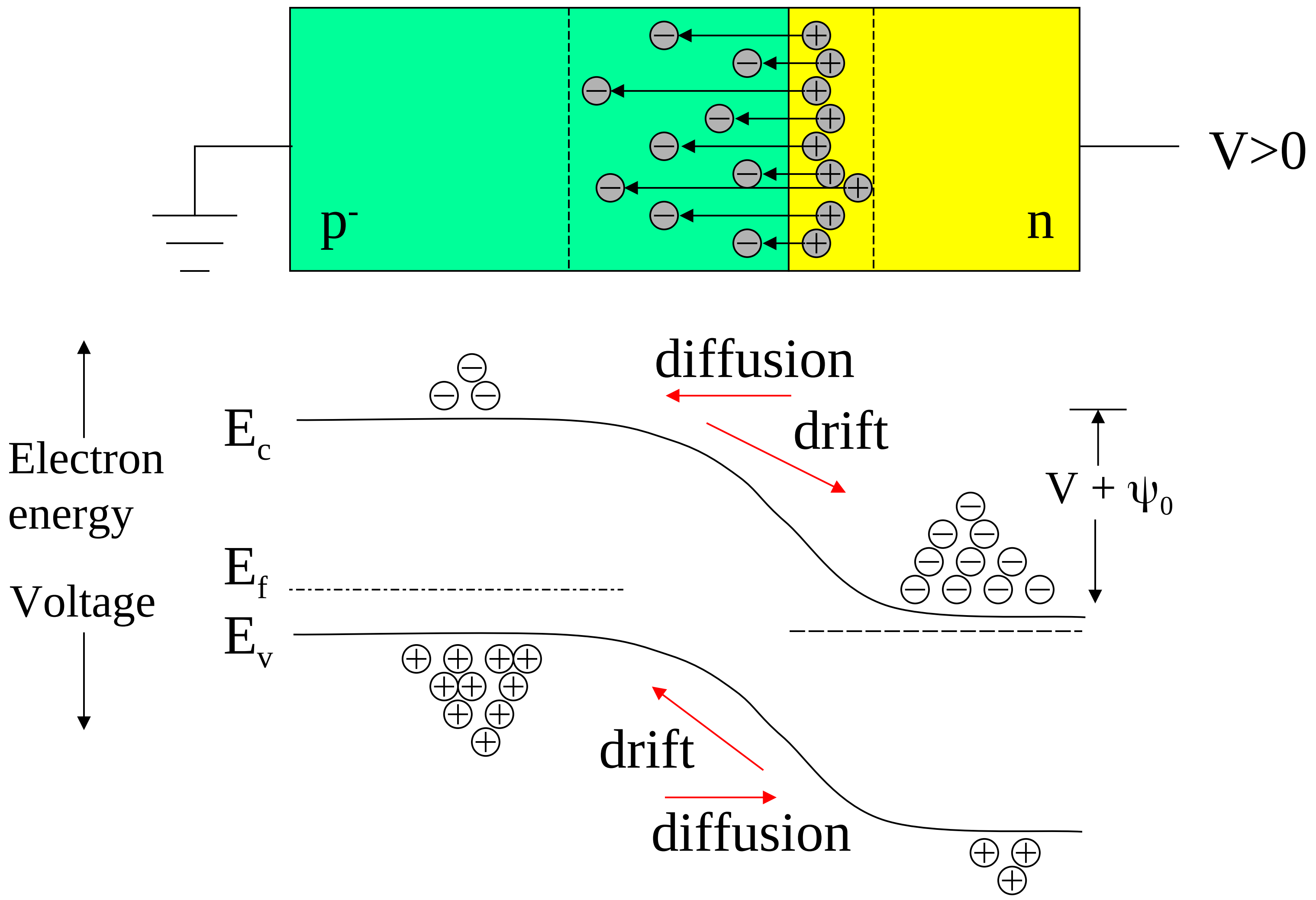
$$n = n_i \exp\left(\frac{E_f - E_i}{kT}\right) = N_D$$

$$p = n_i \exp\left(\frac{E_i - E_f}{kT}\right) = N_A$$

Equilibrium in a p-n Junction



Reverse-biased p-n Junction

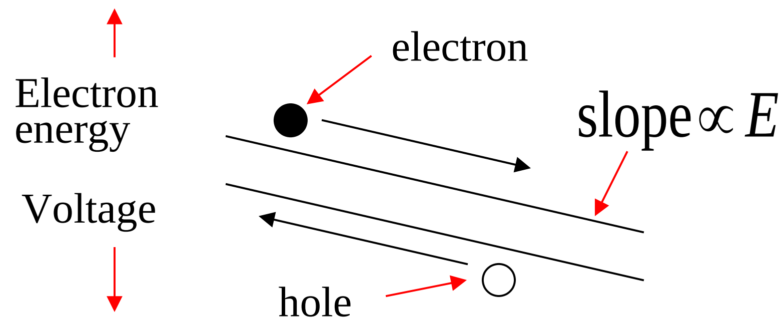


Mechanisms of Carrier Transport

<u>Drift</u>: Movement of charge carriers due to an external field

Current → $I = qN\mu E$

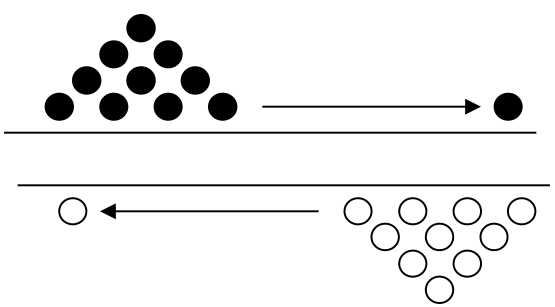
Carrier density — Carrier mobility — Electric field



<u>Diffusion</u>: Movement of carriers due to a concentration gradien

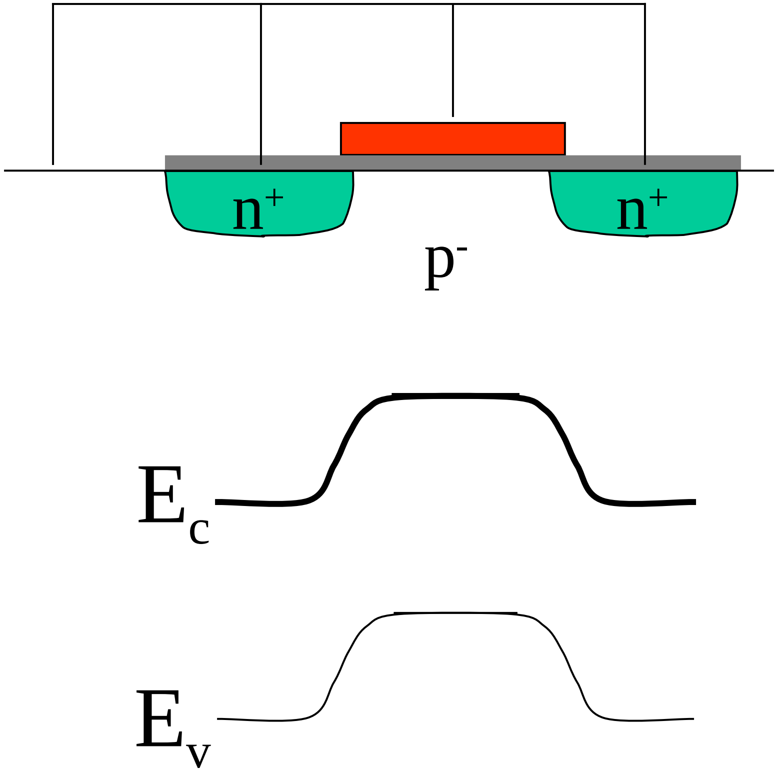
Current → $I = -qD\dfrac{\partial N}{\partial x}$

Diffusion constant — Concentration gradient

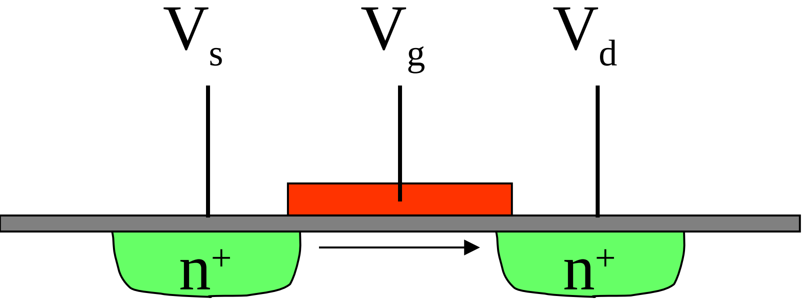


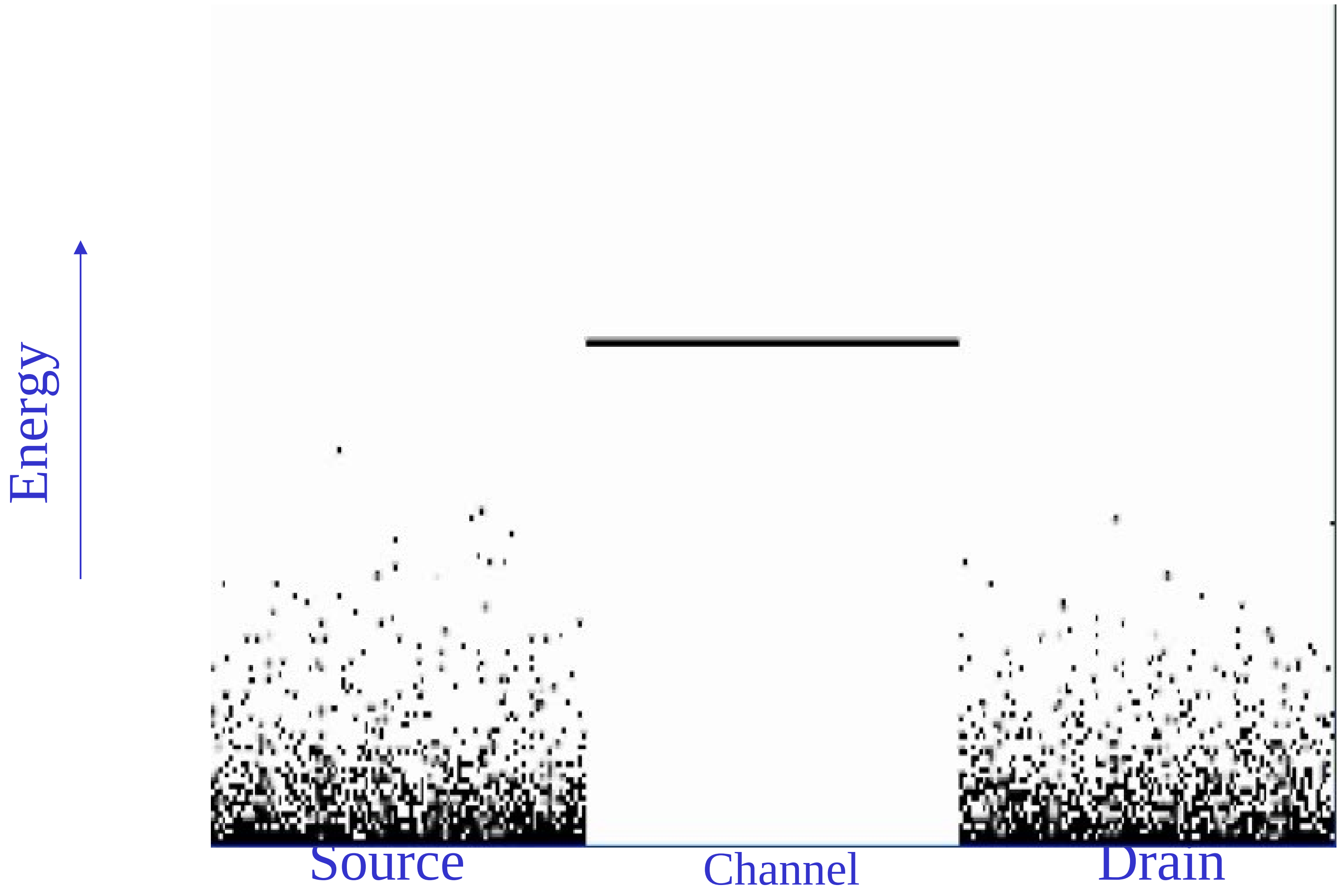
Einstein relation: $\boxed{D = \dfrac{kT}{q}\mu}$

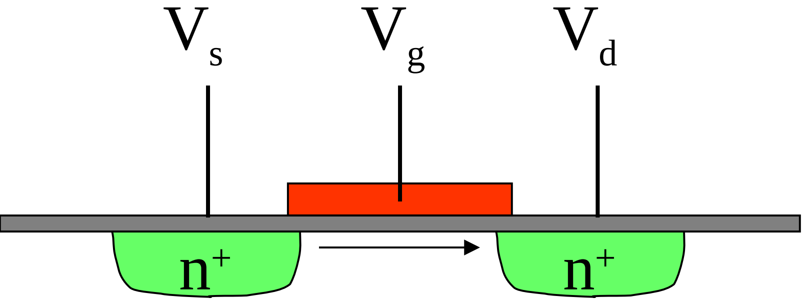
The built-in potentials in the *pn* junctions create an *energy barrier*. Controlling the barrier height controls the diffusion current.



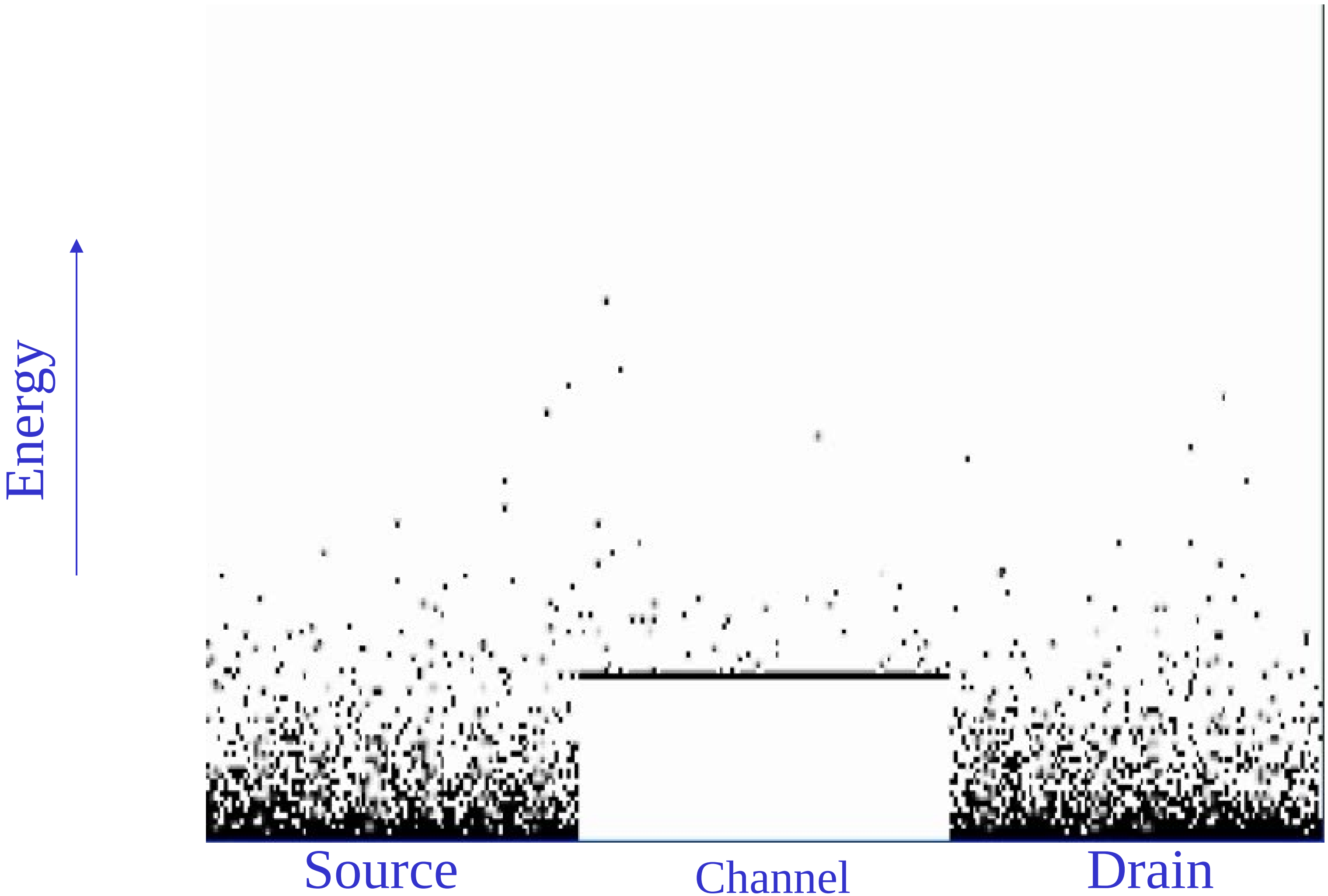
Small Vgs, Vds=0



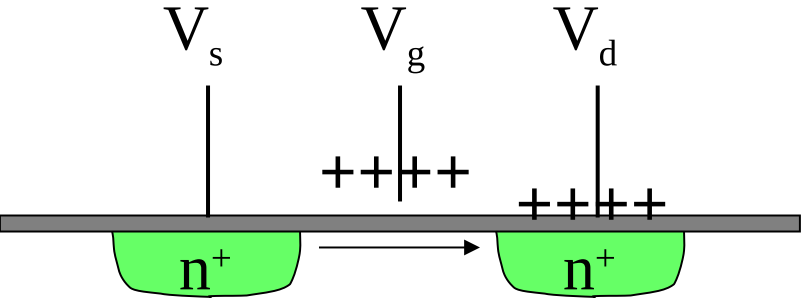


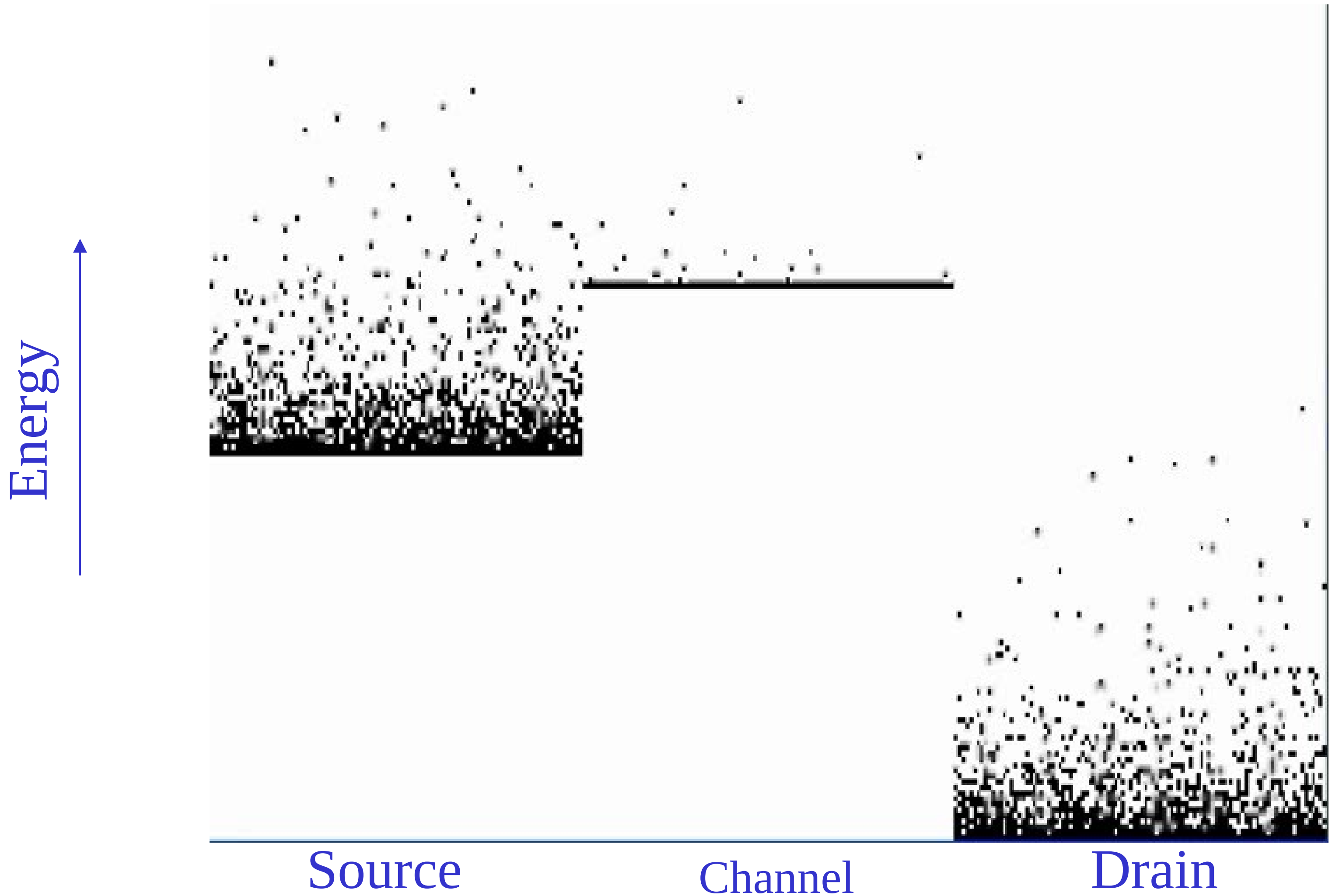


Larger Vgs, Vds=0

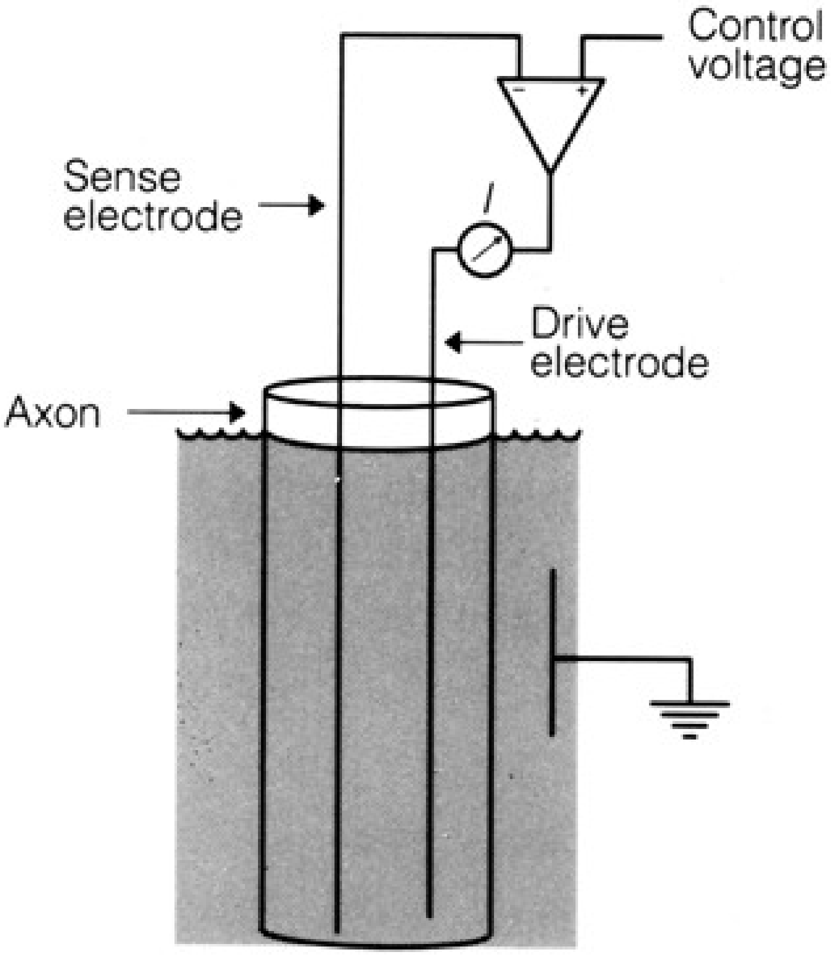


Larger Vgs, Large Vds

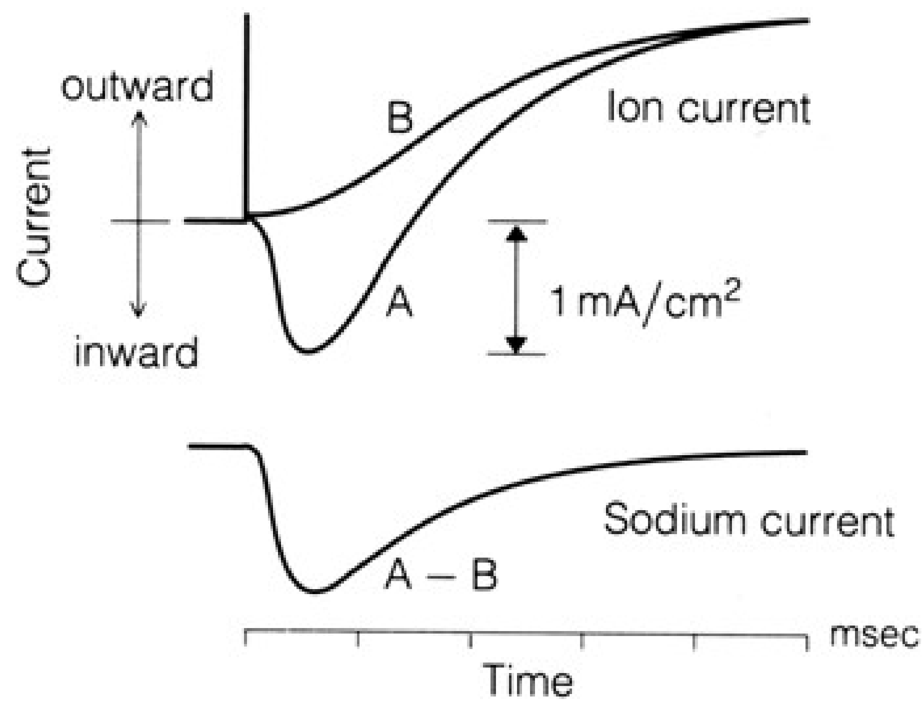




Measuring voltage-dependent nerve membrane currents

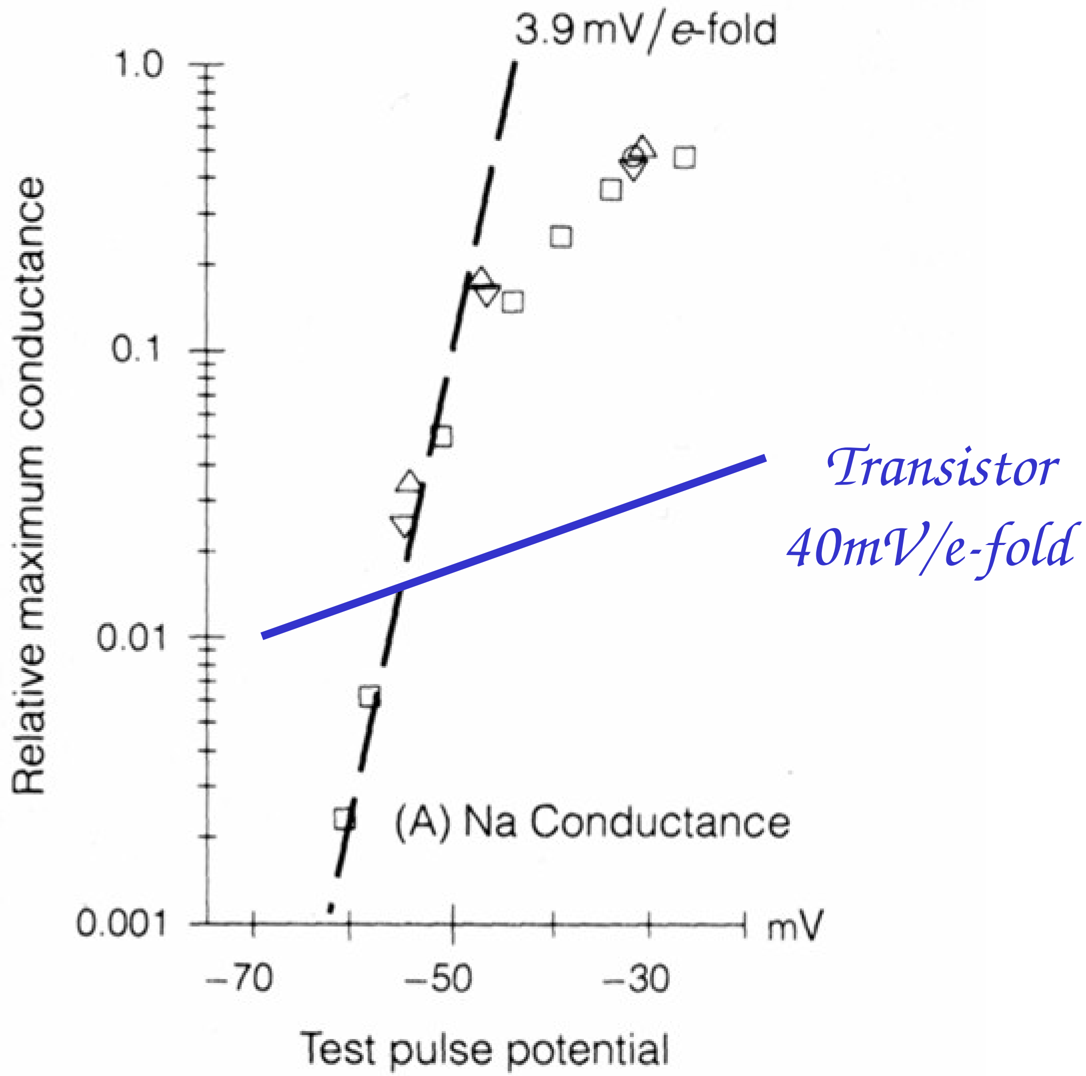


Axon voltage clamp



Hodgkin & Huxley 1952

Comparing transistor and membrane channel currents



Neuron channels and Transistors

Both depend on Boltzmann distributions.

Neurons

- Membrane ionic conductance is exponentially dependent on the voltage across the neuron membrane.
- The **population of open channels** depends exponentially on potential across barrier.

Transistors

- Current flow in transistors is exponentially dependent on barrier height.
- The **population of carriers** depends exponentially on the barrier height.

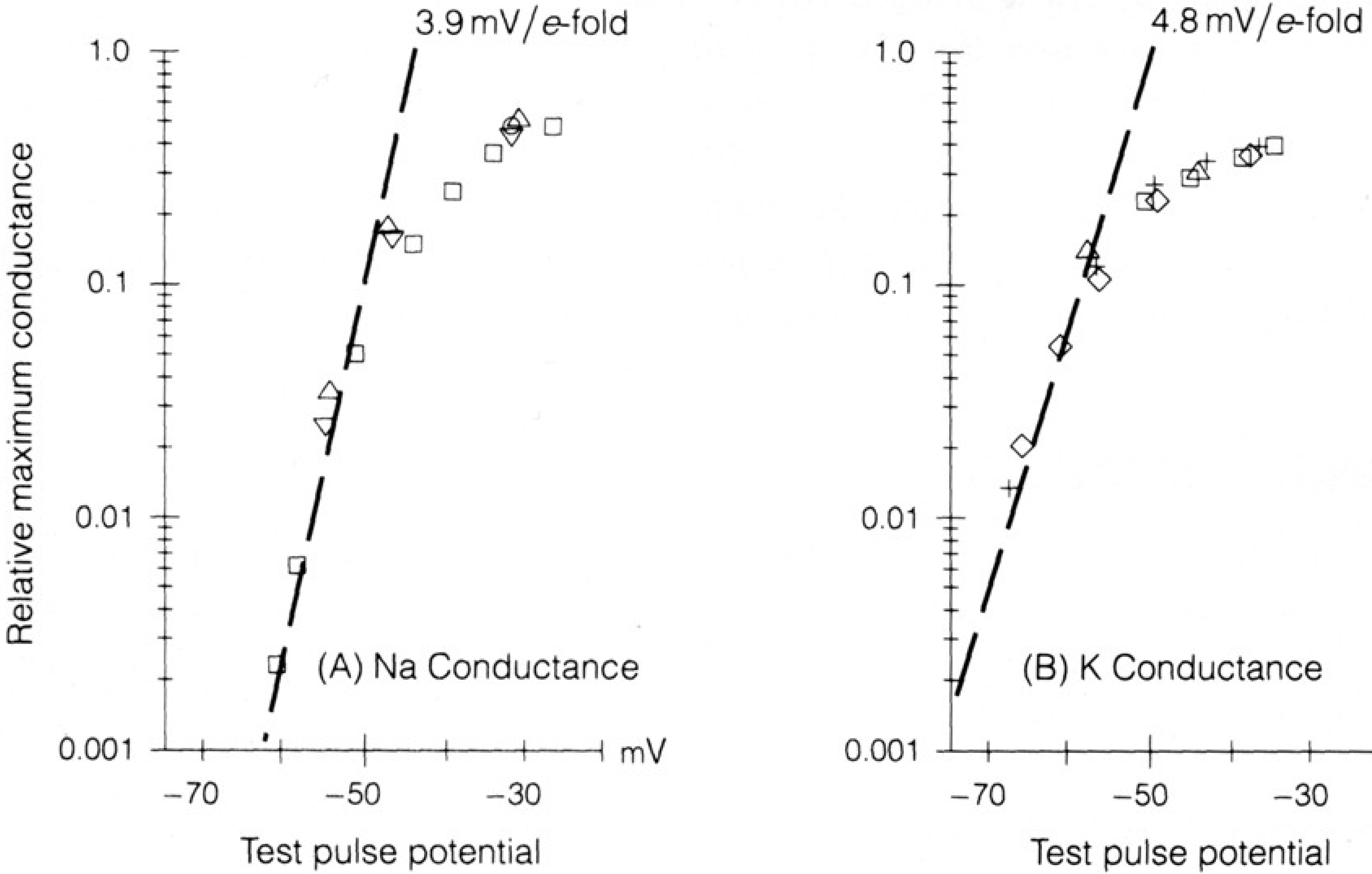
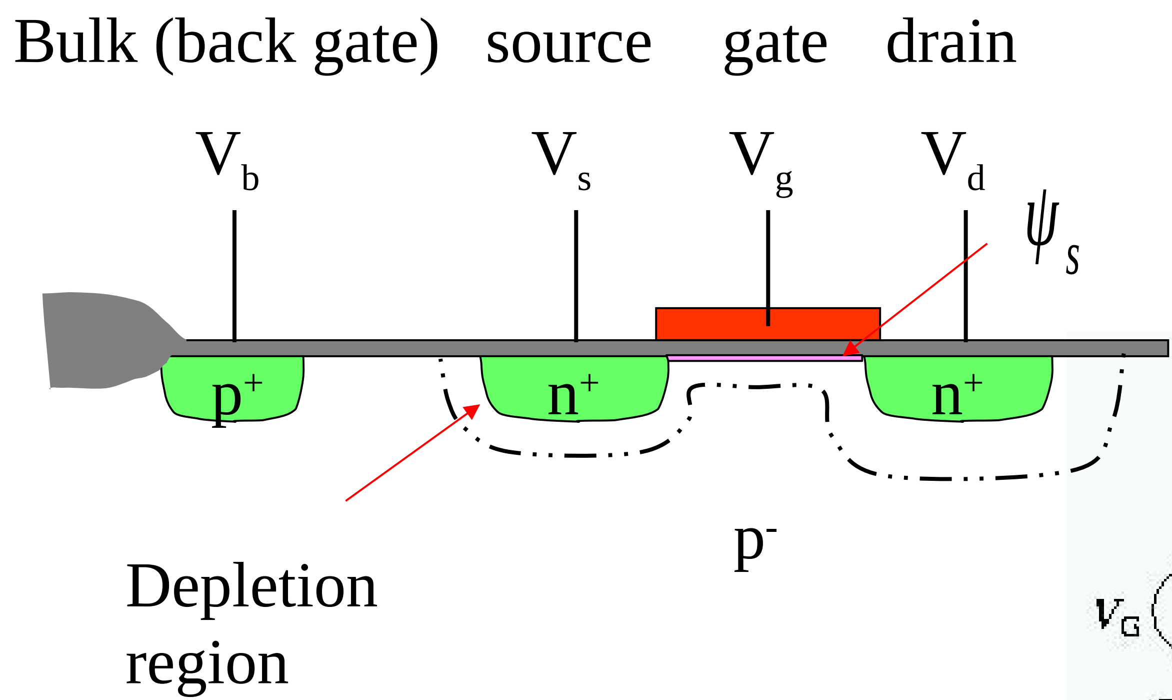


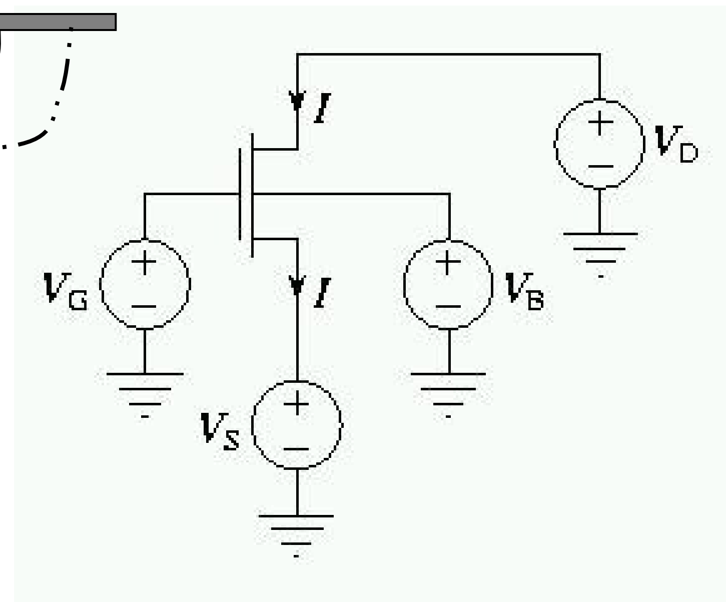
FIGURE 4.6 Exponential current–voltage characteristic of voltage-dependent channels. At high voltages, the fraction of channels that are open approaches unity, causing a saturation of the curves. (*Source:* [Hodgkin et al., 1952b, p. 464].)

n-type MOSFET



$$V_s \geq 0\text{V}$$

$$V_g, V_d \geq V_s$$



All voltages are referenced to V_b = 0V

Regimes of operation for FET (dependent on V_{gs})

- <u>Cutoff </u> - Surface is accumulated

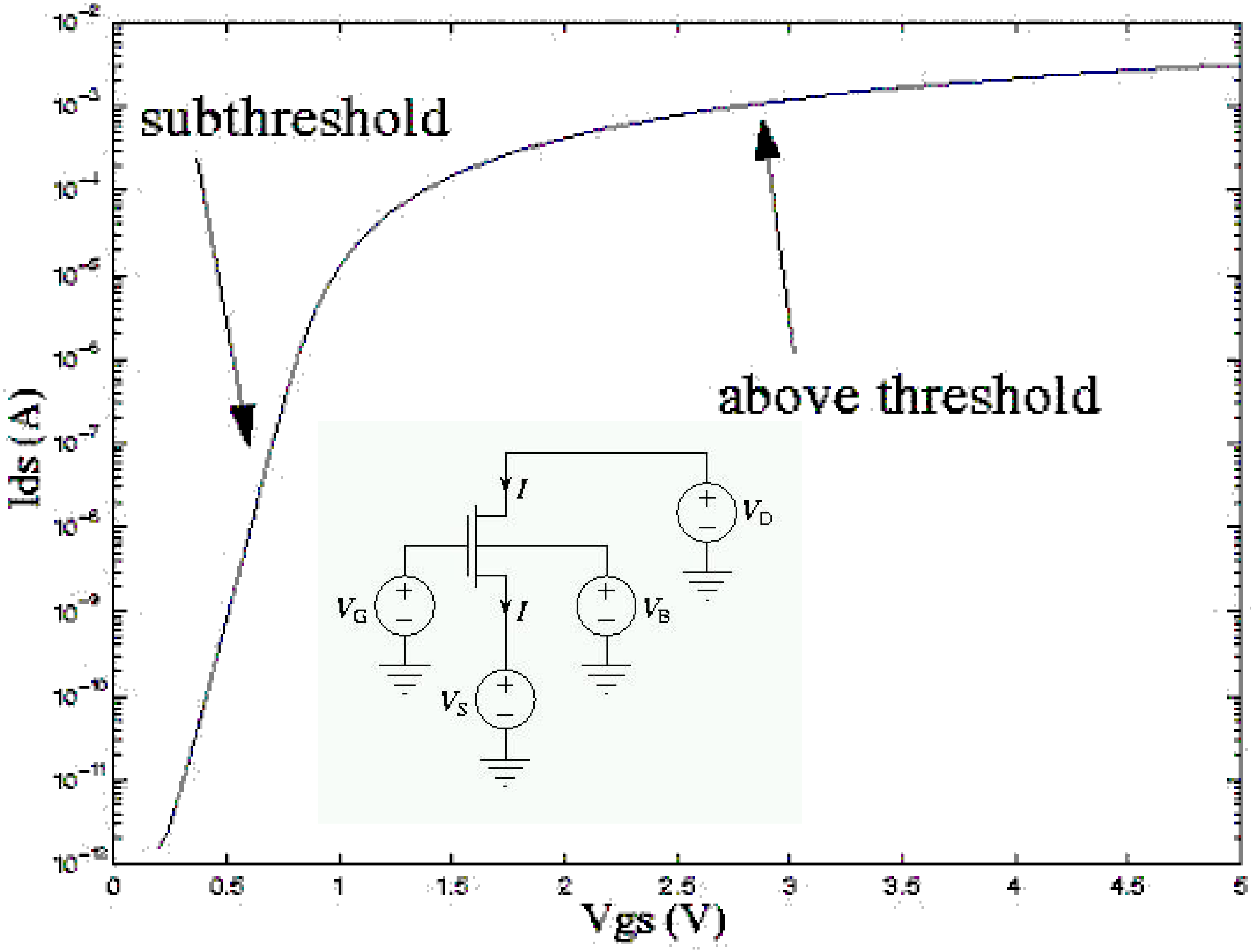
- <u>Subthreshold (Weak Inversion) Regime</u>

  Current flows through diffusion

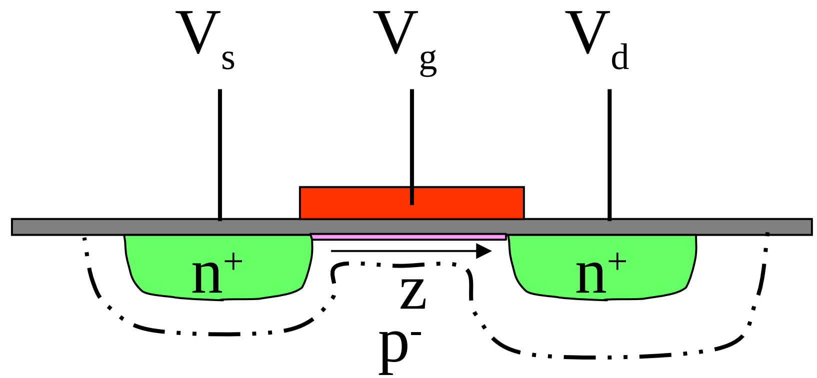
- <u>Above threshold (Strong Inversion) Regime</u>

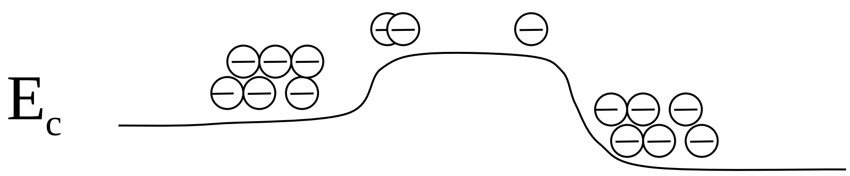
  Current flows through drift

nFet curve: I *vs.* V_{gs}



Subthreshold nFET: Current is diffusion current





$$I = -qD\frac{dN}{dz}$$

Current

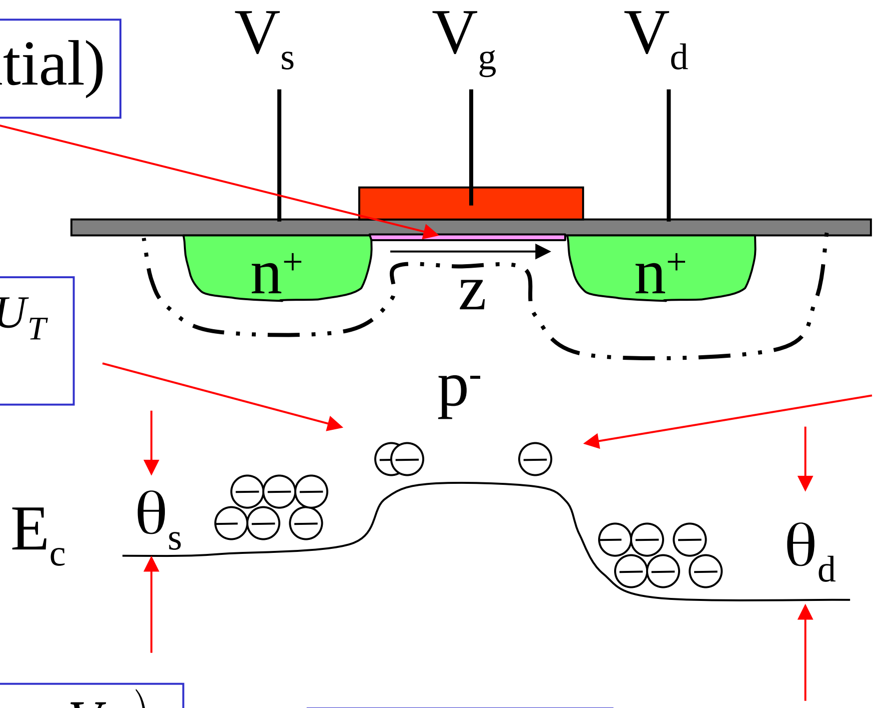
Diffusion constant

Concentration gradient

N=carrier density
D=diffusion constant

Subthreshold nFET: Current is diffusion current

ψ_s (surface potential)



$$N_s = N_o e^{-\theta_s / U_T}$$

$$N_d = N_o e^{-\theta_d / U_T}$$

$$\theta_s = \theta_0 - q(\psi_s - V_s)$$
$$\theta_d = \theta_0 - q(\psi_s - V_d)$$

$$\frac{dN}{dz} = \frac{N_s - N_d}{L}$$

N=carrier density per unit volume
W=channel width
L=channel length
D=diffusion constant
θ_o=built-in voltage

$$I = -qWD_n \frac{dN}{dz} = I_0 e^{\psi_s / U_T} \left(e^{-V_d / U_T} - e^{-V_s / U_T}\right)$$

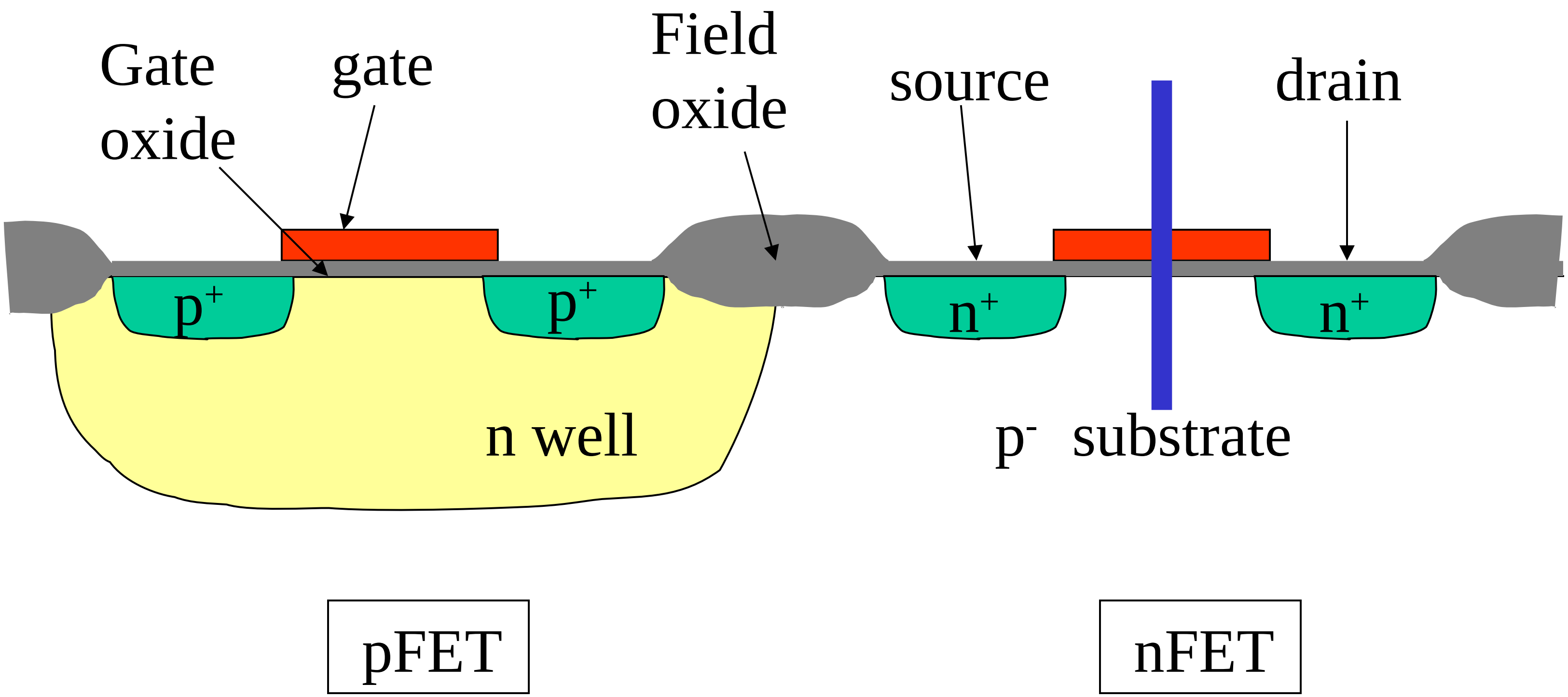
Fwd Rev

We have equation for subthreshold current, but we don't directly control the surface potential

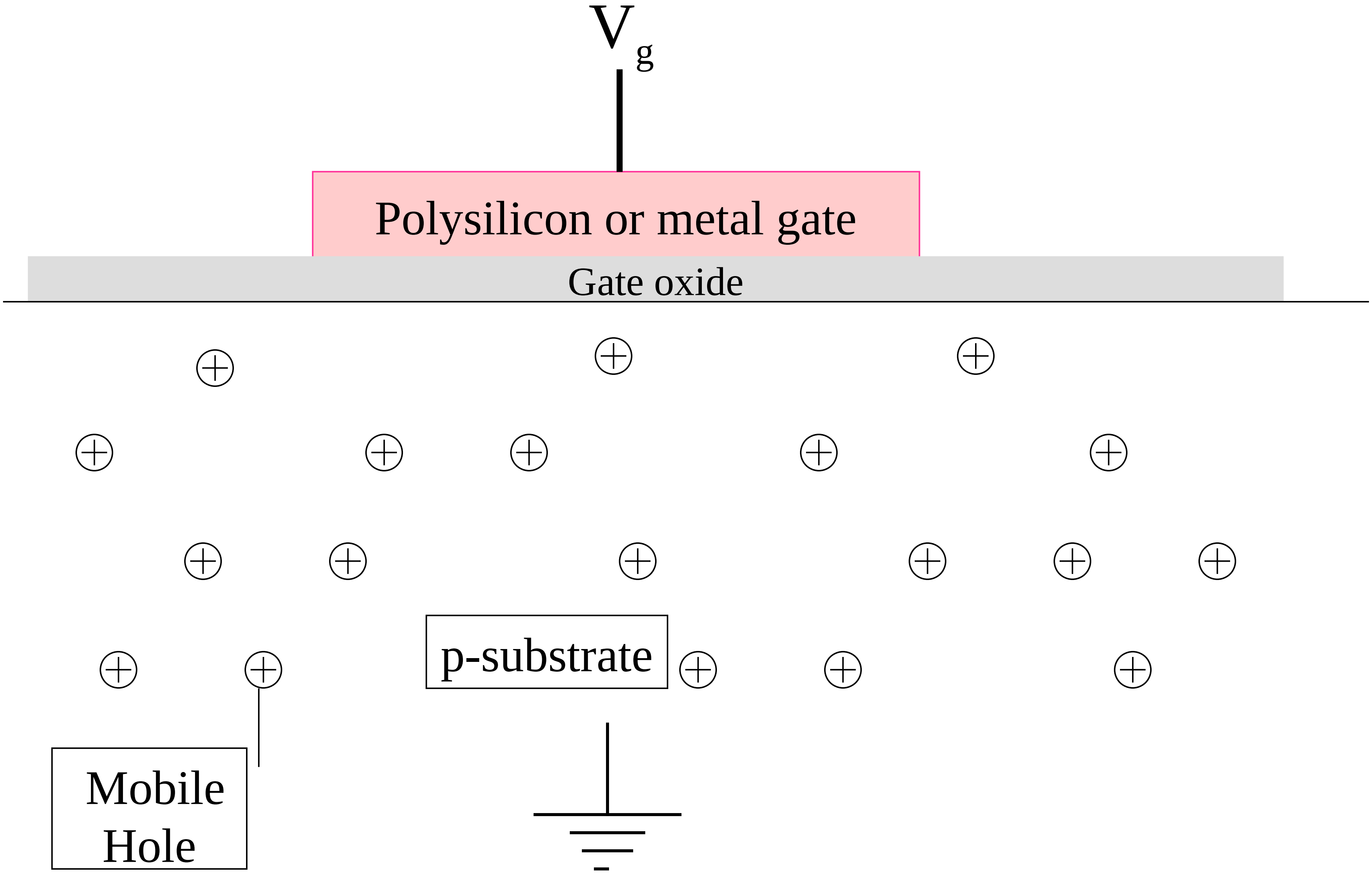
$$\boxed{I = -qWD_n \frac{dN}{dz} = I_0 e^{\psi_s/U_T}\left(e^{-V_d/U_T} - e^{-V_s/U_T}\right)}$$

How is the surface potential related to the gate voltage?

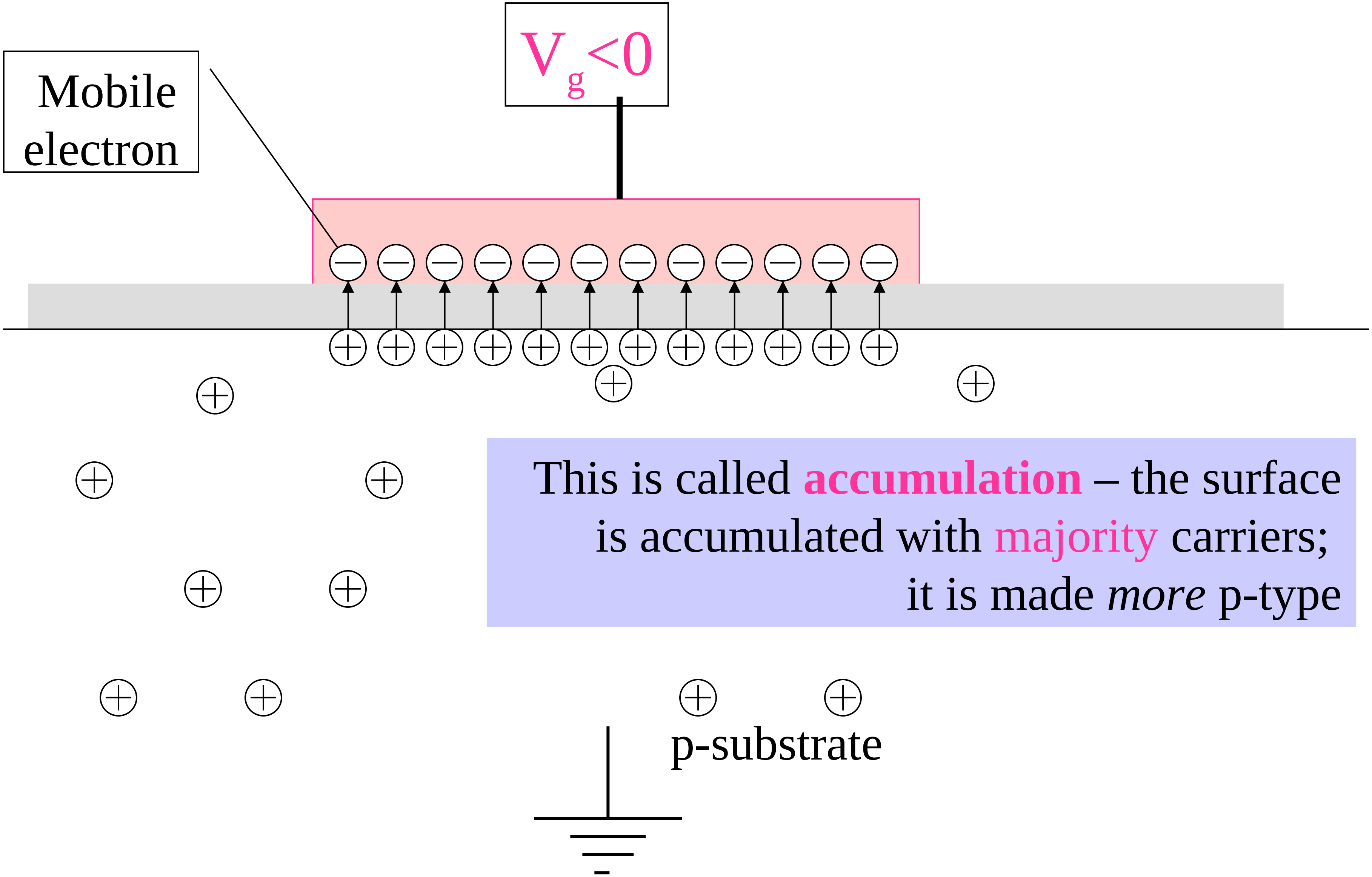
We need to understand effect of gate on surface potential



MOS capacitor structure

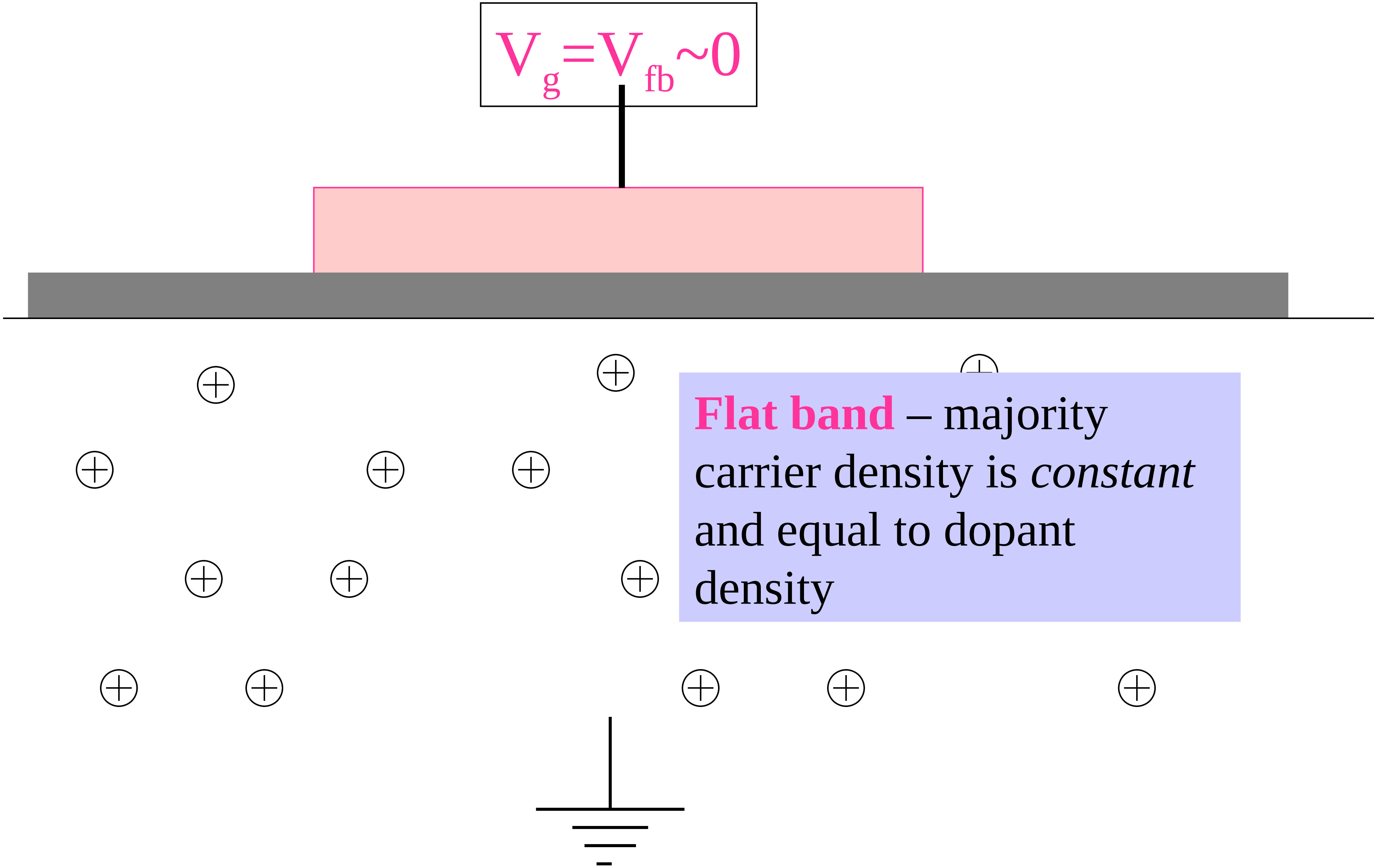


MOS capacitor structure: accumulation



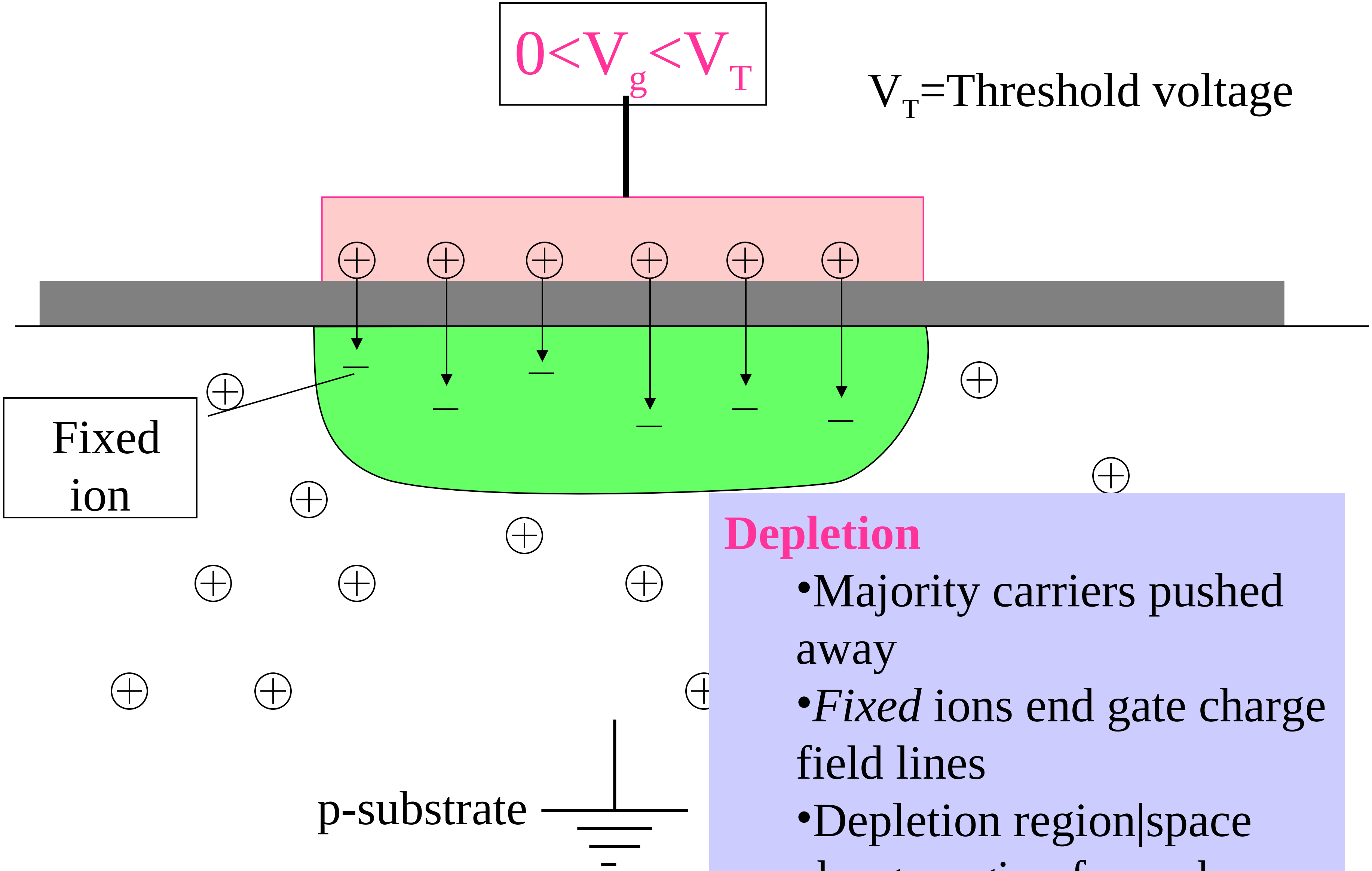
This is called **accumulation** – the surface is accumulated with majority carriers; it is made *more* p-type

MOS capacitor structure: flat band



Flat band – majority carrier density is *constant* and equal to dopant density

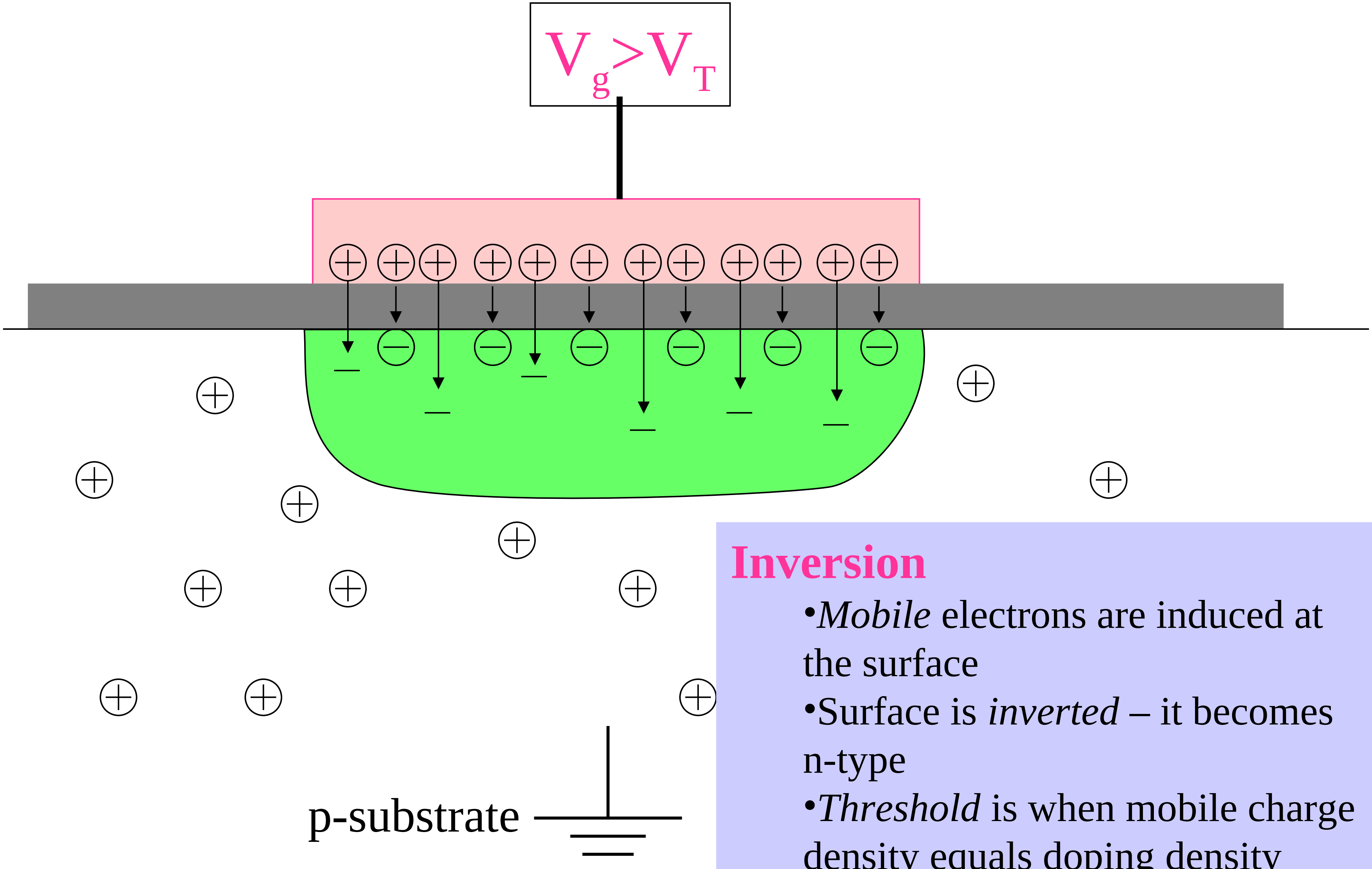
MOS capacitor structure: depletion



Depletion

- Majority carriers pushed away
- *Fixed* ions end gate charge field lines
- Depletion region|space charge region formed

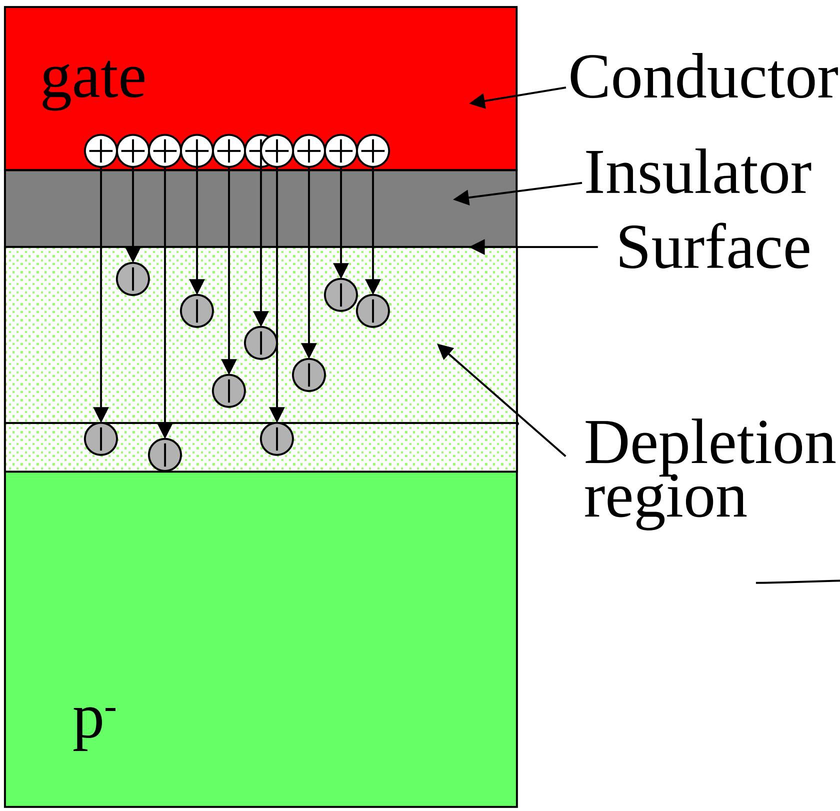
MOS capacitor structure: inversion



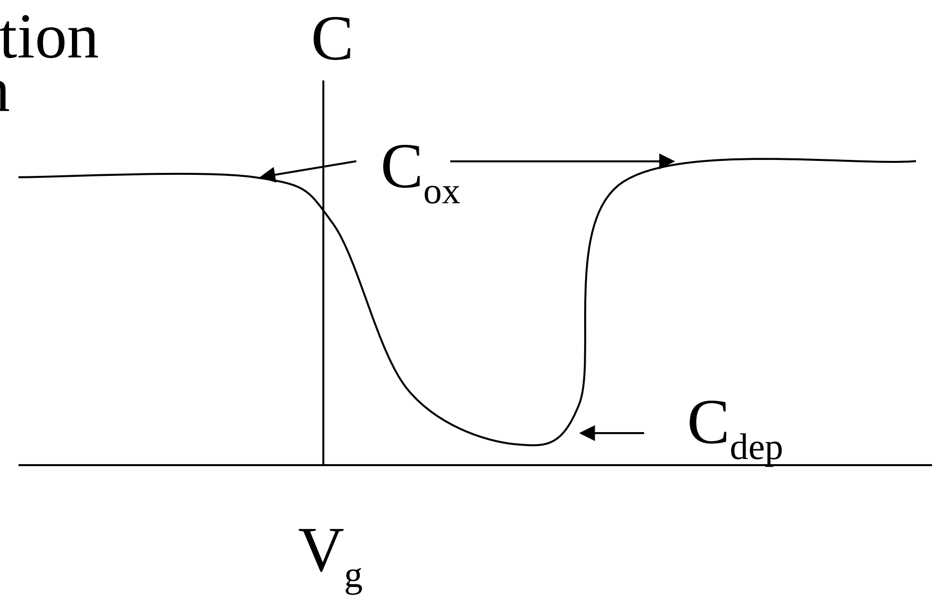
Inversion

- *Mobile* electrons are induced at the surface
- Surface is *inverted* – it becomes n-type
- *Threshold* is when mobile charge density equals doping density

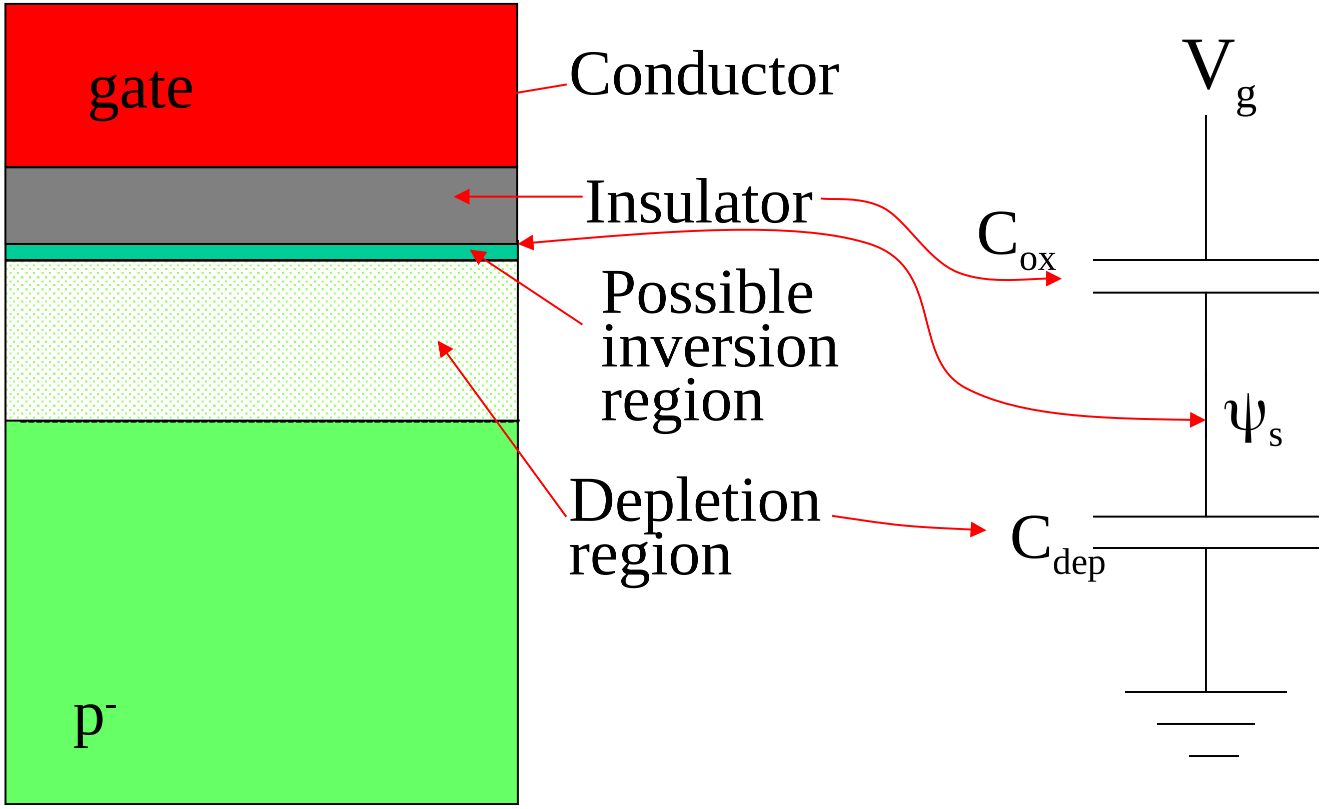
What is a *depletion capacitor*?



$$C = \frac{dQ}{dV}$$



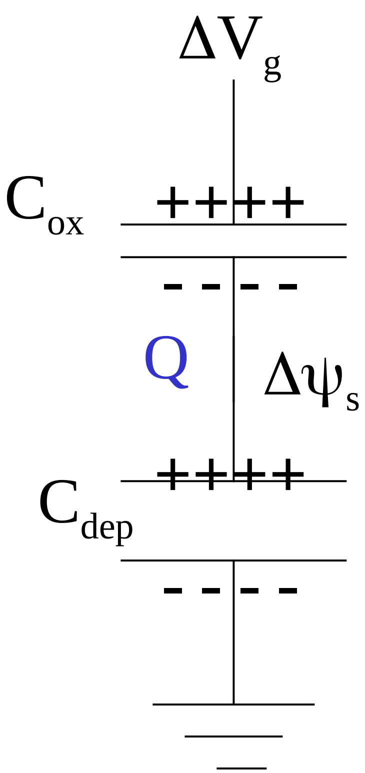
Influence of gate on surface potential



ψ_s = *Surface potential*

$$\kappa(kappa) = \frac{\partial \psi_s}{\partial V_g} = \frac{C_{ox}}{C_{ox} + C_{dep}}$$

Gate-depletion capacitive divider



How does changing V_g change ψ_s?

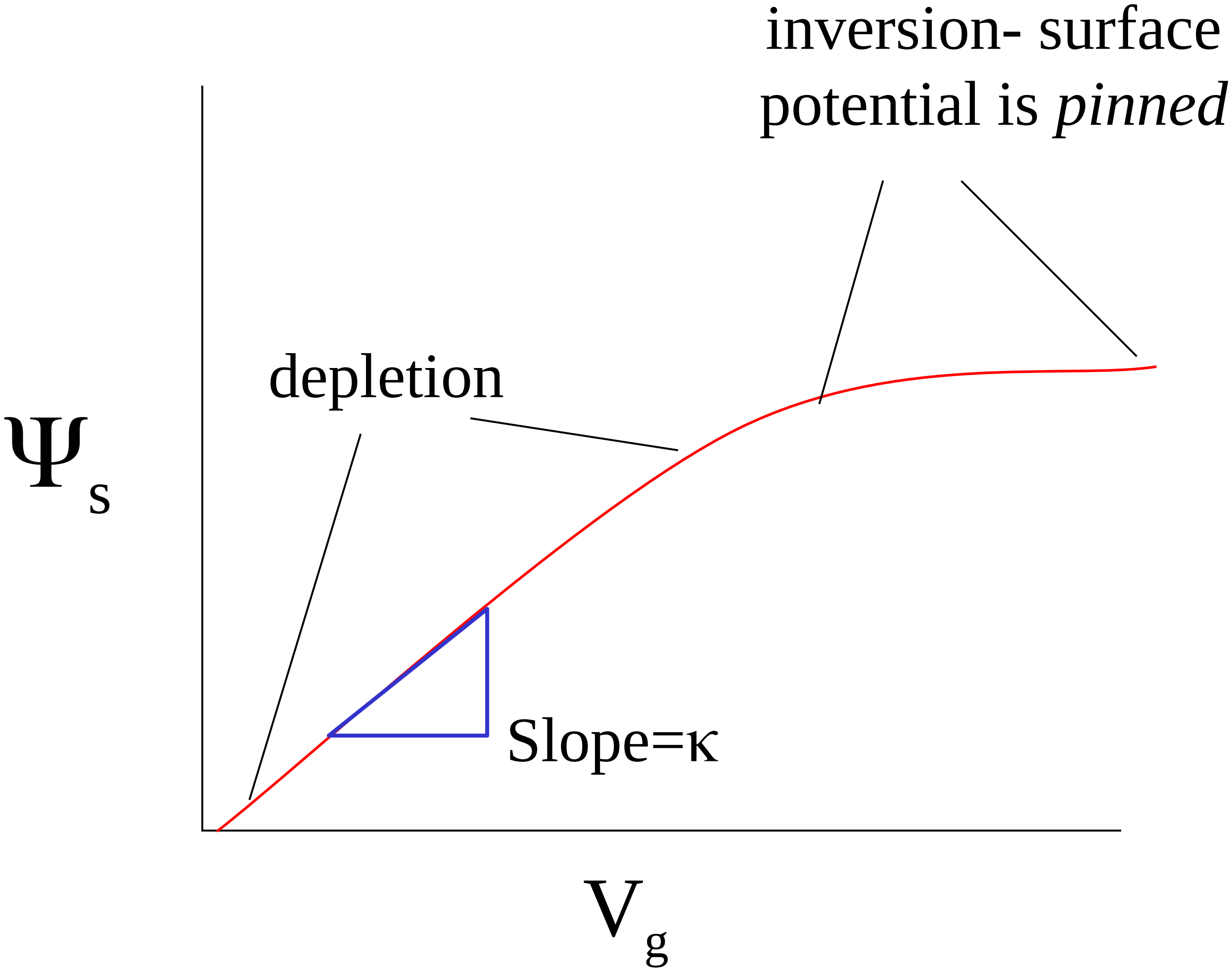
1. CV=Q
2. Charge Q on ψ_s is constant
3. Change V, hold Q constant

$$C_{ox}(\Delta V_g - \Delta\psi_s) = C_{dep}\Delta\Psi_s$$

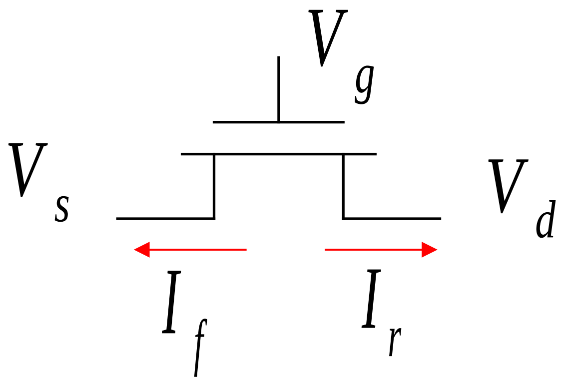
$$C_{ox}\Delta V_g = (C_{ox} + C_{dep})\Delta\Psi_s$$

$$\frac{\Delta\Psi_s}{\Delta V_g} = \frac{C_{ox}}{C_{ox} + C_{dep}} \equiv \boldsymbol{K}$$

Surface potential as function of V_g



Equations for Subthreshold nFET



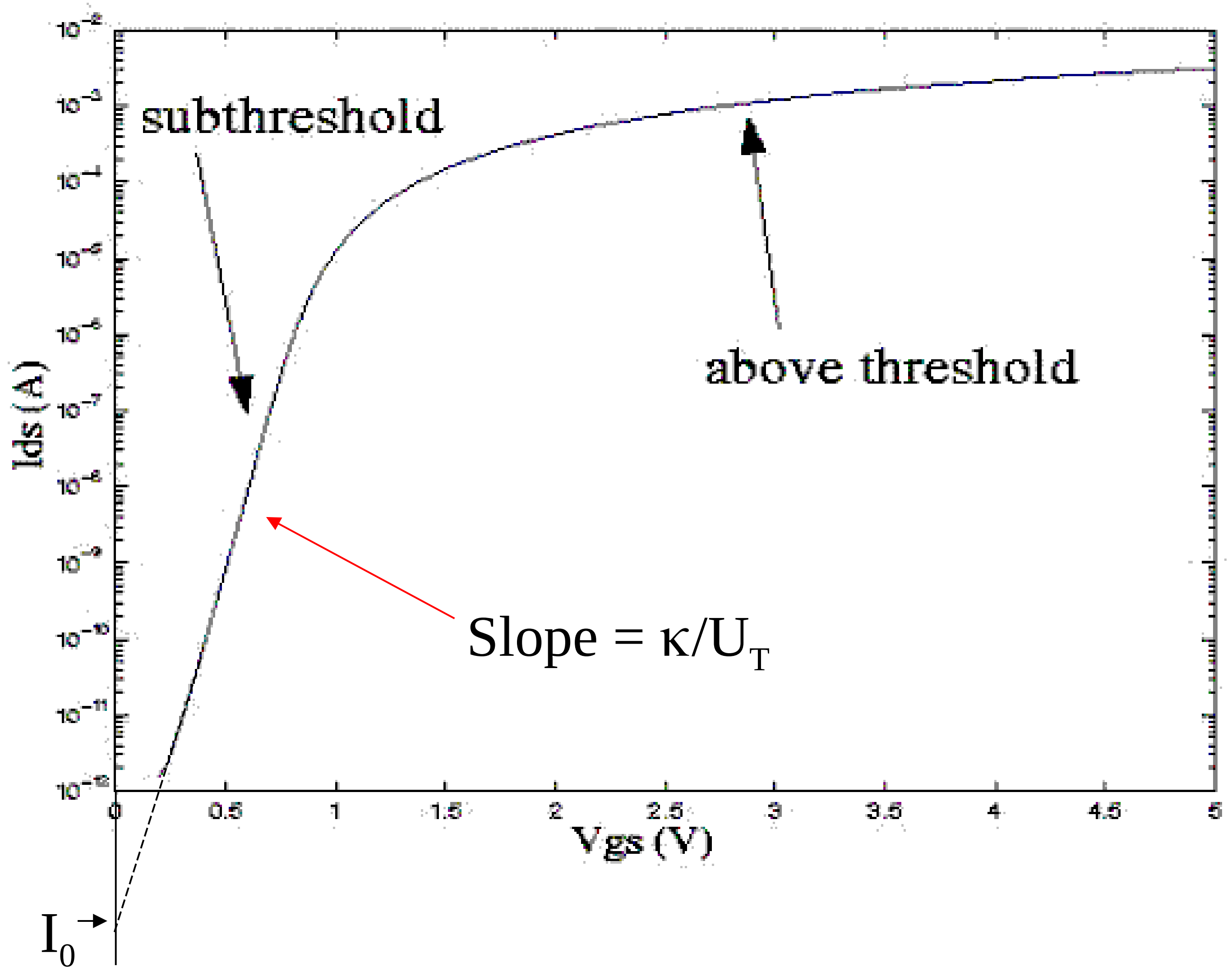
$$\boxed{\begin{aligned} I &= I_0 e^{\kappa V_g / U_T}\left(e^{-V_s/U_T} - e^{-V_d/U_T}\right) \\ &= I_f - I_r \end{aligned}}$$

$I_f =$ *forward current*

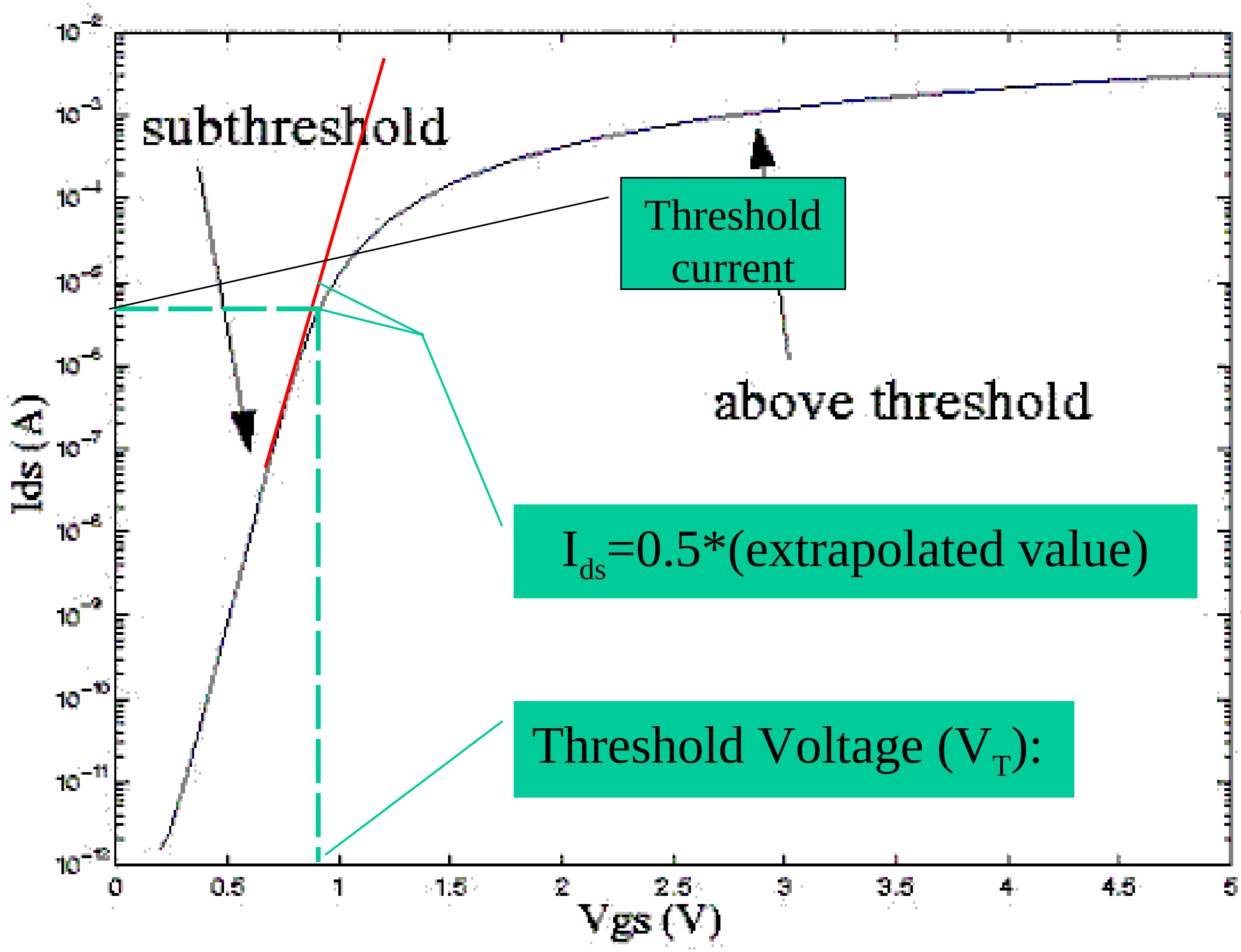
$I_r =$ *reverse current*

$$I_f = I_0 e^{\kappa V_g / U_T} e^{-V_s/U_T} \qquad I_r = I_0 e^{\kappa V_g / U_T} e^{-V_d/U_T}$$

nFET curve: I vs V_{gs}



nFet Threshold



Regimes of Subthreshold Operation (dependence on V_{ds})

Triode/Linear Region

$$\boxed{I = I_0 e^{(\kappa V_g - V_s)/U_T}\left(1 - e^{-(V_d - V_s)/U_T}\right)}$$

Saturation Region

$$\boxed{I = I_f = I_0 e^{(\kappa V_g - V_s)/U_T}}$$

nFET subthreshold Operation
V in units of U_T

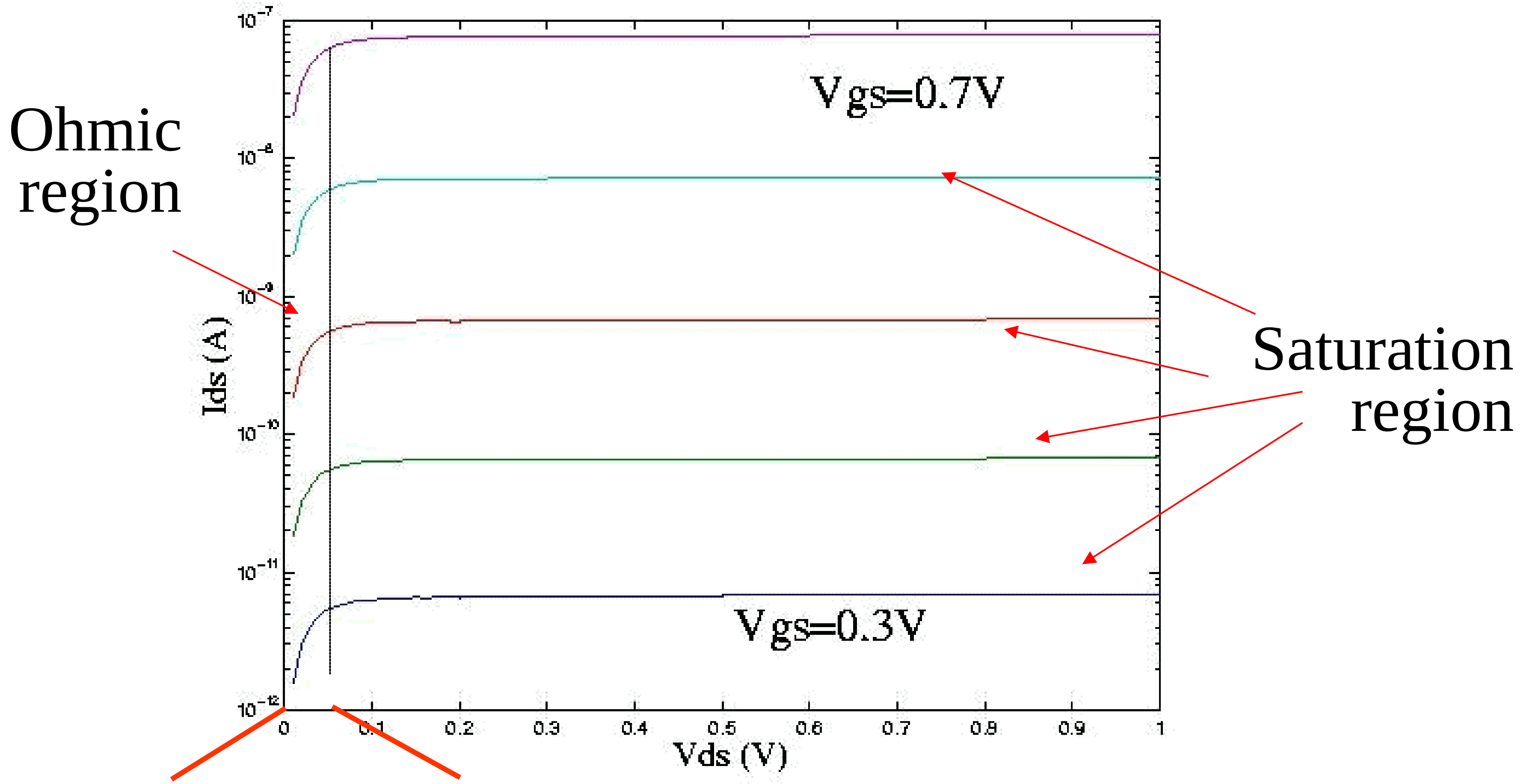
Triode/Linear Region

$$\boxed{I = I_0 e^{\kappa V_g - V_s}(1 - e^{-V_{ds}})}$$

Saturation Region, V_{ds}> a few U_T

$$\boxed{I = I_f = I_0 e^{\kappa V_g - V_s}}$$

nFET drain curve: I vs V_{ds}



$$\frac{4kT}{q} \approx 100\, mV$$

What about the pre-exponential I_0?

$$\boxed{I = I_f = I_0 e^{(\kappa V_g - V_s)/U_T}}$$

- I_0 comes from the built-in barrier and the doping concentrations. It takes the form

$$I_0 = N_s U_T^{\,2} \beta(T) \exp\left(\frac{-\kappa V_T}{U_T}\right)$$

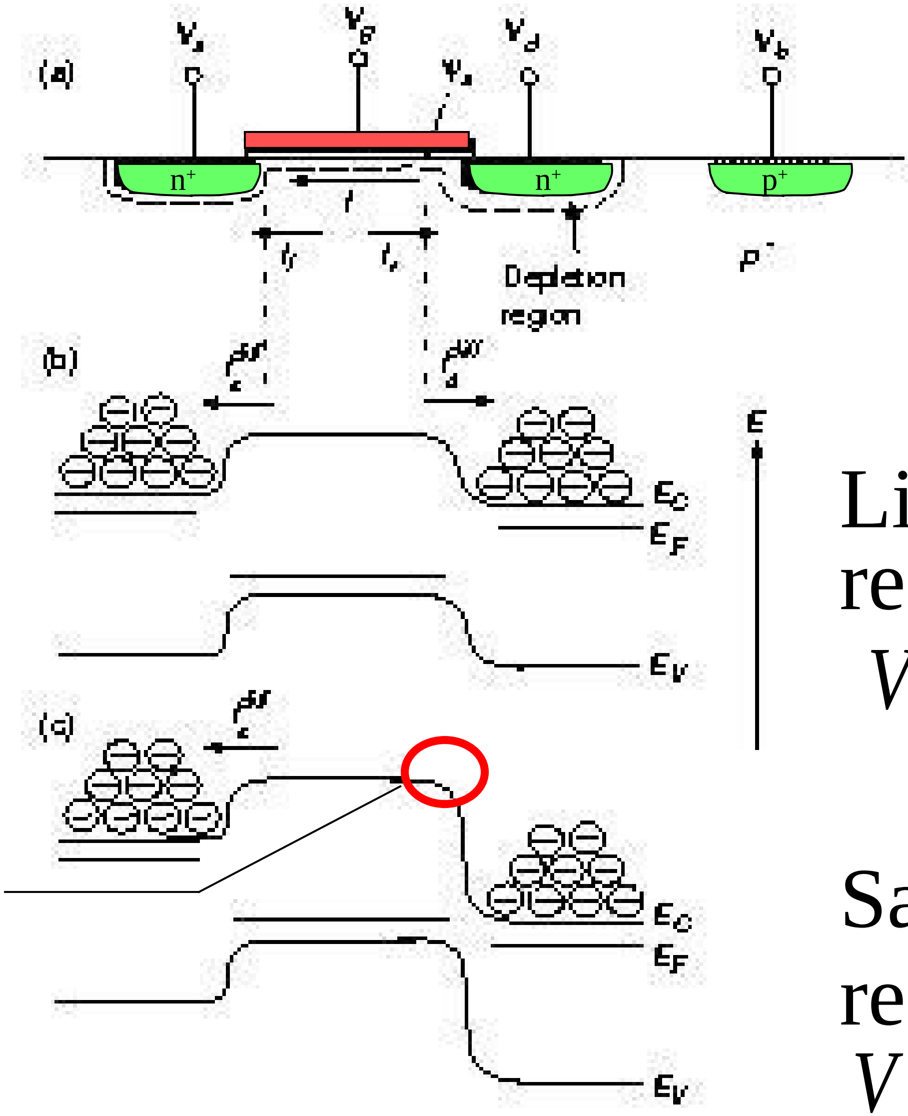
Dimensionless source concentration

$U_T\beta$: diffusivity

U_T : factor for density of states

Concentration at source reduced by barrier

Band Diagram for subthreshold nFET

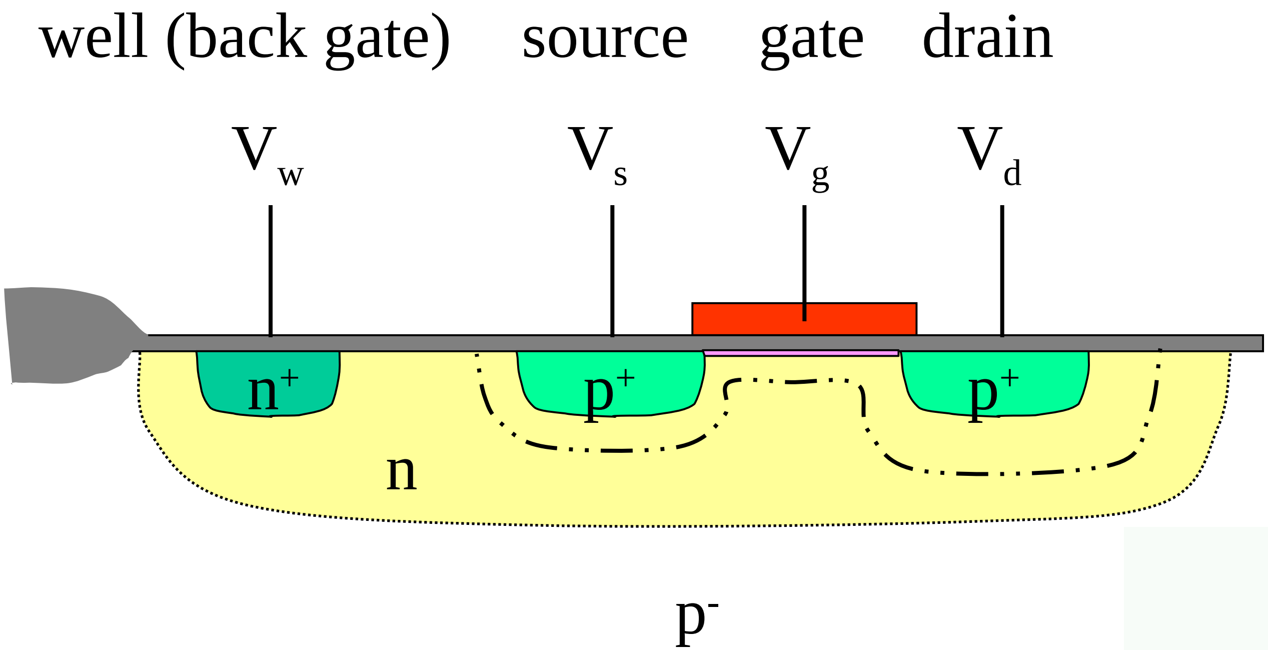


Linear regime
$V_{ds} < 100\,mV$

Saturation regime
$V_{ds} \geq 100\,mV$

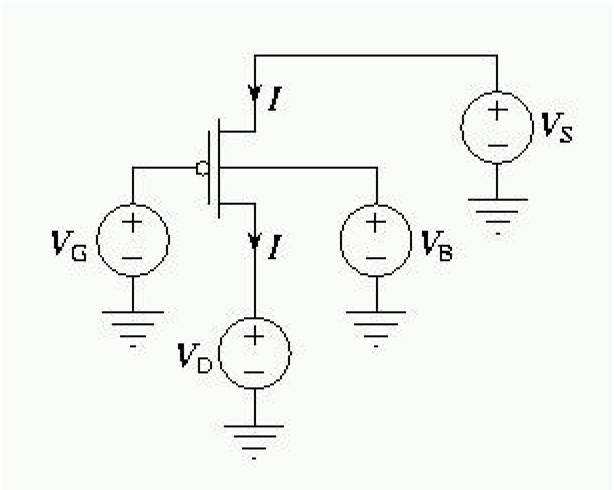
Drain density is zero

p-type MOSFET



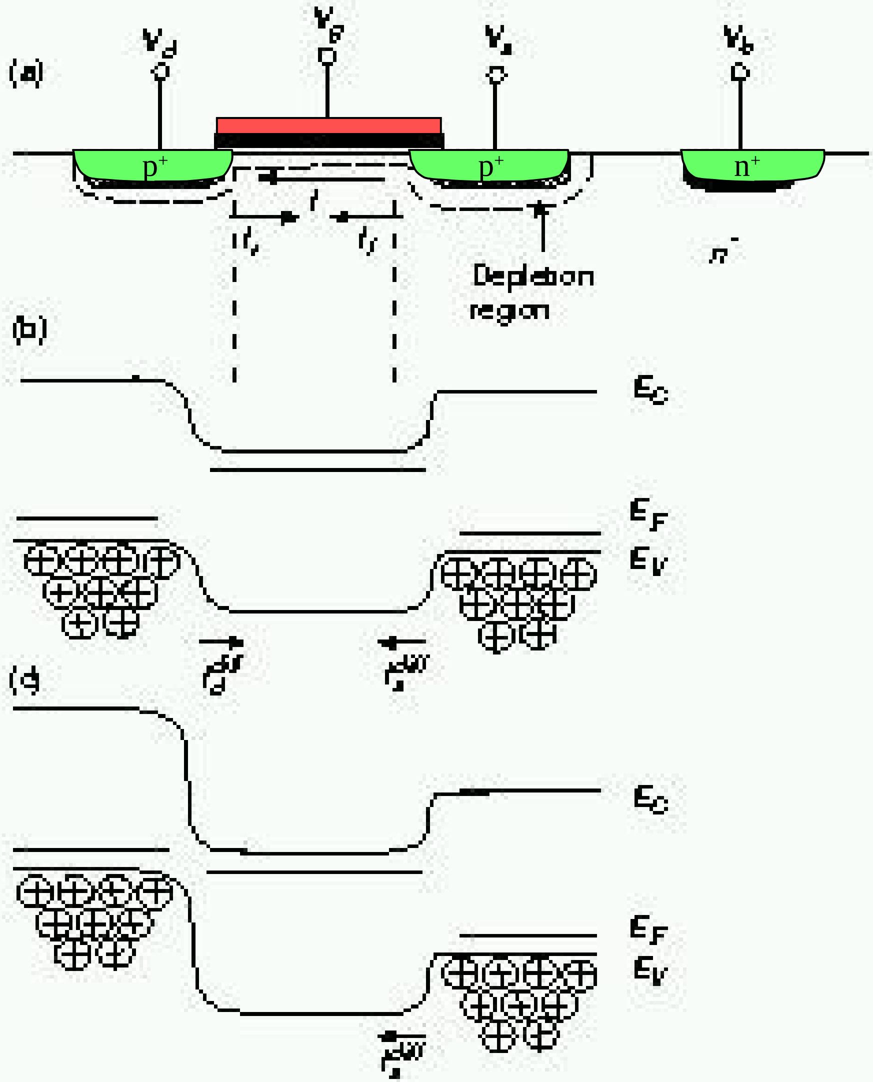
$$V_g, V_d, V_s \leq V_w$$

$$V_s \geq V_d$$



All voltages are referenced to $V_w = V_{dd}$

Band Diagram for subthreshold pFET



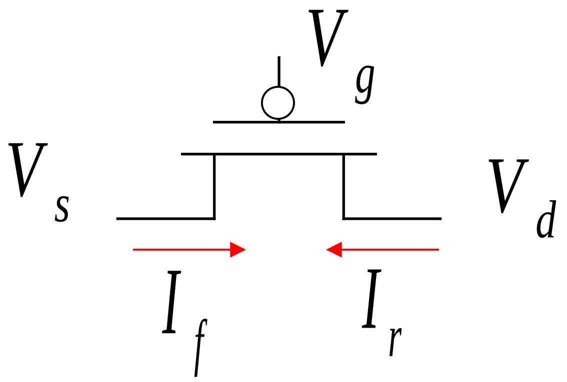
Linear regime

$V_{ds} < 100\,mV$

Saturation regime

$V_{ds} \geq 100\,mV$

Equations for Subthreshold pFET



$$\boxed{\begin{aligned} I &= I_0 e^{-\kappa V_g/U_T}\left(e^{V_s/U_T} - e^{V_d/U_T}\right) \\ &= I_f - I_r \end{aligned}}$$

$I_f =$ *forward current*

$I_r =$ *reverse current*

$$I_f = I_0 e^{-\kappa V_g/U_T} e^{V_s/U_T} \qquad I_r = I_0 e^{-\kappa V_g/U_T} e^{V_d/U_T}$$

pFET subthreshold Operation
V in units of U_T

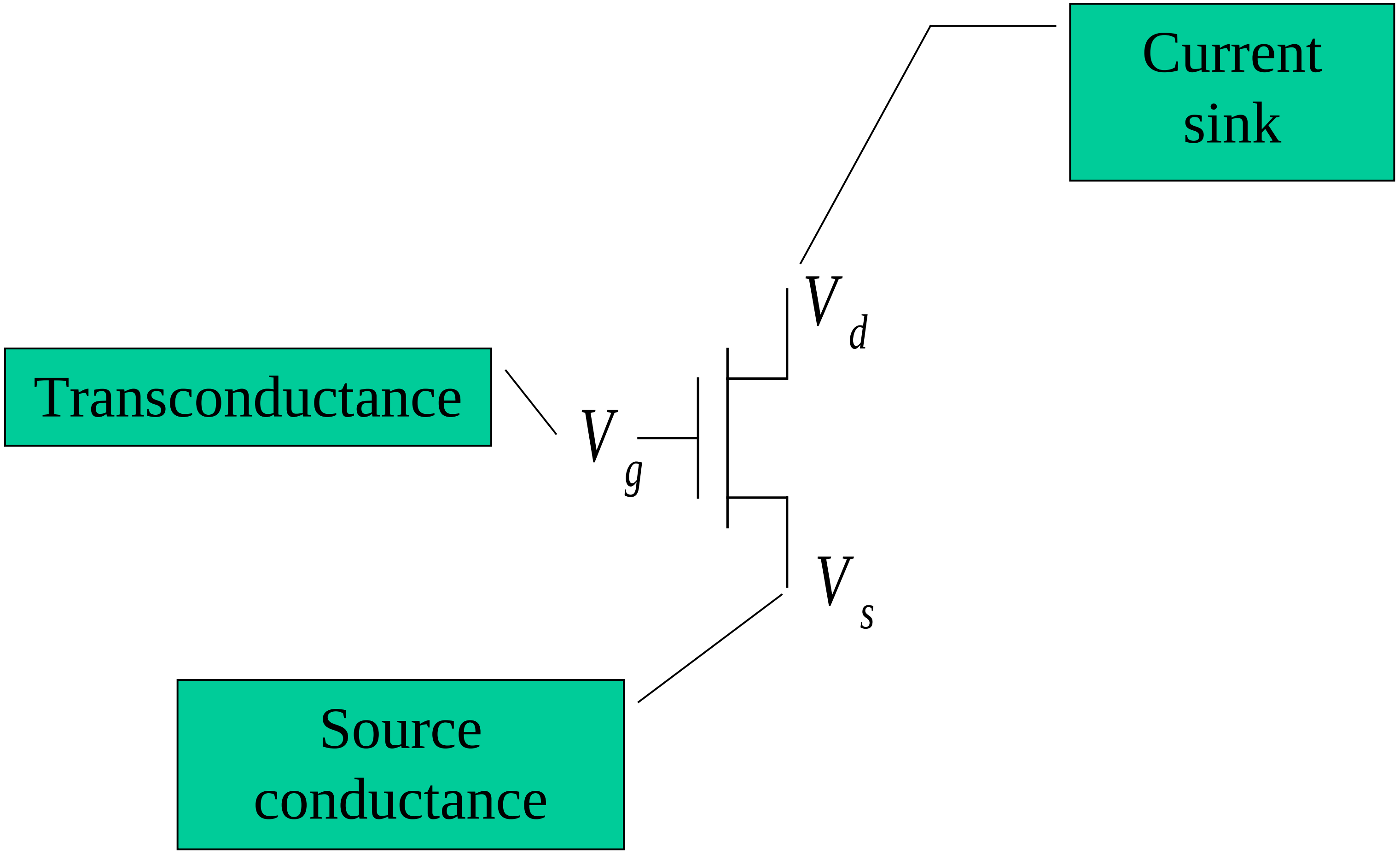
Triode/Linear Region

$$\boxed{I = I_0 e^{-\kappa V_g + V_s}(1 - e^{+V_{ds}})}$$

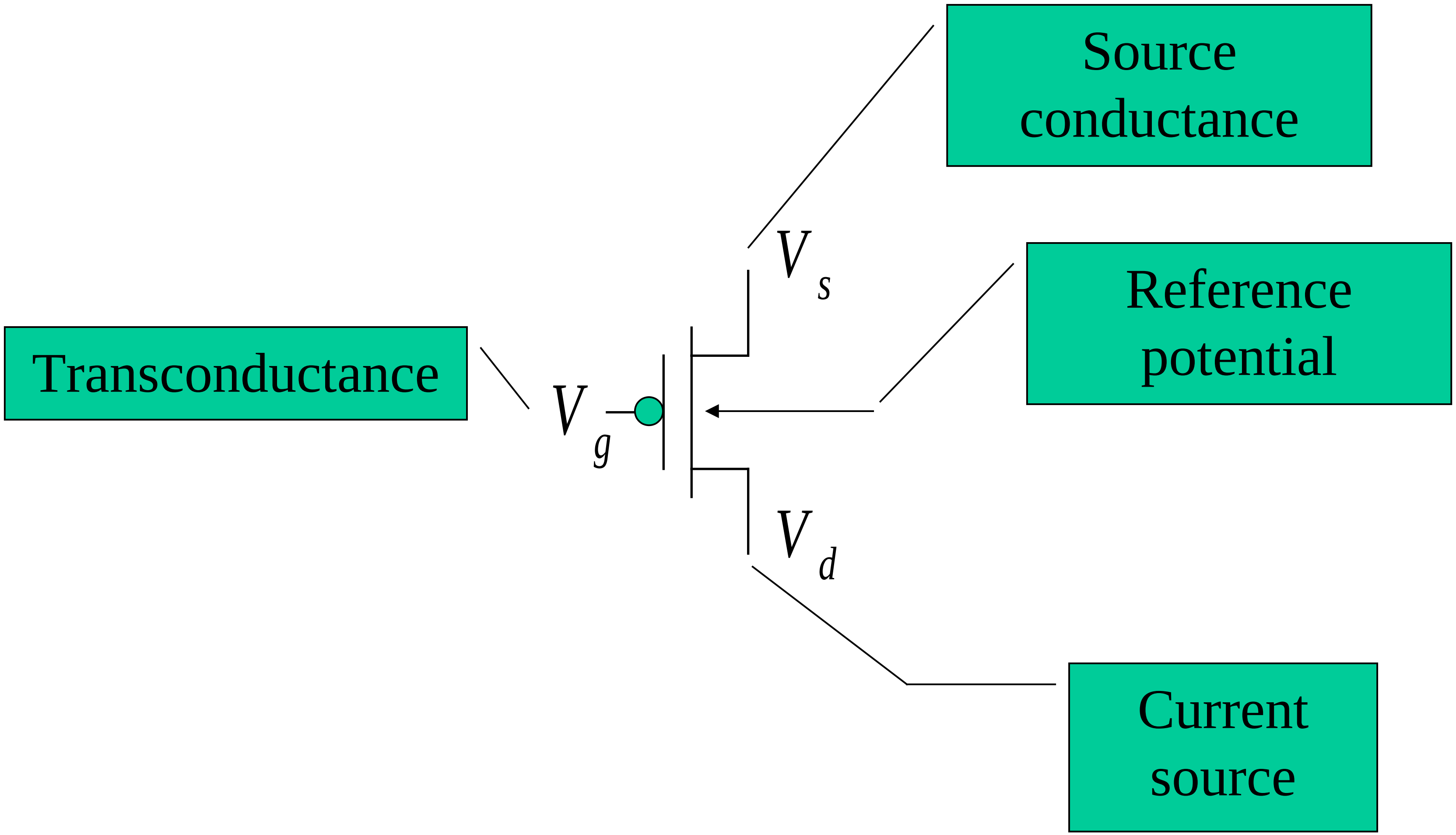
Saturation Region, V_{ds}> a few U_T

$$\boxed{I = I_f = I_0 e^{-\kappa V_g + V_s}}$$

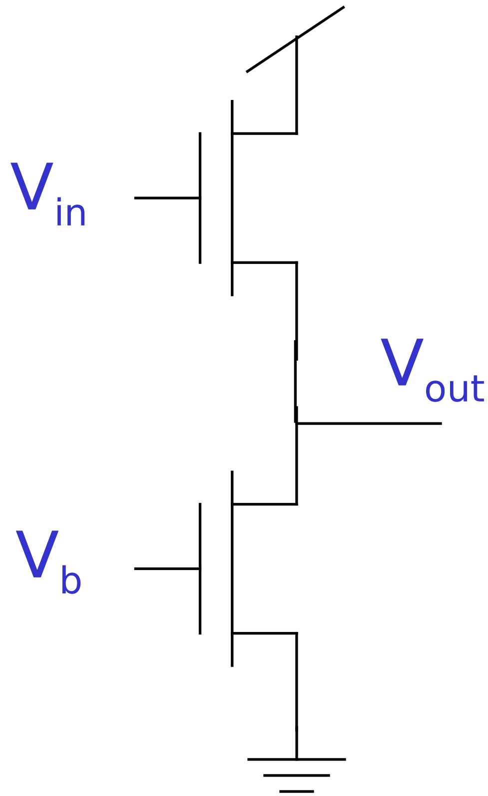
nFET functional behavior



pFET functional behavior



Circuit question



- What is V_{out} *vs.* V_{in}?
- Why is this circuit called a *source follower*?
- How can you use this circuit to measure kappa?

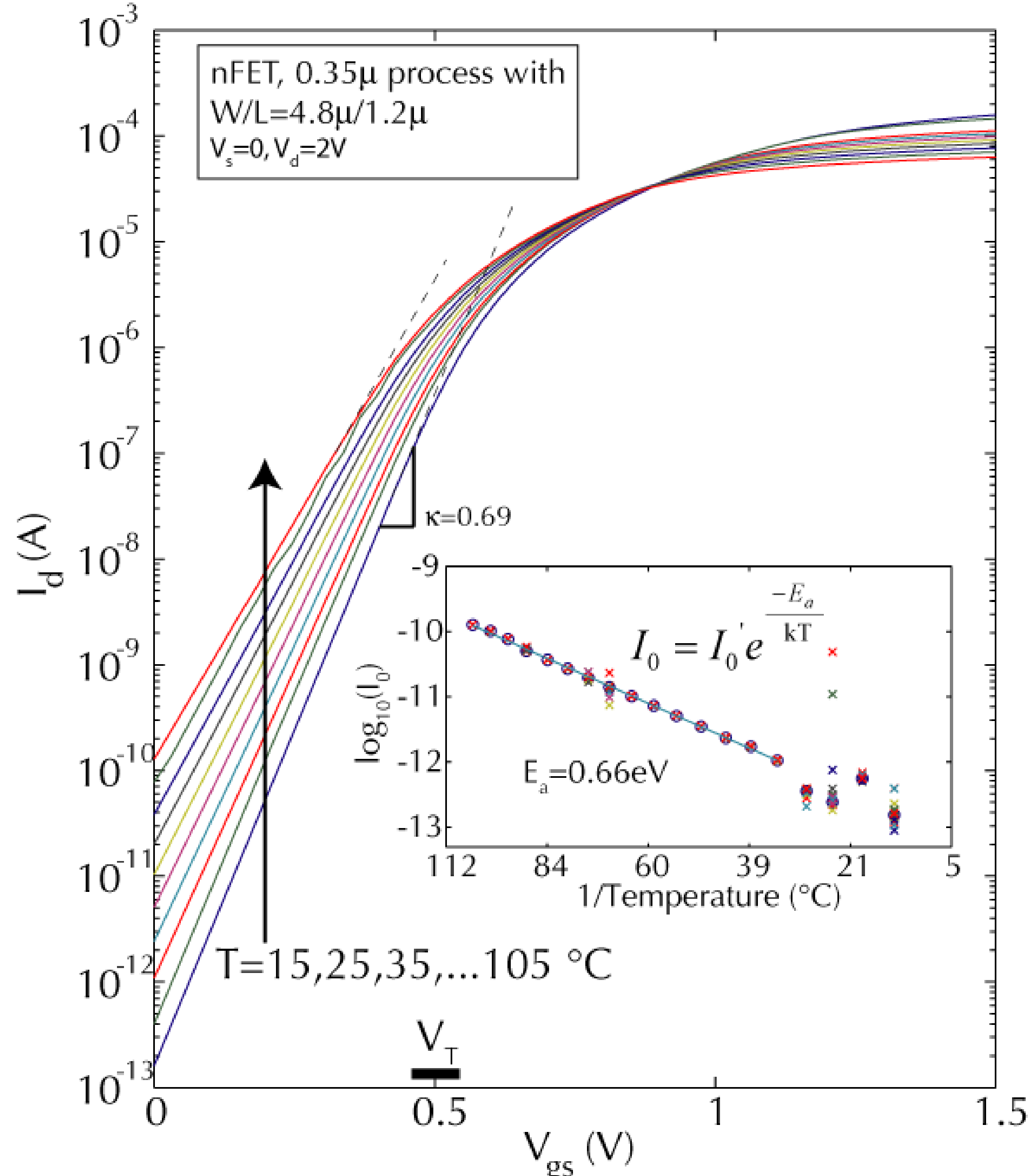
THE END

Next week:

What is the transistor threshold?

Above threshold operation.

Drain conductance-Early effect



nFET, 0.35μ process with
W/L=4.8μ/1.2μ
V_s=0, V_d=2V
κ=0.69
$I_0 = I_0' e^{\frac{-E_a}{kT}}$
E_a=0.66eV
log10(I0)
1/Temperature (°C)
T=15,25,35,...105 °C
V_T
I_d (A)
V_gs (V)