

# INSTITUTE OF NEUROINFORMATICS

CLASSCHIP 2018

IMPLEMENTATION OF 30 AVLSI TEST CIRCUITS FOR A  
NEUROMORPHIC CLASS CHIP

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**CoACH**

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*Author:*

Greg BURMAN

*Supervisor:*

Dr. Giacomo INDIVERI

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# 1 Introduction

This report documents the implementation of 30 test circuits that cover the contents of a neuromorphic engineering university class, spanning from single FET devices to AVLSI building blocks, to the DVS pixel and synapse and neuron models. A number of the more advanced circuits are drawn from research produced at INI.

These circuits form the core of a proposed  $2 \times 2\text{mm}$  test chip, designed for the AMS  $180\mu\text{m}$  process using the Cadence EDA programme. The peripheral circuitry for accessing and operating these core circuits is described in an adjacent report. Where possible, best efforts were made to ensure the implementation of the circuits conforms to good design practices, mostly in the form of managing the effects of mismatch, but also considering the effects of digital switching on analog circuitry, etc.

As the design of any circuit can take years to perfect and entire reports of their own to characterize, this report only intends to provide a sufficient description of the implementation of each. As such, details of circuit operation and design are not included.

## 2 Procedure

The implementation of each circuit and generation of its results in this report was done using the following process:

1. Circuit schematics were initially drawn using XCircuit. This was primarily done before generating schematics in Cadence to formalize signal names used, based on the naming convention described in the adjacent report. This also provided the opportunity to consider modifications required for certain circuits. EPS files of these XCircuit schematics are used in this report. Sizing annotations of FET & capacitor devices were added at a later stage.
2. Circuit schematics were then generated in Cadence based on the work done in XCircuit, as the basis for each cellview. Transistors and capacitors were initially assigned a standard/best-guess sizing, where not otherwise provided. Symbols of each circuit were then generated, with inputs on the left, outputs on the right, biases on top and control signals on the bottom.
3. Test benches were built as their own cellviews, based on schematics containing the circuit symbols, as well as required voltage/current sources for inputs/control signals, and diode-connected transistors for bias inputs. Simulation environments were then configured to test the operation of each circuit, first with a set of base settings, and then with variations in biases and other parameters.
4. Mismatch analyses were done using Monte Carlo simulations. For each analysis, 200 runs were performed. Where large mismatch was observed, transistor sizing was increased to mitigate the effects.
5. Layouts of each circuit were then drawn. DRC & LVS check were continuously run to ensure that the layouts both adhered to the design rules of the technology, as well as to ensure they matched the schematics exactly. Where necessary, dummy devices were added to further mitigate mismatch effects. Unless absolutely necessary, only metals 1 & 2 were used, reserving upper metal layers for routing of signals at a later stage.

### 3 Test Circuits

#### 3.1 N-FET Device

##### 3.1.1 Description

The N-FET is a single, large  $4\mu/4\mu$  n-type transistor providing access to all 3 device terminals. Both source and drain are IO signals, required for experiments that set either  $I_{ds}$  or  $V_{ds}$ , while measuring the other. However, the exposure of these terminals directly to pads without any protection structures means they are vulnerable to damage, which is why a device with larger dimensions is used. Circuit schematic is shown in Figure 1.

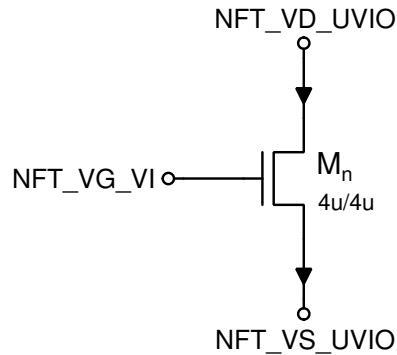


Figure 1: N-FET device schematic.

##### 3.1.2 Simulations

To test the N-FET circuit, a voltage source was connected to the gate terminal, while the drain and source terminals were tied to VDD and GND respectively. For the first simulation, measurements of  $I_{ds}$  were taken while sweeping  $V_g$ . For the second simulation, a constant current source was connected to the source terminal to set  $I_{ds}$  while sweeping  $V_g$  and measuring  $V_{ds}$ . Plots of both simulation outputs are shown in Figure 2. Values of  $I_{ds}$  had to be chosen logarithmically to produce linear shifts in  $V_{ds}$ .

##### 3.1.3 Mismatch Analysis

The simulation of  $I_{ds}$  measured against  $V_g$  was used for the mismatch analysis, as it displays a higher level of sensitivity to variation than the simulation measuring  $V_{ds}$ . The mismatch analysis is displayed in Figure 3.

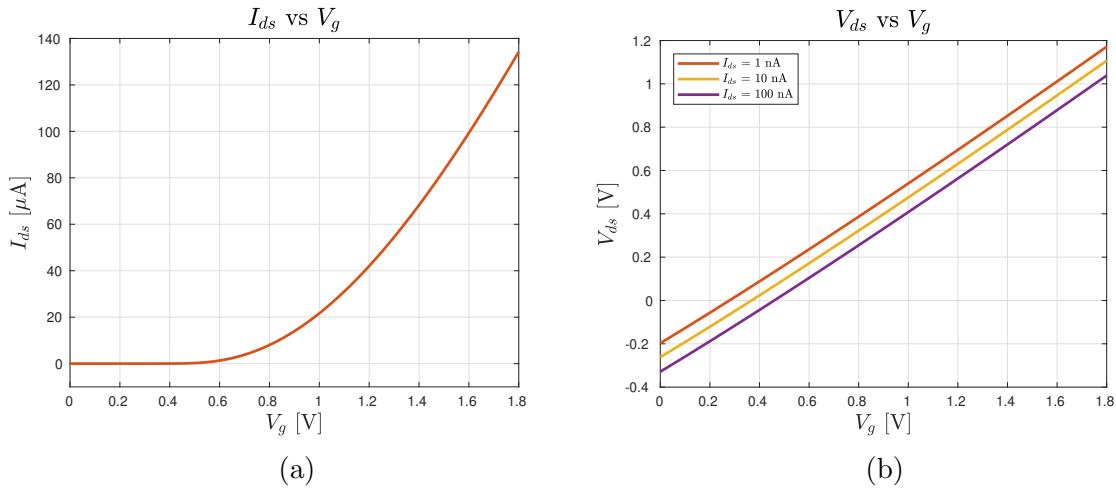


Figure 2: (a) measurements of  $I_{ds}$  while sweeping  $V_g$  (b) measurements of  $V_{ds}$  while sweeping  $V_g$ , for  $I_{ds}$  set as a constant current level.

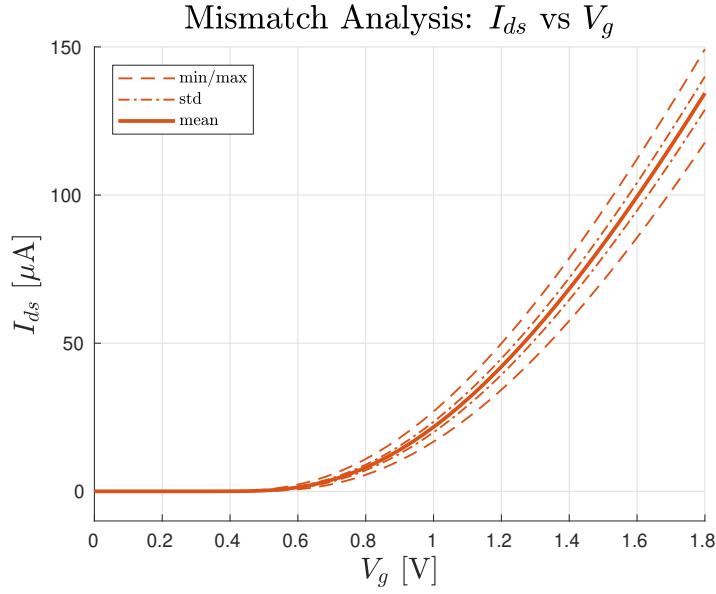


Figure 3: mismatch analysis of the N-FET circuit.

## 3.2 P-FET Device

### 3.2.1 Description

The P-FET is a single, large 4u/4u p-type transistor providing access to all 4 terminals (including the bulk). As with the N-FET, both source and drain are IO signals, allowing either  $I_{ds}$  or  $V_{ds}$  to be set while the other is measured. The bulk is made accessible as an input signal in addition to the gate. The direct exposure of drain and source to pads again requires a larger device geometry to be employed. Because the same W/L ratio as the N-FET is used, a lower conductance is expected, reflecting the lower carrier mobility of p-type devices. Circuit schematic is shown in Figure 4.

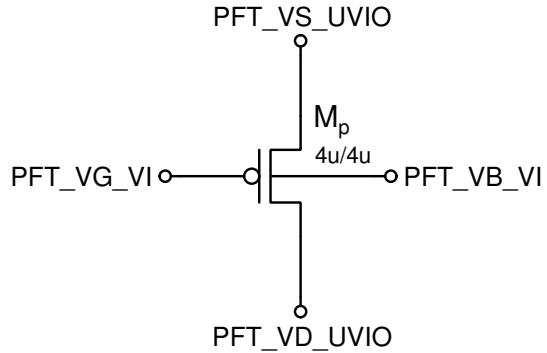


Figure 4: P-FET device schematic.

### 3.2.2 Simulations

To test the P-FET circuit, a voltage source was connected to the gate terminal, while the source and drain terminals were tied to VDD and GND respectively. The bulk terminal, also connected to a voltage source was initially set to VDD. For the first simulation, measurements of  $I_{ds}$  were taken while sweeping  $V_g$ . For the second simulation, a constant current source was connected to the source terminal to set  $I_{ds}$  while sweeping  $V_g$  and measuring  $V_{ds}$ . For the third simulation, with  $I_{ds} = 1nA$ ,  $V_b$  was set to various values while  $V_{ds}$  was measured. Simulation plots are shown in Figure 5.

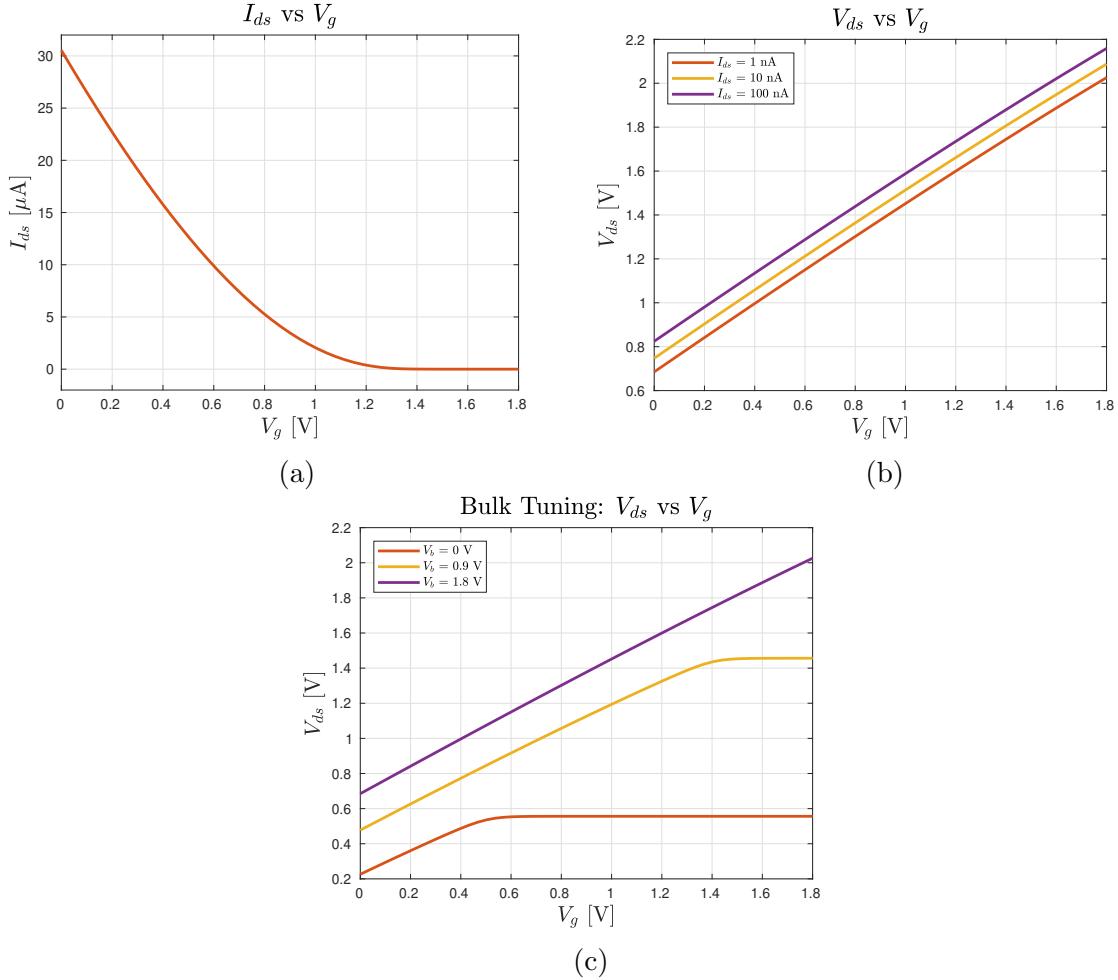


Figure 5: (a) measurements of  $I_{ds}$  while sweeping  $V_g$  (b) measurements of  $V_{ds}$  while sweeping  $V_g$ , for set  $I_{ds}$  values. (c) measurement of  $V_{ds}$  while varying  $V_b$ .

### 3.2.3 Mismatch Analysis

The simulation of  $I_{ds}$  measured against  $V_g$  was used for the mismatch analysis, as it displays a higher level of sensitivity to variation than the simulation measuring  $V_{ds}$ . Of the full mismatch data captured, the min, max, mean and standard-deviation was captured, as displayed in Figure 6.

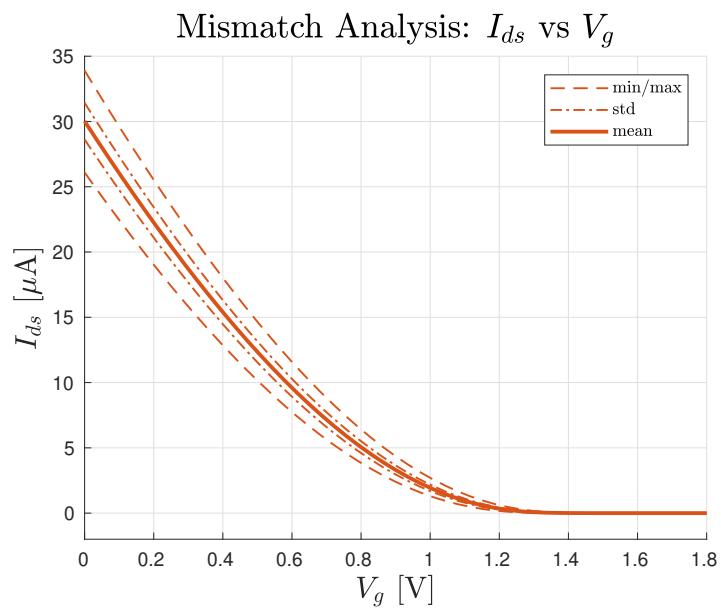


Figure 6: mismatch analysis of the P-FET circuit.

### 3.3 N-FET Array

#### 3.3.1 Description

The N-FET array comprises 16 N-FET devices, with lengths ranging over  $n \times 0.18\mu m$  to  $2.88\mu m$ , where  $n$  is the device number. There are a further two dummy elements on either side of the array, to account for mismatch corner-effects. The cells share a common gate voltage,  $V_g$ , with currents  $I_{ds(n)}$  read out at the drain so as not to affect  $V_{gs(n)}$ . The circuit schematic is shown in Figure 7.

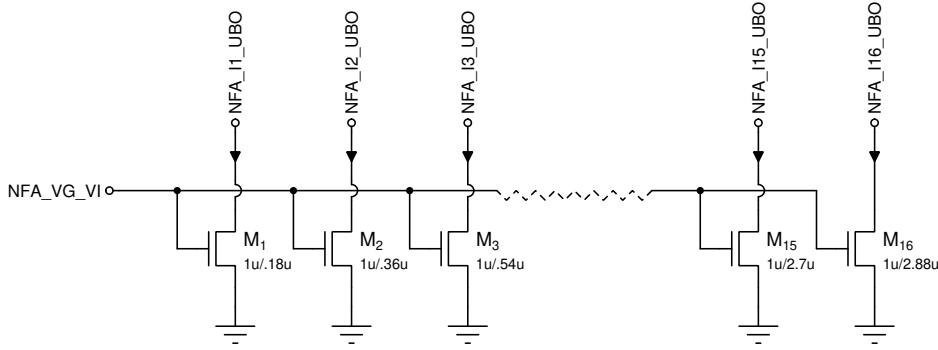


Figure 7: N-FET array schematic.

#### 3.3.2 Simulations

$V_g$  is swept from GND to VDD, with all output currents  $I_{ds(n)}$  read simultaneously. The difference between the output currents decreases as devices lengths are increased. Simulation plots are shown in Figure 8.

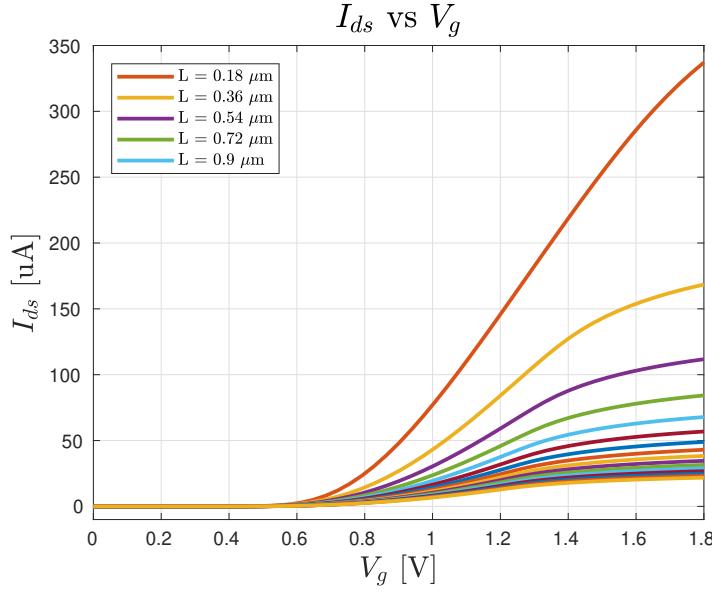


Figure 8: measurements of  $I_{ds}$  for all 16 N-FET devices while sweeping a common input  $V_g$ .

### 3.3.3 Mismatch Analysis

Only devices  $M_1$ ,  $M_4$  and  $M_{16}$  were observed for the mismatch analysis, as these represent the best, worst and average cases. As seen in Figure 9, the smallest device is most susceptible to mismatch effects, while the largest device is far less varied in its response.

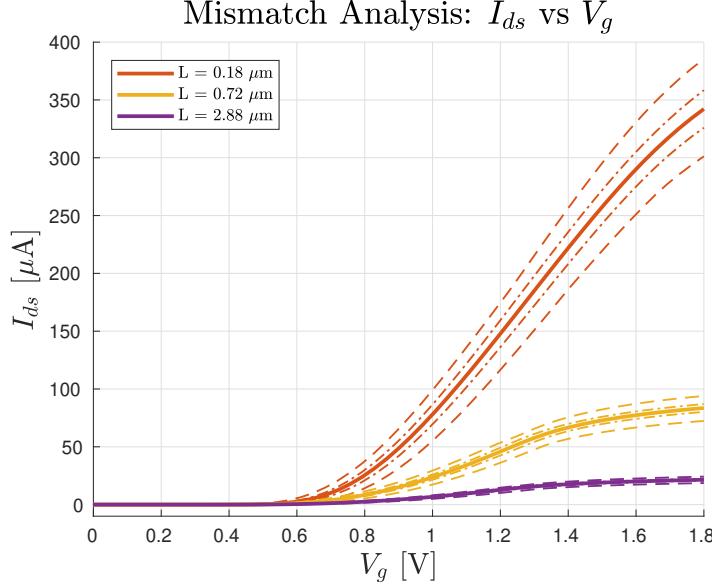


Figure 9: mismatch analysis of the N-FET array circuit.

## 3.4 P-FET Array

### 3.4.1 Description

The P-FET array comprises 16 P-FET devices, with lengths ranging over  $n \times 0.18\mu m$  to  $2.88\mu m$ , where  $n$  is the device number. There are a further two dummy elements on either side of the array, to account for mismatch corner-effects. The cells share a common gate voltage,  $V_g$ , with currents  $I_{ds(n)}$  read out at the drain so as not to affect  $V_{gs(n)}$ . Unlike the P-FET device, there is no bulk input to the devices used in this circuit. The circuit schematic is shown in Figure 10.

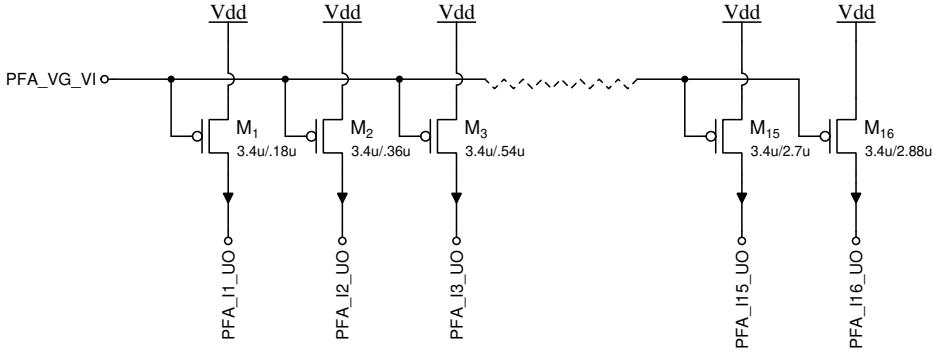


Figure 10: P-FET array schematic.

### 3.4.2 Simulations

As with the N-FET array,  $V_g$  is swept from GND to VDD, with all output currents  $I_{ds(n)}$  read simultaneously. The response is inverse to that observed with the N-FET array, as expected, and conductances are roughly the same, if a little lower. The difference between the output currents decreases as devices lengths are increased. Simulation plots are shown in Figure 11.

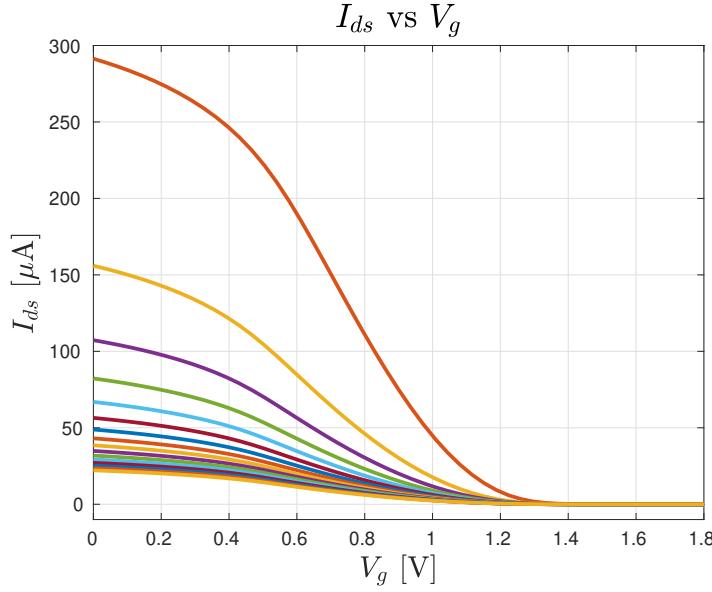


Figure 11: measurements of  $I_{ds}$  for all 16 P-FET devices while sweeping a common input  $V_g$ .

### 3.4.3 Mismatch Analysis

Again, only devices  $M_1$ ,  $M_4$  and  $M_{16}$  were observed for the mismatch analysis, as these represent the best, worst and average cases. As with the N-FET array, and seen in Figure 12, the smallest device is most susceptible to mismatch effects, while the largest device is far less varied in its response.

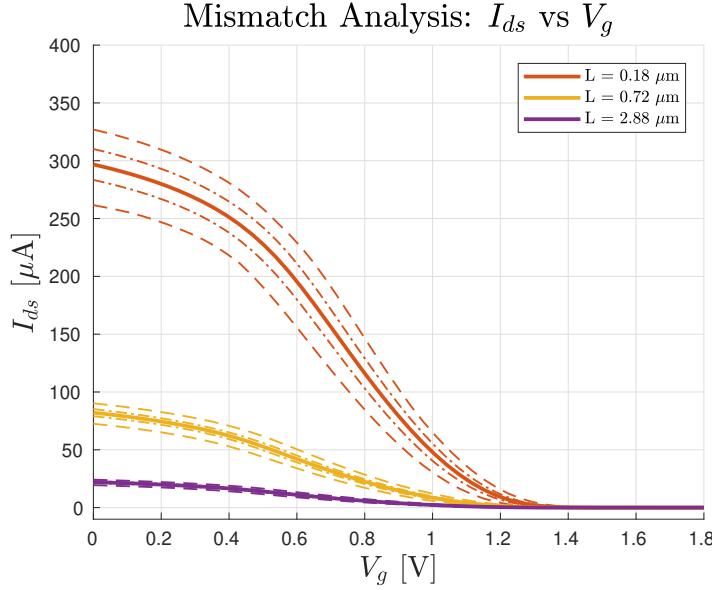


Figure 12: mismatch analysis of the P-FET array circuit.

## 3.5 N-Type Source-Follower

### 3.5.1 Description

The N-type source-follower provides an output voltage  $V_{out}$  that "follows" a given input voltage  $V_{in}$ . The degree to which  $V_{out}$  matches  $V_{in}$  is modulated by the input to the bias device. The circuit schematic is shown in Figure 13.

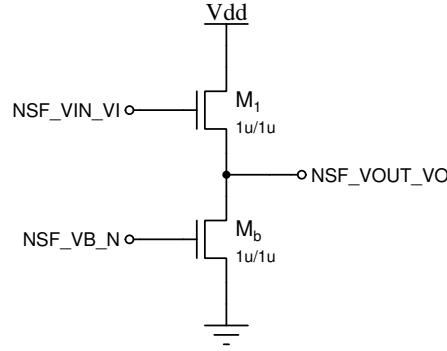


Figure 13: N-Type source-follower schematic.

### 3.5.2 Simulations

For the first simulation,  $V_{in}$  is swept from GND to VDD, with the input bias set to  $I_b = 1\text{nA}$ , while observing  $V_{out}$ . In the second simulation, this measurement is made for different values of  $I_b$ . Logarithmic changes in  $I_b$  result in linear changes in  $V_{out}$ . Simulation plots are shown in Figure 14.

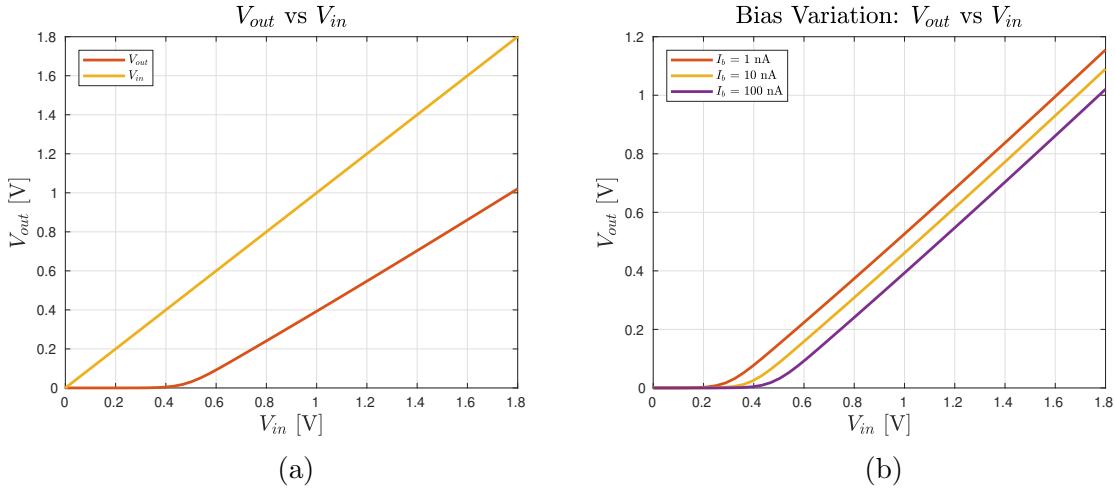


Figure 14: (a) measurements of  $V_{out}$  while sweeping  $V_{in}$  (b) measurements of  $V_{out}$  while sweeping  $V_g$ , for variations of  $I_b$

### 3.5.3 Mismatch Analysis

A Mismatch analysis was done using the first simulation setup. As observed in Figure 15, the circuit is minimally affected by mismatch.

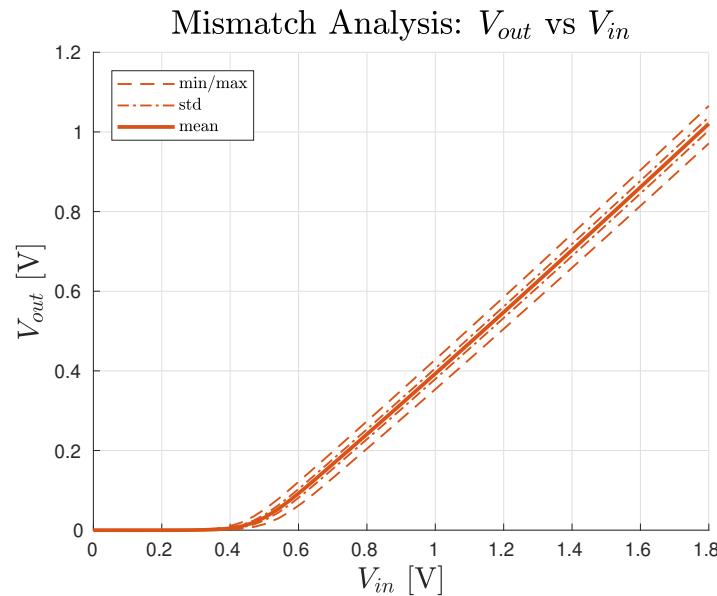


Figure 15: mismatch analysis of the N-type source-follower circuit.

## 3.6 P-Type Source Follower

### 3.6.1 Description

The P-type source-follower provides an output voltage  $V_{out}$  that "follows" a given input voltage  $V_{in}$ . The bulk of the input device is tied to the output node. The degree to which  $V_{out}$  matches  $V_{in}$  is modulated by the input to the bias device. The circuit schematic is shown in Figure 16.

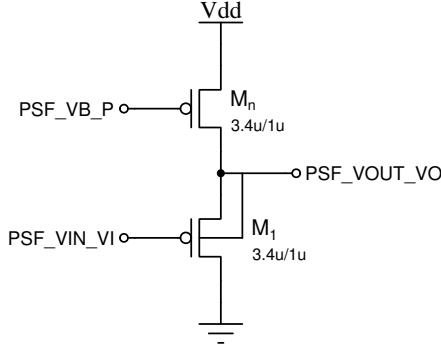


Figure 16: P-Type source-follower schematic.

### 3.6.2 Simulations

For the first simulation,  $V_{in}$  is swept from GND to VDD, with the input bias set to  $I_b = 1\text{nA}$ , while observing  $V_{out}$ . In the second simulation, this measurement is made for different values of  $I_b$ . Logarithmic changes in  $I_b$  result in linear changes in  $V_{out}$ . Simulation plots are shown in Figure 17.

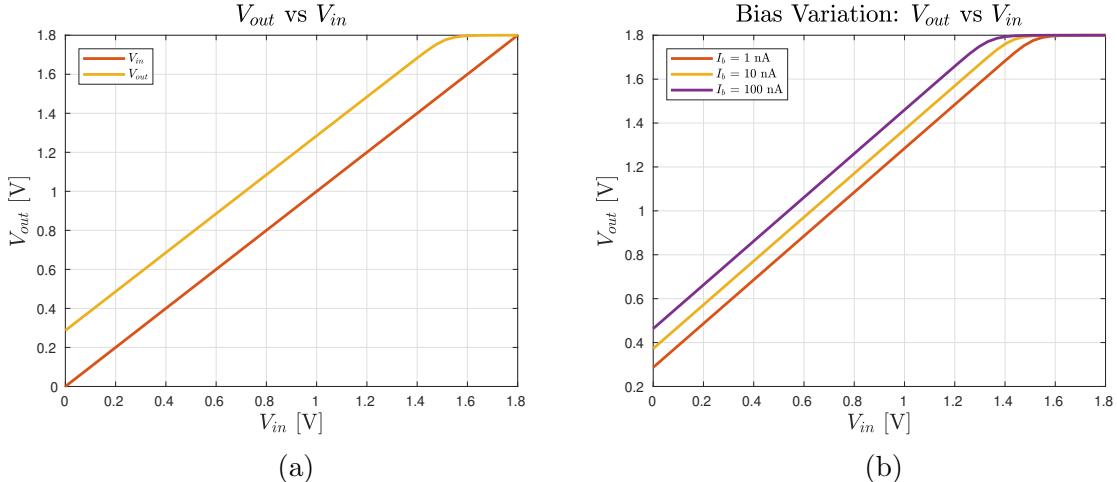


Figure 17: (a) measurements of  $V_{out}$  while sweeping  $V_{in}$  (b) measurements of  $V_{out}$  while sweeping  $V_g$ , for variations of  $I_b$

### 3.6.3 Mismatch Analysis

A Mismatch analysis was done using the first simulation setup. As observed in Figure 18, the circuit is minimally affected by mismatch.

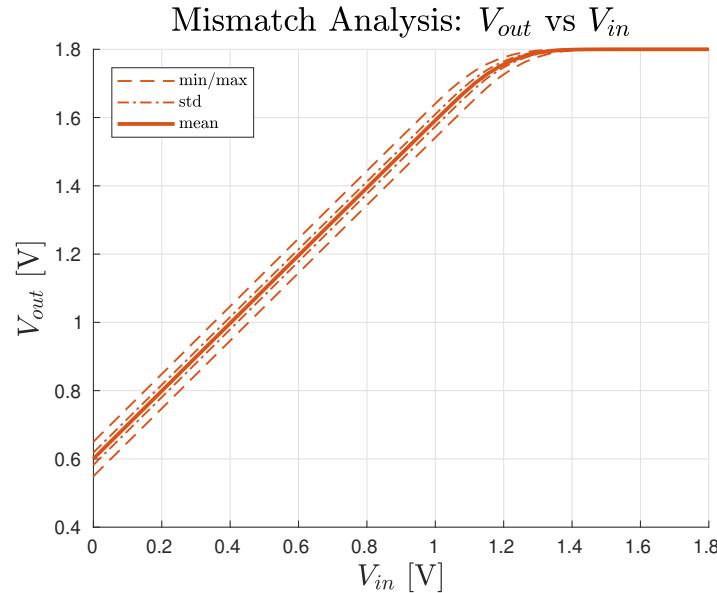


Figure 18: mismatch analysis of the P-type source-follower circuit.

## 3.7 N-Type Differential Pair

### 3.7.1 Description

The N-type differential pair takes in two input voltages,  $V_1$  &  $V_2$ , and outputs currents  $I_1$  &  $I_2$  that correspond to the difference between them. The amount of current available to be "shared" between the two branches is modulated by the bias  $I_b$ . The circuit schematic is shown in Figure 19.

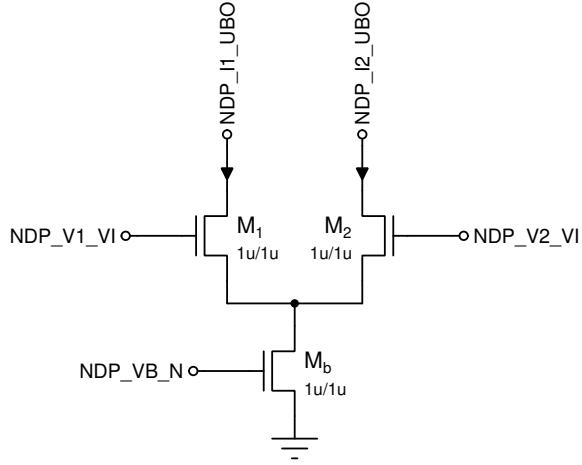


Figure 19: N-Type differential-pair schematic.

### 3.7.2 Simulations

For all simulations, the inputs are tied as a common differential input,  $V_{diff}$ , with a common-mode voltage  $V_{cm} = 0.9V$ . In the first simulation,  $I_1$  &  $I_2$  are observed over an input sweep  $-0.3V < V_{diff} < 0.3V$ , with  $I_b = 1nA$ . In the second simulation,  $I_b$  is set to different levels. In the third simulation  $V_{cm}$  is modulated, showing the sensitivity of this circuit to the input common-mode. Simulation plots are shown in Figure 20.

$V_{diff}$  is a single differential input voltage, that connects to both circuit inputs (typically this is implemented by using a resistor-divider pair).  $V_{cm}$  is a common-mode voltage, which sets the base input level over which  $V_{diff}$  modulates the two inputs it is tied to. This base voltage level is necessary to ensure that the bias transistor in the circuit common branch is fully turned on.

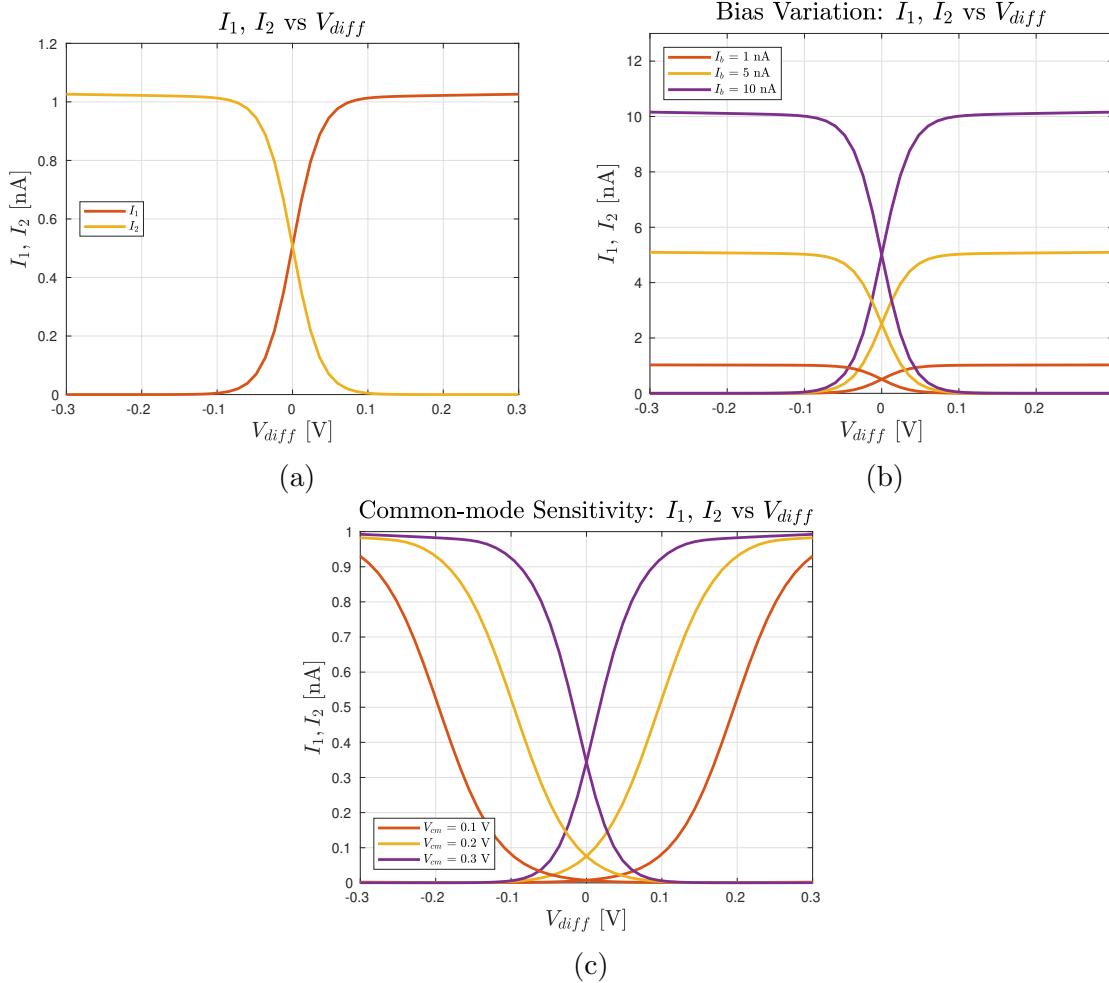


Figure 20: (a) measurements of  $I_1$ ,  $I_2$  while sweeping  $V_{diff}$  (b) variation of bias parameter  $I_b$  (c) variation of the input common-mode,  $V_{cm}$ .

### 3.7.3 Mismatch Analysis

A mismatch analysis was done using the first simulation setup. As observed in Figure 21, the amplitude of the output currents is mostly affected, with a small offset in the crossing between the two plots introduced as a result.

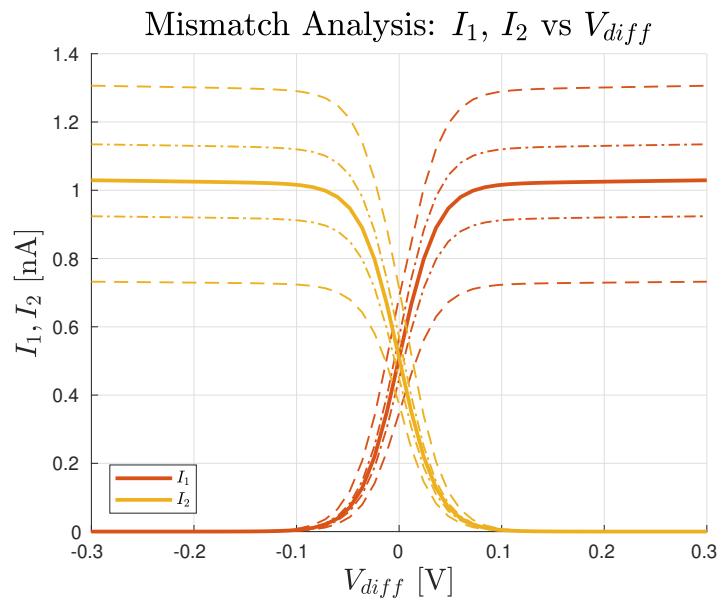


Figure 21: mismatch analysis of the N-type differential pair circuit.

## 3.8 P-Type Differential Pair

### 3.8.1 Description

The P-type differential pair takes in two input voltages,  $V_1$  &  $V_2$ , and outputs currents  $I_1$  &  $I_2$  that correspond to the difference between them. The amount of current available to be "shared" between the two branches is modulated by the bias  $I_b$ . The circuit schematic is shown in Figure 22.

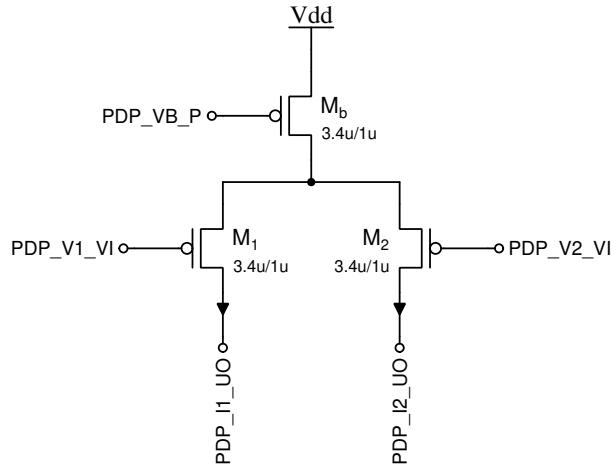


Figure 22: P-Type differential-pair schematic.

### 3.8.2 Simulations

For all simulations, the inputs are tied as a common differential input,  $V_{diff}$ , with a common-mode voltage  $V_{cm} = 0.9V$ . In the first simulation,  $I_1$  &  $I_2$  are observed over an input sweep  $-0.3V < V_{diff} < 0.3V$ , with  $I_b = 1nA$ . In the second simulation,  $I_b$  is set to different levels. In the third simulation  $V_{cm}$  is modulated, showing the sensitivity of this circuit to the input common-mode. Simulation plots are shown in Figure 23.

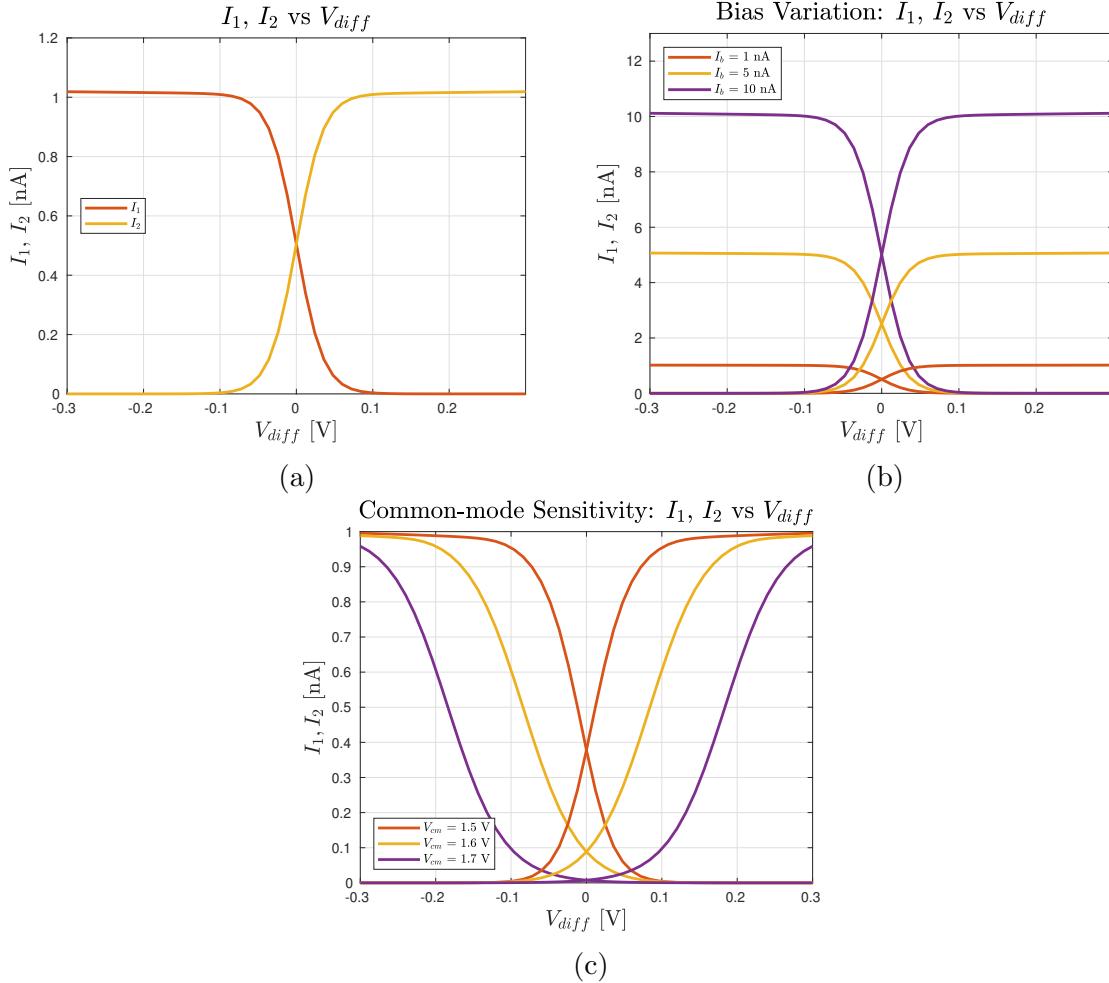


Figure 23: (a) measurements of  $I_1$ ,  $I_2$  while sweeping  $V_{diff}$  (b) variation of bias parameter  $I_b$  (c) variation of the input common-mode,  $V_{cm}$ .

### 3.8.3 Mismatch Analysis

A mismatch analysis was done using the first simulation setup. As with the N-type circuit, and as observed in Figure 24, the amplitude of the output currents is mostly affected, with a small offset in the crossing between the two plots introduced as a result. Less mismatch is observed than in the N-type circuit, resulting from larger FET devices being used.

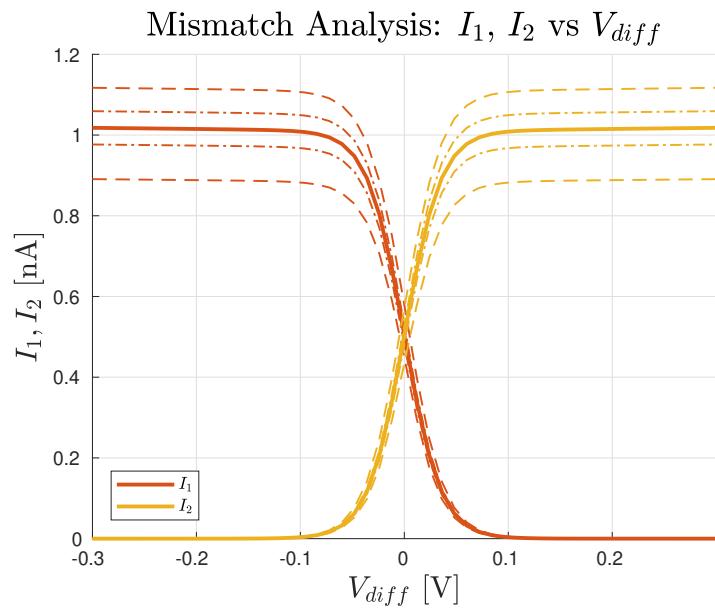


Figure 24: mismatch analysis of the P-type differential pair circuit.

## 3.9 Current Correlator

### 3.9.1 Description

The current correlator receives two input currents  $I_1$  &  $I_2$  and provides an output current  $I_{out}$  that is maximized when these inputs are the same. The circuit schematic is shown in Figure 25.

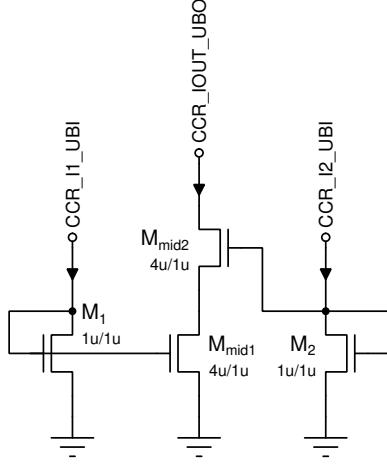


Figure 25: Current Correlator schematic.

### 3.9.2 Simulations

A common differential input current,  $I_{diff}$ , is used for both simulations. To keep the inputs positive, a positive offset  $c = 100nA$  is added to it. In the first simulation,  $I_{out}$  is observed while sweeping the input over the range  $0nA < I_{diff} < 100nA$ . In the second simulation, the S-ratio of the circuit is modulated by changing the widths of the inner devices, resulting in a corresponding change in circuit gain. Simulation plots are shown in Figure 26.

### 3.9.3 Mismatch Analysis

A mismatch analysis was done using the first simulation setup. While there is a big difference in gain between min and max observations, most of the resulting variation resides within a relatively tight band, as shown by the std and observed in Figure 27.

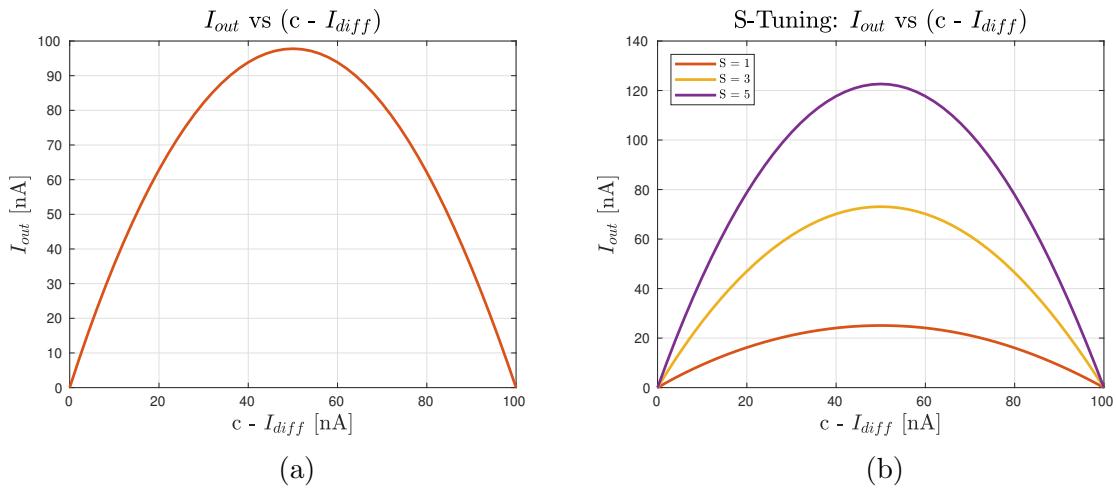


Figure 26: (a) measurements of  $I_{out}$  while sweeping  $I_{in}$  (b) tuning of the S-ratio. Offset  $c$  is set to  $100\text{nA}$ .

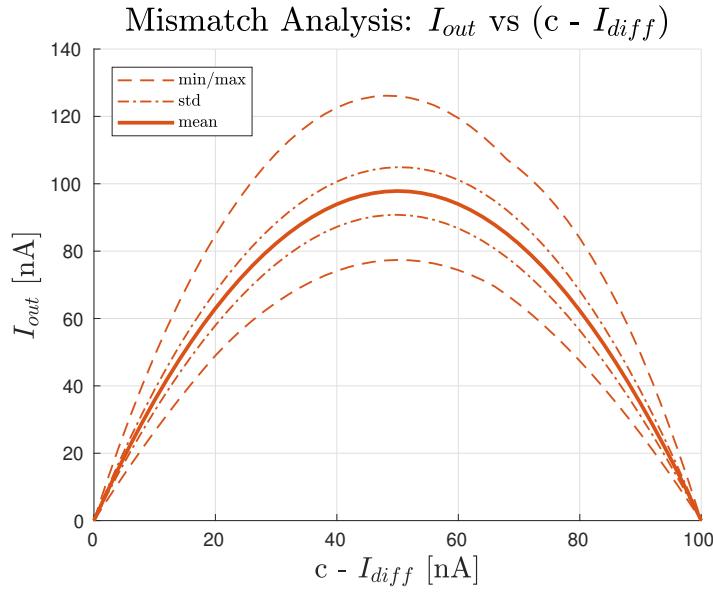


Figure 27: mismatch analysis of the current correlator circuit.

## 3.10 Bump Antibump

### 3.10.1 Description

The bump antibump circuit is an extension of the differential pair: it takes in two input voltages  $V_1$  &  $V_2$  and two currents,  $I_1$  &  $I_2$  that correspond to the difference between them. It also outputs a third current,  $I_{mid}$  that, (similar to the current correlator) is maximized when the two inputs are the same. The amount of current shared between the branches is modulated by the input bias  $I_b$ . The circuit schematic is shown in Figure 28.

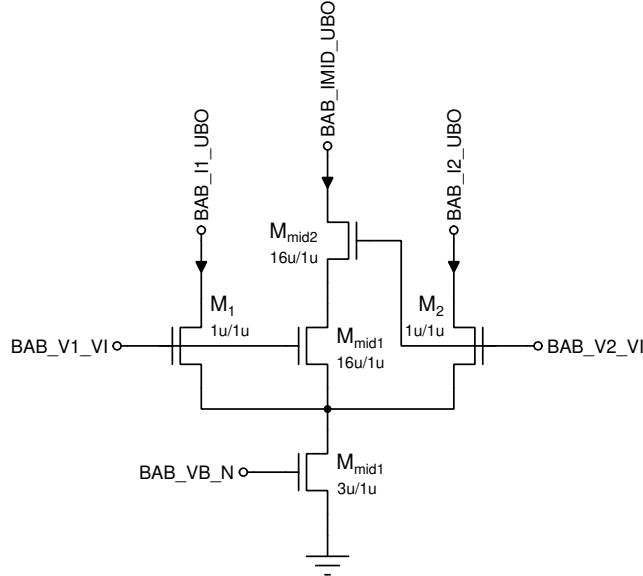


Figure 28: Bump Antibump schematic.

### 3.10.2 Simulations

The bump antibump uses the same simulation setup as the differential pair, sweeping a differential input voltage over the range  $-0.3V < V_{diff} < 0.3V$ , with  $I_b = 1nA$ , and a common mode  $V_{cm} = 1V$ . In the first simulation,  $I_1 + I_2$  and  $I_1 + I_2 + I_{mid}$  are additionally calculated, showing both the "antibump" and the "ceiling". In the second simulation, this sweep is taken for different values of  $I_b$ , while the third simulation observes modulation of the S-ratio. Simulation plots are shown in Figure 29.

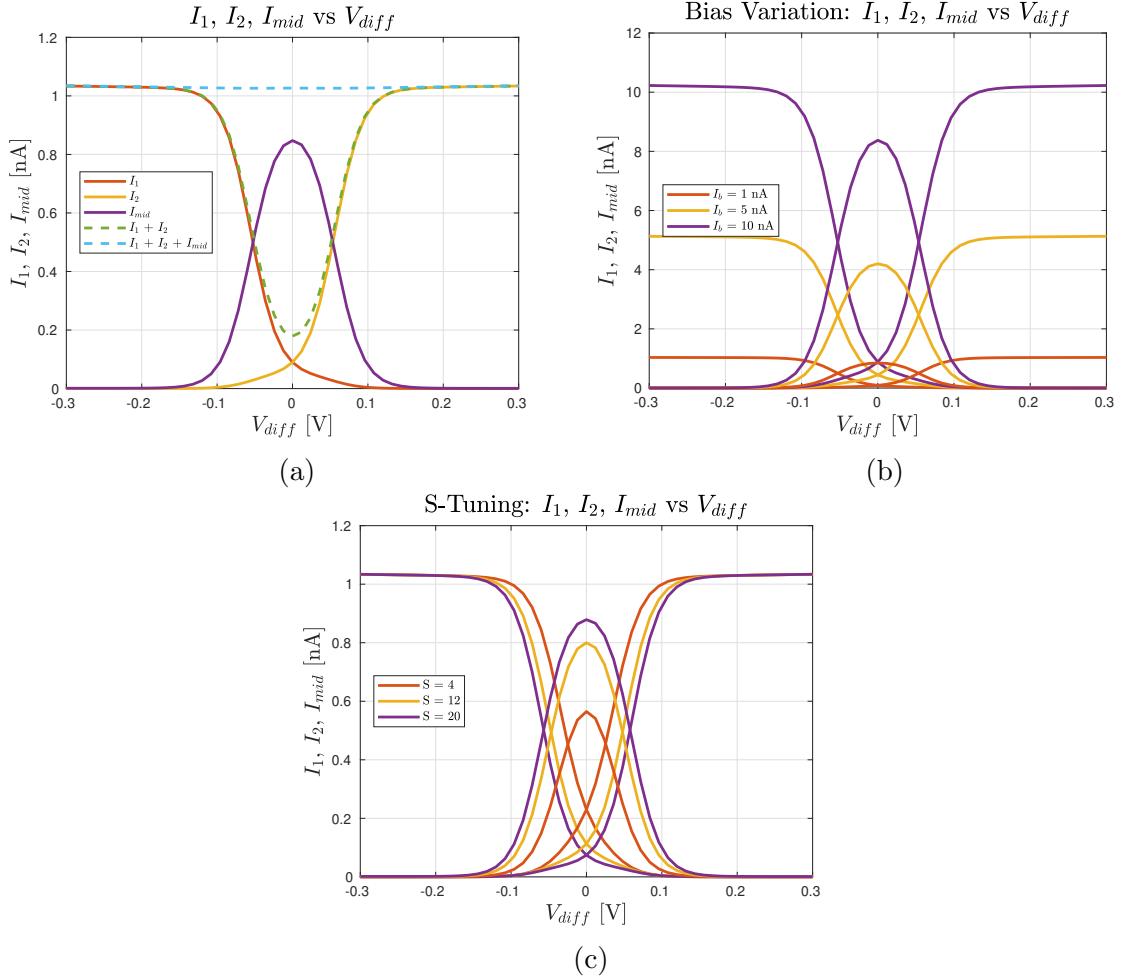


Figure 29: (a) measurements of  $I_1$ ,  $I_2$  while sweeping  $V_{diff}$  (b) variation of bias parameter  $I_b$  (c) tuning of the S-ratio.

### 3.10.3 Mismatch Analysis

A mismatch analysis was done using the first simulation setup. The variation of results is very similar to that of the differential pair, as observed in Figure 30.

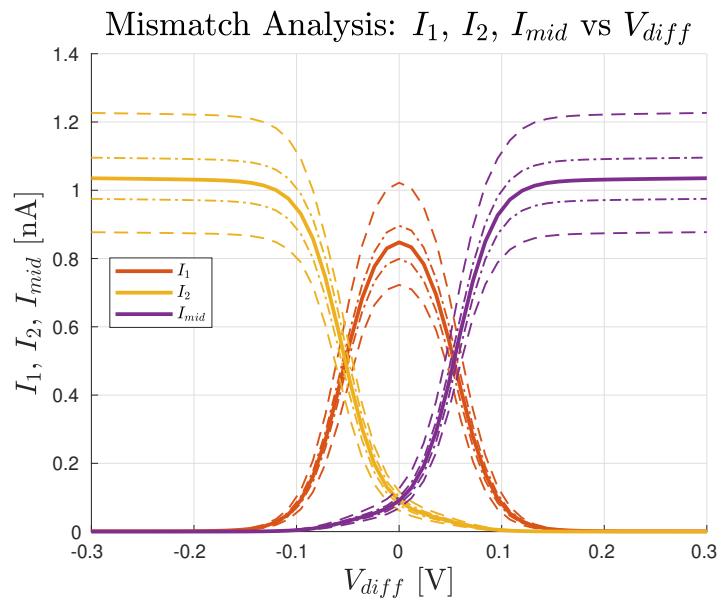


Figure 30: mismatch analysis of the bump antibump circuit.

## 3.11 N-Type 5T Transamp

### 3.11.1 Description

The N-type 5T transamp receives two input voltages,  $V_+$  &  $V_-$  and provides a single output  $V_{out}$ , as well as a single, bidirectional output current  $I_{out}$ . The circuit is primarily used as a comparator, outputting a high output signal if  $V_+ > V_-$ , and a low output signal if  $V_+ < V_-$ . The circuit schematic is shown in Figure 31.

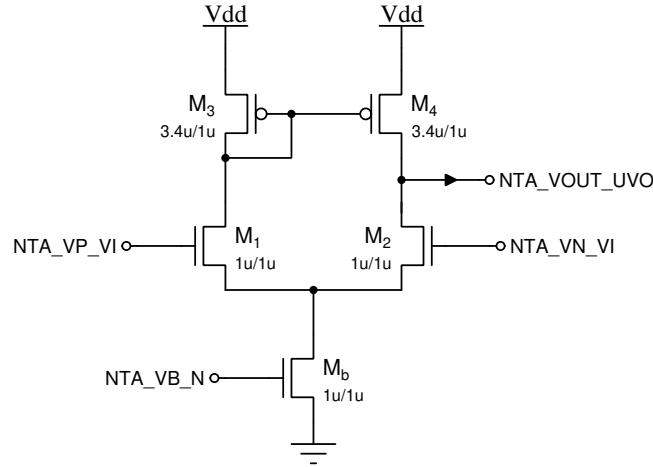


Figure 31: N-Type 5T transamp schematic.

### 3.11.2 Simulations

Both  $V_{out}$  and  $I_{out}$  are observed in the simulations. For simulations measuring  $V_{out}$ ,  $V_+$  is swept while  $V_- = 0.5V$ . For simulations measuring  $I_{out}$ , both inputs are tied to a common  $V_{diff}$ , which is swept over the range  $-0.9V < V_{diff} < 0.9V$ , with an input common-mode  $V_{cm} = 1V$ . In order to measure  $I_{out}$ ,  $V_{out}$  must be tied to a set voltage, and can't be left floating: for these simulations it is set to  $V_{out} = 1V$ . Where not specified, the input bias  $I_b = 1nA$ . Simulation plots are shown in Figure 32.

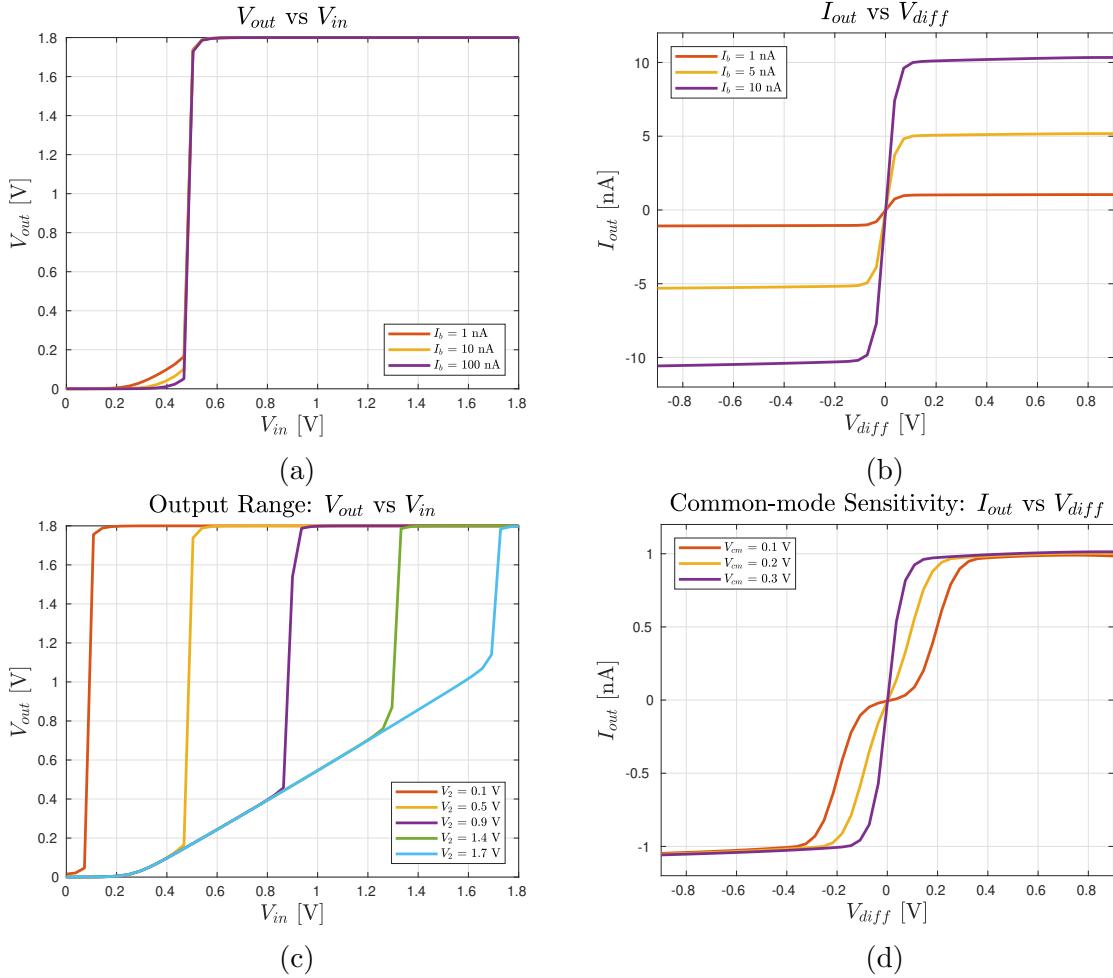


Figure 32: measurements of  $V_{out}$ ,  $I_{out}$  for (a) & (b) variation in  $I_b$  (c) set levels of  $V_2$ , (d) different input common-modes,  $V_{cm}$ .

### 3.11.3 Mismatch Analysis

A mismatch analysis was performed using both simulation setups needed for observing  $V_{out}$  &  $I_{out}$ . Variation in  $V_{out}$  was minimal, only becoming visible on the slope. Note that the "spike" in the max measurement is a plotting artefact, and doesn't appear in the actual data results. Variation in  $I_{out}$  was more pronounced, especially at the "tail". This is likely due to mismatch between in current-mirror pair. Analysis results are shown in Figure 33.

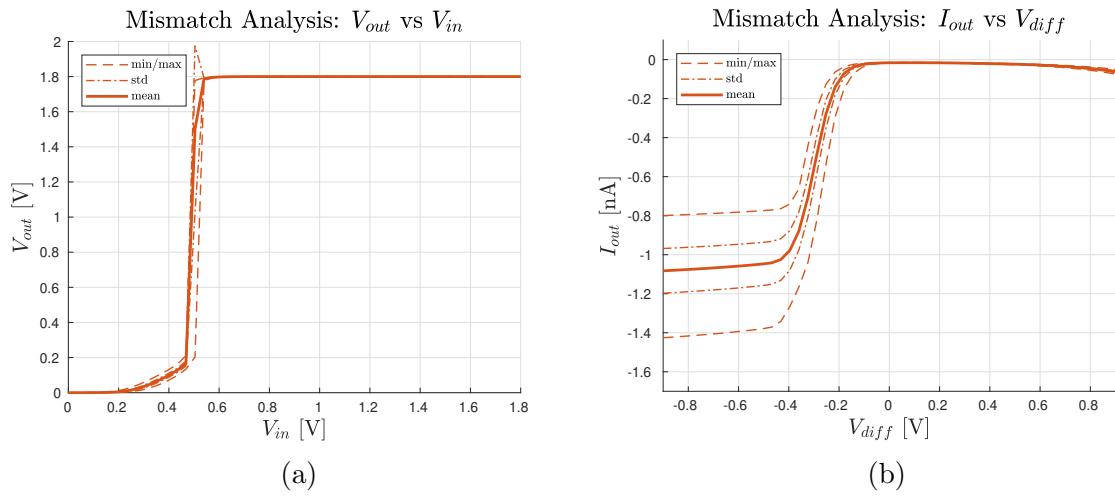


Figure 33: mismatch analysis of the N-type 5T transamp circuit, observing (a)  $V_{out}$  and (b)  $I_{out}$

## 3.12 P-Type 5T Transamp

The P-type 5T transamp receives two input voltages,  $V_+$  &  $V_-$  and provides a single output  $V_{out}$ , as well as a single, bidirectional output current  $I_{out}$ . The circuit is primarily used as a comparator, outputting a high output signal if  $V_+ > V_-$ , and a low output signal if  $V_+ < V_-$ . The circuit schematic is shown in Figure 34.

### 3.12.1 Description

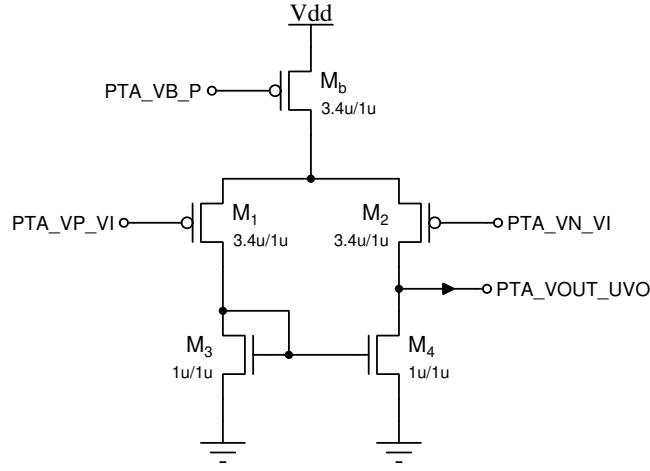


Figure 34: P-Type 5T transamp schematic.

### 3.12.2 Simulations

Both  $V_{out}$  and  $I_{out}$  are observed in the simulations. For simulations measuring  $V_{out}$ ,  $V_+$  is swept while  $V_- = 0.5V$ . For simulations measuring  $I_{out}$ , both inputs are tied to a common  $V_{diff}$ , which is swept over the range  $-0.9V < V_{diff} < 0.9V$ , with an input common-mode  $V_{cm} = 1V$ . In order to measure  $I_{out}$ ,  $V_{out}$  must be tied to a set voltage, and can't be left floating: for these simulations it is set to  $V_{out} = 1V$ . Where not specified, the input bias  $I_b = 1nA$ . Simulation plots are shown in Figure 35.

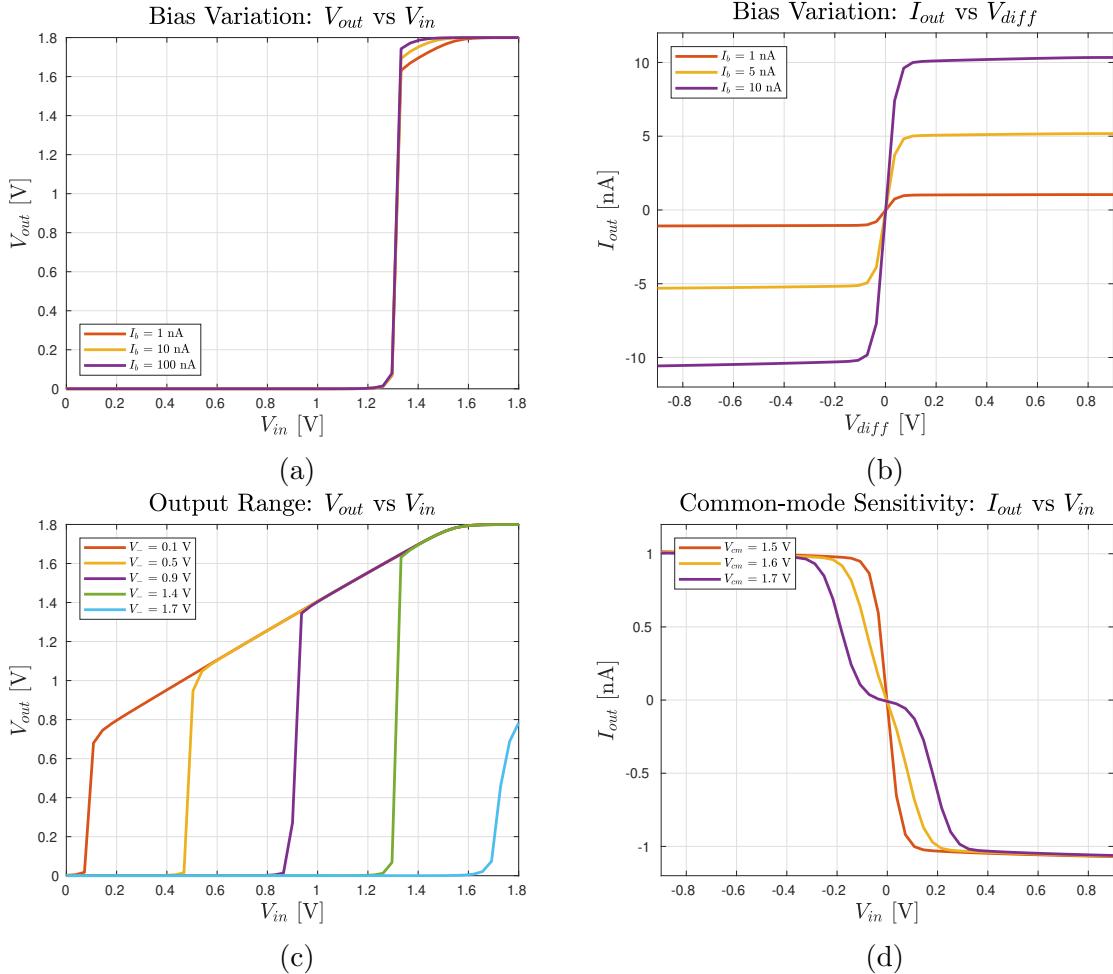


Figure 35: measurements of  $V_{out}$ ,  $I_{out}$  for (a) & (b) variation in  $I_b$  (c) set levels of  $V_2$ , (d) different input common-modes,  $V_{cm}$ .

### 3.12.3 Mismatch Analysis

A mismatch analysis was performed using both simulation setups needed for observing  $V_{out}$  &  $I_{out}$ . Variation in  $V_{out}$  was minimal, only becoming visible on the slope. Note that the "spike" in the max measurement is a plotting artefact, and doesn't appear in the actual data results. Again, variation in  $I_{out}$  was more pronounced, especially at the "tail". This is likely due to mismatch between in current-mirror pair. Analysis results are shown in Figure 36.

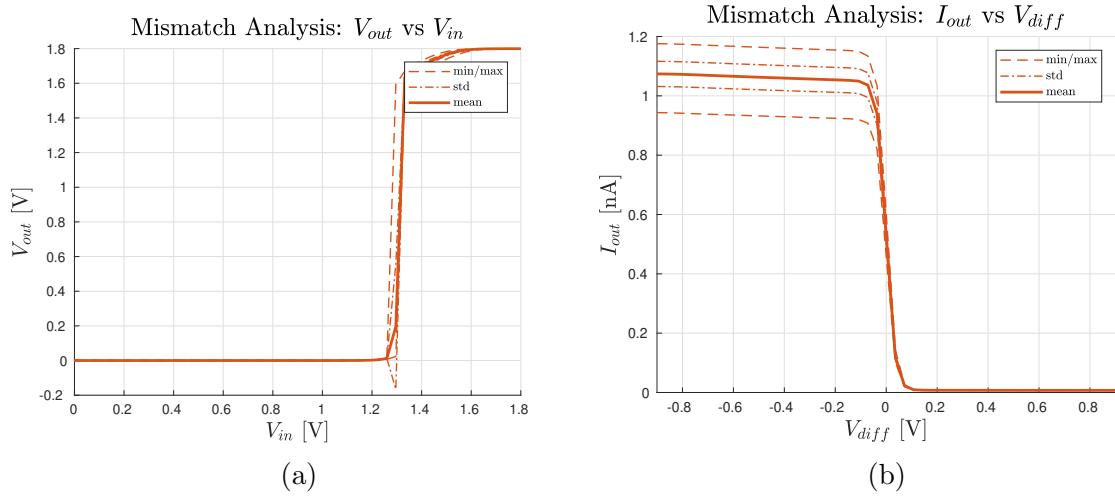


Figure 36: mismatch analysis of the P-type 5T transamp circuit, observing (a)  $V_{out}$  and (b)  $I_{out}$

### 3.13 Wide-Range Transamp

#### 3.13.1 Description

The wide-range transamp is an extension of the N-type 5T transamp (there also exists an extension of the P-type variant), which extends the output range from GND to VDD, regardless of the value of  $V_-$ . Like the 5T transamp, it receives two input voltages,  $V_+$  and  $V_-$  and provides a single output voltage  $V_{out}$ , as well as a single, bidirectional output current  $I_{out}$ . The circuit can be used either as an amplifier or a buffer. The circuit schematic is shown in Figure 37.

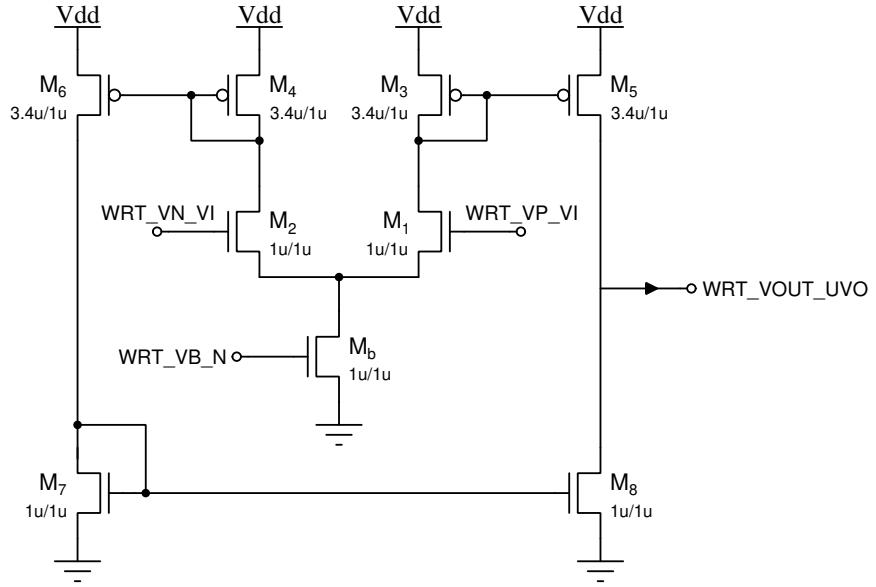


Figure 37: Wide-range transamp schematic.

#### 3.13.2 Simulations

Again, both  $V_{out}$  and  $I_{out}$  are observed in the simulations. For simulations measuring  $V_{out}$ ,  $V_+$  is swept while  $V_- = 0.5V$ . For simulations measuring  $I_{out}$ , both inputs are tied to a common  $V_{diff}$ , which is swept over the range  $-0.9V < V_{diff} < 0.9V$ , with an input common-mode  $V_{cm} = 1V$ . In order to measure  $I_{out}$ ,  $V_{out}$  must be tied to a set voltage, and can't be left floating: for these simulations it is set to  $V_{out} = 1V$ . Where not specified, the input bias  $I_b = 1nA$ . Simulation plots are shown in Figure 32. Other than the extension of the output range, results are very similar to that of the N-type 5T transamp.

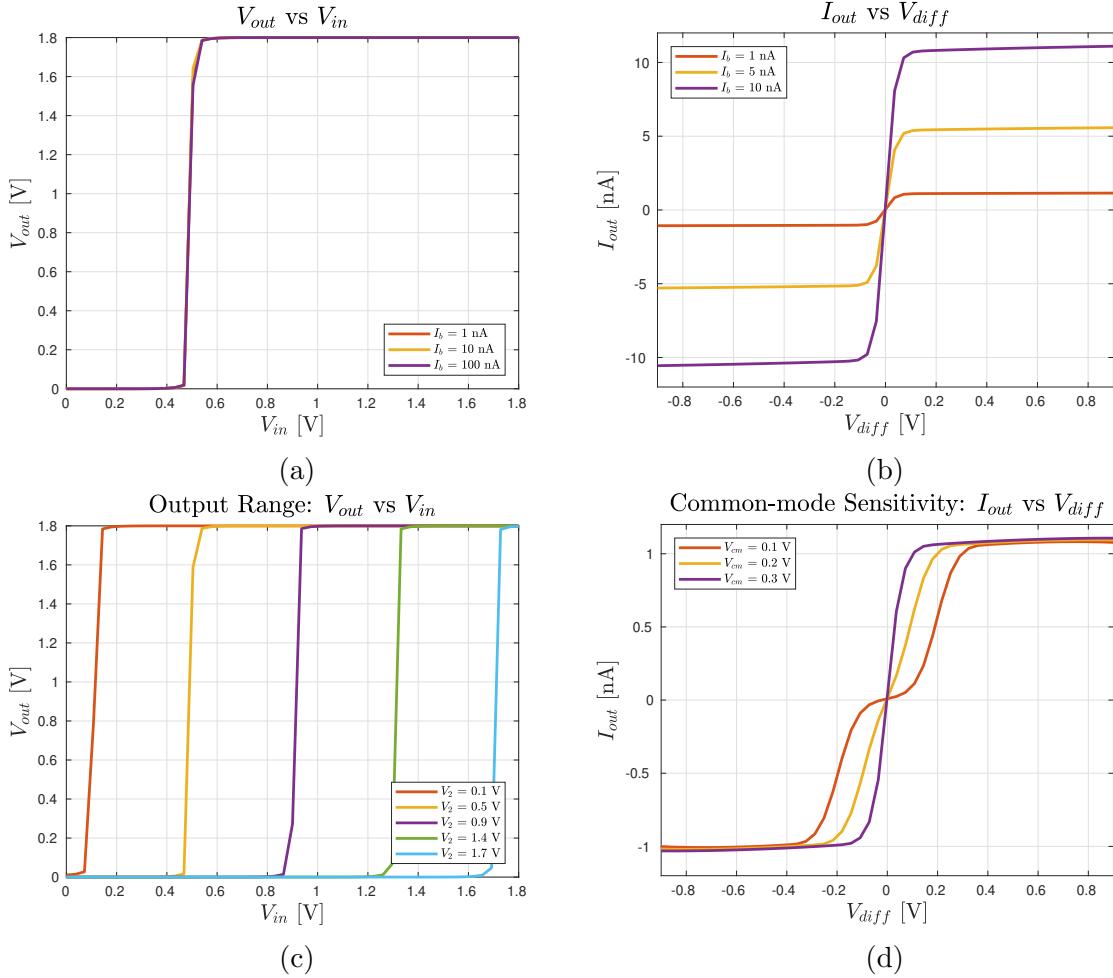


Figure 38: measurements of  $V_{out}$ ,  $I_{out}$  for (a) & (b) variation in  $I_b$  (c) set levels of  $V_2$ , (d) different input common-modes,  $V_{cm}$ .

### 3.13.3 Mismatch Analysis

A mismatch analysis was performed using both simulation setups needed for observing  $V_{out}$  &  $I_{out}$ . Variation in  $V_{out}$  was minimal, only becoming visible on the slope. Note that, unlike the two 5T transamps, there is no "spike" max measurement. Variation in  $I_{out}$  was more pronounced, especially at the "tail". In this case, the variation at the tail was significantly larger, spanning several hundred nanoamperes. Analysis results are shown in Figure 33.

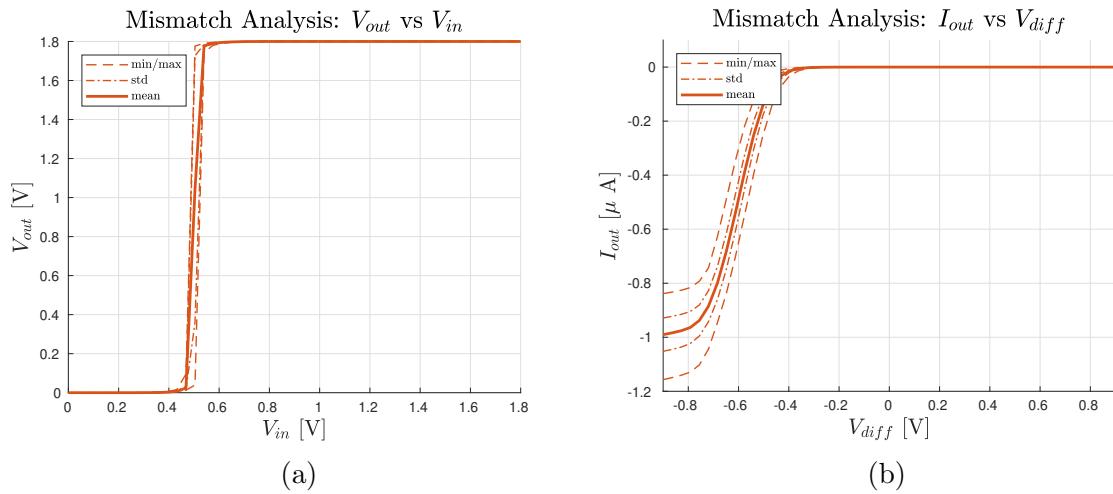


Figure 39: mismatch analysis of the wide-range transamp circuit, observing (a)  $V_{out}$  and (b)  $I_{out}$

## 3.14 Current-Splitter Array

### 3.14.1 Description

The current splitter comprises 16 cells, each cell outputting a current that is half that output by the previous cell, ie by a division of  $2^{n-1}$ ,  $1 \leq n \leq 16$ . The base current is set by an input voltage  $V_g$ , with a bias parameter  $V_t$  available to tune this base current to an exact measure. The circuit schematic is shown in Figure 40.

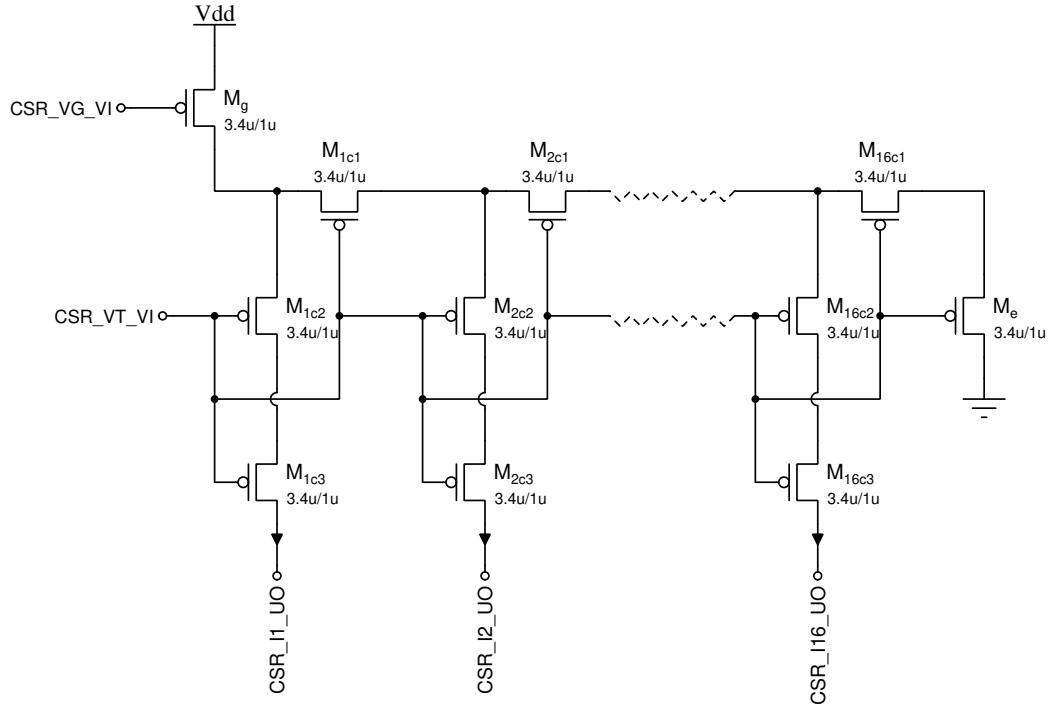


Figure 40: Current-splitter array schematic.

### 3.14.2 Simulations

The first four output currents,  $I_1$ ,  $I_2$ ,  $I_3$  and  $I_4$  were observed for  $V_g = 200mV$ . In the first simulation,  $I_t = 1nA$ , while in the second simulation,  $I_t$  is varied. Simulation plots are shown in Figure 41.

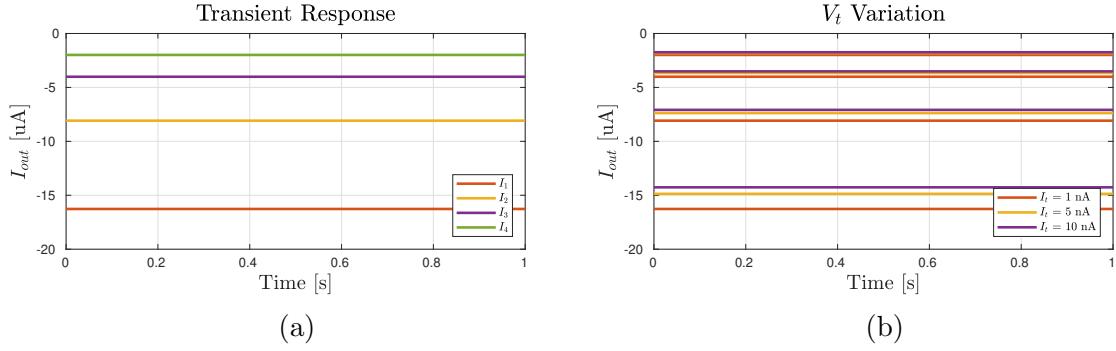


Figure 41: measurements of the outputs of the first four cells:  $I_1$ ,  $I_2$ ,  $I_3$ ,  $I_4$  (a) over time and (b) with variation in  $V_t$ .

### 3.14.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup, with outputs  $I_1$  and  $I_{16}$  observed. While the amount of absolute variation in output current was larger for the first cell, the relative variation was greater for the last cell. Analysis results are shown in Figure 42.

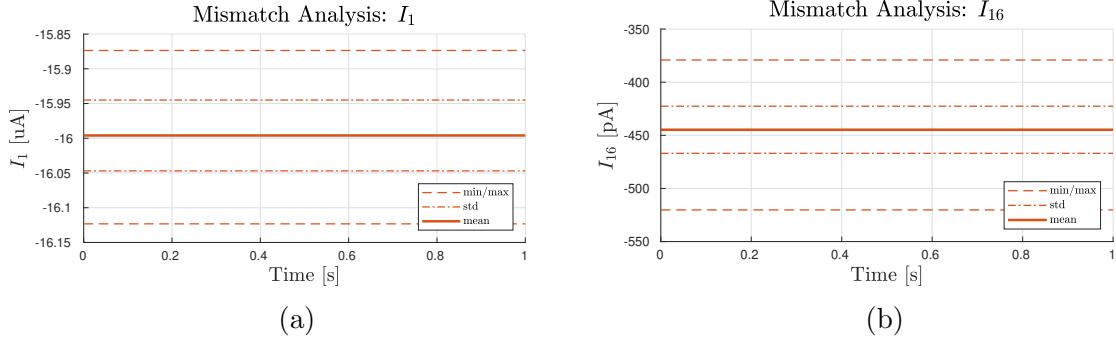


Figure 42: mismatch analysis of the current splitter array, observing (a) the first cell  $I_1$ , and (b) the last cell  $I_{16}$ .

## 3.15 Winner-Take-All Array

### 3.15.1 Description

The winner-take-all circuit also comprises 16 cells, with the first cell connected to the last cell by "wrap-around lines", VO & VC. The cell with the largest input voltage  $V_{in(n)}$  "takes" all of the current, which is read at  $I_{out(n)}$ .  $V_{out(n)}$  and  $I_{all(n)}$  are available to read cell states. There are four circuit biases parameters, shared by all cells:  $V_b$ ,  $V_{ex}$ ,  $V_{inh}$  and  $V_{gain}$ . The circuit has two modes of operation: hysteretics ON and OFF, which is set by  $V_{hen}$ , an active-low control line that is also shared by all cells.

As this circuit is known to be sensitive to mismatch, dummies were used extensively: both within the cells to ensure cell devices are surrounded by same geometries, as well as by placing dummy cells on either side of the array to mitigate corner effects on  $Cell_1$  &  $Cell_{16}$ . Schematics of the cell and the array are shown in Figures 43 & 44.

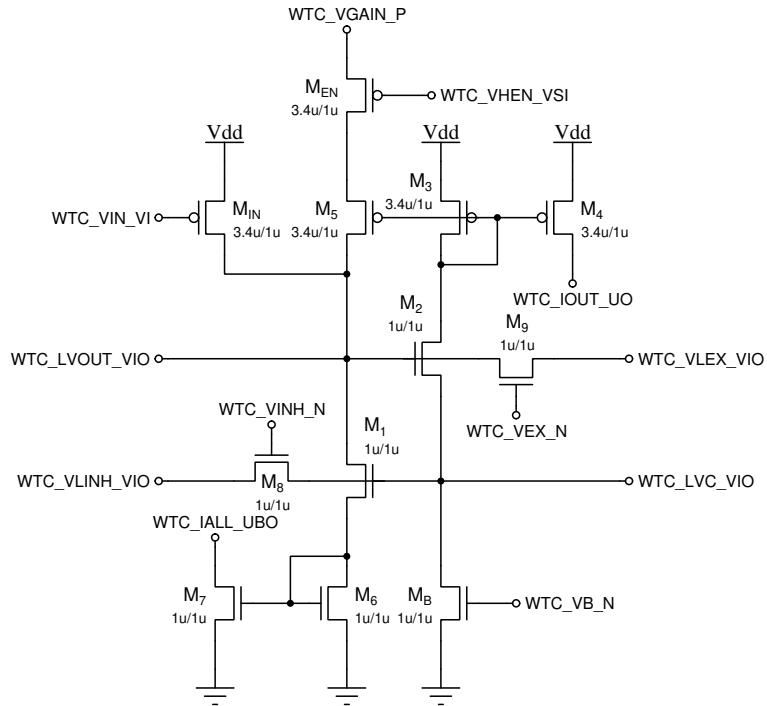


Figure 43: Current-splitter cell schematic.

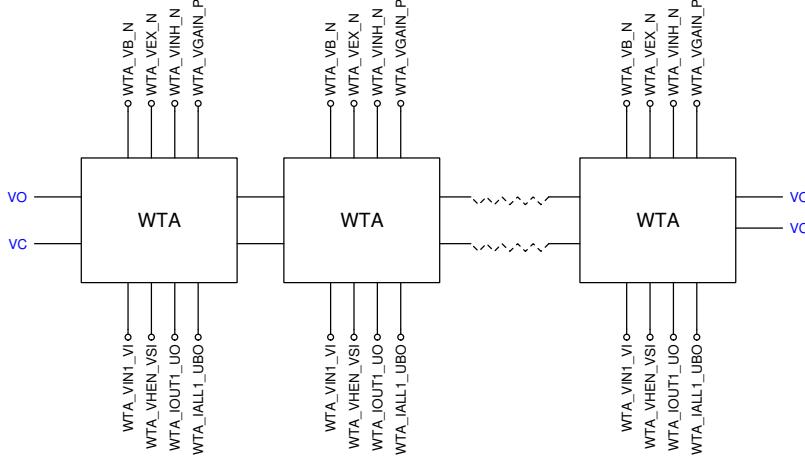


Figure 44: Current-splitter array schematic.

### 3.15.2 Simulations

In the first simulation,  $Cell_1$  and  $Cell_2$  are observed, with their input voltages stepped by some amount below VDD and their outputs observed over time. Biases are set to  $I_b = 1nA$ ,  $I_{ex} = 1nA$ ,  $I_b = 1nA$  ( $I_{gain}$  is left unset) and  $V_{hen}$  is tied to VDD. Results of this first simulation are shown in Figure 45.

In the remaining simulations,  $Cell_3$  and  $Cell_4$  are observed, with their inputs tied to a common differential voltage  $V_{diff}$  that is swept over the range  $-0.1V < V_{diff} < 0.1V$ , and is offset against an input common-mode  $V_{cm} = 1.8V$ .  $I_b = 500nA$  (necessary for the hysteretic effects to be observed) and  $I_{gain} = 50nA$ , with the remaining biases remaining the same. For the second simulation, hysteretics is OFF, while in the third simulation hysteretics is ON. In the fourth simulation,  $I_{gain}$  is varied. Results of these simulations are shown in Figure 46.

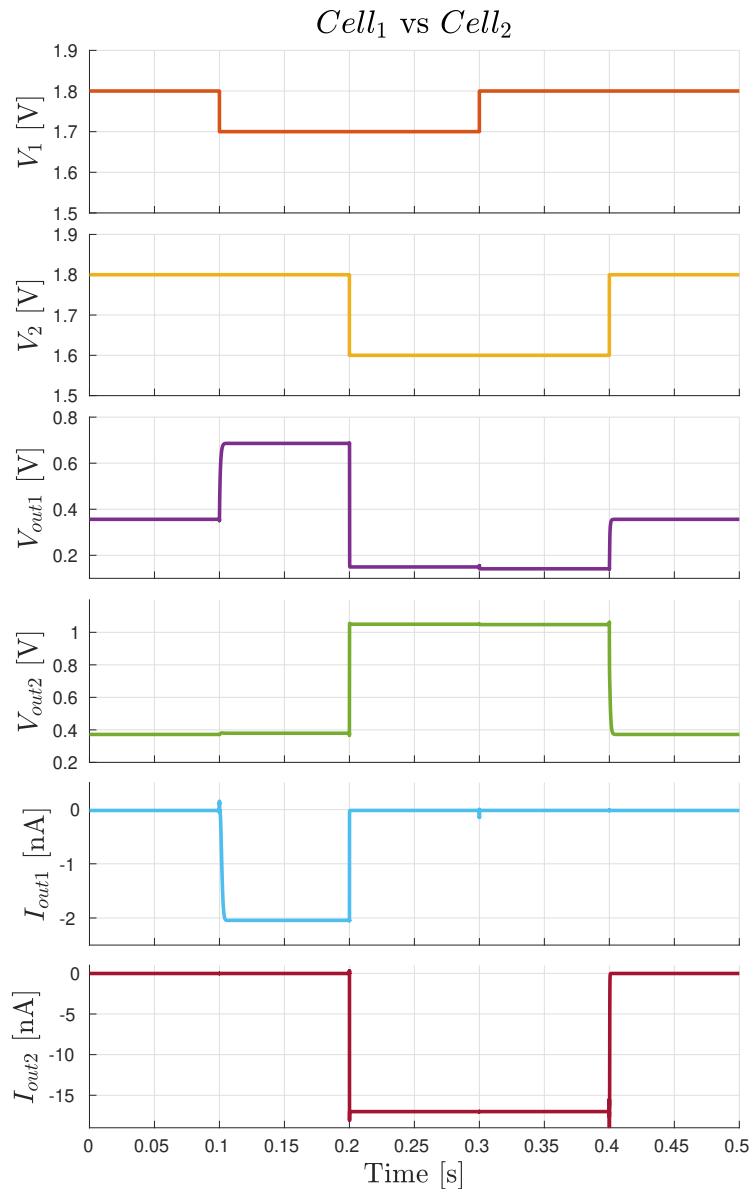


Figure 45: measurements of the output voltages,  $V_{out1}$  &  $V_{out2}$ , and the output currents,  $I_{out1}$  &  $I_{out2}$ , of the first two cells for their given inputs,  $V_{in1}$  &  $V_{in2}$ .

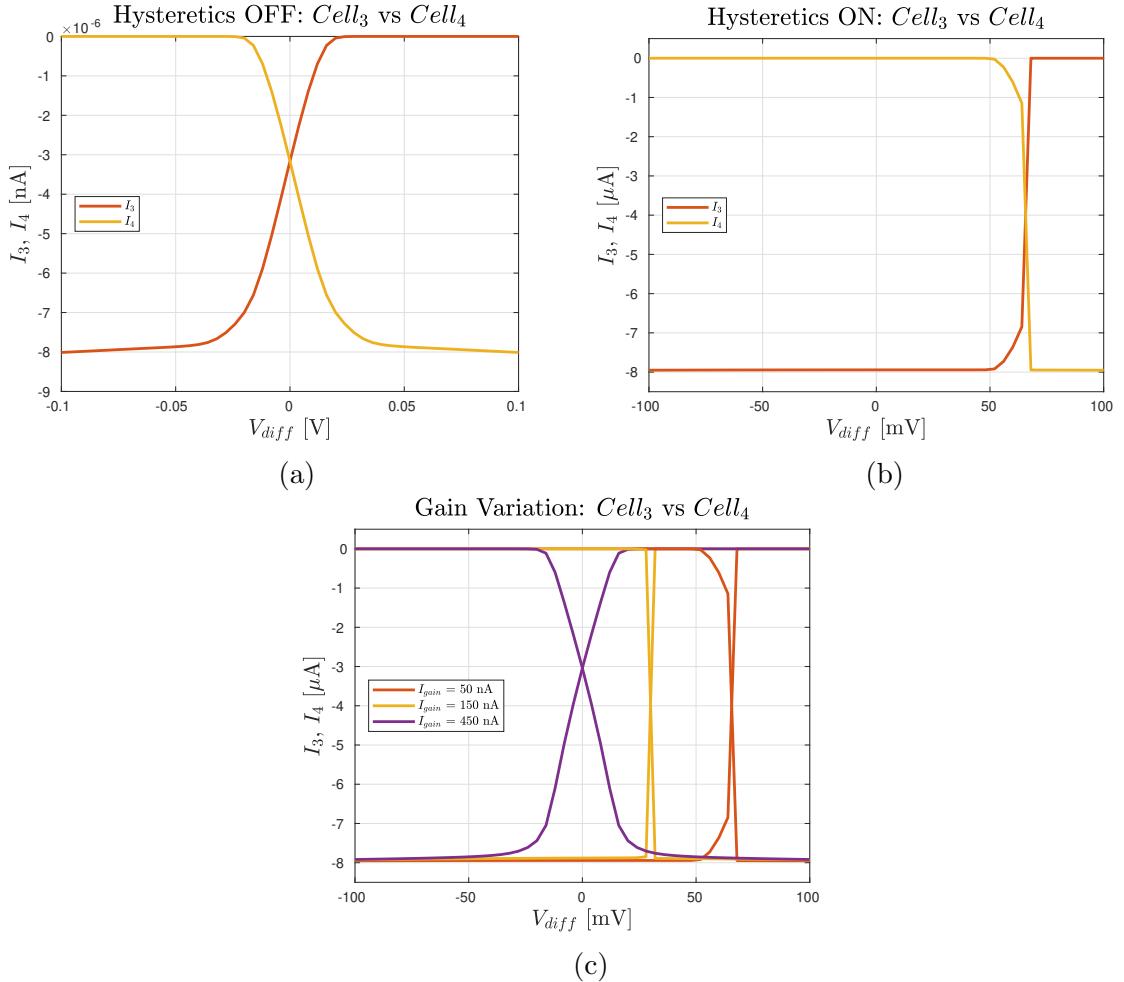


Figure 46: measurements of the output currents,  $I_{out3}$  &  $I_{out4}$  with (a) hysteretic mode OFF (b) hysteretic mode ON (c) variations in  $I_{gain}$  with hysteretic mode ON.

### 3.15.3 Mismatch Analysis

A mismatch analysis was performed using the second simulation setup. As noted, this circuit is quite sensitive to mismatch, which will affect the amount of input required to get one cell to "beat" another. Analysis results are shown in Figure 47.

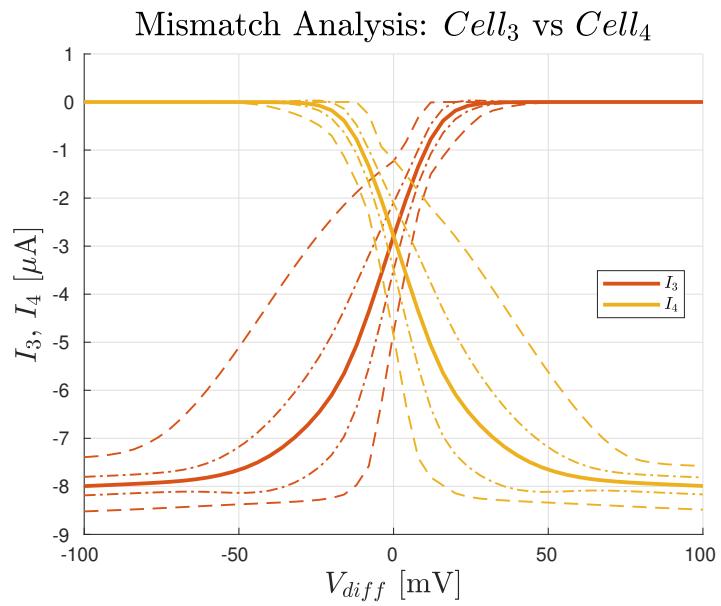


Figure 47: mismatch analysis of the winner-take-all array, observing output currents  $I_{out3}$  &  $I_{out4}$ .

## 3.16 Follower-Integrator

### 3.16.1 Description

The follower-integrator comprises a single wide-range transamp connected to a capacitor. The circuit implements a first-order low-pass filter. It has a single input voltage  $V_{in}$  and input bias  $V_b$ . The circuit schematic is shown in Figure 48. Capacitor sizing was chosen for a capacitance value of  $2pF$ .

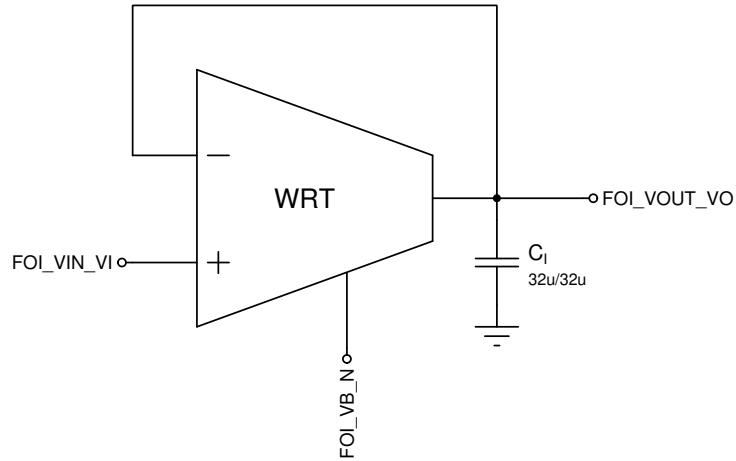


Figure 48: Follower Integrator schematic.

### 3.16.2 Simulations

Both transient and frequency analyses were performed in simulations. For the transient analysis, an  $V_{in}$  was fed an input pulse train with a  $1ms$  period, while for the frequency analysis a synusoid was provided, with frequency swept from  $100Hz$  to  $1MHz$ . The input bias was set to  $I_b = 1nA$  when not varied. Simulation results are shown in Figure 49.

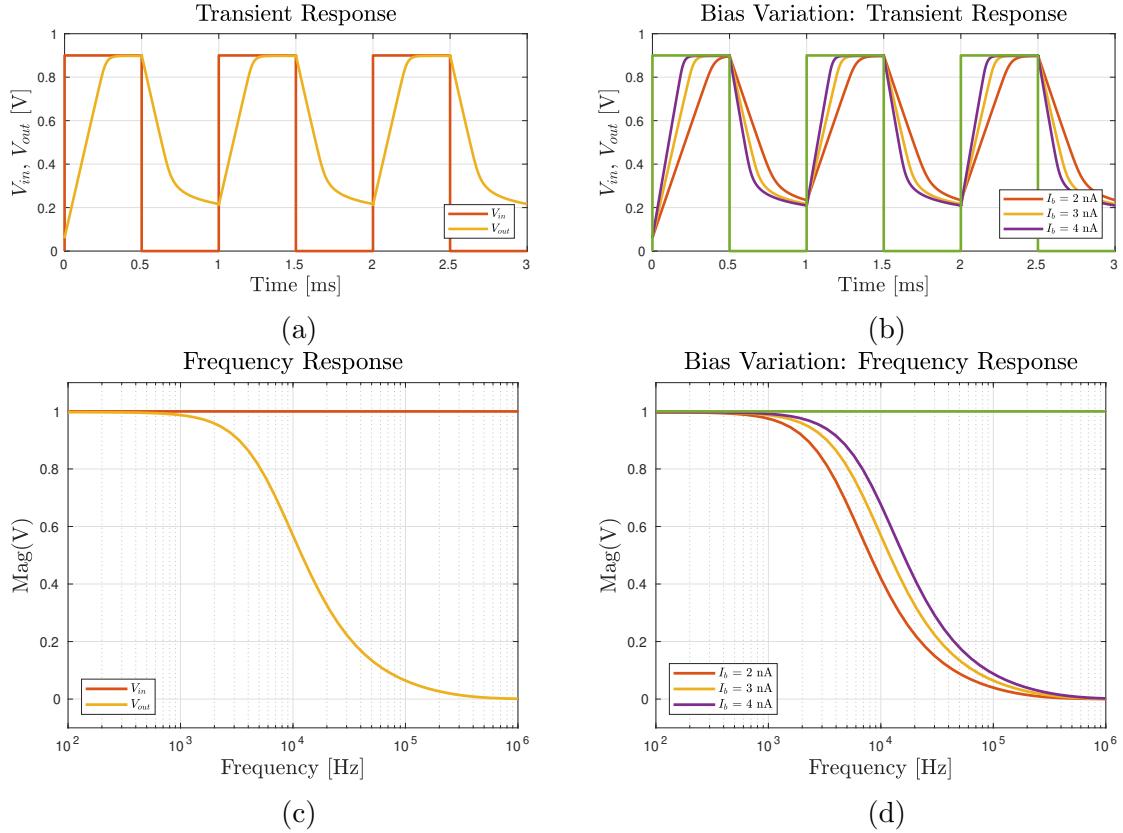


Figure 49: (a) transient response (b) with variation in  $I_b$ ; (c) frequency response (d) with variation in  $I_b$ .

### 3.16.3 Mismatch Analysis

A mismatch analysis was performed using the transient response setup. Most variation was observed in the filter response, however the amplitude of  $V_{out}$  also shifted slightly in outlier cases. Analysis results are shown in Figure 50.

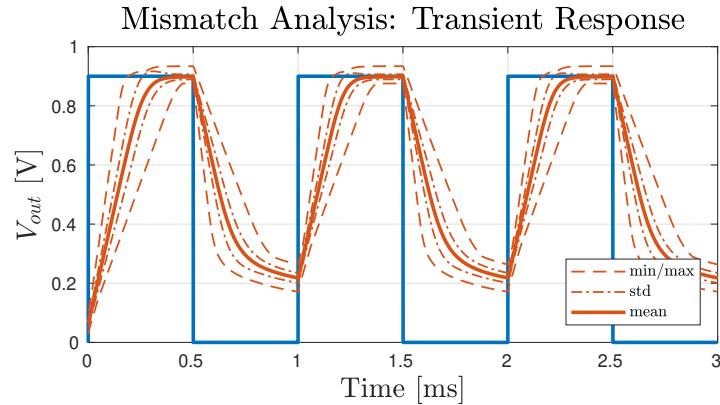


Figure 50: mismatch analysis of the follower integrator circuit.

## 3.17 Follower-Differentiator

### 3.17.1 Description

The follower-differentiator, like the follower-integrator, comprises a single wide-range transamp connected to a capacitor, though in a different configuration. The circuit implements a first-order high-pass filter. It has both an input voltage  $V_{in}$  and  $V_{ref}$ , and input bias  $V_b$ . The circuit schematic is shown in Figure 48. Capacitor sizing was chosen for a capacitance value of  $2pF$ .

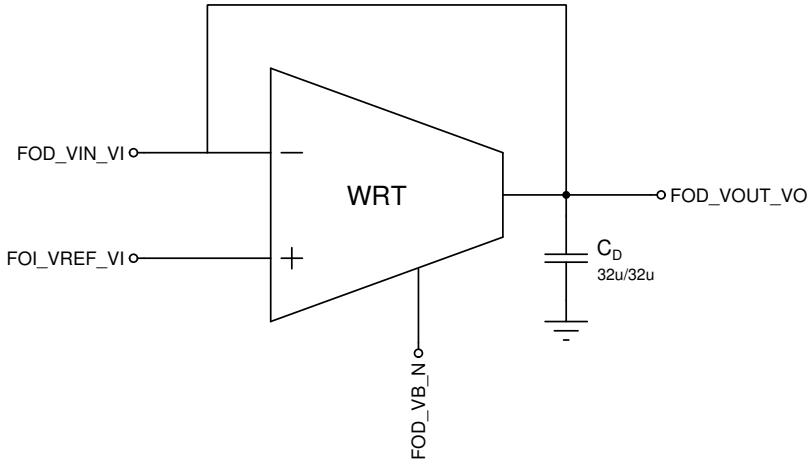


Figure 51: Follower Differentiator schematic.

### 3.17.2 Simulations

Both transient and frequency analyses were performed in simulations. For the transient analysis, an  $V_{in}$  was fed an input pulse train with a  $1ms$  period and a  $0.5V$  offset, while for the frequency analysis a synusoid was provided, with frequency swept from  $100Hz$  to  $1MHz$ .  $V_{ref} = 0.5V$ , and the input bias was set to  $I_b = 1nA$  when not varied. Simulation results are shown in Figure 52.

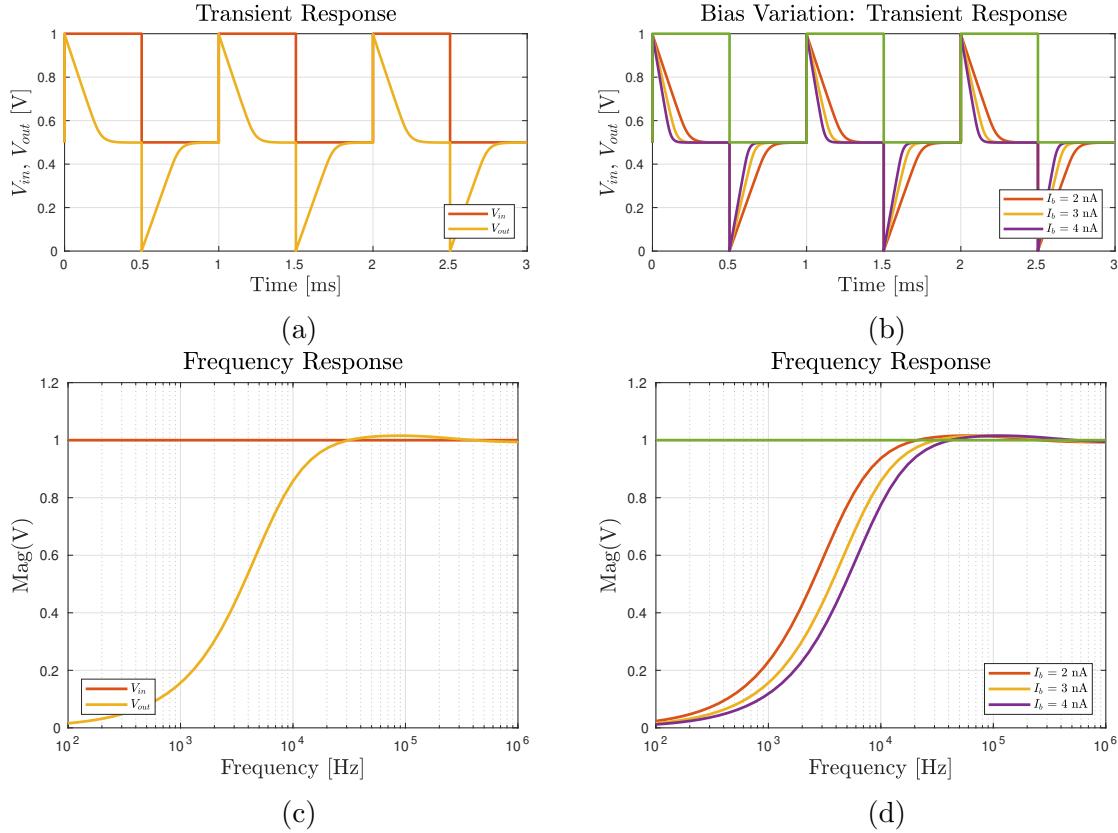


Figure 52: (a) transient response (b) with variation in  $I_b$ ; (c) frequency response (d) with variation in  $I_b$ .

### 3.17.3 Mismatch Analysis

As with the follower-integrator, a mismatch analysis was performed using the transient response setup. In this case, all variation was observed in the filter response, with no observable variation in the output amplitude. Analysis results are shown in Figure 53.

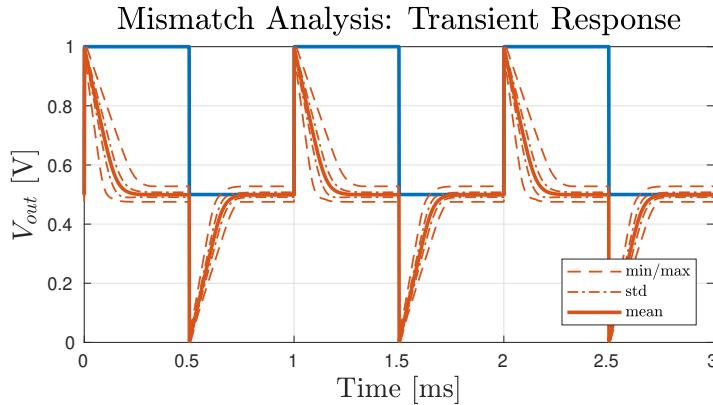


Figure 53: mismatch analysis of the follower differentiator circuit.

## 3.18 Resistive Element

### 3.18.1 Description

The resistive element is a single P-FET device with the gate tied to one terminal and the bulk tied to the other. In this configuration, it acts as a non-linear resistor. The circuit schematic is shown in Figure 54.

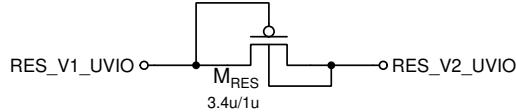


Figure 54: Resistive Element schematic.

### 3.18.2 Simulations

A single simulation was done, with both inputs  $V_1$  &  $V_2$  tied to a common differential voltage  $V_{diff}$ , which was swept over the range  $-0.3V < V_{diff} < 0.3V$ . Current was read at both terminals as  $I_1$  &  $I_2$ . Simulation plots are shown in Figure 55.

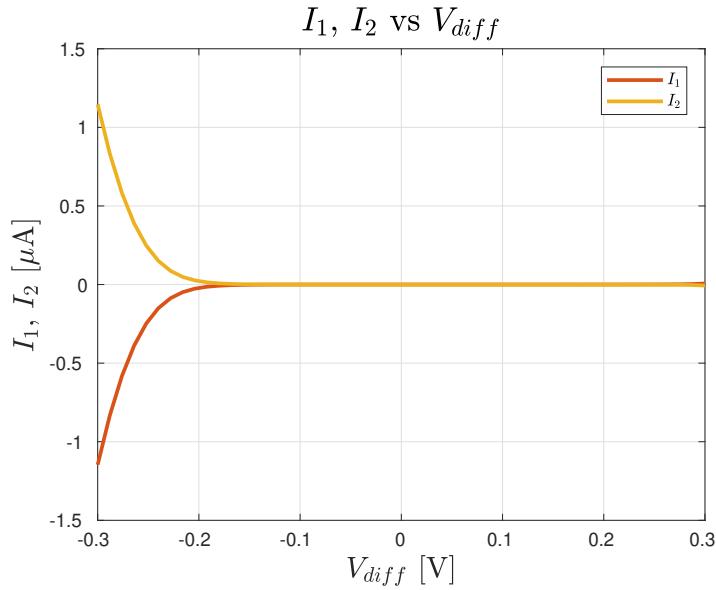


Figure 55: measurements of output currents  $I_1$  &  $I_2$  while sweeping a common input  $V_{diff}$ .

### 3.18.3 Mismatch Analysis

A mismatch analysis was done using the simulation setup described. A variation in device conductance was observed.

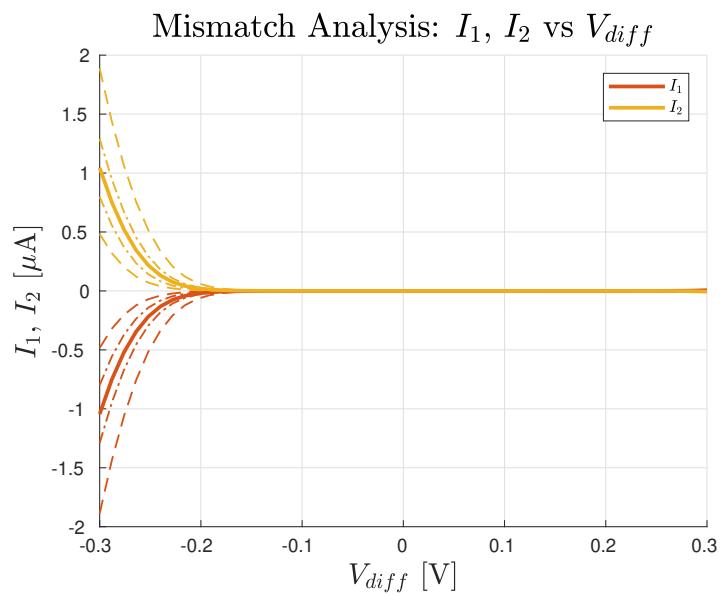


Figure 56: mismatch analysis of the resistive element circuit.

## 3.19 Symmetric Resistive Element

### 3.19.1 Description

The symmetric resistive element extends the resistive element by providing for a variable conductance, and comprises two branches of P-FET devices that are each tied to the inputs and outputs of source-follower. This circuit has two input biases,  $V_{b1}$  &  $V_{b2}$ . With the second branch enabled (set by an active-low  $V_{en}$ ), the non-linear conductance is mirrored. The circuit schematic is shown in Figure 57.

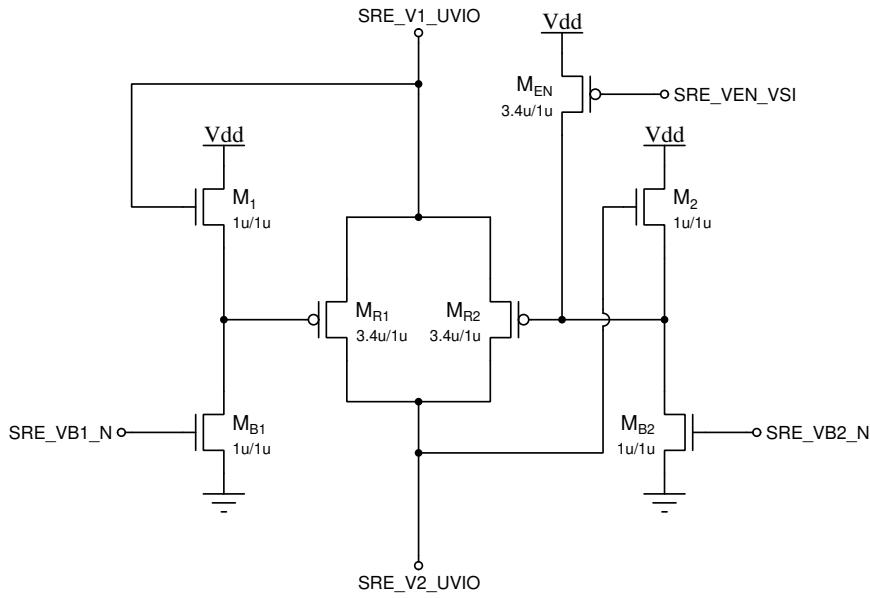


Figure 57: Symmetric resistive element schematic.

### 3.19.2 Simulations

As with the resistive element, both inputs  $V_1$  &  $V_2$  tied to a common differential voltage  $V_{diff}$ , which was swept over the range  $-0.3V < V_{diff} < 0.3V$ , with a common mode  $V_{cm} = 0.9V$ . Current was read at both terminals as  $I_1$  &  $I_2$ . In the first simulation  $V_{en}$  was set OFF, while in the second simulation  $V_{en}$  was set ON. Input biases were set to  $I_{b1} = I_{b2} = 1nA$  for simulations, and were varied in the third simulation. Simulation plots are shown in Figure 55.

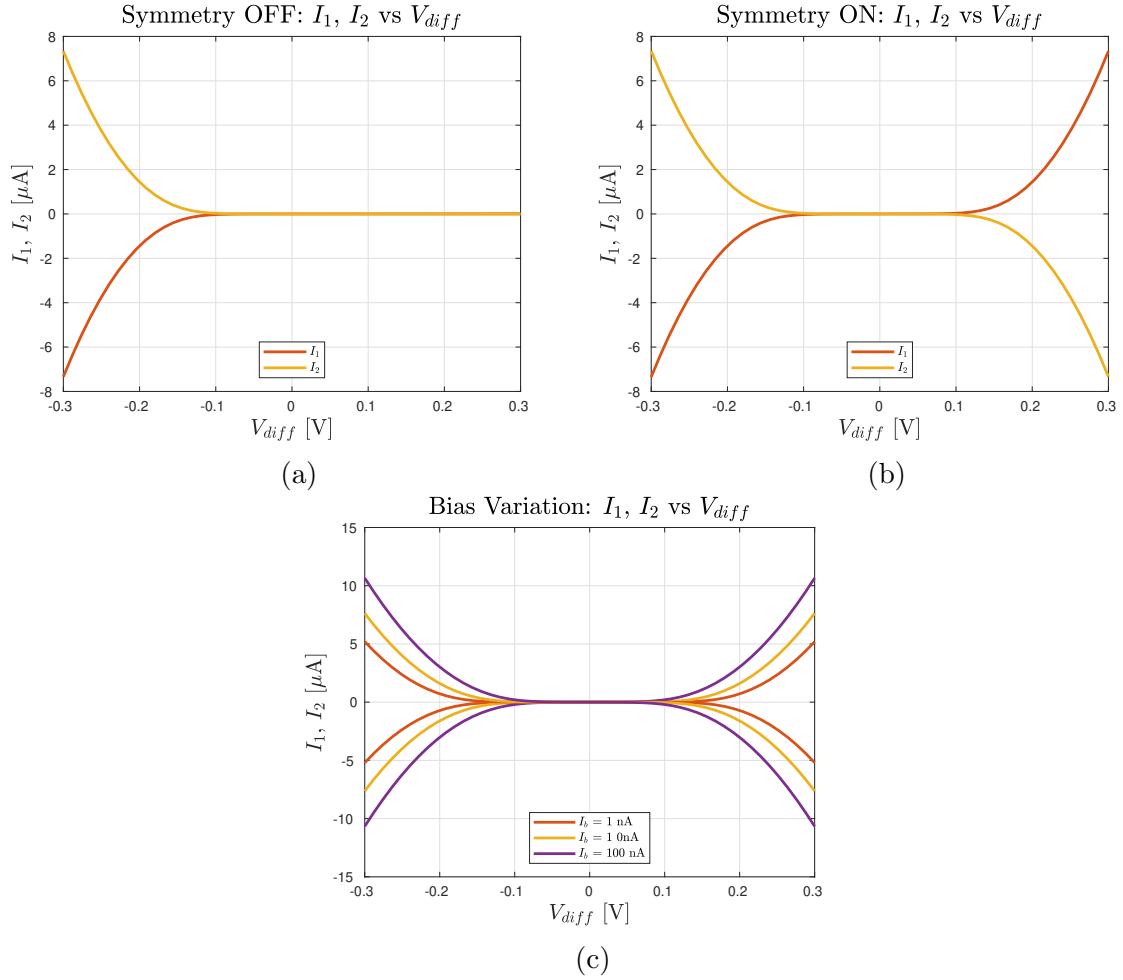


Figure 58: measurements of output currents  $I_1$  &  $I_2$  while sweeping  $V_{diff}$  with (a) symmetry OFF (b) symmetry ON (c) variation of the input common-mode,  $V_{cm}$ .

### 3.19.3 Mismatch Analysis

A mismatch analysis was performed using the second simulation setup. Like the resistive element, variation in the output conductance is observed.

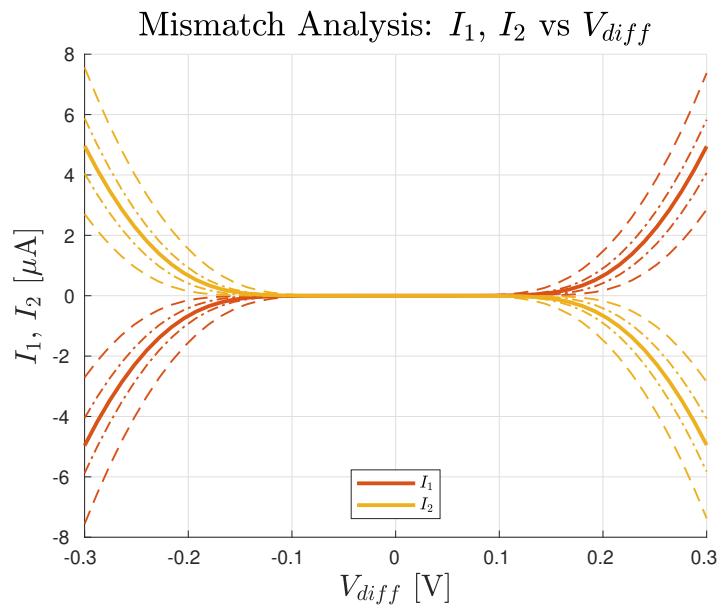


Figure 59: mismatch analysis of the symmetricresistive element circuit.

## 3.20 Source-Follower Photoreceptor

### 3.20.1 Description

The source-follower photoreceptor is a diode connected in source-follower configuration with a single N-FET device. The diode is a large block of exposed n-well that absorbs light and converts it into a current. The circuit has a single input bias,  $V_b$ , and outputs a voltage  $V_{out}$ . A schematic of the circuit is shown in Figure 60.

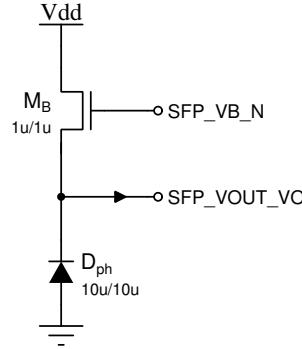


Figure 60: Source-follower photoreceptor schematic.

### 3.20.2 Simulations

For simulations, the diode was replaced with a DC input current source, which was swept from  $1fA < I_{ph} < 1nA$ . For the first simulation,  $I_b = 1nA$ , while in the second simulation it was varied. Simulation plots are shown in Figure 61.

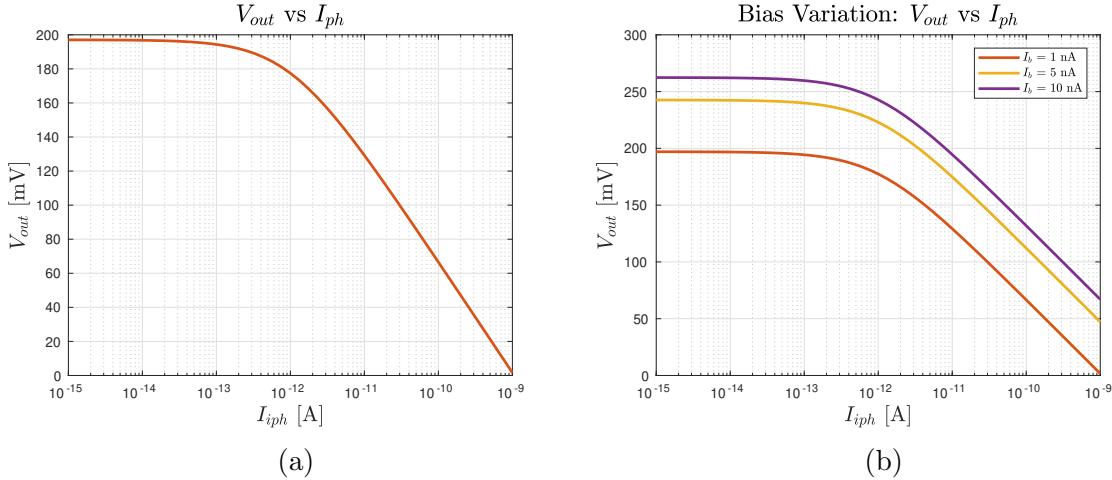


Figure 61: (a) measurements of output voltage  $V_b$  while sweeping an input current  $I_{ph}$   
(b) for variations of  $I_b$ .

### 3.20.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup. The circuit is shown to be minimally and uniformly affected by mismatch variation. Analysis results are shown in Figure 62.

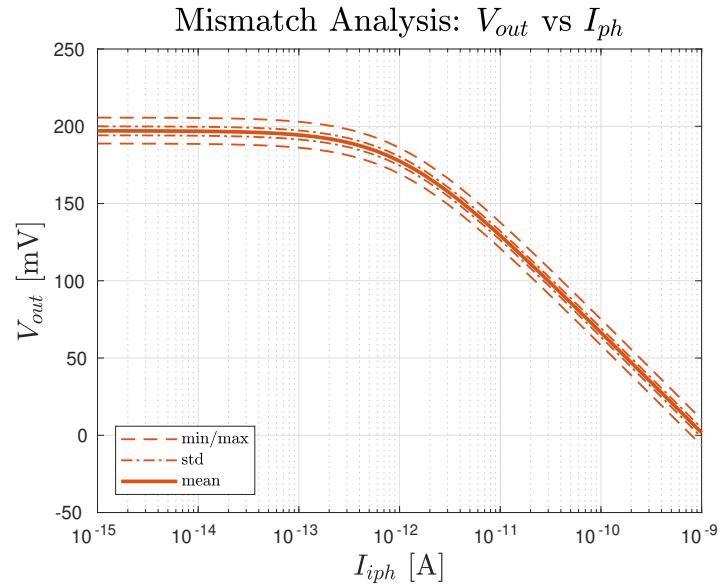


Figure 62: mismatch analysis of the source-follower photoreceptor circuit.

## 3.21 DVS Pixel

### 3.21.1 Description

The DVS pixel measures changes in scene illuminance and produces ON and OFF events that correspond to observed changes in illumination [1]. It comprises three stages: a front-stage logarithmic conversion, followed by a differencing/comparison operation and an end stage that splits out ON and OFF events to separate outputs. The input to the pixel is a large photodiode. MIM capacitors are used in the circuit proper, while a MOSCAP is used in the reset circuit to conserve space. Further, digital power rails are provided for output lines and reset circuit, as the logarithmic conversion stage is highly sensitive and strongly affected by switching in the rails. A schematic of the circuit is shown in Figure 63.

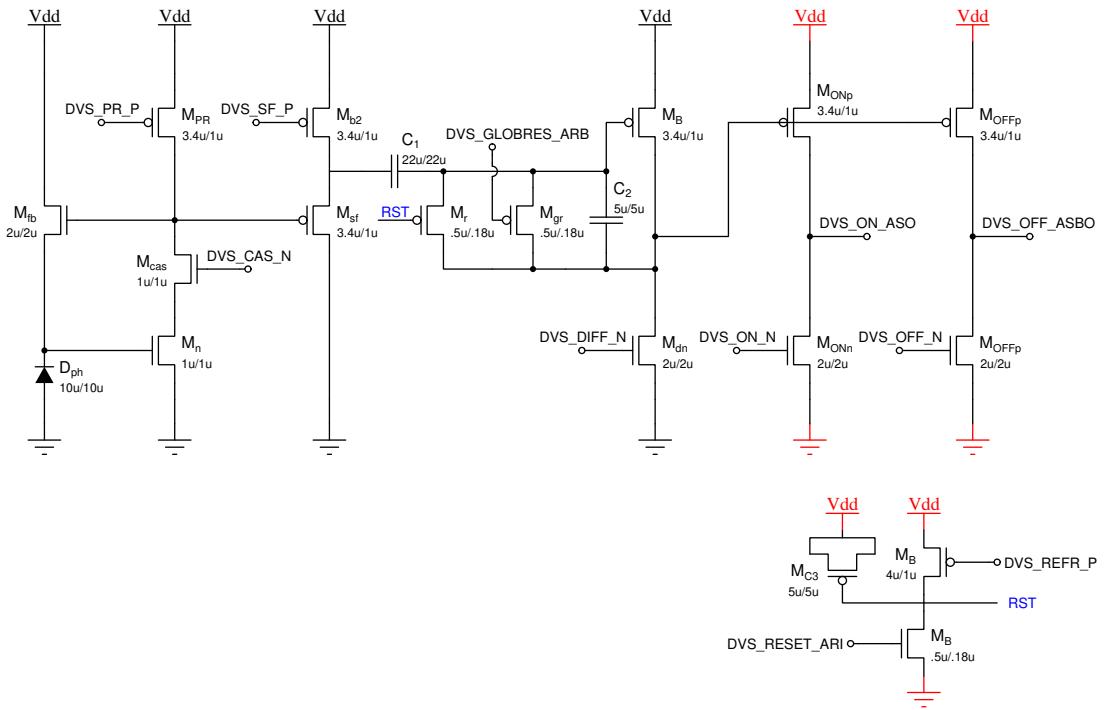


Figure 63: DVS pixel schematic. Where indicated in red, dGND & dVDD are used.

### 3.21.2 Simulations

A single transient analysis was run, showing the input  $I_{ph}$ , intermediate circuit voltages  $V_{log}$  &  $V_{rst}$  and the outputs  $V_{off}$  &  $V_{on}$ . The diode was replaced with a piece-wise current source, which was swept to show the behaviour of the circuit in different equivalent light conditions (that is to say: continuously more light; continuously same light; and continuously less light). The following circuit biases were used:  $I_b = 100nA$ ;  $I_{cas} = 8nA$ ;  $I_{diff} = 60nA$ ;  $I_{off} = 5nA$ ;  $I_{on} = 200nA$ ;  $I_{pr} = 1nA$ ;  $I_{refr} = 4.4nA$  &  $I_{sf} = 2nA$ . GLOBRES was set OFF.

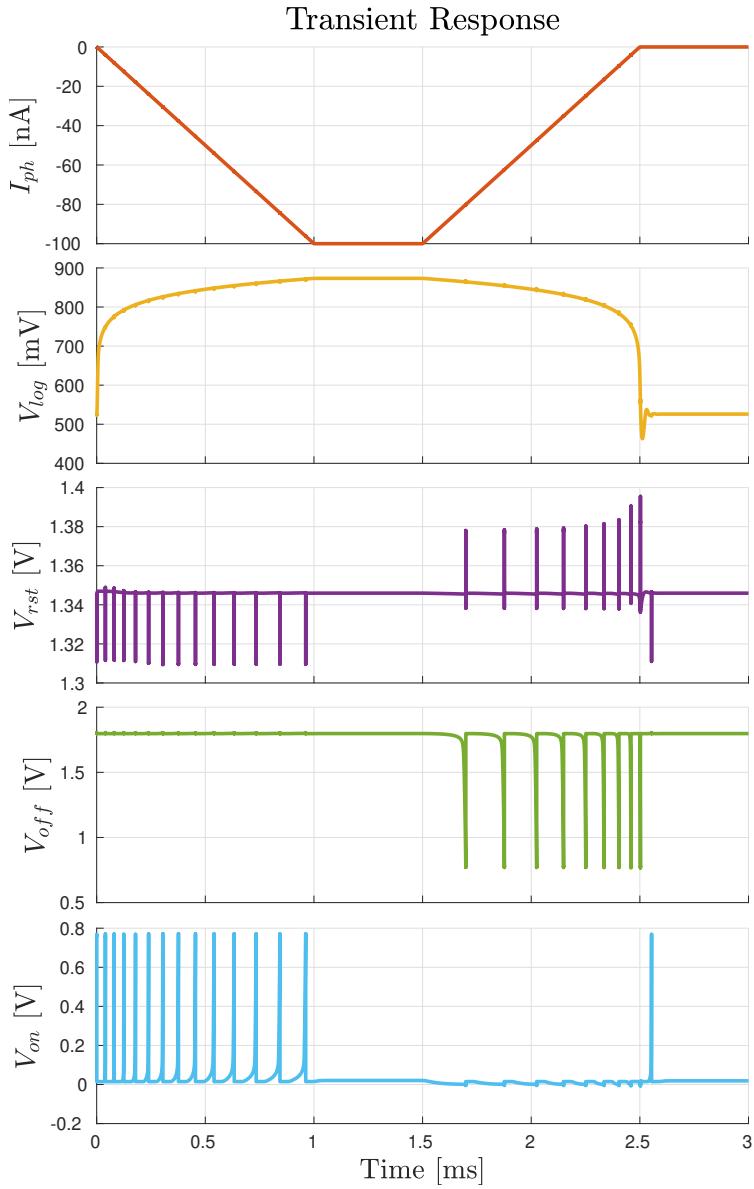
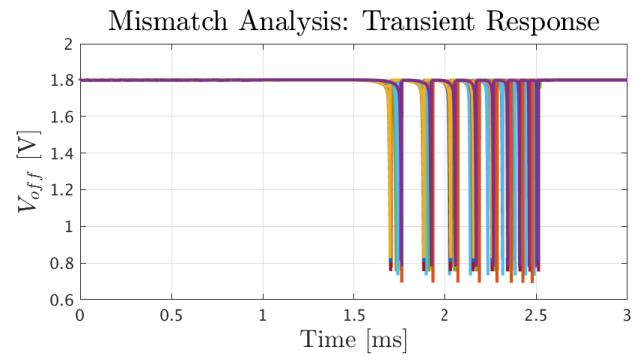


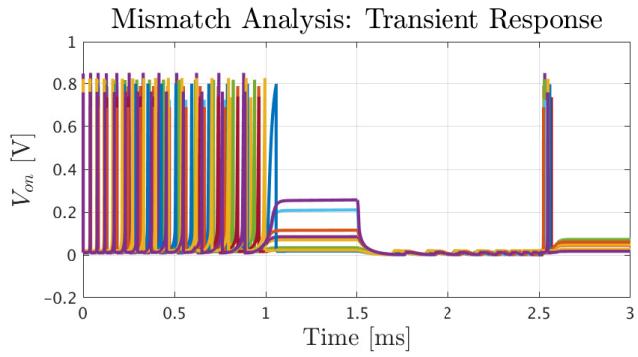
Figure 64: measurements of internal circuit voltages  $V_{log}$  &  $V_{rst}$  and outputs  $V_{off}$  &  $I_{on}$  as the input current  $I_{ph}$  changes over time.

### 3.21.3 Mismatch Analysis

A mismatch analysis was performed using the simulation setup above. As events/spikes are difficult to provide a statistical analysis of variation on, a subsection of the raw mismatch data is provided, for qualitative observation. Analysis results are shown in Figure 65. Primarily, we observe that the amplitude of the outputs is affected, as well as the refractory of the response. In the case of the  $V_{on}$ , we observe that for some variations the biases used don't permit full spikes be produced.



(a)



(b)

Figure 65: Mismatch analysis of the DVS pixel circuit, observing variations in outputs (a)  $V_{off}$  and (b)  $V_{on}$ .

## 3.22 Second-Order Section

### 3.22.1 Description

The second-order section is a circuit which generates sinusoidal responses. It consists of two degenerative transamps in feedforward, and one N-type 5T transamp in feedback. The circuit has a single input  $V_{in}$ , two input biases  $V_{b1}$  &  $V_{b2}$ , and outputs two voltages  $V_{s1}$  &  $V_{s2}$ . A schematic of the circuit is shown in Figure 66. Capacitor sizing for  $C_1$  &  $C_2$  was chosen to give a capacitance of  $2pF$  each.

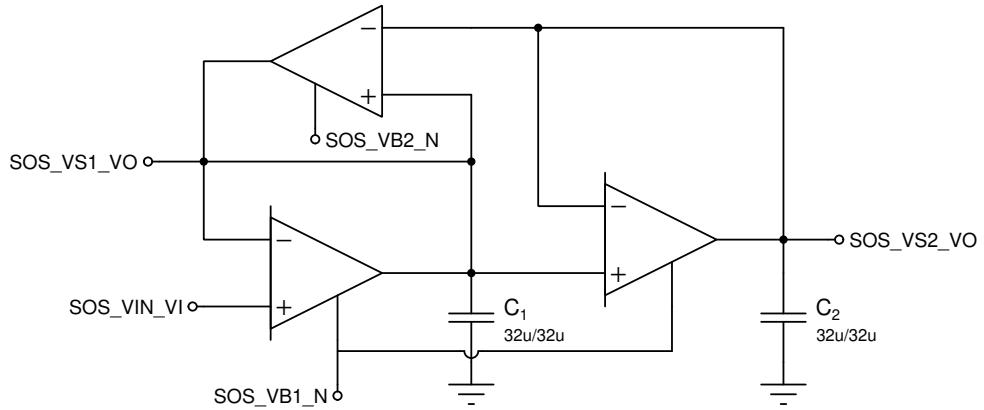


Figure 66: Second-order section schematic.

### 3.22.2 Simulations

A short input pulse was fed into the circuit, with bias parameters set to  $I_{b1} = 1nA$  &  $I_{b2} = 750pA$ , while output responses  $V_{s1}$   $V_{s2}$  were observed. Plots of the first simulation are shown in Figure 67. In the second and third simulations,  $I_{b1}$  and  $I_{b2}$  were varied respectively. Plots of these simulations are shown in Figure 68.

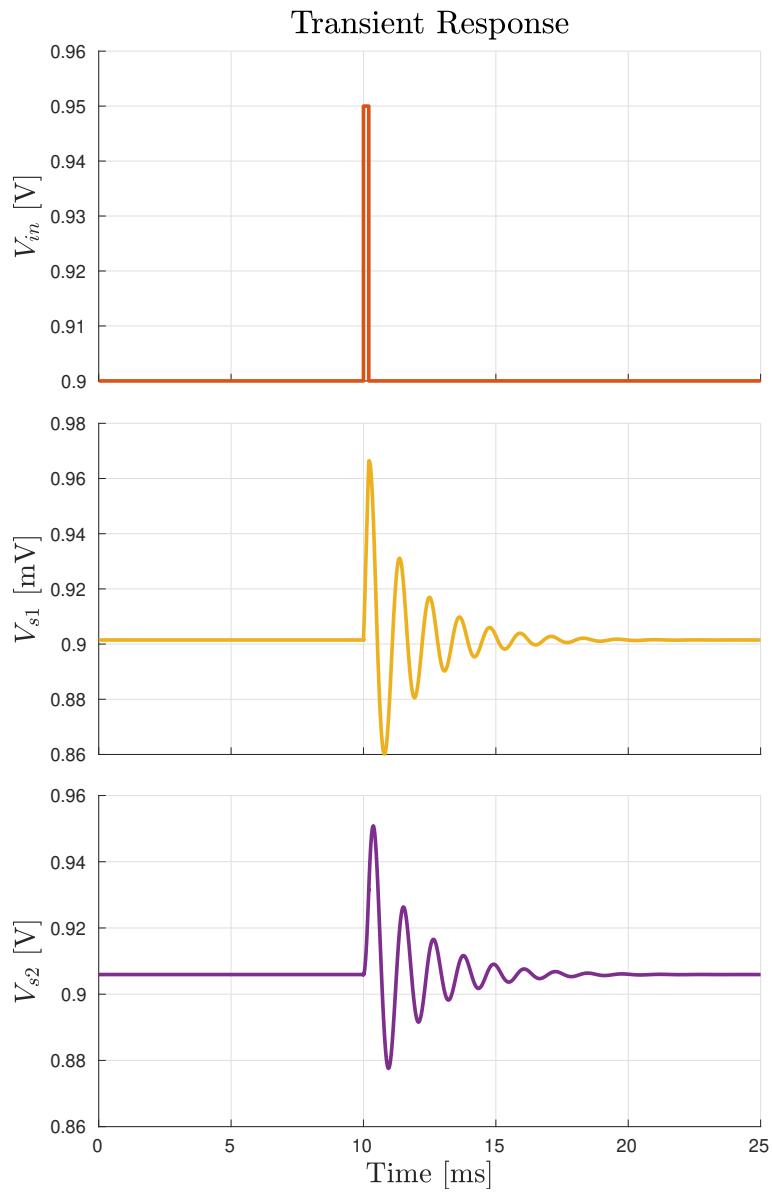


Figure 67: measurements of output voltages  $V_{out1}$  &  $V_{out2}$  resulting from a given input pulse  $V_{in}$ .

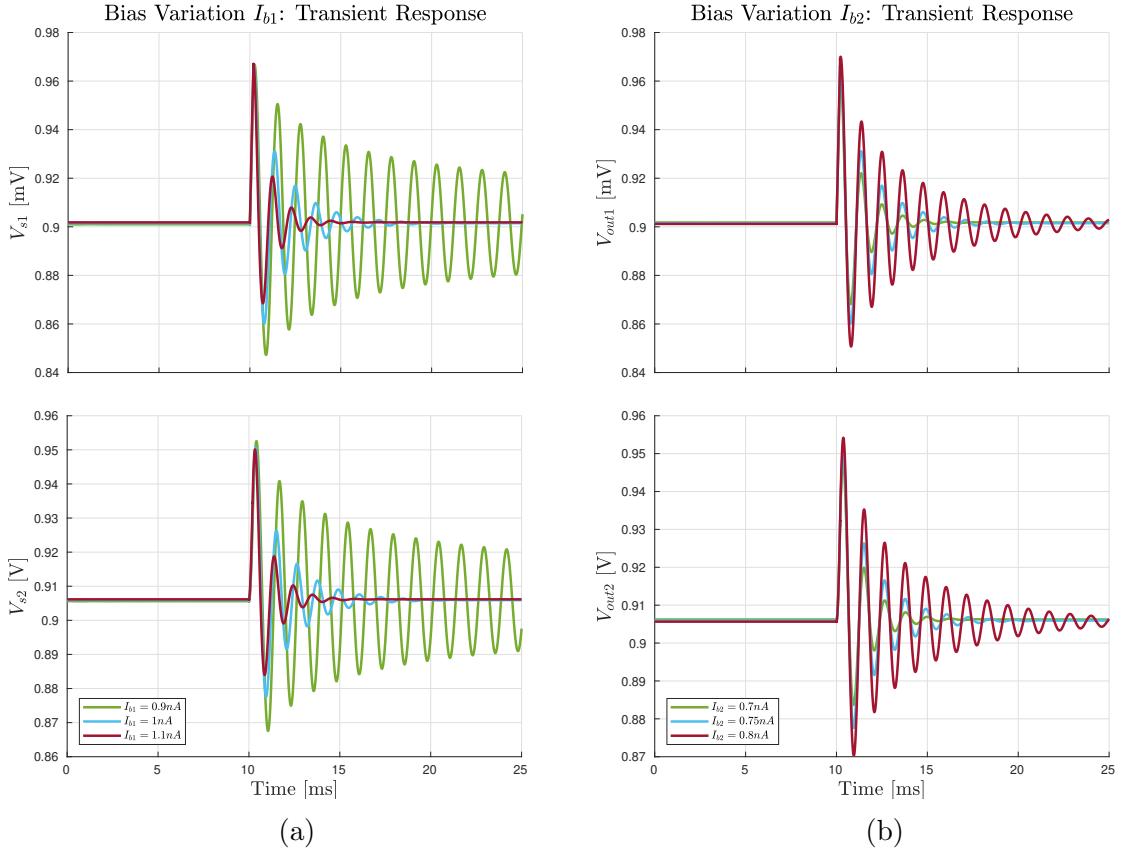


Figure 68: measurements of output voltages  $V_{out1}$  &  $V_{out2}$  for variations in bias parameters (a)  $I_{b1}$  and (b)  $I_{b2}$ .

### 3.22.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup, observing only  $V_{s1}$ . As simulation statistics were difficult to obtain, a subsection of the raw mismatch data is provided. As observed, the circuit is highly susceptible to mismatch, either flat-lining or bouncing between the rails, regardless of bias settings used. This is to be expected, as the circuit is unstable by nature given its feedback. It is therefore advised that biases will need to be carefully selected, as those utilized in the simulations are likely to not work for actual implementations.

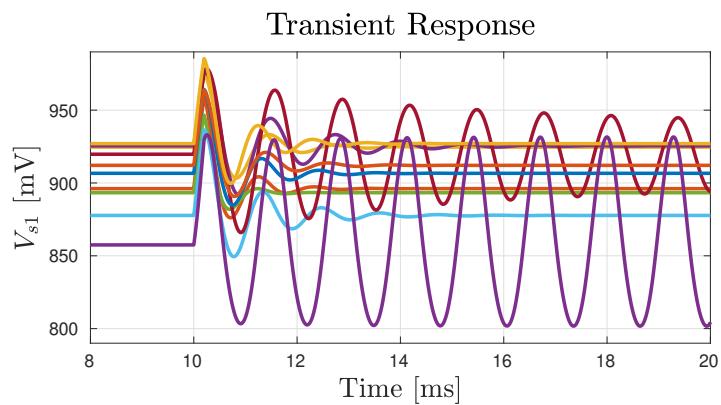


Figure 69: mismatch analysis of the second order section circuit.

## 3.23 Log Domain Synapse

### 3.23.1 Description

The log domain synapse is an AVLSI implementation of a biological synapse, performing an integration operation. The circuit receives a voltage pulse train,  $V_{pulse}$ , as input and outputs a corresponding synaptic current,  $I_{syn}$ . Additionally, the synaptic voltage,  $V_{syn}$ , is provided. Bias parameters  $V_{weight}$  &  $V_{tau}$  affect the amplitude and decay of the response.

The output current is mirrored 6 times, to provide output externally and to the 5 neuron circuits. These mirror transistors are very wide, to account for the low conductance of this synapse implementation. The increased sizing of  $M_{weight}$  &  $M_{tau}$  is to mitigate mismatch effects.  $C_{syn}$  sizing was chosen for a capacitance of  $2pF$ . A schematic of the circuit is shown in Figure 70.

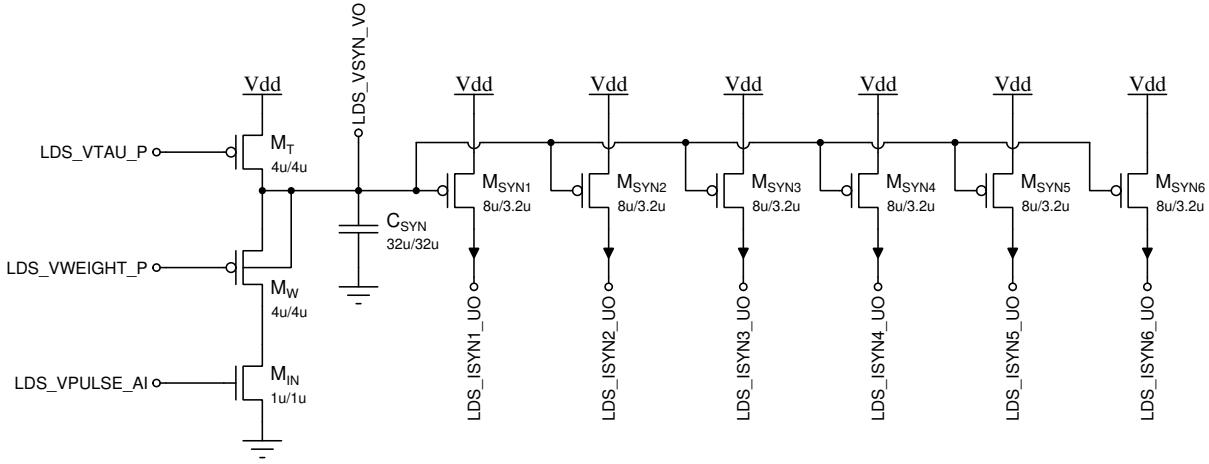


Figure 70: Log domain synapse schematic.

### 3.23.2 Simulations

A transient analysis was performed, with an input pulse  $V_{pulse}$  of width  $100\mu s$  and period  $10ms$  provided, and outputs  $V_{syn}$  &  $I_{syn}$  observed. In the first simulation,  $I_{tau} = 100pA$  &  $I_{weight} = 500nA$ . In the second simulation,  $I_{weight}$  is varied, while in the third simulation  $I_{tau}$  is. Simulation results are shown in Figures 71 & 72.

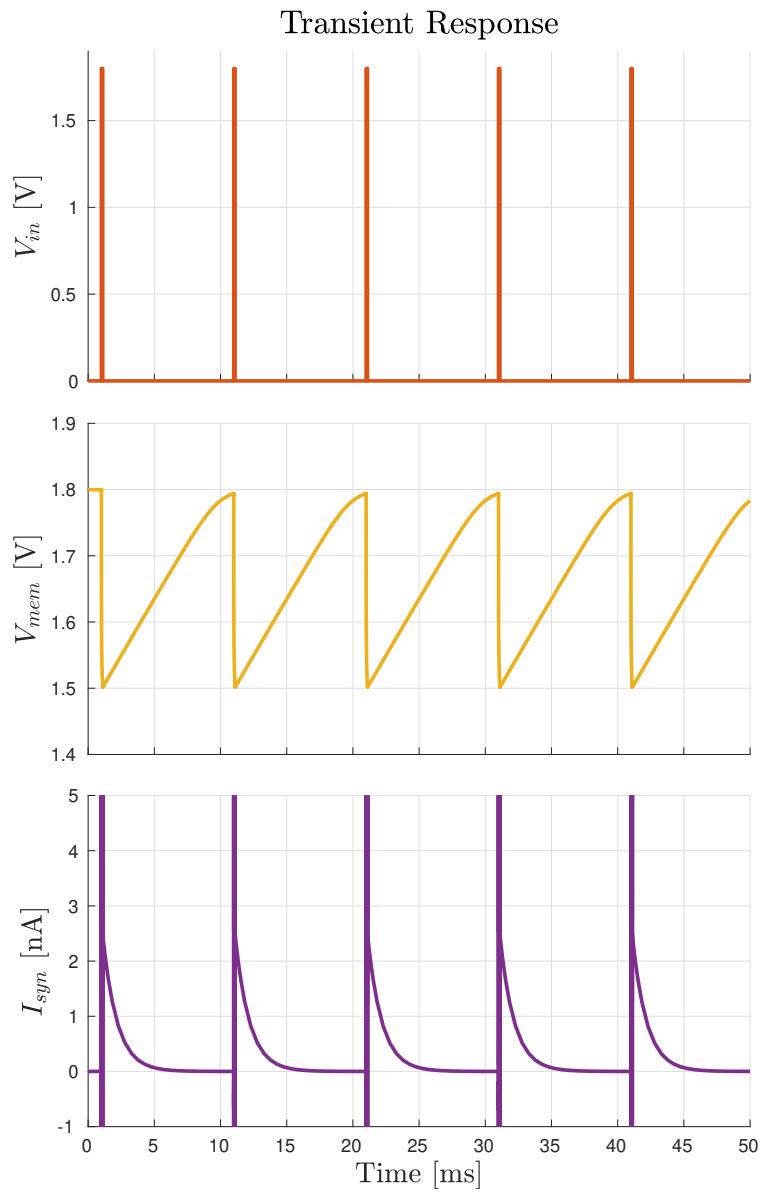


Figure 71: measurements of output voltage  $V_{mem}$  & output current  $I_{syn}$  resulting from a given input pulse train  $V_{in}$ .

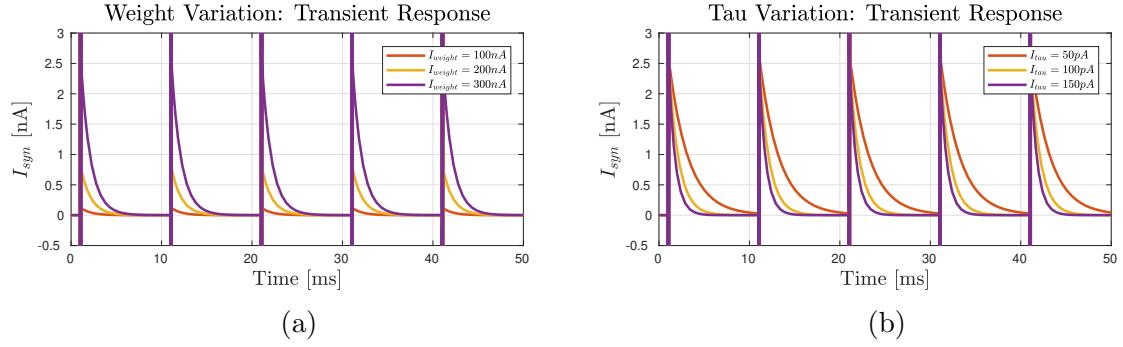


Figure 72: measurements of output current  $I_{syn}$  for variations in bias parameters (a)  $I_{weight}$  and (b)  $I_{tau}$ .

### 3.23.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup, but with  $I_{tau} = 25\text{pA}$ . Most variation appears to be in the response amplitude. Analysis results are shown in Figure 73.

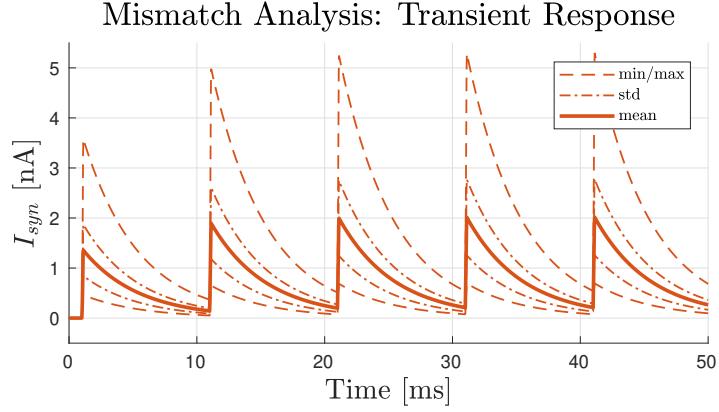


Figure 73: mismatch analysis of the log domain synapse circuit.

## 3.24 DPI Synapse

### 3.24.1 Description

The DPI (Differential-Pair Integrator) synapse is an AVLSI implementation of a biological synapse, performing an integration operation [2]. It extends the log-domain synapse, by using a differential-pair to provide a third bias,  $V_{thr}$  to increase the amplitude of the response. The circuit receives a voltage pulse train,  $V_{pulse}$ , as input and outputs a corresponding synaptic current,  $I_{syn}$ . Additionally, the synaptic voltage,  $V_{syn}$ , is provided.

Bias parameters  $V_{weight}$  &  $V_{tau}$  affect the amplitude and decay of the response, while  $V_{thr}$  acts as an additional weight bias. The output current is mirrored 6 times, to provide output externally and to the 5 neuron circuits. The increased sizing of  $M_{weight}$  &  $M_{tau}$ , as well as the output devices, is to mitigate mismatch effects.  $C_{syn}$  sizing was chosen for a capacitance of  $2pF$ . A schematic of the circuit is shown in Figure 74.

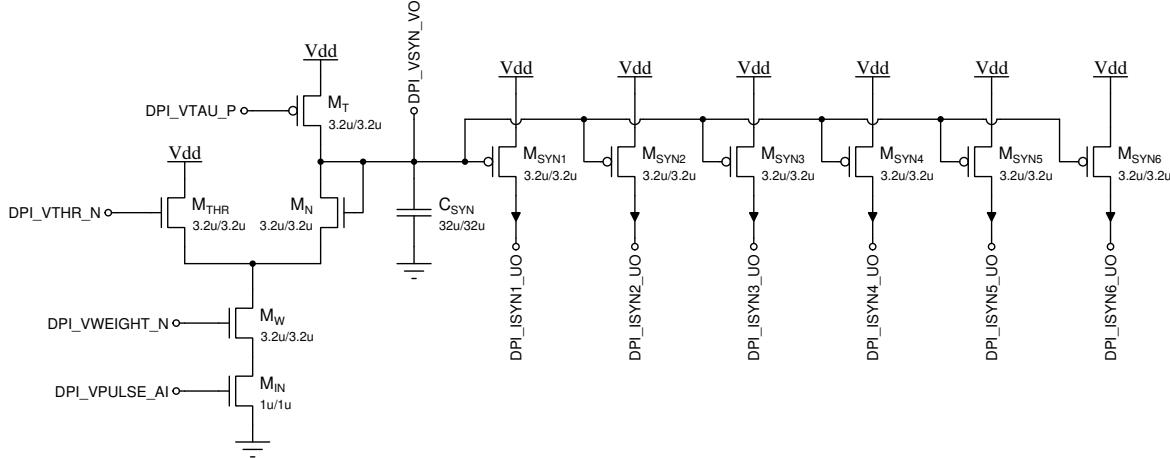


Figure 74: DPI synapse schematic.

### 3.24.2 Simulations

A transient analysis was performed, with an input pulse  $V_{pulse}$  of width  $1ms$  and period  $10ms$  provided, and outputs  $V_{syn}$  &  $I_{syn}$  observed. In the first simulation,  $I_{tau} = 100pA$ ,  $I_{thr} = 1nA$  &  $I_{weight} = 100nA$ . In the second simulation,  $I_{weight}$  is varied, while in the third simulation  $I_{tau}$  is. Simulation results are shown in Figures 75 & 76.

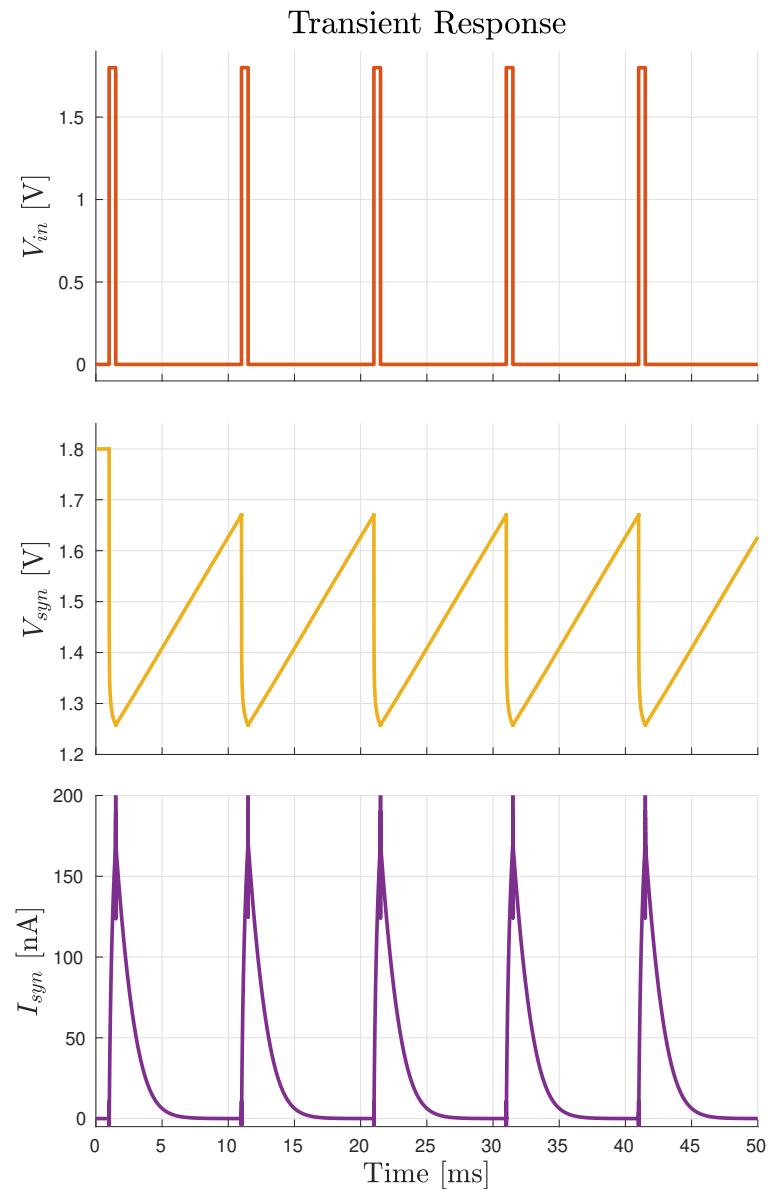


Figure 75: measurements of output voltage  $V_{mem}$  & output current  $I_{syn}$  resulting from a given input pulse train  $V_{in}$ .

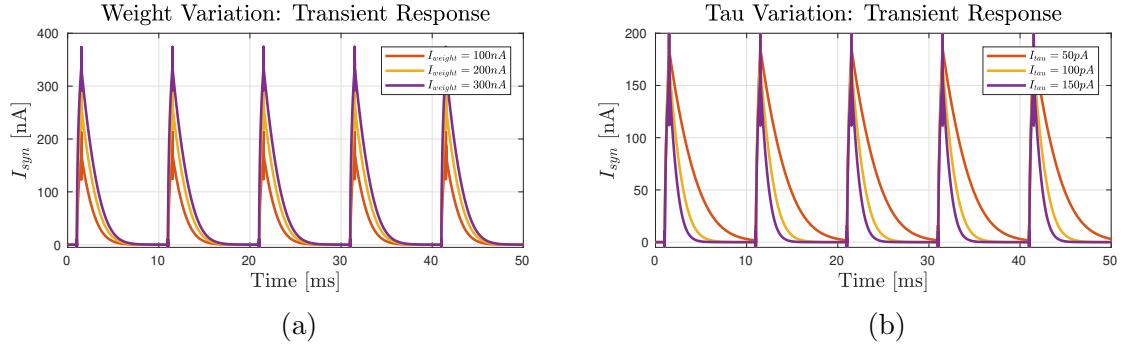


Figure 76: measurements of output current  $I_{syn}$  for variations in bias parameters (a)  $I_{weight}$  and (b)  $I_{tau}$ .

### 3.24.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup, but with  $I_{tau} = 25pA$ . The circuit appears quite robust to mismatch, compared to the log domain synapse. Most variation appears to be in the response amplitude. Analysis results are shown in Figure 77.

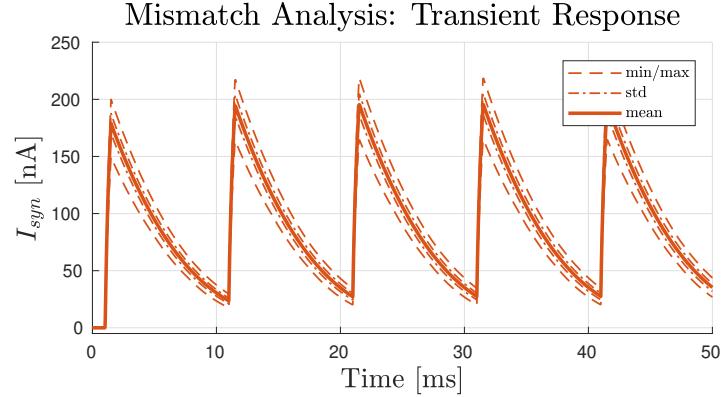


Figure 77: mismatch analysis of the DPI synapse circuit.

## 3.25 Dual-DPI Synapse

### 3.25.1 Description

The Dual-DPI (Differential-Pair Integrator) synapse is an AVLSI implementation of a biological synapse, performing an integration operation. It consists of two DPI synapses, one excitatory and the other inhibitory [3]. Both branches receive the same voltage pulse train,  $V_{pulse}$ , as input and outputs a corresponding synaptic current,  $I_{syn}$ . Additionally, the synaptic voltages,  $V_{exsyn}$  &  $V_{inhsyn}$ , are provided.

Bias parameters  $V_{weight}$  &  $V_{tau}$  affect the amplitude and decay of the response, while  $V_{thr}$  acts as an additional weight bias (the bias inputs of both branches are tied together). The output current is mirrored 6 times, to provide output externally and to the 5 neuron circuits. The increased sizing of  $M_{weight}$  &  $M_{tau}$ , as well as the output devices, is to mitigate mismatch effects.  $C_{exsyn}$  sizing was chosen for a capacitance of  $2pF$  and  $C_{inhsyn} = 0.7C_{exsyn}$ . A schematic of the circuit is shown in Figure 78.

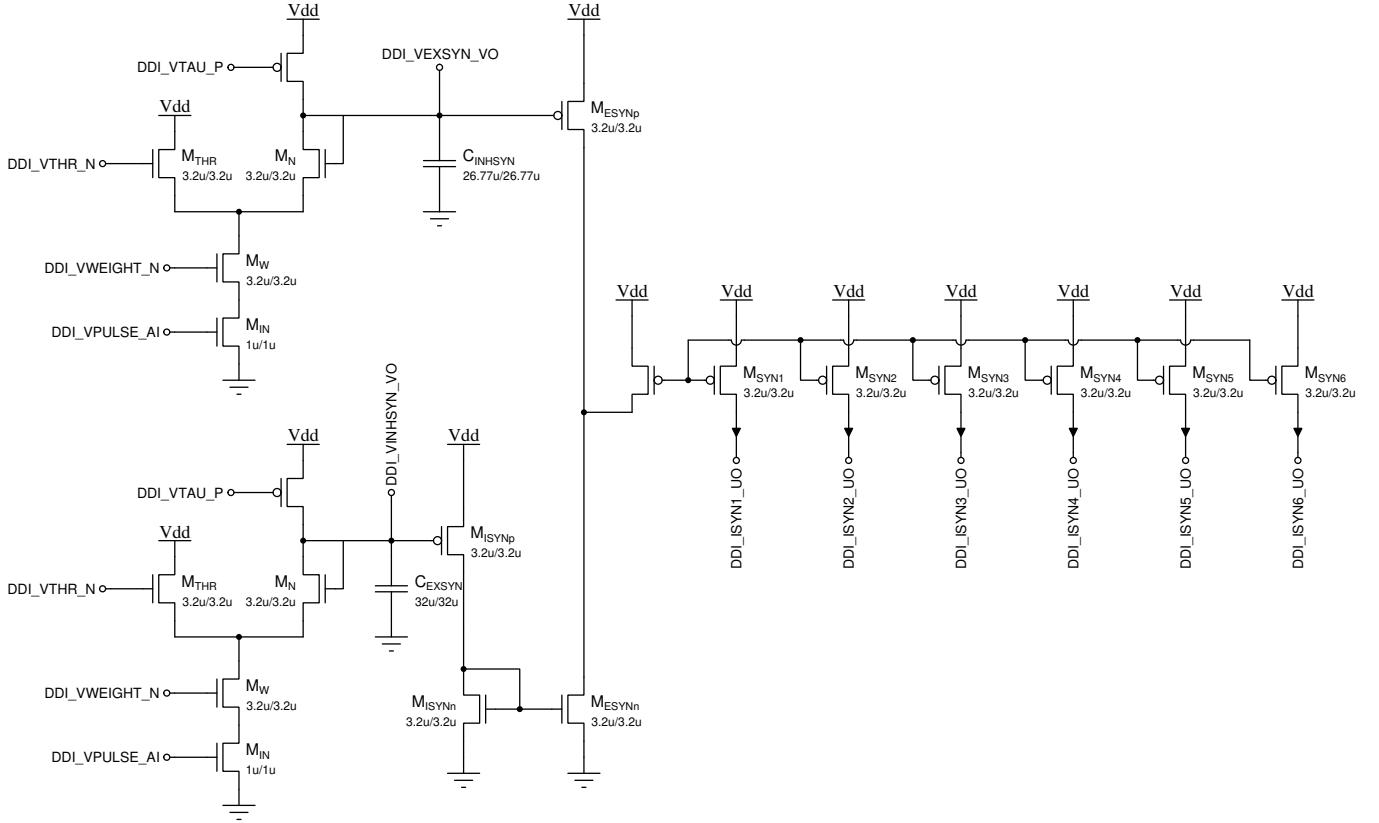


Figure 78: Dual-DPI synapse schematic.

### 3.25.2 Simulations

A transient analysis was performed, with an input pulse  $V_{pulse}$  of width  $1ms$  and period  $10ms$  provided, and outputs  $V_{exsyn}$ ,  $V_{inhsyn}$  &  $I_{syn}$  observed. In the first simulation,

$I_{tau} = 100\text{pA}$ ,  $I_{thr} = 1\text{nA}$  &  $I_{weight} = 100\text{nA}$ . In the second simulation,  $I_{weight}$  is varied, while in the third simulation  $I_{tau}$  is. Simulation results are shown in Figures 79 & 80.

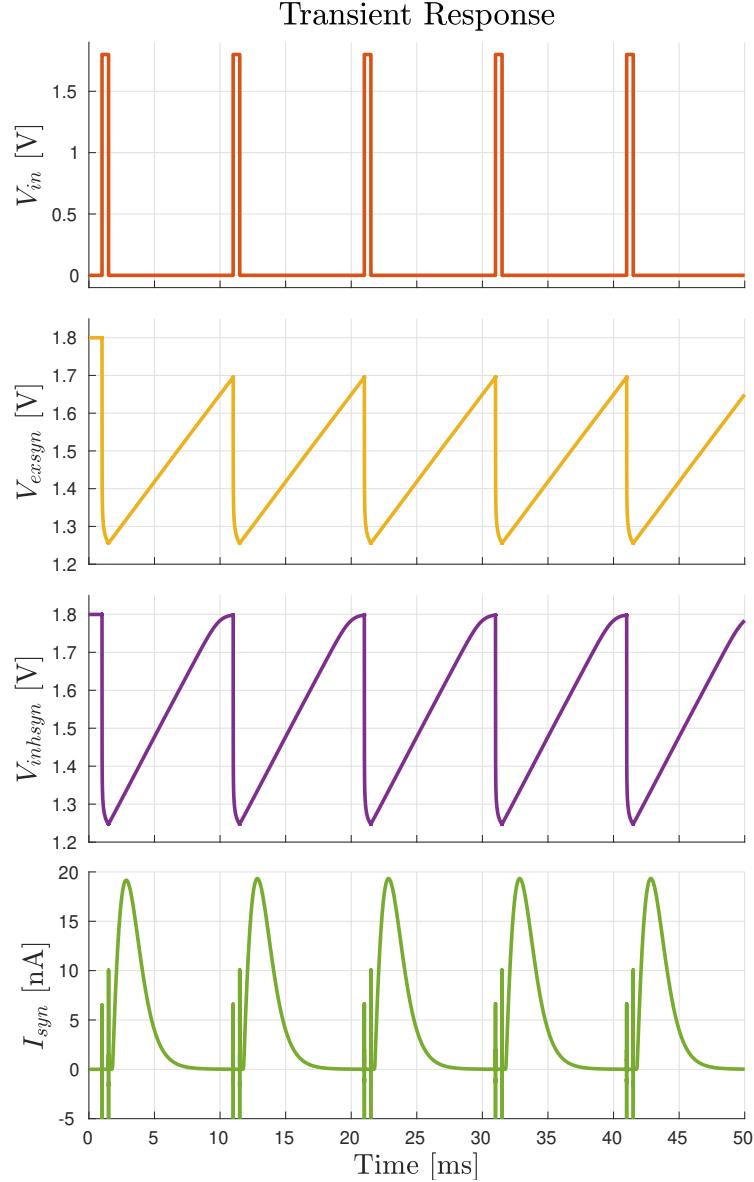


Figure 79: measurements of output voltages  $V_{exsyn}$  &  $V_{inhsyn}$  and output current  $I_{syn}$ , resulting from a given input pulse train  $V_{in}$ .

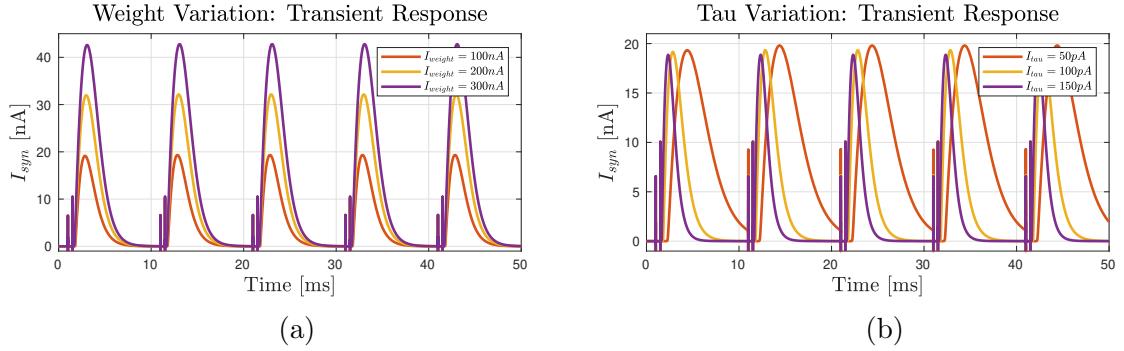


Figure 80: measurements of output current  $I_{syn}$  for variations in bias parameters (a)  $I_{weight}$  and (b)  $I_{tau}$ .

### 3.25.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup, but with  $I_{tau} = 50pA$ . Most variation appears to be in the response amplitude. Analysis results are shown in Figure 81.

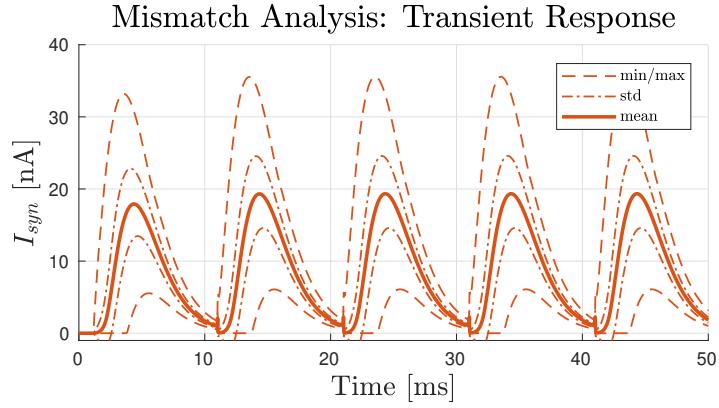


Figure 81: mismatch analysis of the dual-DPI synapse circuit.

## 3.26 Axon-Hillock IF Neuron

### 3.26.1 Description

The Axon-Hillock IF (Integrate & Fire) neuron is an AVLSI implementation of a biological synapse, performing a differentiation operation. The circuit receives an input current  $I_{in}$  (typically the output of a synapse,  $I_{syn}$ ) and outputs an AER event. Additionally, the membrane voltage  $V_{mem}$  is provided as output.

The circuit has a single bias parameter,  $V_{pw}$ , which affects the rate of response.  $C_m$  &  $C_{fb}$  sizing was chosen for capacitance values  $2pF$  & approx.  $1pF$  respectively. A schematic of the circuit is shown in Figure 82. The circuit was modified to provide and accept AER REQ & ACK events.

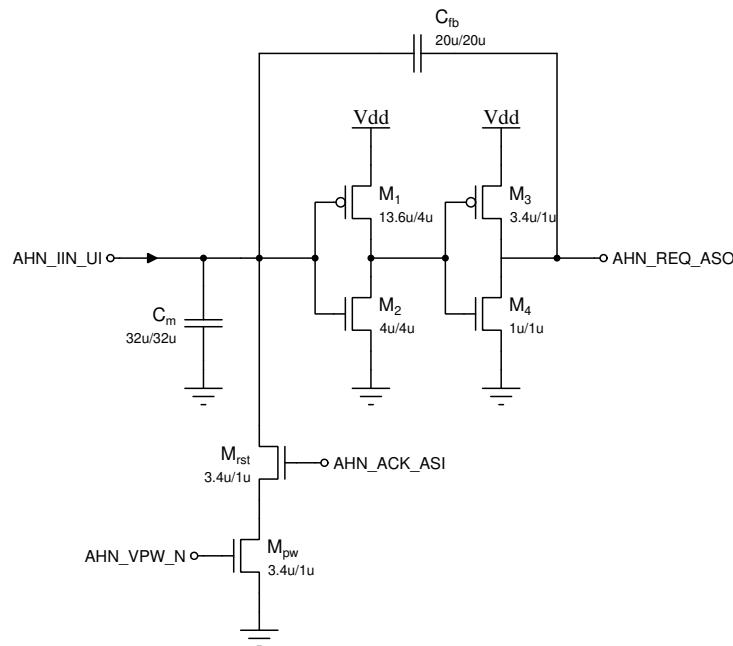


Figure 82: Axon-Hillock neuron schematic.

### 3.26.2 Simulations

A transient analysis was done, with a DC input current of  $I_{in} = 1nA$  provided. For the first simulation,  $I_{pw} = 2nA$  and was varied in the second simulation. Simulation plots are shown in Figure 83.

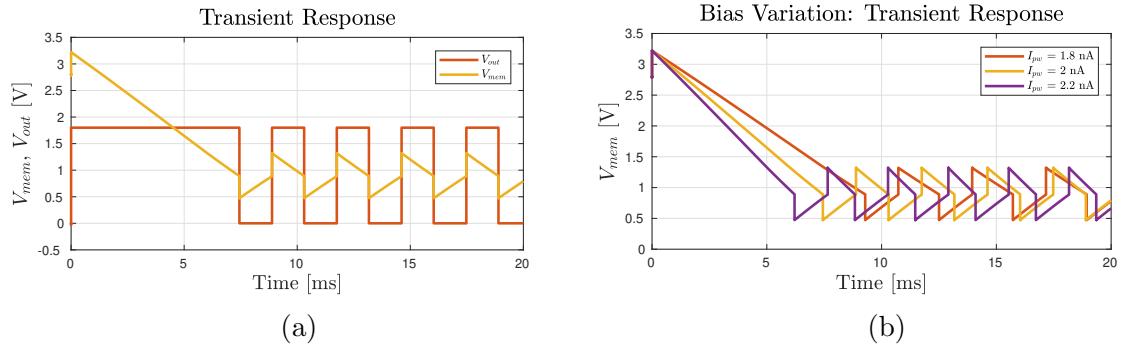


Figure 83: measurements of output voltages  $V_{mem}$ , (a) showing  $V_{out}$  and (b) with variation in bias  $I_{pw}$ .

### 3.26.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup. As statistics of the variation was difficult to provide, a subsection of the raw mismatch data is provided. Most variation is observed in the rate of response. Analysis results are shown in Figure 84.

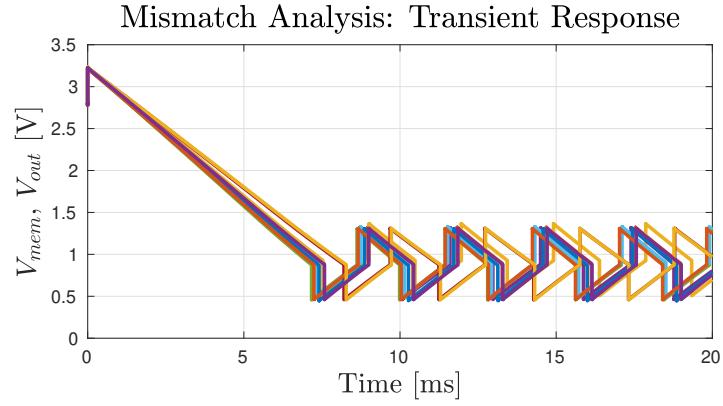


Figure 84: mismatch analysis of the Axon-Hillock neuron circuit.

## 3.27 ADEXIF Classic Neuron

### 3.27.1 Description

The ADEXIF (Adaptive Exponential Integrate & Fire) classic neuron is the original implementation of this neuron circuit [4]. The neuron comprises four major functional blocks: a leak DPI, starved-inverter, refractory and adaptation. The adaptation block receives an input pulse through a pulse extender circuit, as described in the appendix. The circuit receives an input current  $I_{in}$  (typically the output of a synapse,  $I_{syn}$ ) and outputs an AER event. Additionally, the membrane voltage  $V_{mem}$  is provided to observe the internal neuron state.

The circuit has 9 input biases:  $V_{dc}$ ,  $V_{gain}$ ,  $V_{leak}$ ,  $V_{refr}$ ,  $V_{adpgain}$ ,  $V_{adpweight}$ ,  $V_{adptau}$ ,  $V_{adpcasc}$  &  $V_{adpptau}$  (for the pulse extender), and two mode lines:  $V_{adpen}$  to enable/disable adaptation, and  $V_{dcen}$  to enable/disable the  $V_{dc}$  bias input.

FET device sizing was inherited from a previous implementation, and tweaked to mitigate mismatch.  $C_m$  sizing was chosen for a capacitance value of  $2pF$ , while  $C_{refr}$  &  $C_{adp}$  were chosen for a value of  $1pF$ . A schematic of the circuit is shown in Figure 85. Note that the input to  $M_{rst}$  in the leak DPI block has been tied to GND, enabling it.

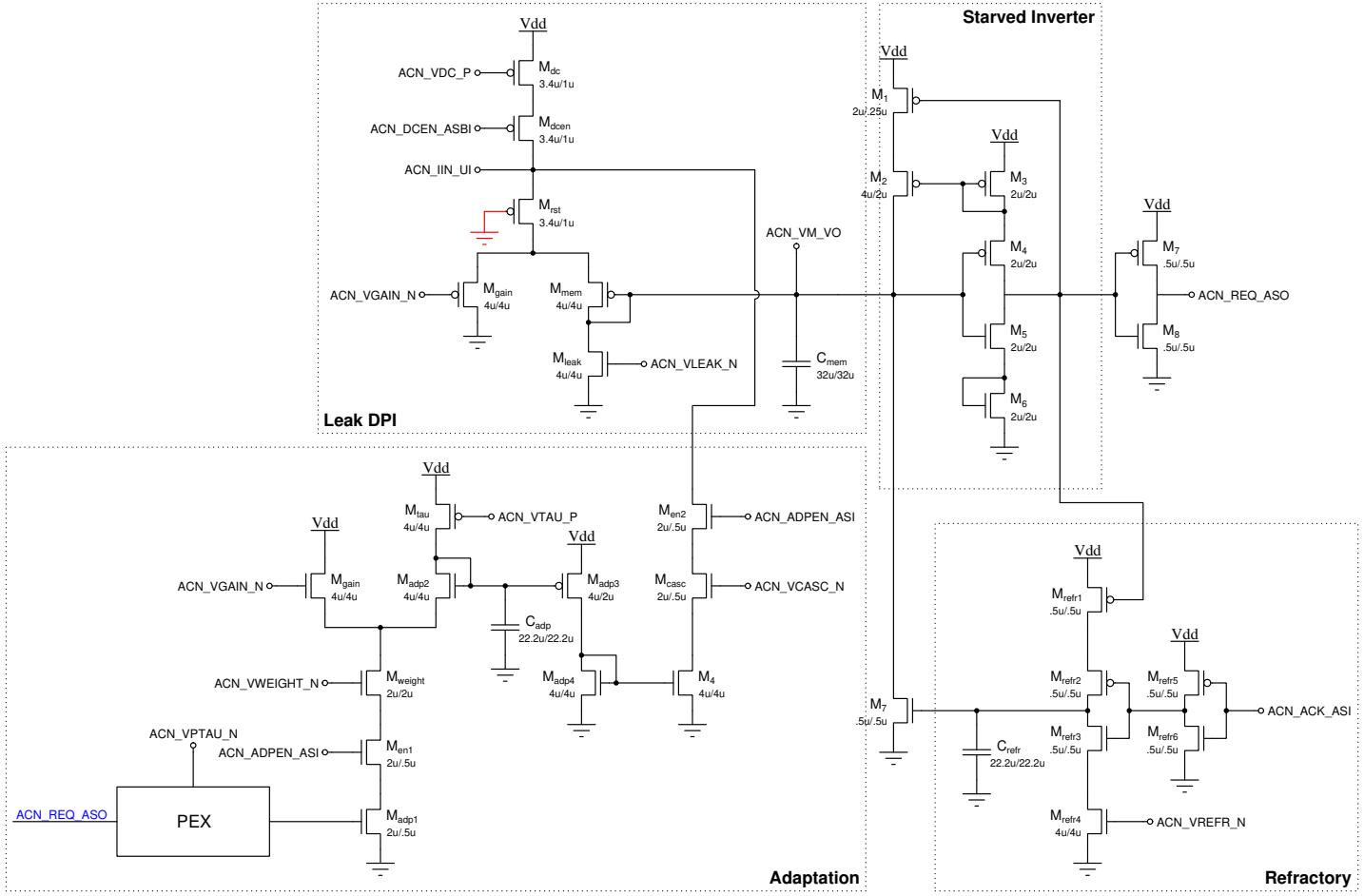


Figure 85: ADEXIF classic neuron schematic. Where indicated in red, the input is pulled down to GND.

### 3.27.2 Simulations

A transient analysis was done, with a DC input current of  $I_{in} = 100\text{pA}$  provided.  $V_{dcen}$  &  $V_{adpen}$  were tied to GND, enabling/disabling them respectively. Biases were set as follows:  $I_{dc} = 110\text{pA}$ ,  $I_{gain} = 8\text{nA}$ ,  $I_{leak} = 20\text{pA}$ ,  $I_{refr} = 100\text{pA}$ ,  $I_{adpgain} = I_{adpweight} = I_{adptau} = I_{adpcasc} = I_{adpptau} = 0$ . In the second simulation,  $I_{refr}$  was varied, while in the third simulation  $I_{gain}$  was. Simulation plots are shown in Figure 86.

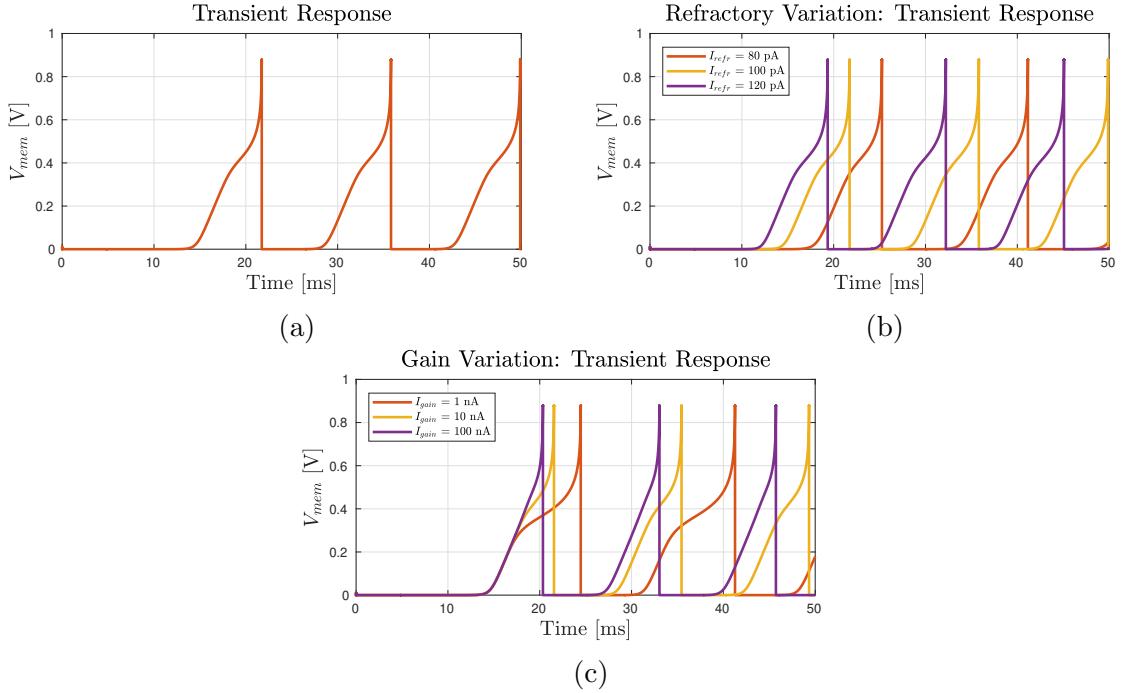


Figure 86: (a) measurements of the membrane voltage  $V_{mem}$  (b) variation of refractory bias  $I_{refr}$  (b) variation of gain bias  $I_{gain}$ .

### 3.27.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup. A subsection of the mismatch data is provided. Variation in rate and width of response is observed. Analysis results are shown in Figure 87.

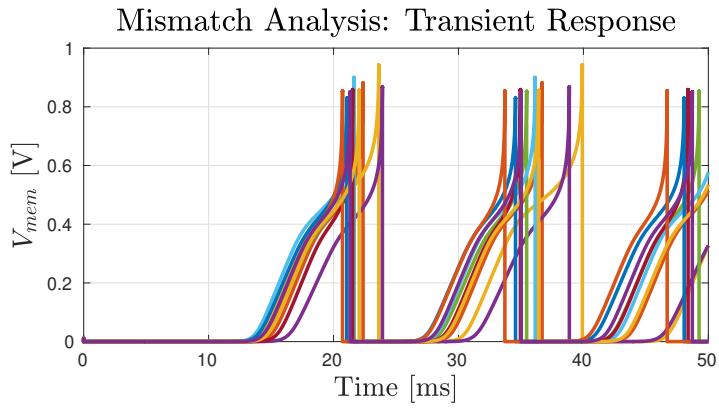


Figure 87: mismatch analysis of the ADEXIF classic neuron circuit.

## 3.28 ADEXIF Thresholded Neuron

### 3.28.1 Description

The ADEXIF (Adaptive Exponential Integrate & Fire) thresholded neuron is a modified implementation of the ADEXIF Classic neuron [5]. The neuron comprises four major functional blocks: a leak DPI, current comparator, refractory and adaptation. The use of a current comparator instead of a starved inverter results in a much lower power draw. The adaptation block receives an input pulse through a pulse extender circuit, as described in the appendix. The circuit receives an input current  $I_{in}$  (typically the output of a synapse,  $I_{syn}$ ) and outputs an AER event. Additionally, the membrane voltage  $V_{mem}$  is provided to observe the internal neuron state.

The circuit has 10 input biases:  $V_{dc}$ ,  $V_{gain}$ ,  $V_{leak}$ ,  $V_{refr}$ ,  $V_{spkthr}$ ,  $V_{cc}$ ,  $V_{adpgain}$ ,  $V_{adpweight}$ ,  $V_{adptau}$ ,  $V_{adpcasc}$  &  $V_{adpptau}$  (for the pulse extender), and two mode lines:  $V_{adpen}$  to enable/disable adaptation, and  $V_{dcen}$  to enable/disable the  $V_{dc}$  bias input.

FET device sizing was inherited from a previous implementation, and tweaked to mitigate mismatch.  $C_m$  sizing was chosen for a capacitance value of  $2pF$ , while  $C_{refr}$  &  $C_{adp}$  were chosen for a value of  $1pF$ . A schematic of the circuit is shown in Figure 88. Note that the input to  $M_{cc1}$  in the current comparator block has been tied to VDD, disabling it.

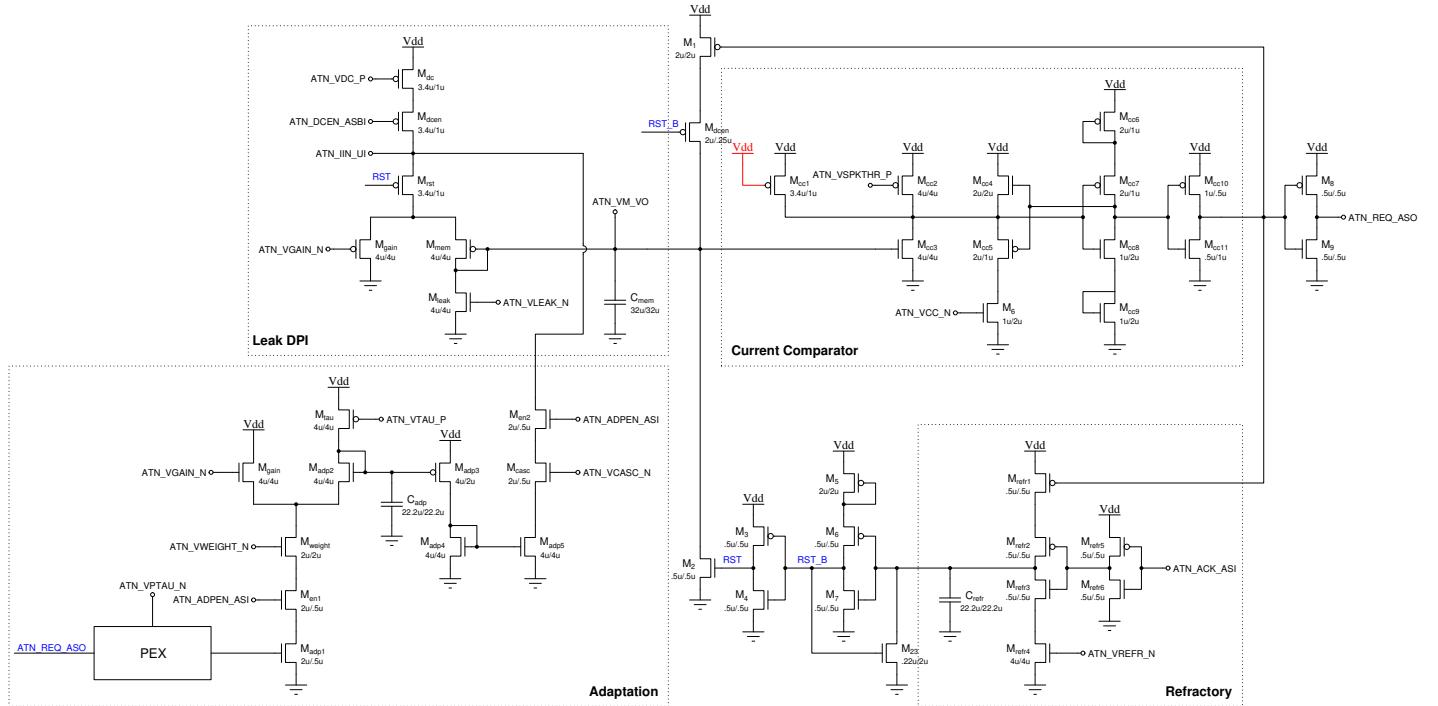


Figure 88: ADEXIF thresholded neuron schematic. Where indicated in red, the input is pulled up to VDD.

### 3.28.2 Simulations

A transient analysis was done, with a DC input current of  $I_{in} = 100\text{pA}$  provided.  $V_{dcen}$  &  $V_{adpen}$  were tied to GND, enabling/disabling them respectively. Biases were set as follows:  $I_{dc} = 110\text{pA}$ ,  $I_{gain} = 5\text{nA}$ ,  $I_{leak} = 20\text{pA}$ ,  $I_{refr} = 100\text{pA}$ ,  $I_{spkthr} = 5\text{nA}$ ,  $I_{cc} = 100\text{pA}$ ,  $I_{adpgain} = I_{adpweight} = I_{adptau} = I_{adpcasc} = I_{adpptau} = 0$ . In the second simulation,  $I_{refr}$  was varied, while in the third simulation  $I_{gain}$  was. Simulation plots are shown in Figure 89.

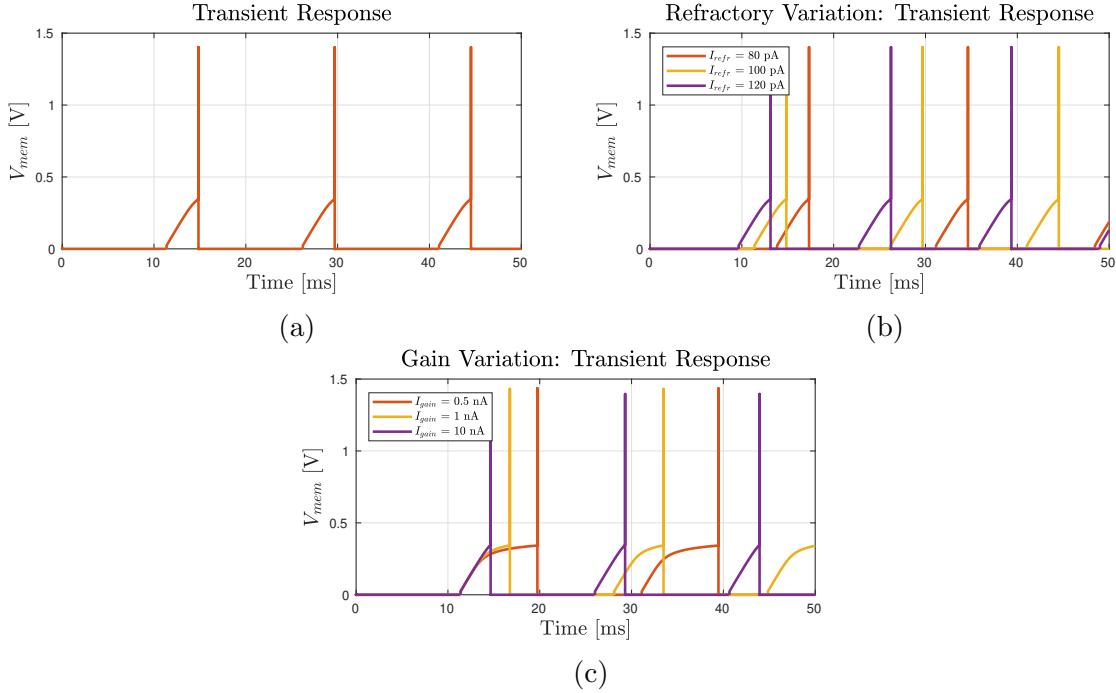


Figure 89: (a) measurements of the membrane voltage  $V_{mem}$  (b) variation of refractory bias  $I_{refr}$  (b) variation of gain bias  $I_{gain}$ .

### 3.28.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup. A subsection of the mismatch data is provided. Variation in rate and width of response is observed. Analysis results are shown in Figure 90.

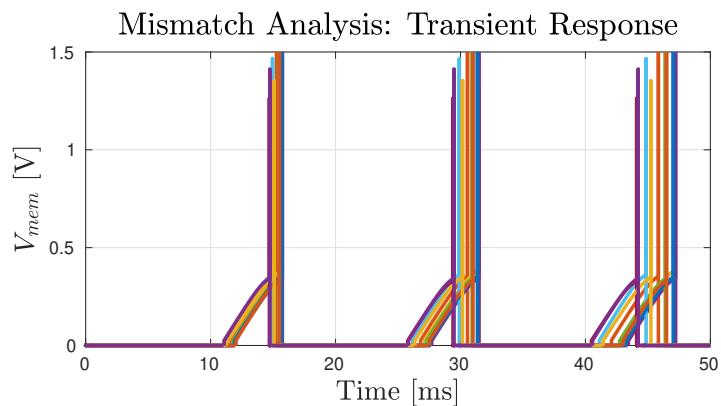


Figure 90: mismatch analysis of the ADEXIF thresholded neuron circuit.

## 3.29 ADEXIF Sigma-Delta Neuron

### 3.29.1 Description

The ADEXIF (Adaptive Exponential Integrate & Fire) thresholded neuron is a modified implementation of the ADEXIF Thresholded neuron [6]. The neuron comprises three major functional blocks: a leak DPI, current comparator and adaptation. Here the output of the adaptation block is fed back to the leak DPI block, as with the other two implementations. The adaptation block receives an input pulse through a pulse extender circuit, as described in the appendix. The circuit receives an input current  $I_{in}$  (typically the output of a synapse,  $I_{syn}$ ) and outputs an AER event. Additionally, the membrane voltage  $V_{mem}$  is provided to observe the internal neuron state.

The circuit has 11 input biases:  $V_{dc}$ ,  $V_{gain}$ ,  $V_{leak}$ ,  $V_{spkthr}$ ,  $V_{cc}$ ,  $V_{adpgain}$ ,  $V_{adpweight}$ ,  $V_{adptau}$ ,  $V_{adpcasc}$  &  $V_{adpptau}$  (for the pulse extender), and one mode line:  $V_{dcen}$  to enable/disable the  $V_{dc}$  bias input.

FET device sizing was inherited from a previous implementation, and tweaked to mitigate mismatch.  $C_m$  sizing was chosen for a capacitance value of  $2pF$ , while  $C_{adp}$  was chosen for a value of  $1pF$ . A schematic of the circuit is shown in Figure 91. Note that the inputs to  $M_{en1}$  &  $M_{en2}$  in the adaptation block have been tied to VDD, enabling it. The circuit was modified to provide and accept AER REQ & ACK events in a similar manner to the other two ADEXIF implementations.

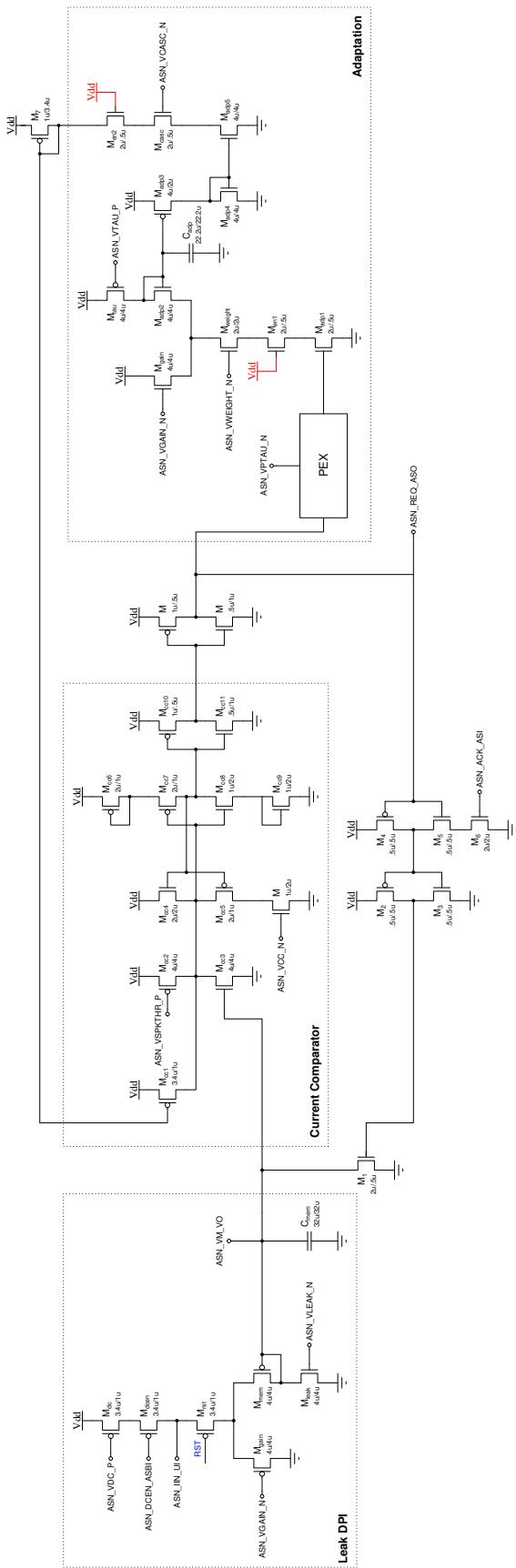


Figure 91: ADEXIF sigma-delta neuron schematic. Where indicated in red, the input is pulled up to VDD

### 3.29.2 Simulations

A transient analysis was done, with a DC input current of  $I_{in} = 150\text{pA}$  provided.  $V_{dcen}$  was tied to GND, enabling it. Biases were set as follows:  $I_{dc} = 0$ ,  $I_{gain} = 1.1\text{nA}$ ,  $I_{leak} = 20\text{pA}$ ,  $I_{spkthr} = 5\text{nA}$ ,  $I_{cc} = 100\text{pA}$ ,  $I_{adpgain} = 1\text{nA}$ ,  $I_{adpweight} = 100\text{nA}$ ,  $I_{adptau} = 1\text{nA}$ ,  $I_{adpcasc} = 100\text{nA}$  &  $I_{adpptau} = 10\text{nA}$ . In the second simulation,  $I_{gain}$  was varied. Simulation plots are shown in Figure 92.

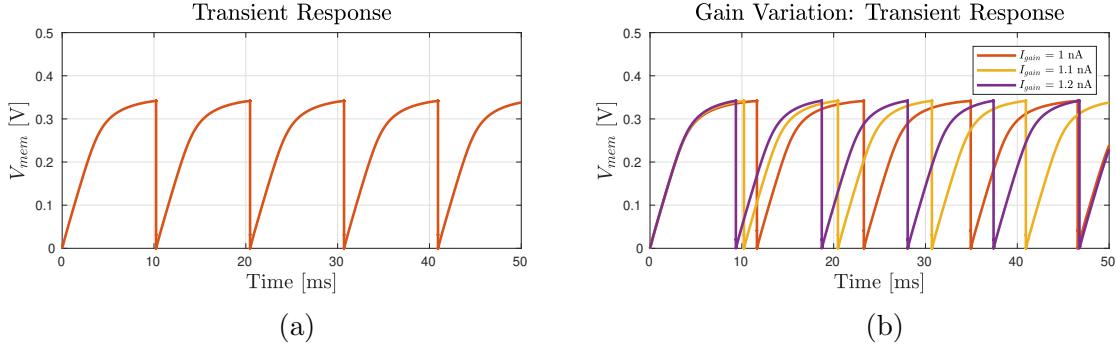


Figure 92: (a) measurements of the membrane voltage  $V_{mem}$  (b) variation of gain bias  $I_{gain}$ .

### 3.29.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup. A subsection of the mismatch data is provided. Variation in rate and width of response is observed. Analysis results are shown in Figure 93.

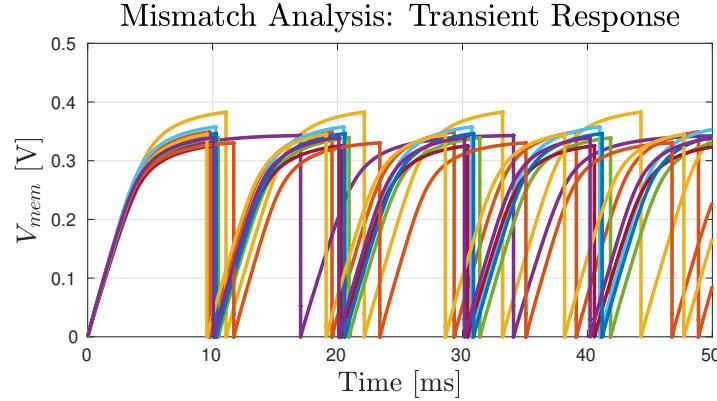


Figure 93: mismatch analysis of the ADEXIF sigma delta neuron circuit.

## 3.30 Hodgekin-Huxley Neuron

### 3.30.1 Description

The Hodgekin-Huxley neuron is a conductance-based neuron-model, modelling the five conductances: Leak, Na<sup>+</sup>, K<sup>+</sup>, Ca & AHP (after-hyperpolarization) [7]. The neuron is divided into five corresponding circuit blocks, which consist of wide-range transamps (or degenerative transamps, in the case of Ca), current mirrors & Capacitors. The circuit receives an input current  $I_{in}$  (typically the output of a synapse,  $I_{syn}$ ) and outputs the membrane voltage  $V_m$ , provided through an output amplifier. Additionally, conductance voltages  $V_{Na}$ ,  $V_K$  &  $V_{Ca}$  are provided, to observe the internal neuron state.

The Spike Discriminator, which provides input to the Ca block, generates pulses of fixed-width in response to a spike in the membrane voltage,  $V_m$  (before amplification). To do this, the discriminator is comprised of a comparator, which compares  $V_m$  to a set threshold. The output is amplified through two inverters, and then passed to a rising edge detector. Schematics of these circuits are shown in Figure 95.

The circuit has 17 biases:  $V_{dc}$ ,  $V_{nasat}$ ,  $V_{natau}$ ,  $V_{kdsat}$ ,  $V_{kdtau}$ ,  $V_{ahpsat}$ ,  $V_{eleak}$ ,  $V_{gleak}$ ,  $V_{carest}$ ,  $V_{carest2}$ ,  $V_{cabuf}$ ,  $V_{cain}$ ,  $V_{thres}$ ,  $V_{puthres}$ ,  $V_{padbias}$  &  $V_{puwidth}$  (for the spike discriminator) &  $V_{buf}$  (for the output amplifier). FET device & Capacitor sizings were inherited from a previous implementation, and tweaked to mitigate mismatch. A schematic of the circuit is shown in Figure 94.

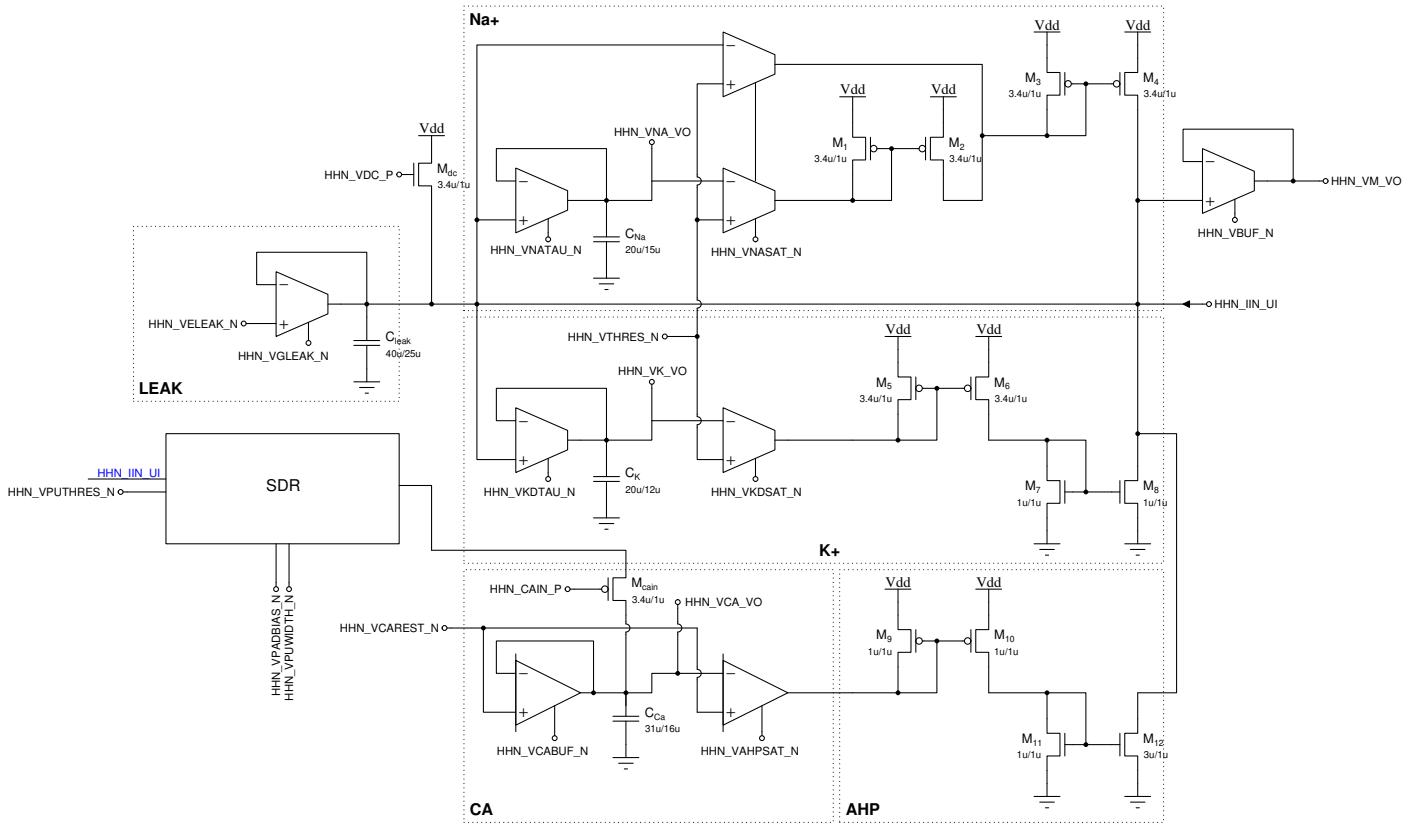


Figure 94: Hodgkin-Huxley neuron schematic.

### 3.30.2 Simulations

In the first simulation, a transient analysis was done to illustrate regular spiking, with a DC input current of  $I_{in} = 1nA$  provided. Biases were set as follows:  $I_{dc} = 1nA$ ,  $I_{nasat} = 10nA$ ,  $I_{natau} = 200pA$ ,  $I_{kdsat} = 2nA$ ,  $I_{kdtau} = 200pA$ ,  $I_{ahpsat} = 1nA$ ,  $I_{leak} = 100nA$ ,  $I_{gleak} = 100pA$ ,  $I_{carest} = 100nA$ ,  $I_{carest2} = 600nA$ ,  $I_{cabuf} = 20pA$ ,  $I_{cain} = 0$ ,  $I_{thres} = 1\mu A$ ,  $I_{puthres} = 1nA$ ,  $I_{padbias} = 700nA$ ,  $I_{puwidth} = 1nA$  &  $I_{buf} = 100nA$ . In the second simulation,  $I_{gain}$  was varied.

In the second simulation, a transient analysis was done to illustrate adaptation, with a DC input current of  $I_{in} = 1nA$  provided. The following biases were changed:  $I_{kdsat} = 5nA$  &  $I_{cain} = 5nA$ . Simulation plots are shown in Figure 96.

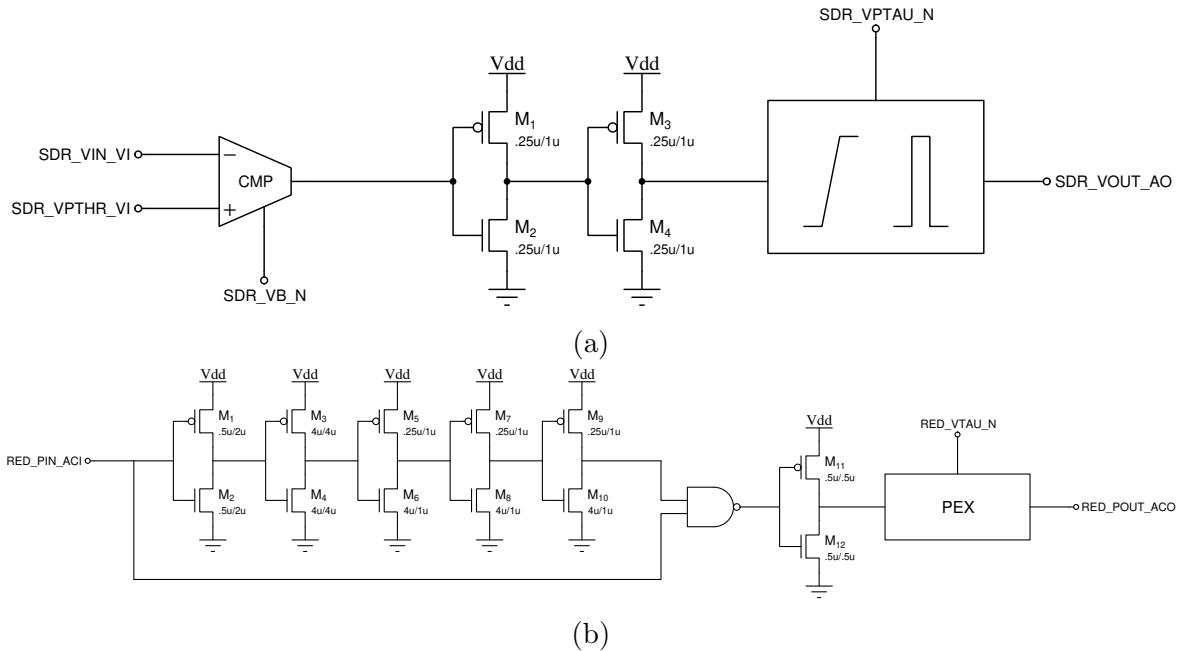


Figure 95: Schematics of (a) the spike discriminator and (b) it's rising edge detector

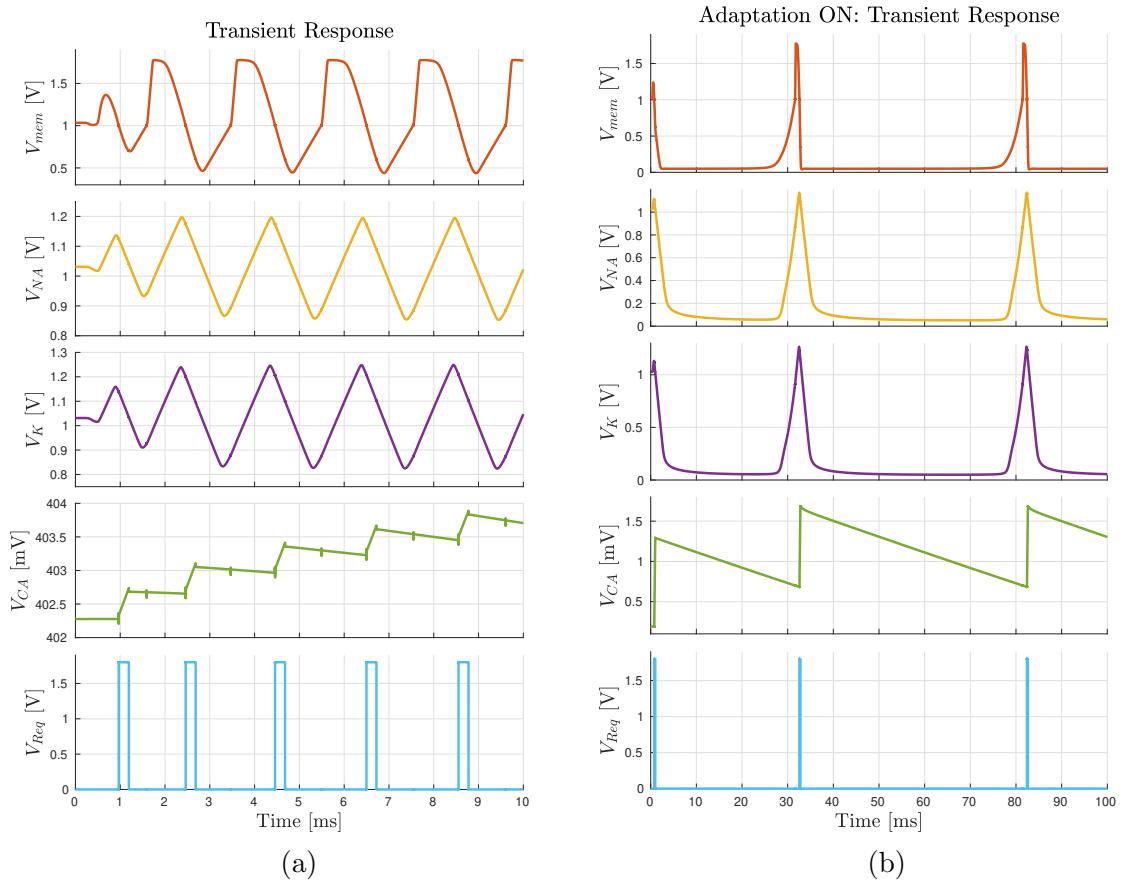


Figure 96: measurements of output voltages  $V_{mem}$ ,  $V_{NA}$ ,  $V_K$  &  $V_{CA}$  (a) in regular spiking mode and (b) with adaptation ON.

### 3.30.3 Mismatch Analysis

A mismatch analysis was performed using the first simulation setup. A subsection of the mismatch data is provided. Due to the feedback dynamics present in this circuit, the utilized bias settings resulted in a zero response in several of the variations produced. Analysis results are shown in Figure 97.

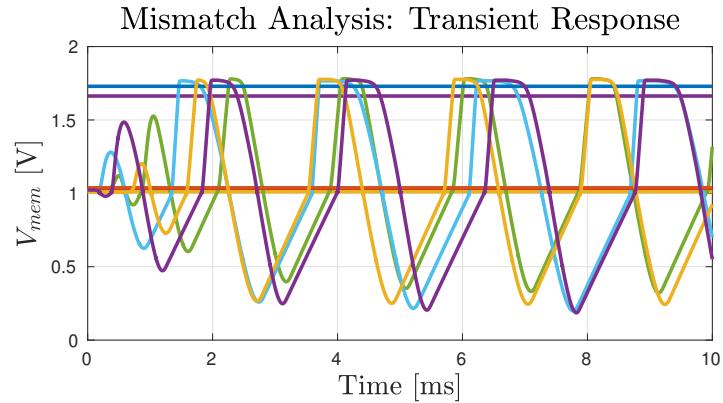


Figure 97: mismatch analysis of the Hodgekin Huxley neuron circuit.

## Acknowledgement

I wish to thank Carsten Nielsen, for starting this project up with me, and sticking it through as far as he could, and Ole Richter, who regardless of the time of day (or current location), would advise me on any of the very many questions I had.

## References

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# A

## Common Circuits

### A.1 Degenerative Transamp

The Degenerative transamp has a wide input range, due to the diode connected transistors inserted on each branch. This circuit is used in the second-order section and the Hodgkin-Huxley neuron. Circuit schematic and layout are shown in Figures 98 & 99 respectively.

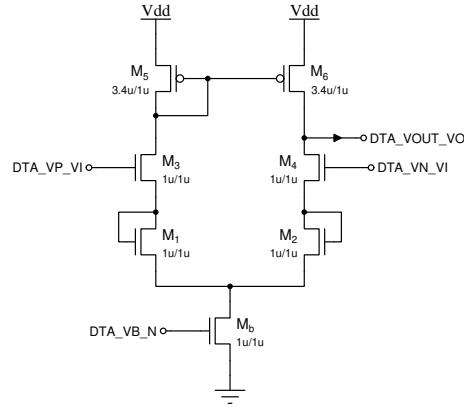


Figure 98: Degenerative transamp schematic.

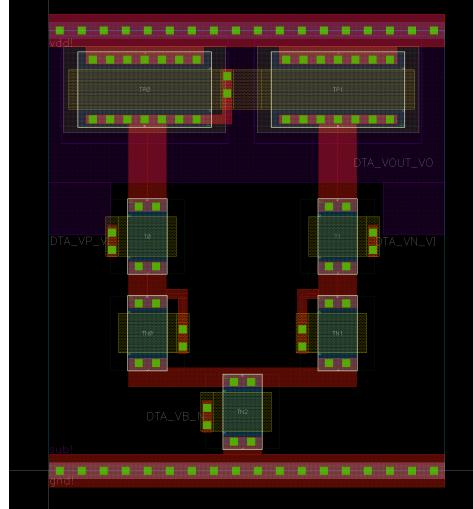


Figure 99: Degenerative transamp layout.

## A.2 Pulse Extender

The pulse extender receives input pulses with widths on order of nanoseconds (AER spikes), and extends them to a timescale range the synapses and neurons can receive (typically hundreds of microseconds to tens of milliseconds). The extender is used as a common input to all of the synapses, as well as in the adaptation block of the ADEXIF neurons and the (equivalent) spike discriminator block of the Hodgekin-Huxley neuron.

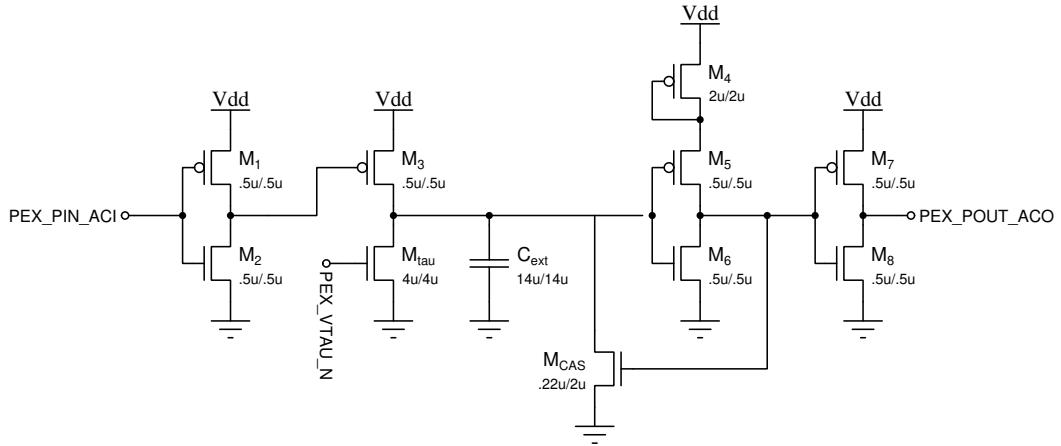


Figure 100: Pulse extender schematic.

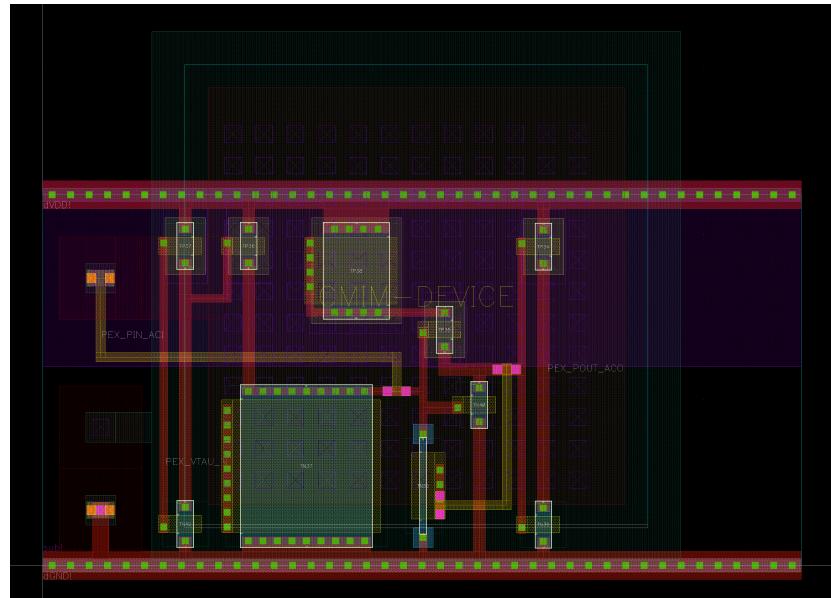


Figure 101: Pulse extender layout.

## B Layouts

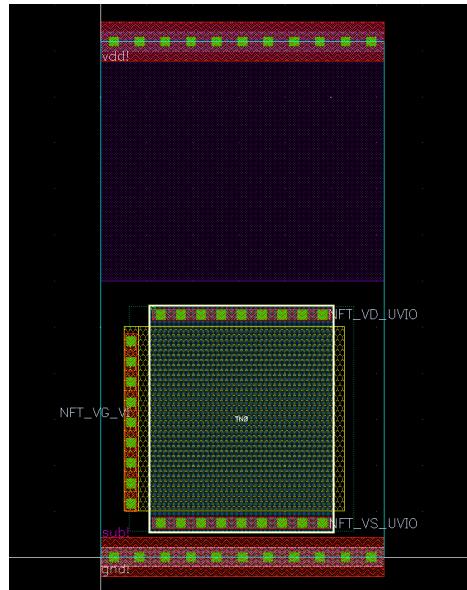


Figure 102: N-FET device layout.

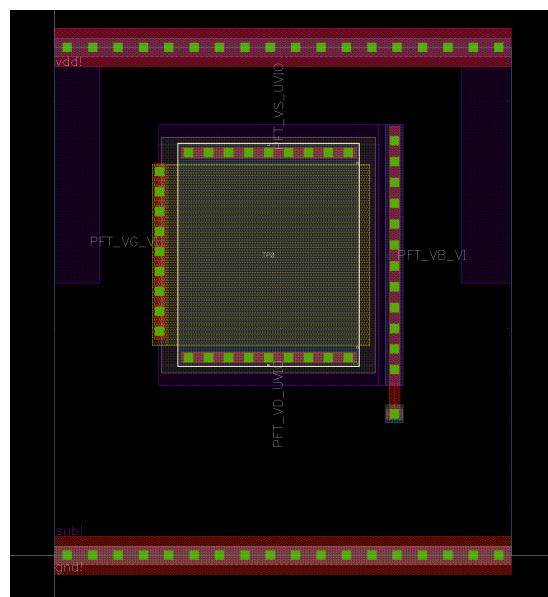


Figure 103: N-FET device layout.

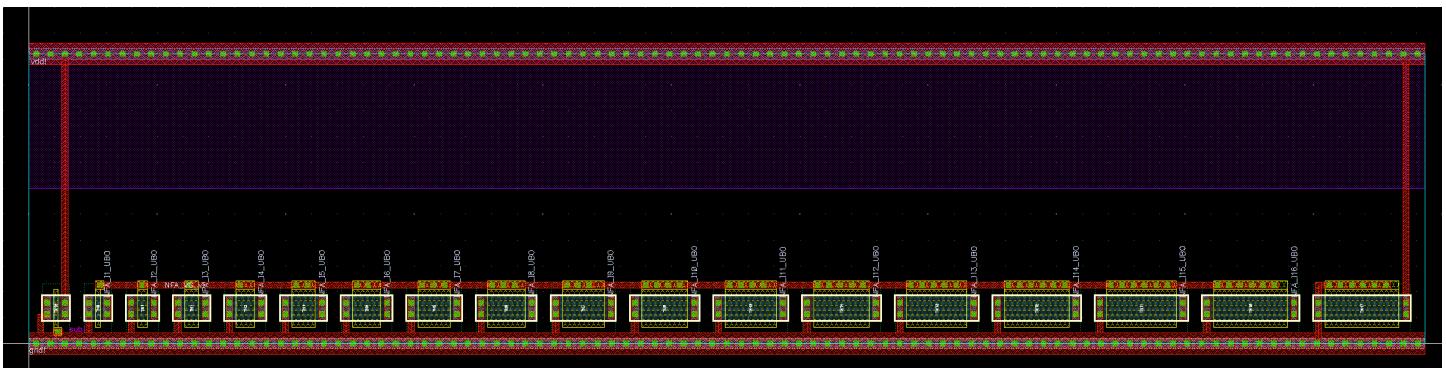


Figure 104: N-FET array layout.

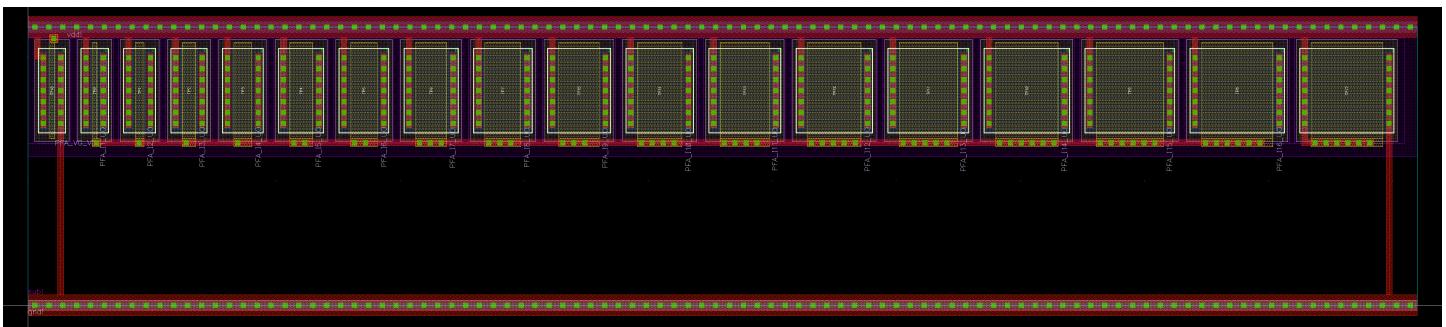


Figure 105: P-FET array layout.

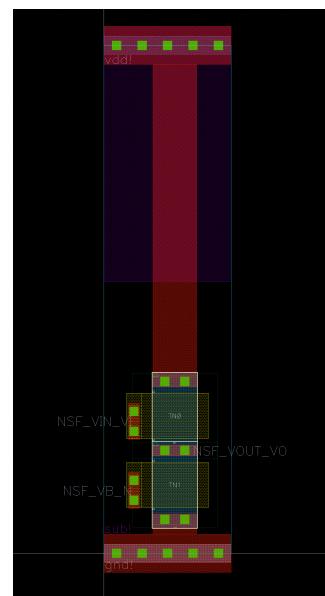


Figure 106: N-type source-follower layout.

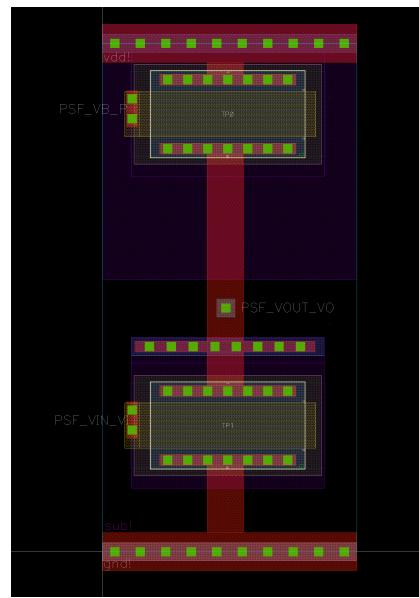


Figure 107: P-type source-follower layout.

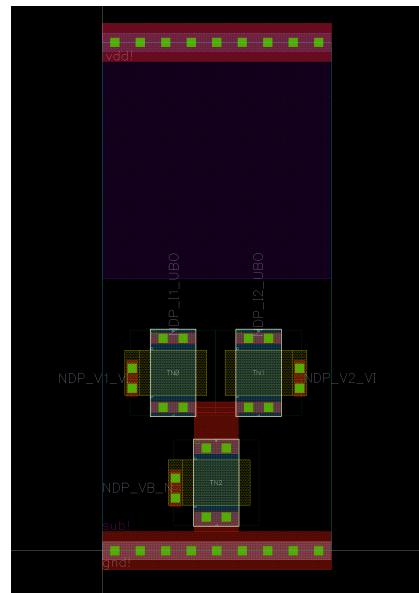


Figure 108: N-type differential-pair layout.

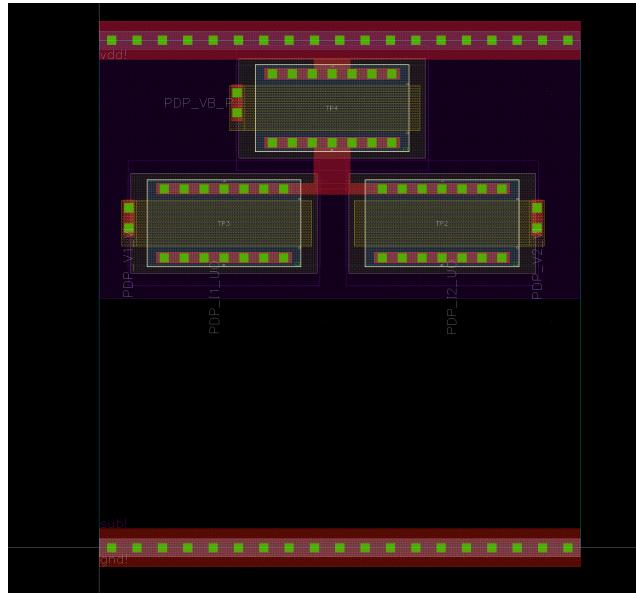


Figure 109: P-type differential-pair layout.

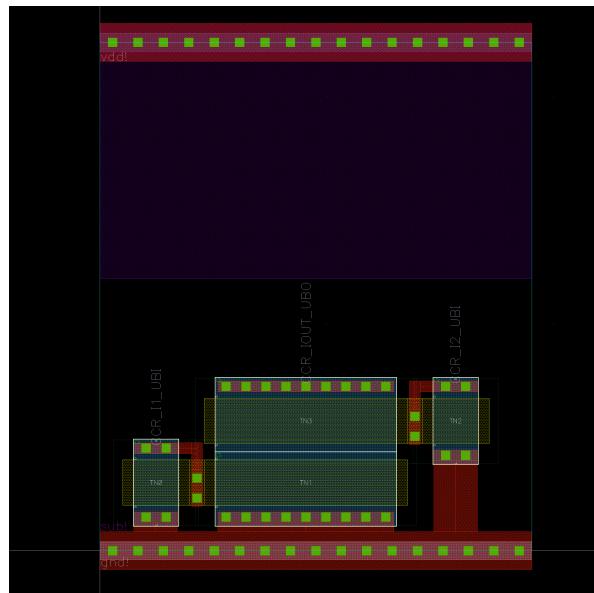


Figure 110: Current correlator layout.

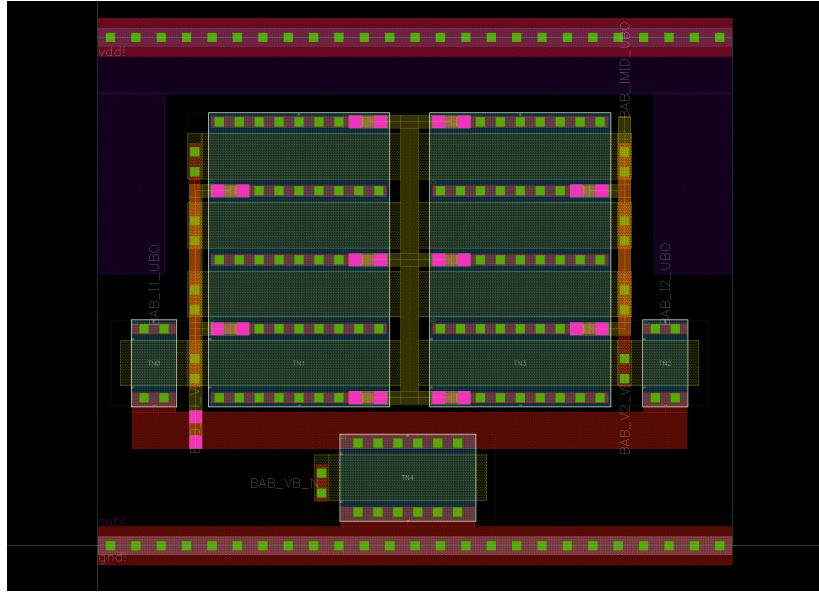


Figure 111: Bump antibump layout.

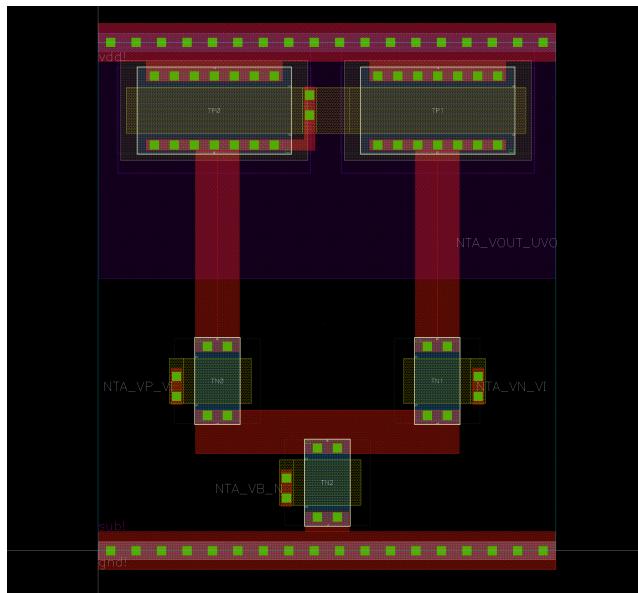


Figure 112: N-type 5T transamp layout.

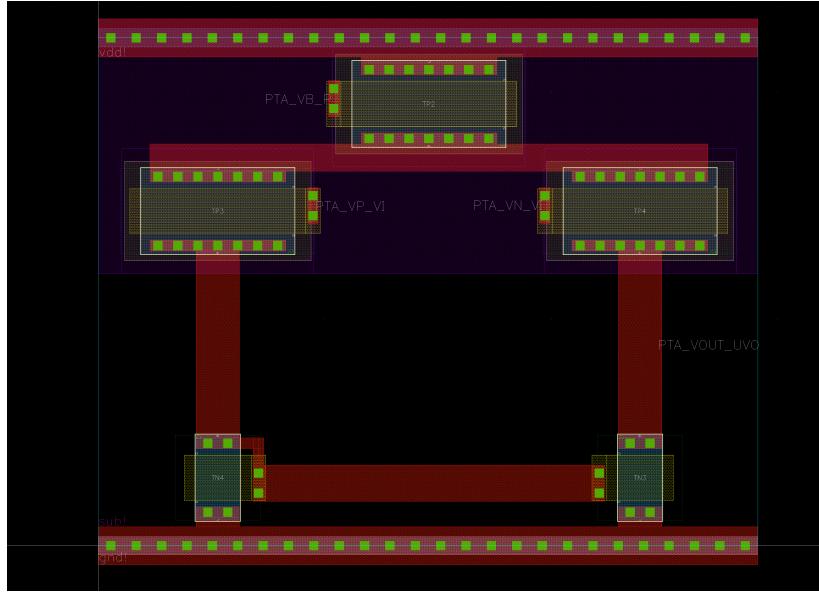


Figure 113: P-type 5T transamp layout.

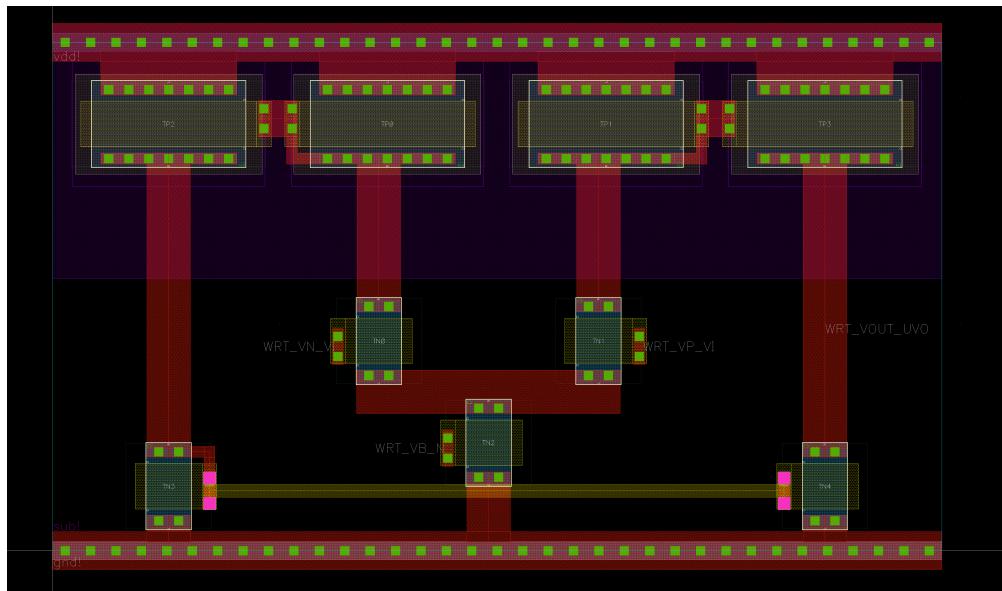


Figure 114: Wide-range transamp layout.

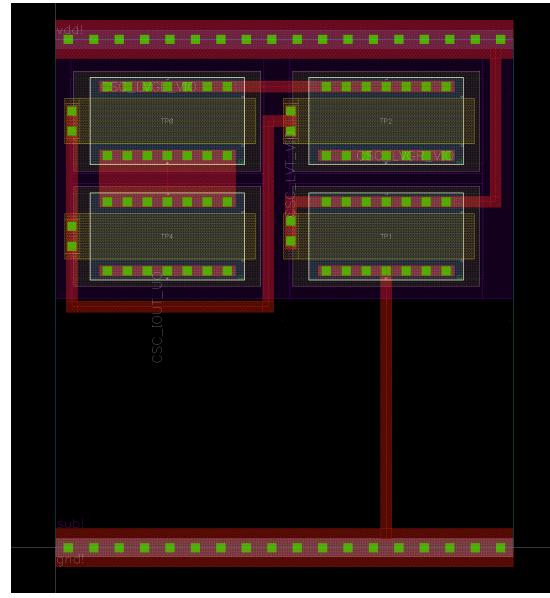


Figure 115: Current Splitter cell layout.

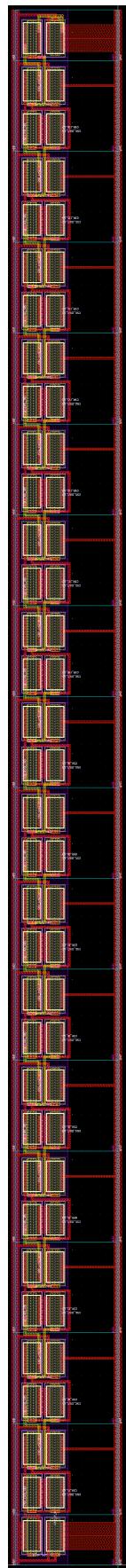


Figure 116: Current Splitter cell layout.

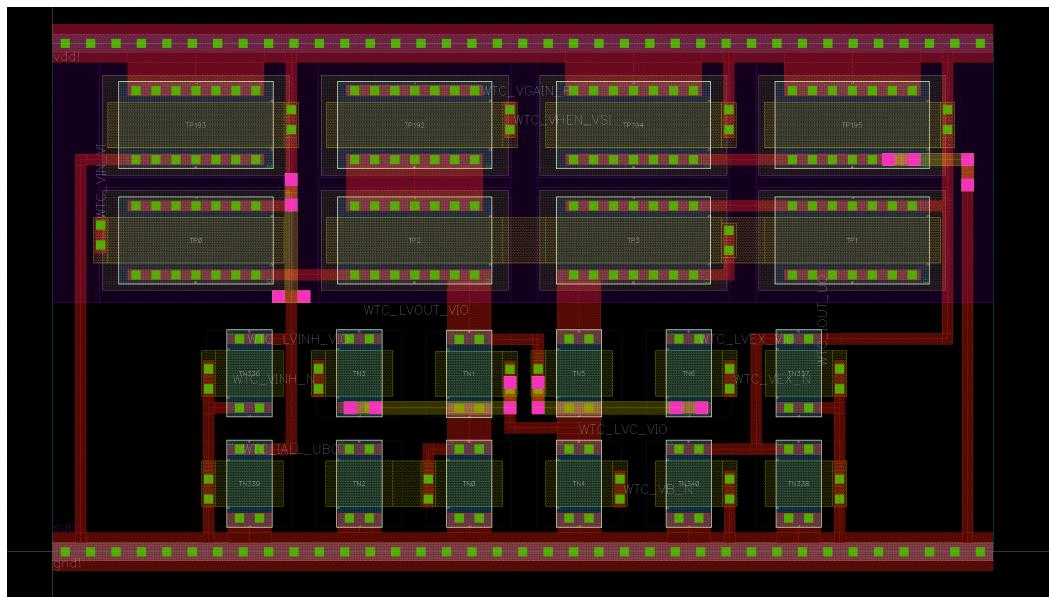


Figure 117: Winner-take-all cell layout.



Figure 118: Winner-take-all cell layout.

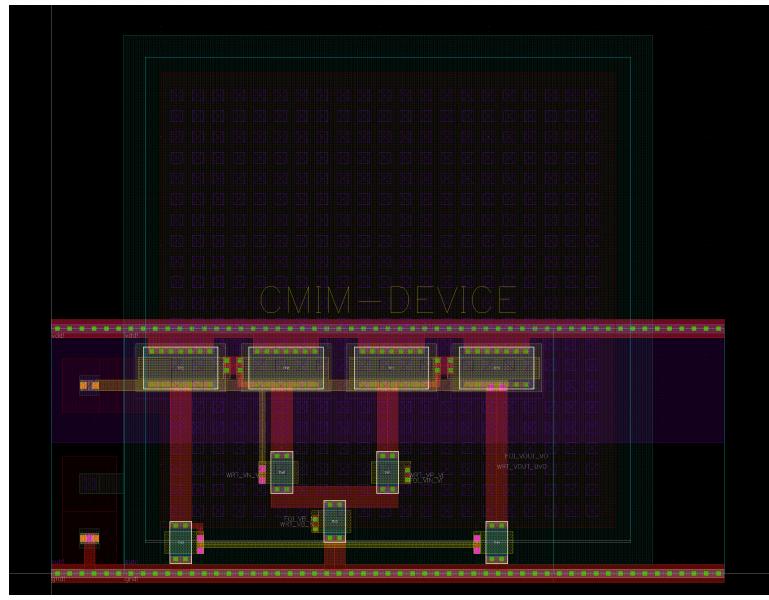


Figure 119: Follower integrator layout.

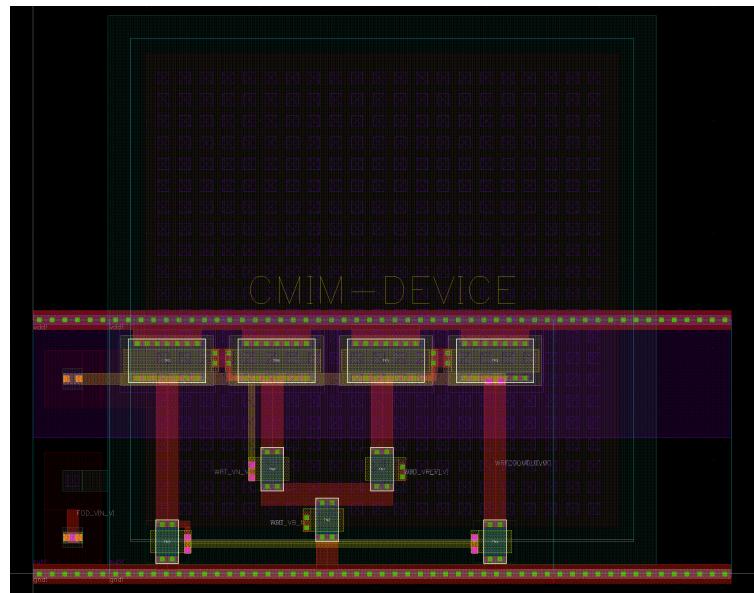


Figure 120: Follower differentiator layout.

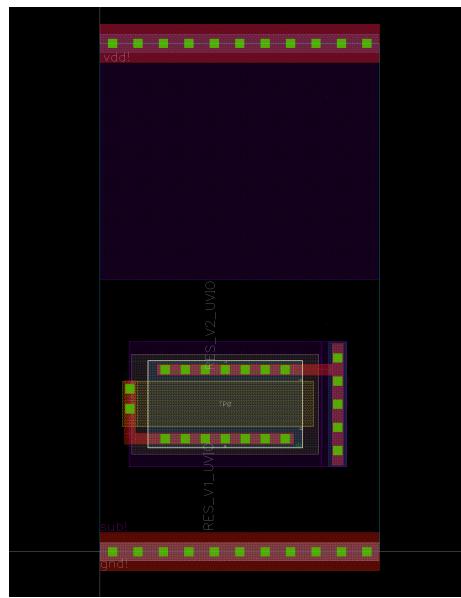


Figure 121: Resistive element layout.

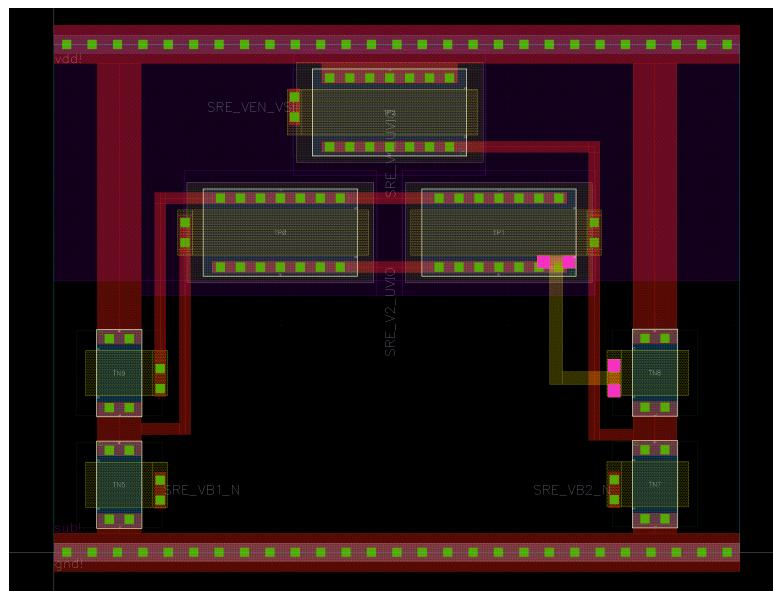


Figure 122: Symmetric resistive element layout.

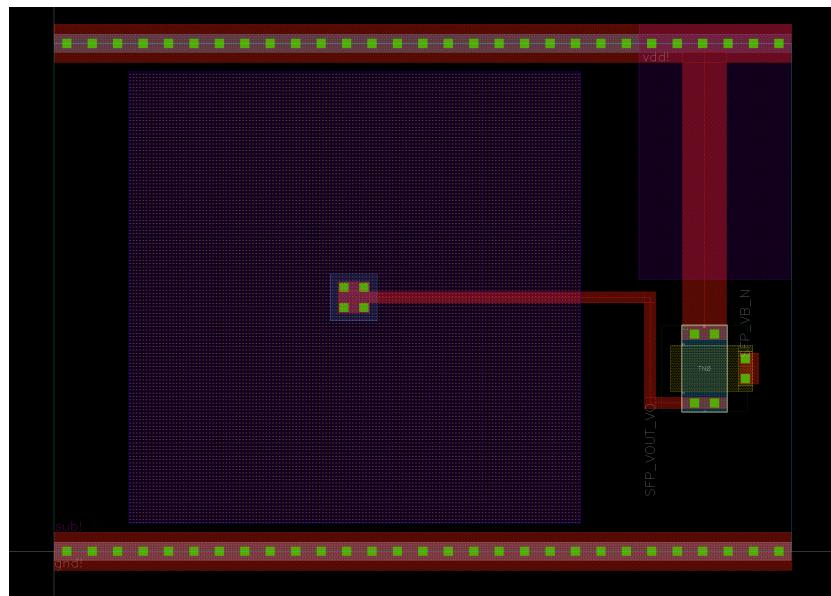


Figure 123: Source-follower photoreceptor layout.

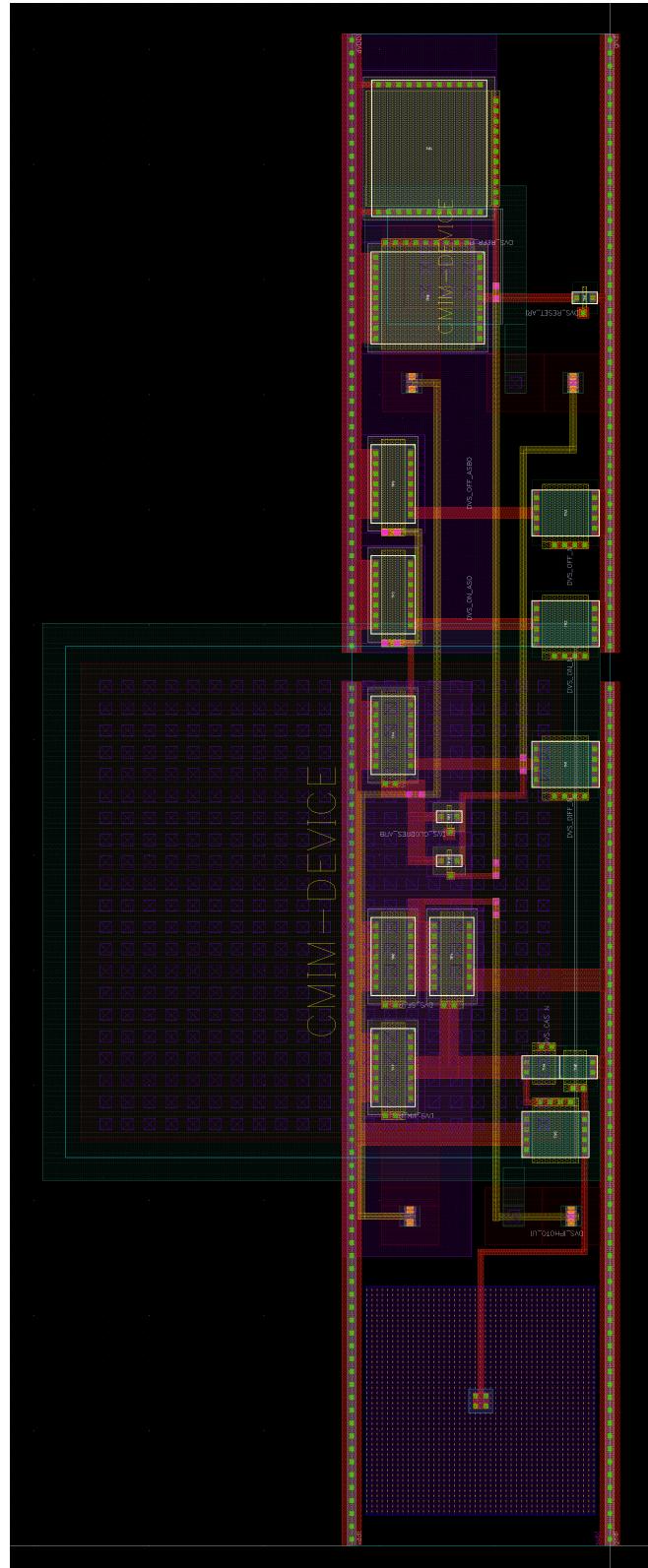


Figure 124: DVS pixel layout.

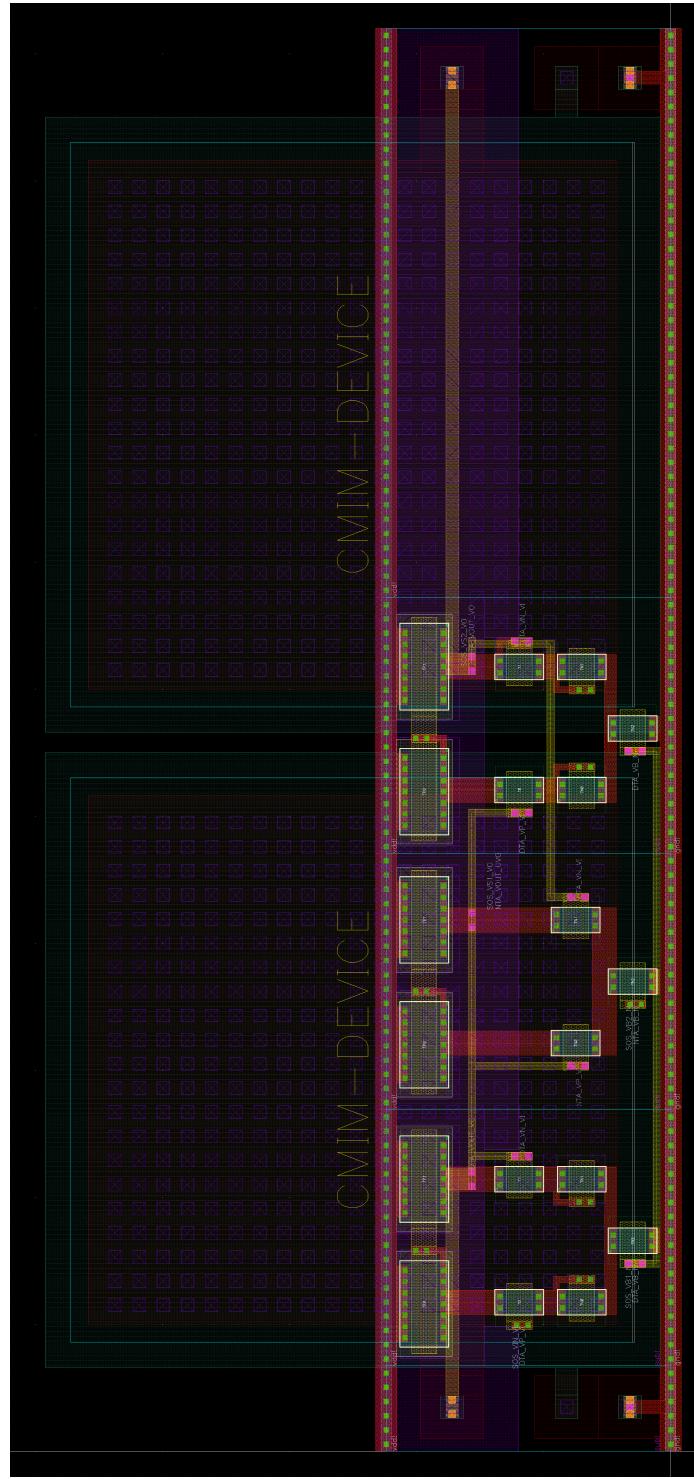


Figure 125: Second-order section layout.

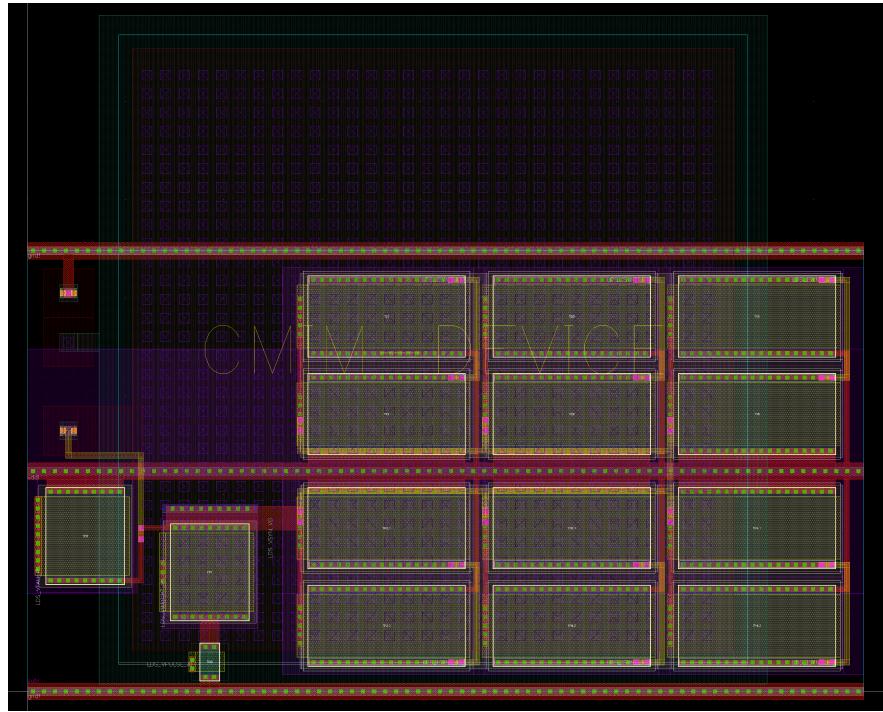


Figure 126: Log domain synapse layout.

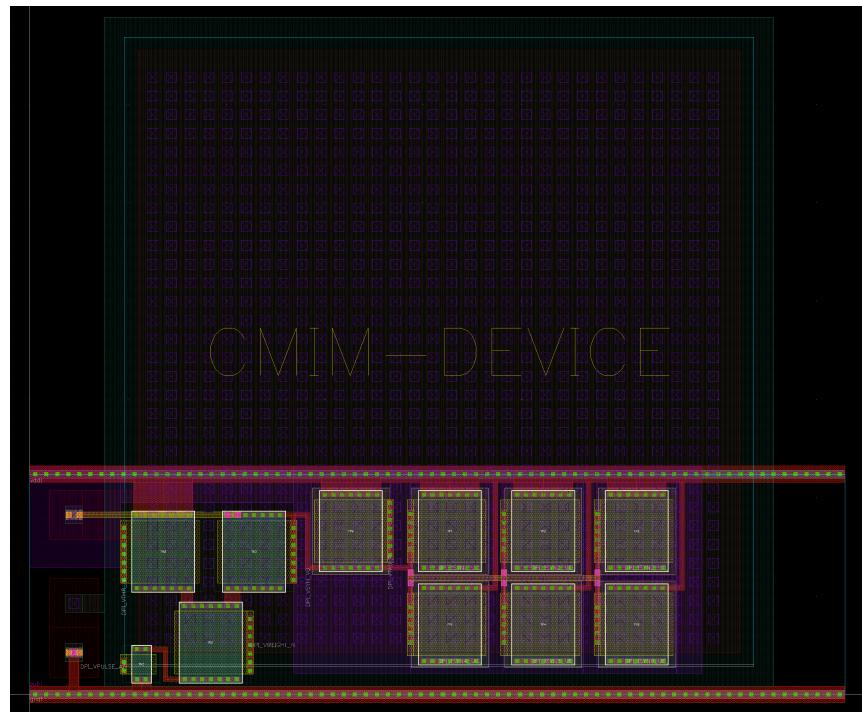


Figure 127: DPI synapse layout.

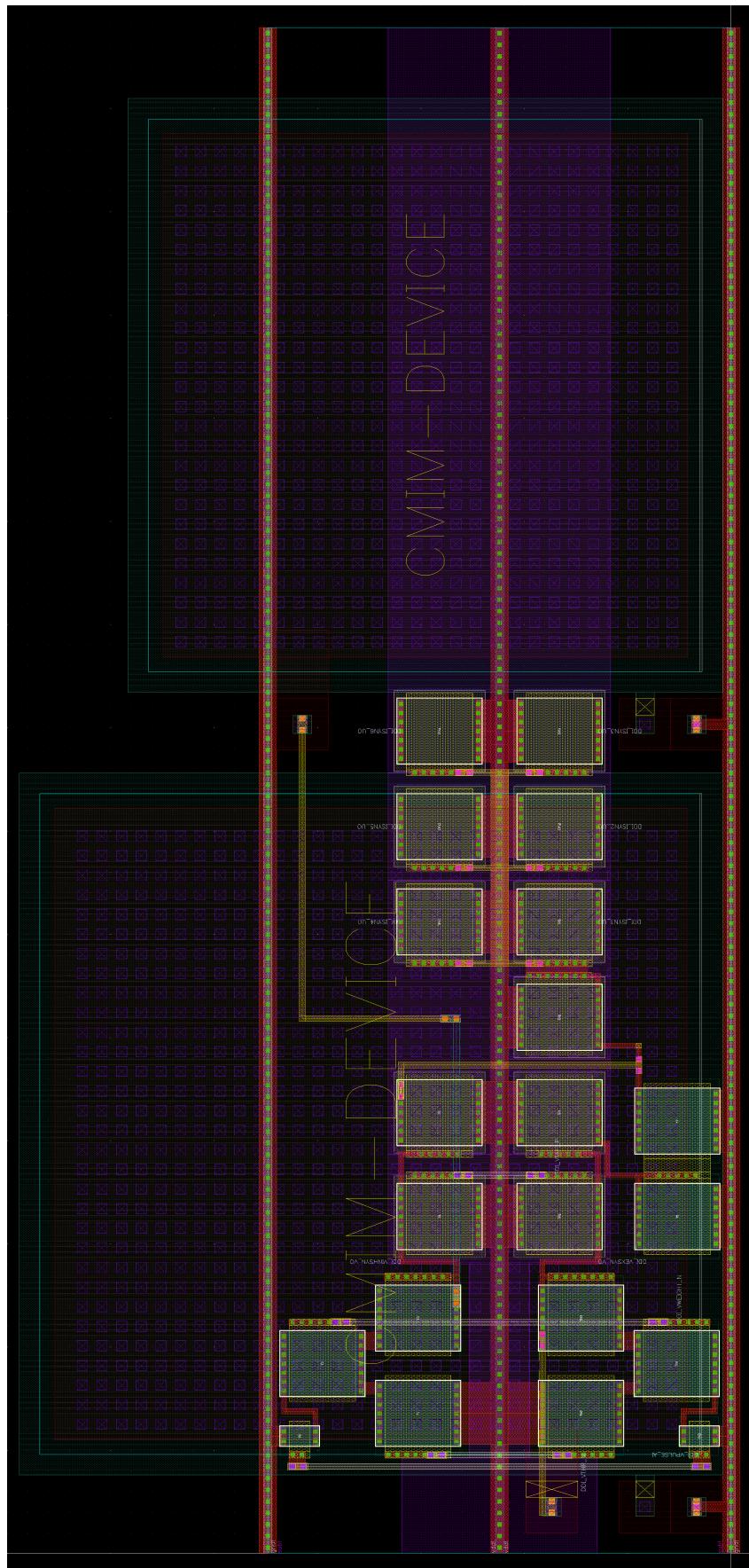


Figure 128: Dual-DPI synapse layout.

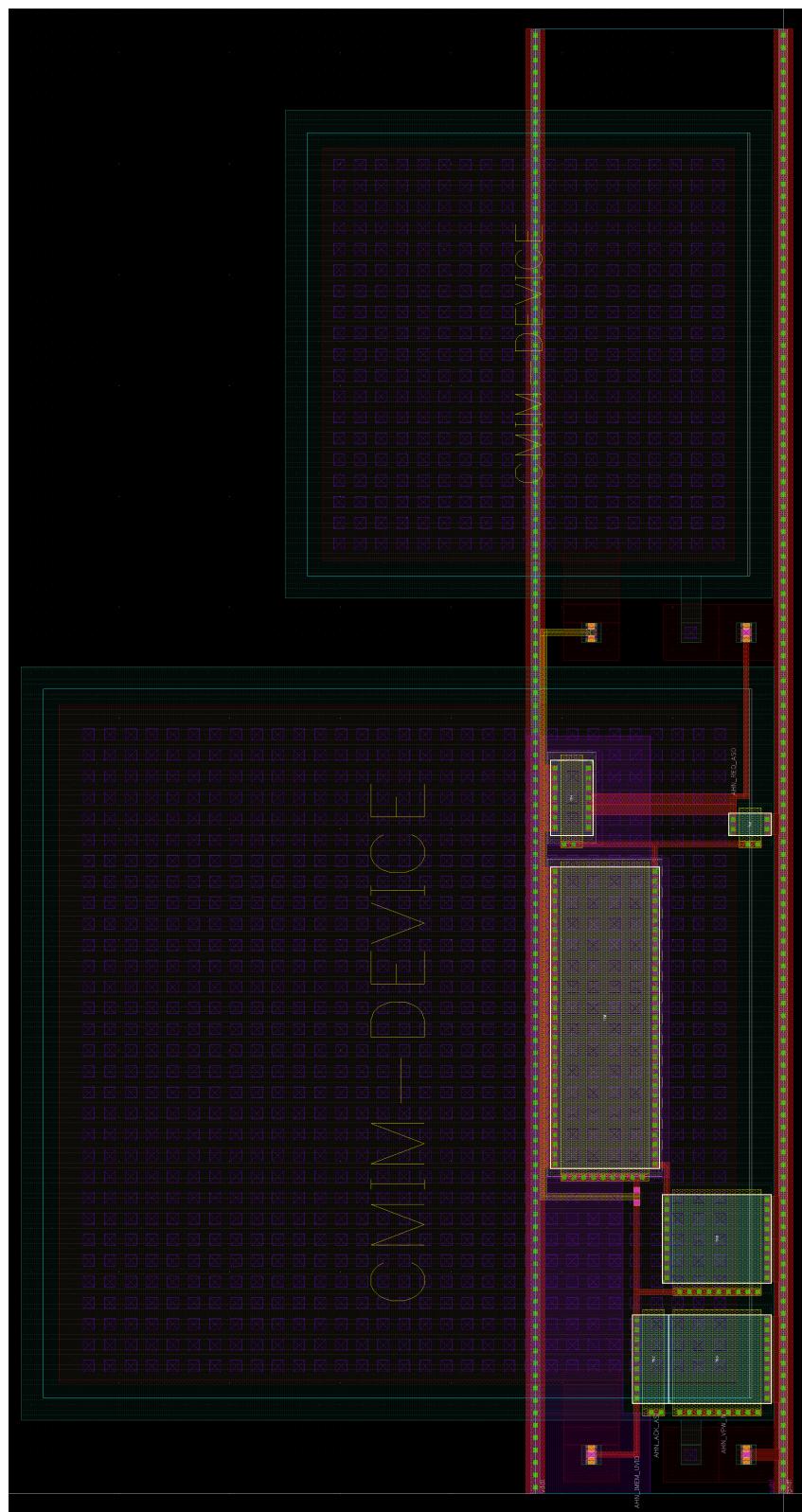


Figure 129: Axon-Hillock neuron layout.

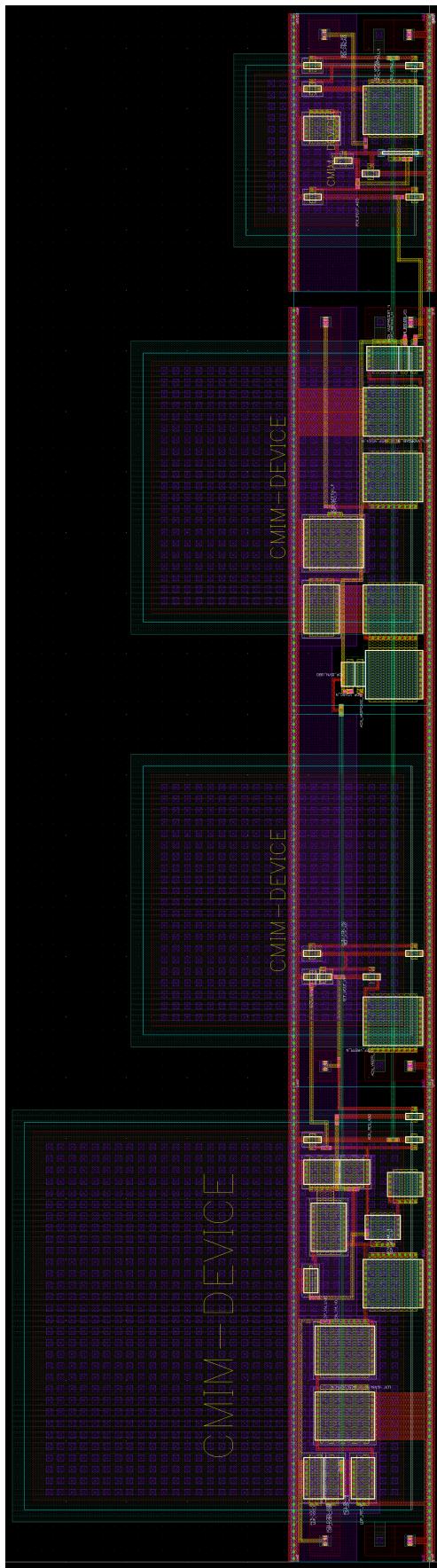


Figure 130: ADEXIF classic neuron layout.

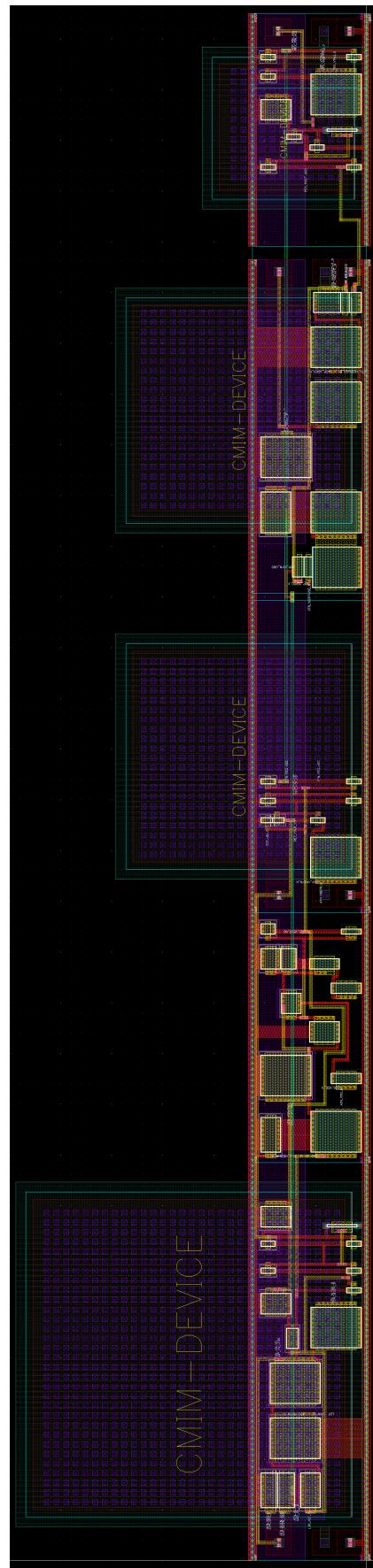


Figure 131: ADEXIF thresholded neuron layout.

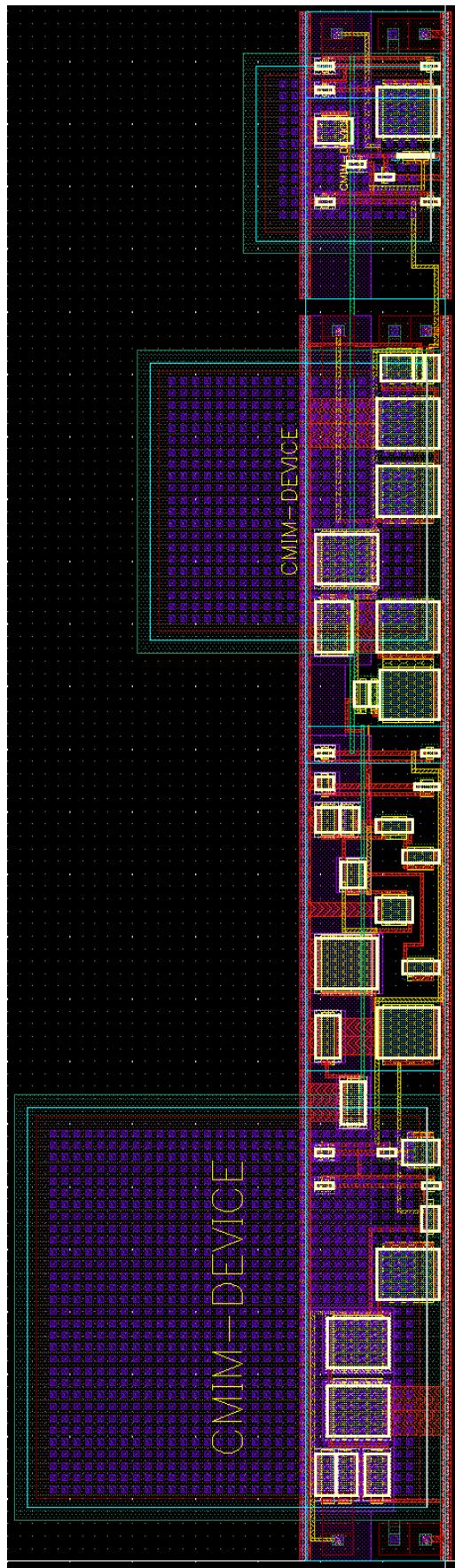


Figure 132: ADEXIF sigma-delta neuron layout.

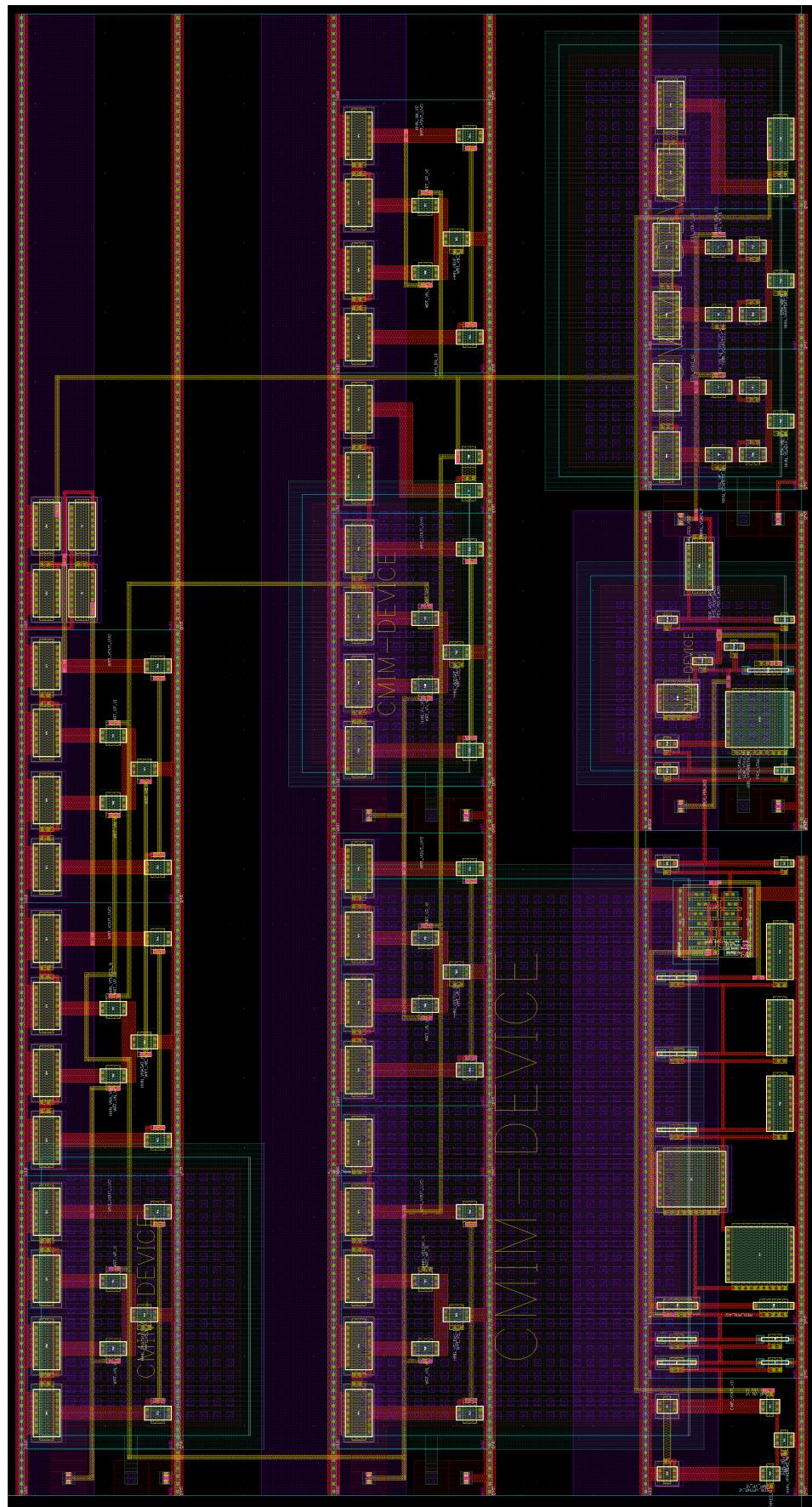


Figure 133: Hodgekin-Huxley neuron layout.