Neuromorphic Engineering I

Time and day : Lecture **Mondays, 14:15-16:00**
Lab exercise location: In Institute of Neuroinformatics Y55 (TAs will advice)
Credits: **6 ECTS** credit points
Exam*:* Oral 20-30 minutes at INI
Labs**:** Reports (**max 2 persons**). You must successfully **complete at least 9 lab exercises**. These exercises should include **the first 3 labs (mandatory)** and **at least one of the last 2 labs**. If you do all lab exercises, we will drop your 3 lowest lab grades.
Grade**:** 70% exam + 30% lab exercises
Lectures from**:** Tobi Delbruck, Giacomo Indiveri, Melika Payvand, Shih-Chii Liu,
Teaching assistants**:** Lavinia Moretti, Oscar Hrynkevch, Lola Ardura, Zhe Su

Tobi Delbruck

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Lola Oscar Lavinia

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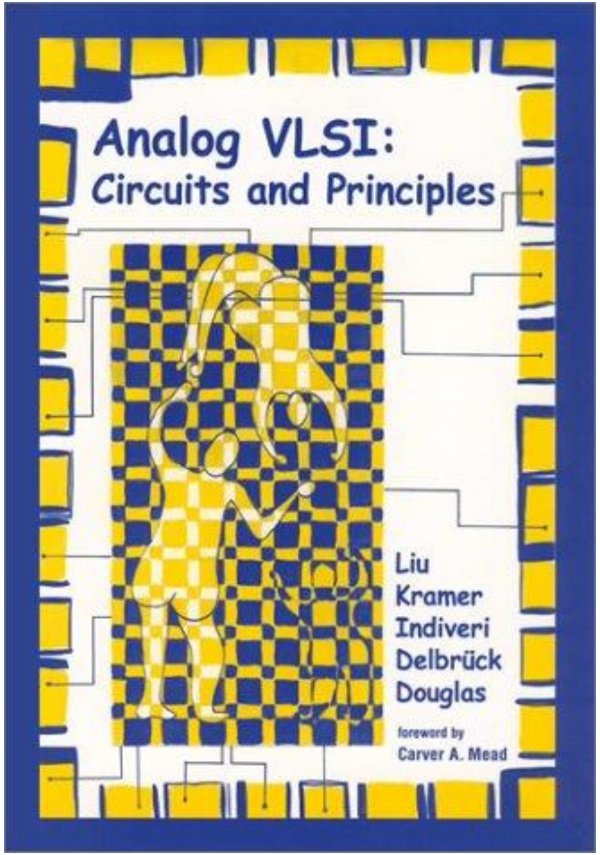
To do today

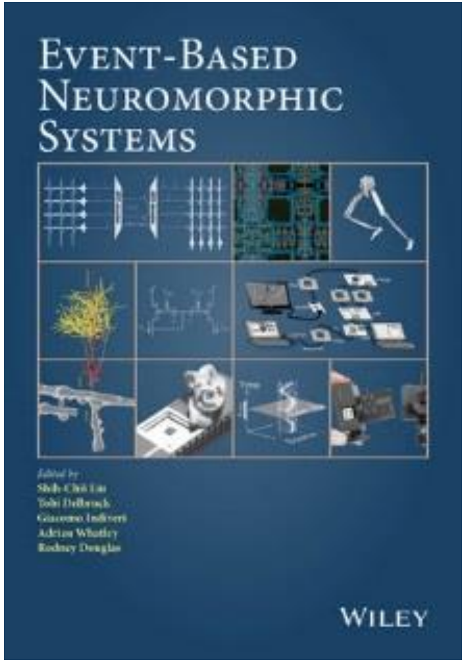
- Introduce book
- Arrange lab times (by doodle) and introduce new classchip and exercises (Slot 1: Tues 8:00 – 11:00, Slot 2: Thursdays 13:30 – 16:30, 30 spots/slot)
- Demo lab setup and class-chip use will be explained by TAs
- Introduce device physics

Book(s)

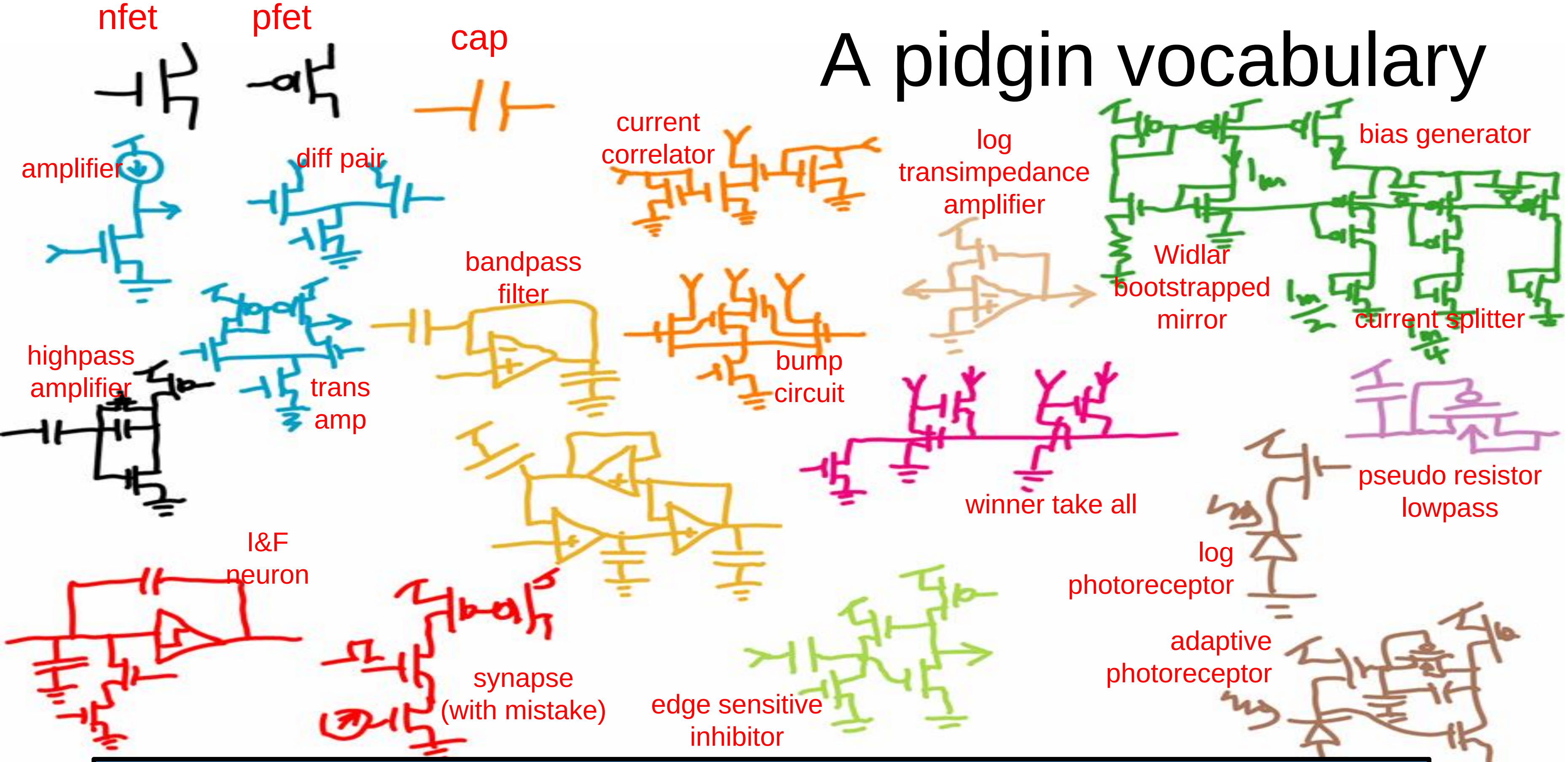
Introductory textbook (2002)
Amazon



System examples (2015)
Amazon



A pidgin vocabulary



By the end of this semester, you should recognize many of these circuits and be able to <u>reason</u> your way through the others.

Neuromorphic Electronics?

What is it all about?

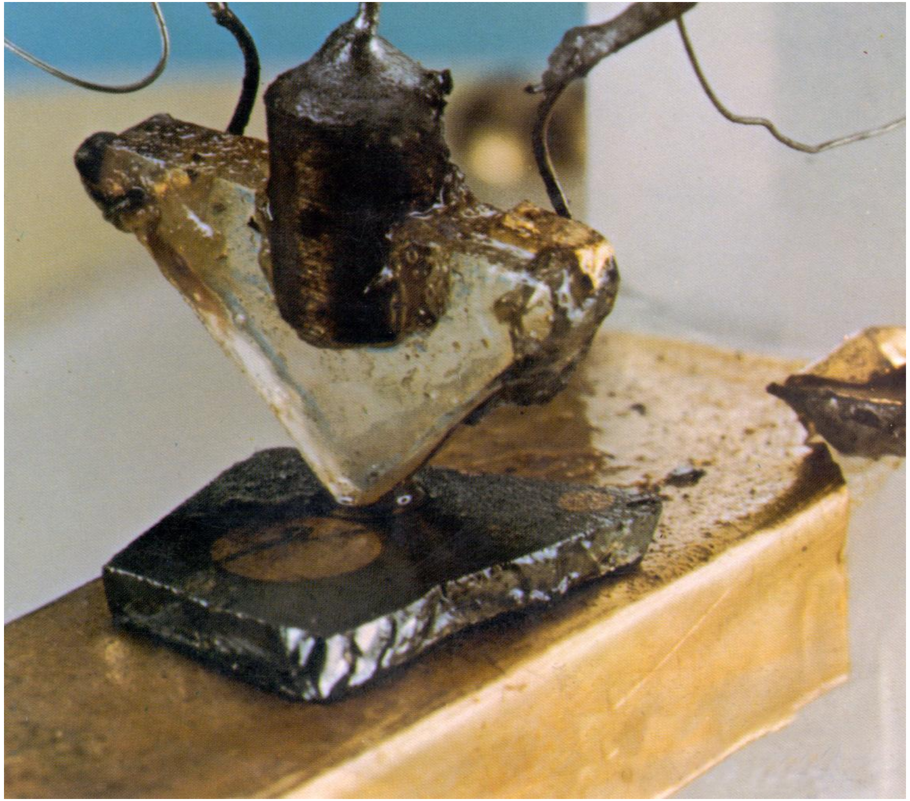
See Shih-Chii Liu talk from 2020 Telluride Neuromorphic Workshop:

Neuromorphic electronics, A historical perspective

The context

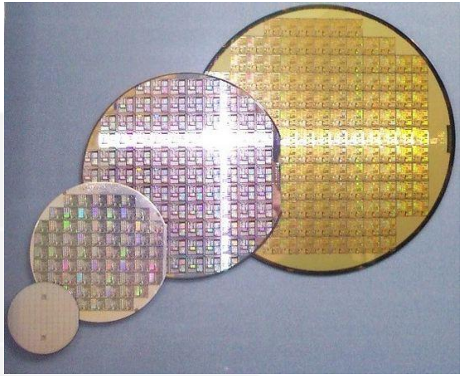
Bardeen and Brattain

1947

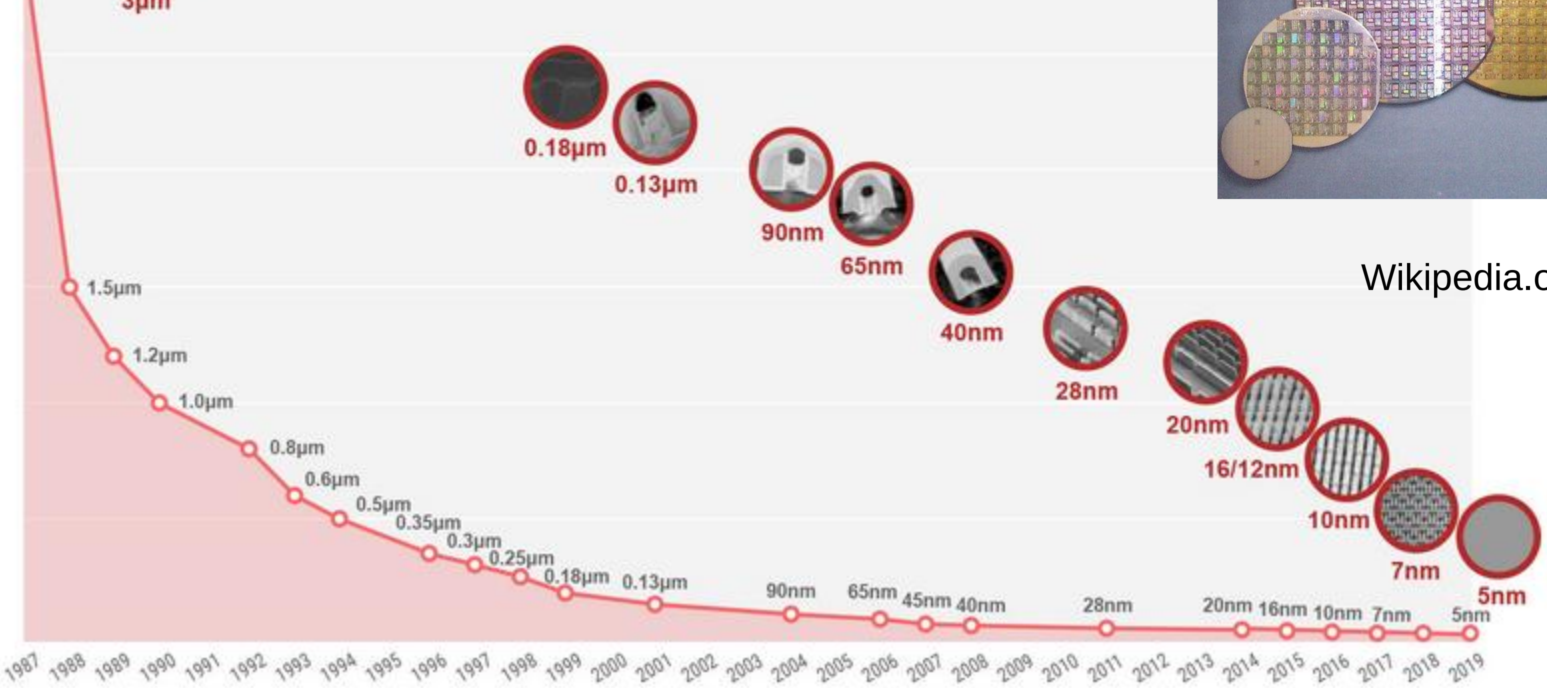


Technology Growth

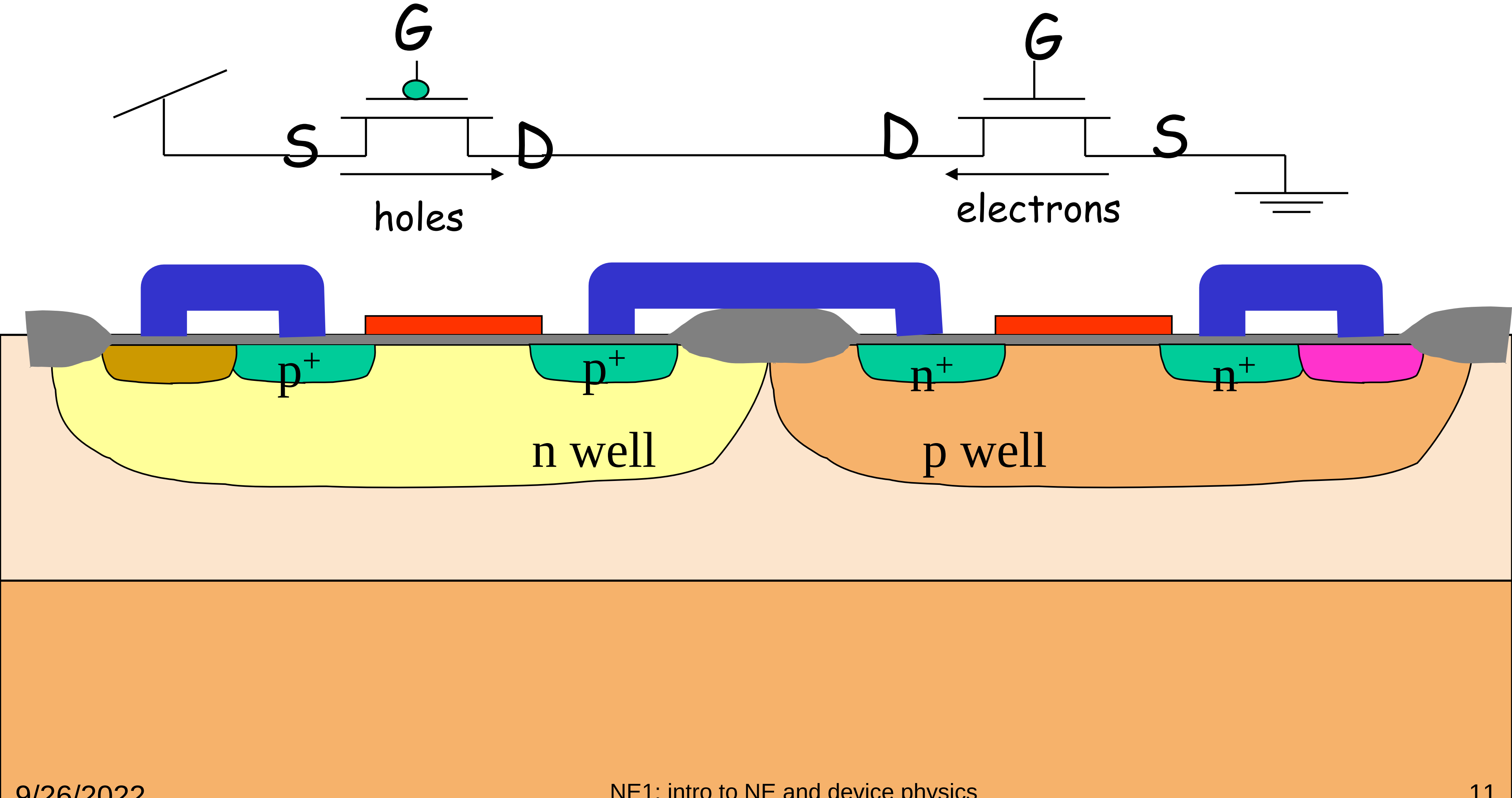
8-inch (200 mm)



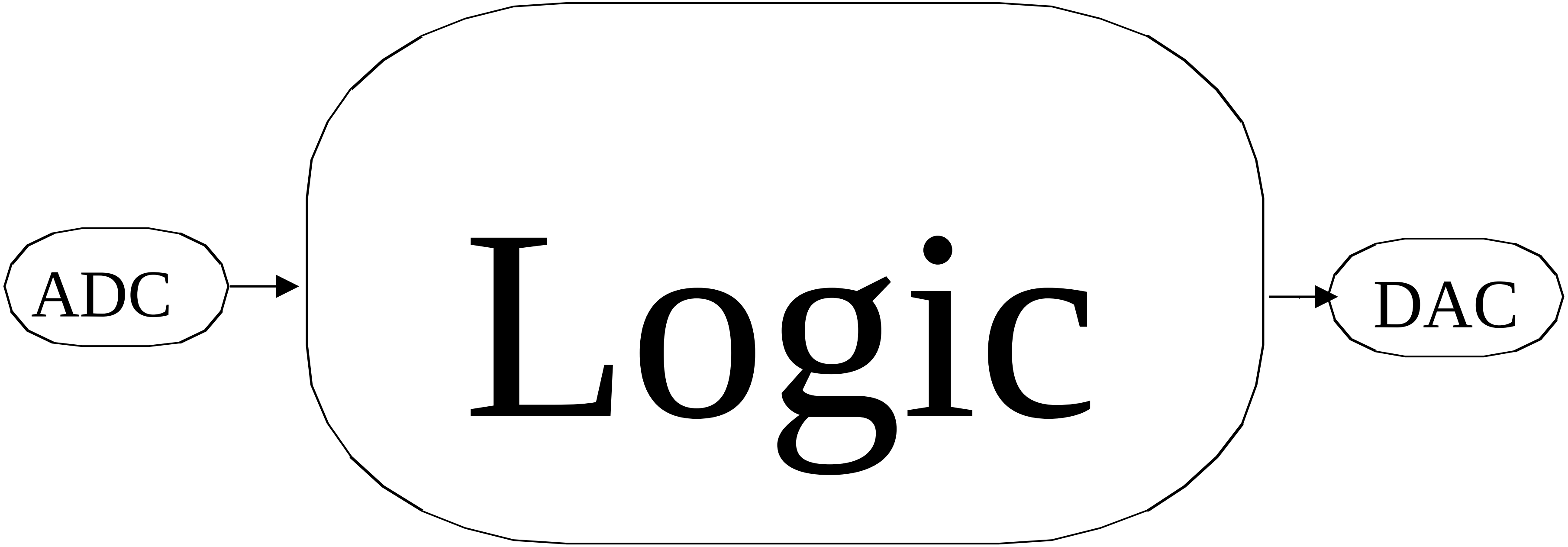
International Technology Roadmap for Semiconductors



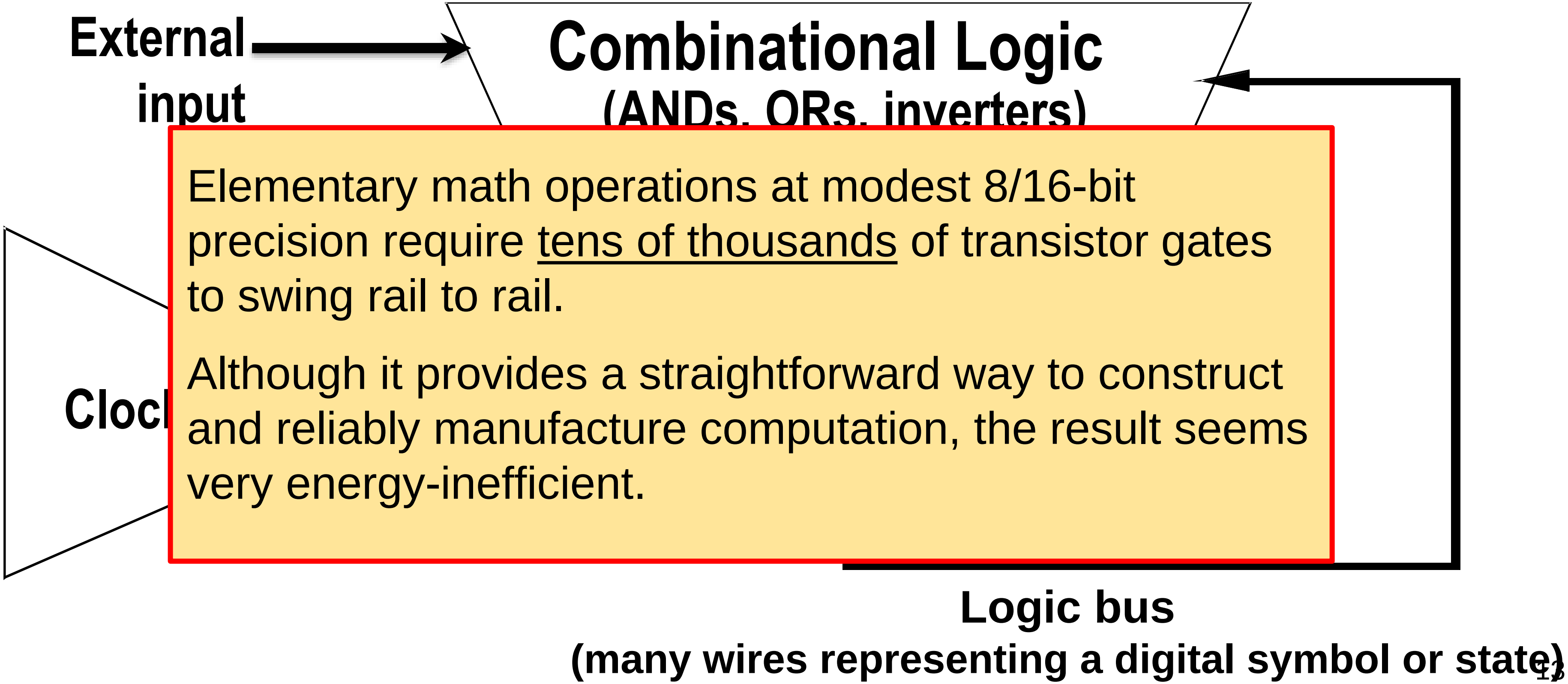
Wikipedia.org


G
S
D
holes
G
D
S
electrons
p+
p+
n+
n+
n well
p well

Artificial real-world computation
(or: How industry thinks of analog)



Synchronous logic is ubiquitously used to implement Finite State Machines (FSMs)



Elementary math operations at modest 8/16-bit precision require <u>tens of thousands</u> of transistor gates to swing rail to rail.

Although it provides a straightforward way to construct and reliably manufacture computation, the result seems very energy-inefficient.

The motivation from biological computation

Natural computation

even with 10kW computer power we cannot do this

Flies acrobatically
Recognizes patterns
Navigates
Forages
Communicates

10uW bee brain
10^6 neurons, 10^9 synapses
10 op/s/synapse

10^{-15} J/op
(op=synaptic activation)

Digital silicon 10^{-7} to 10^{-13} J/op (MAC)

Biology is 10^8 to 10^3 times as efficient as digital silicon

Sparsity

Estimate energy use and spike rate in the human brain

$$\underset{\text{Neurons*}}{10^{11}} \times \underset{\text{Syn/neuron}}{10^{4}} \times \underbrace{\underset{\text{V}}{10^{-1}} \times \underset{\text{A}}{10^{-9}} \times \underset{\text{sec}}{10^{-3}}}_{\text{J/syn. Act.}=10^{-13}\text{J}=\mathbf{0.1pJ}} \times \underset{\text{Avg. spike rate}}{X} = \underset{\text{W}}{10^{1}}$$

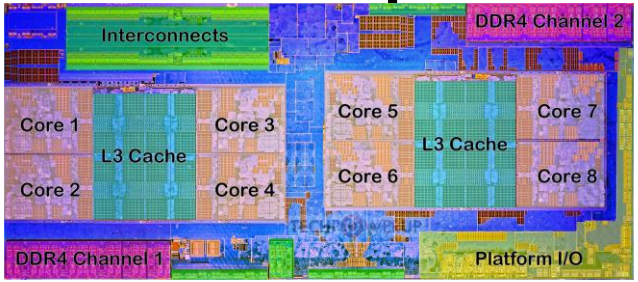
Avg. **output** spike rate = 1 Hz

10^4 fan-out means avg. synaptic **input** rate per neuron = 10 kHz

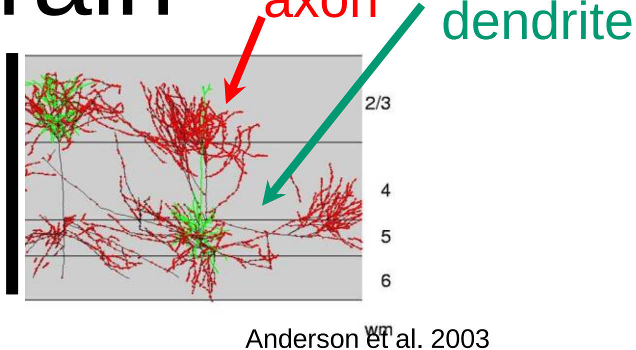
It is very different than conventional DNNs, where every neuron sends its messages to all recipients at the frame rate, e.g. 100Hz

Computer vs. Brain

AMD Ryzen
$192 mm^2$
5B FETs
180W



Cortex
$1 mm^3$
100k neurons
1B synapses
~1mW



Anderson et al. 2003

At the system level, brains are about 1 million times more power efficient than computers. Why?
Cost of elementary operation (turning on transistor or activating synapse) is about the same. It's not some magic about physics.

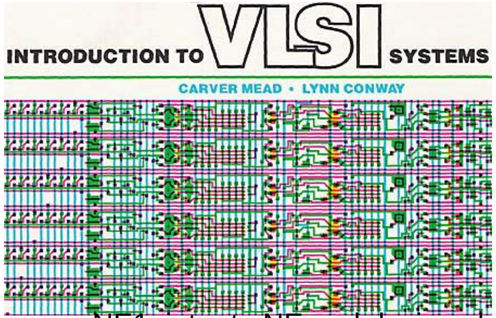
Computer	Brain
Fast global clock	Self-timed, sparse computation (avg spike rate in brain ~1Hz)
Bit-perfect deterministic logical state	Synapses are stochastic! 20% probability. Computation dances: digital→analog→digital
Memory distant in time and space to computation	Memory in synapses, at computation
Devices frozen on fabrication	Constant adaptation and self-modification

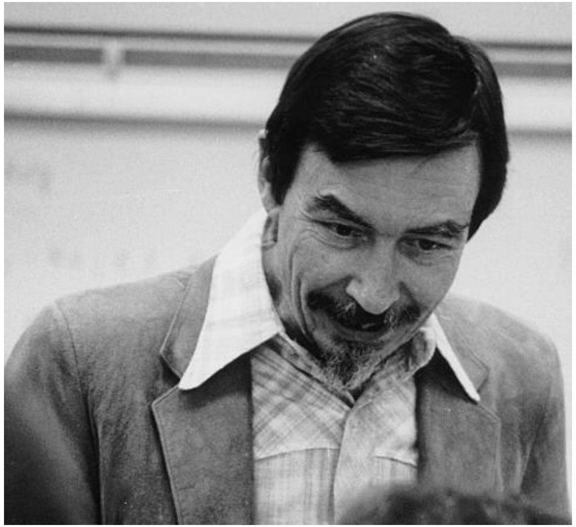
The fact that we can build devices that implement the same basic operations as those the nervous system uses leads to the inevitable conclusion that we should be able to build entire systems based on the organizing principles used by the nervous system.

Proc. IEEE, 1990

Carver Mead, Physicist by inclination

1966 Inventor of GaAs MESFET transistor
1970's: Coiner of term "Moore's Law"
1980 Co-author of main logic design textbook for 20 years
2013: ISSCC keynote talk (see more cool talks here)
"The high priest of silicon"





T Delbruck, CNS182 class, Caltech, ca 1989

Lab exercises organization

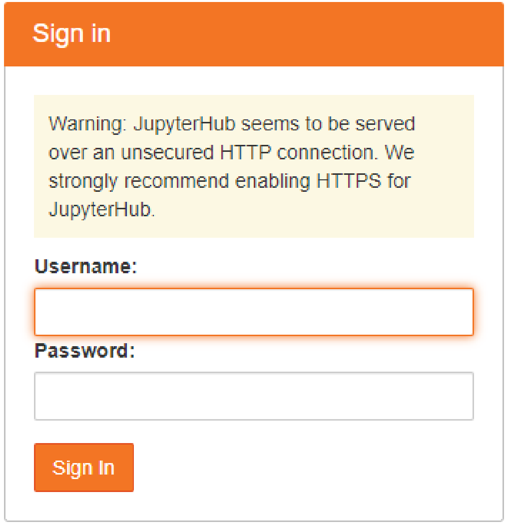
- The labs are done in groups of 2, sign up on the google sheet.
- The first three labs last 2 hours, the rest are 4 hours (the whole morning/afternoon in which you sign up), the material for the corresponding week will be published at the end of the lecture.
- Please use the OLAT Forum to look for your lab partner or in class.
- You should hand in the prelab, lab report and post-lab as a group on OLAT dropbox before the next lab starts.
- For questions regarding the labs, please contact TAs.

Links for the lab exercises

lab1-scheduling: Sign up at this lab exercise doodle.

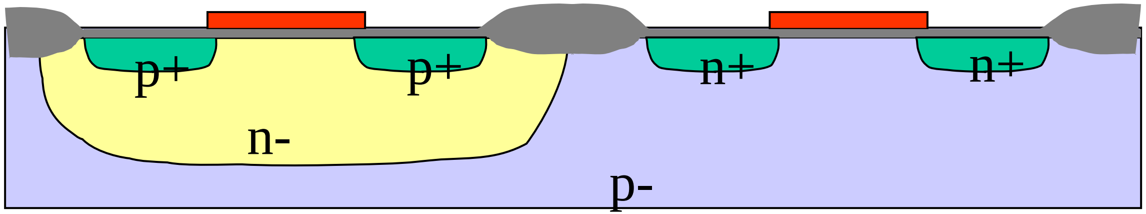
Jupyter notebooks https://code.ini.uzh.ch/CoACH/CoACH-labs

- Lab 1: Automated Data Acquisition and Analysis (Running the classchip)
- Lab 2-3: Subthreshold Behavior of Transistors, Transistor superthreshold saturation current and drain characteristics
- Lab 4-5: Static Circuits: Current Mirror, Differential Pair, Current Correlator, Bump Circuit, and Transconductance Amplifier
- Lab 6: Winner-Take-All circuit
- Lab 7: Integrator Circuits
- Lab 8: Photoreceptors I: Phototransduction
- Lab 9: Photoreceptors II: Photoreceptor Circuits
- Lab 10: Silicon Synaptic Circuits
- Lab 11: Silicon Neuron Circuits
- Lab 12: *TBA*



First look at semiconductors and transistors

MOS transistors – semiconductor device physics



We need to understand enough about semiconductors and junctions to understand how MOS transistors work

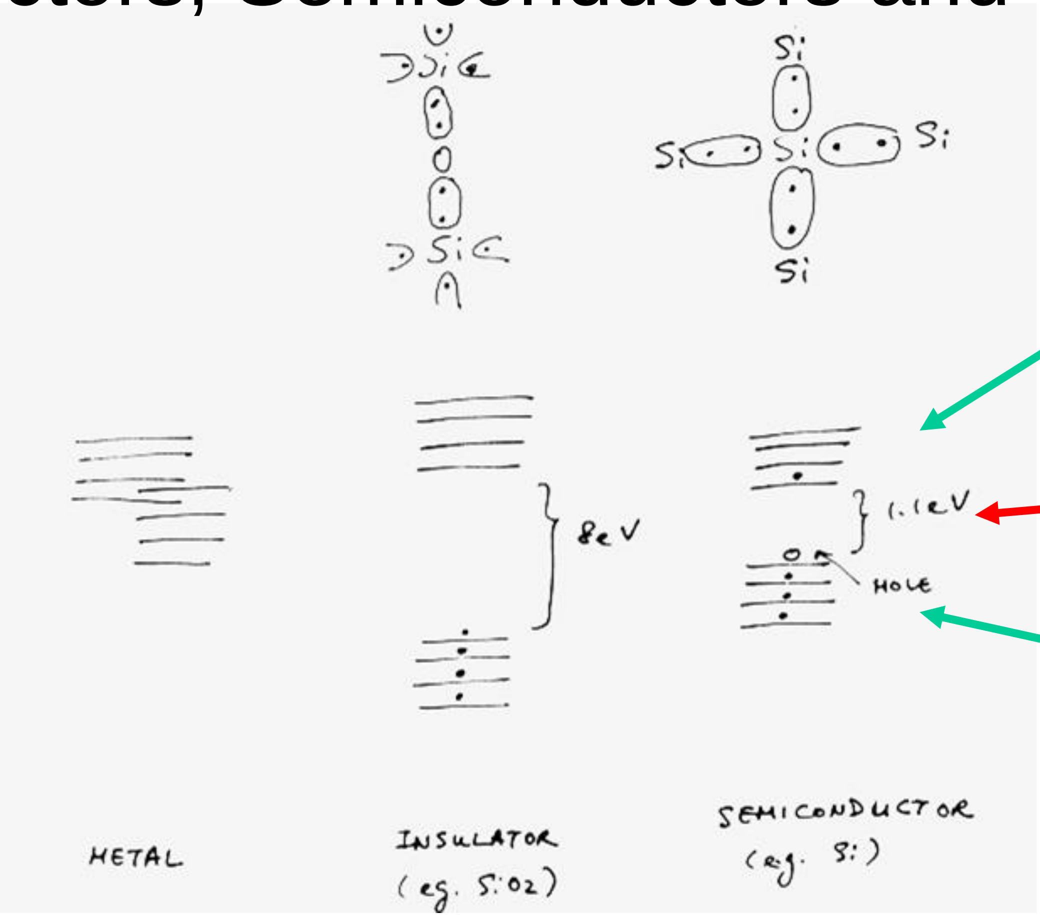
- Insulators, conductors, semiconductors
- Crystal structure of silicon
- Band structure (valence, conduction, and forbidden bands)
- Holes and electrons
- Mechanisms of charge transport (diffusion & drift)
- Doping with donors and acceptors
- Fermi-Dirac distribution
- Law of mass action ($np=n_i^2$)
- p-n junction
- Reverse biased junction and its capacitance

Donors and acceptors in the periodic table

I	II	III	IV	V	VI	VII	Zero
H							He
Li	Be	B	C	N	O	F	Ne
Na	Mg	Al	Si	P	S	Cl	Ar
K	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Cd	In	Sn	Sb	Te	I	Xe

Acceptors | Donors
1 missing electron | 1 extra electron

Conductors, Semiconductors and Insulators



Conduction band

Bandgap

Valence band

Mead, ca 1989, from Andy Grove

Donors and acceptors in the periodic table

I	II	III	IV	V	VI	VII	Zero
H							He
Li	Be	B	C	N	O	F	Ne
Na	Mg	Al	Si	P	S	Cl	Ar
K	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Cd	In	Sn	Sb	Te	I	Xe

Acceptors | Donors

1 missing electron | 1 extra electron

The silicon lattice with an electron donor atom

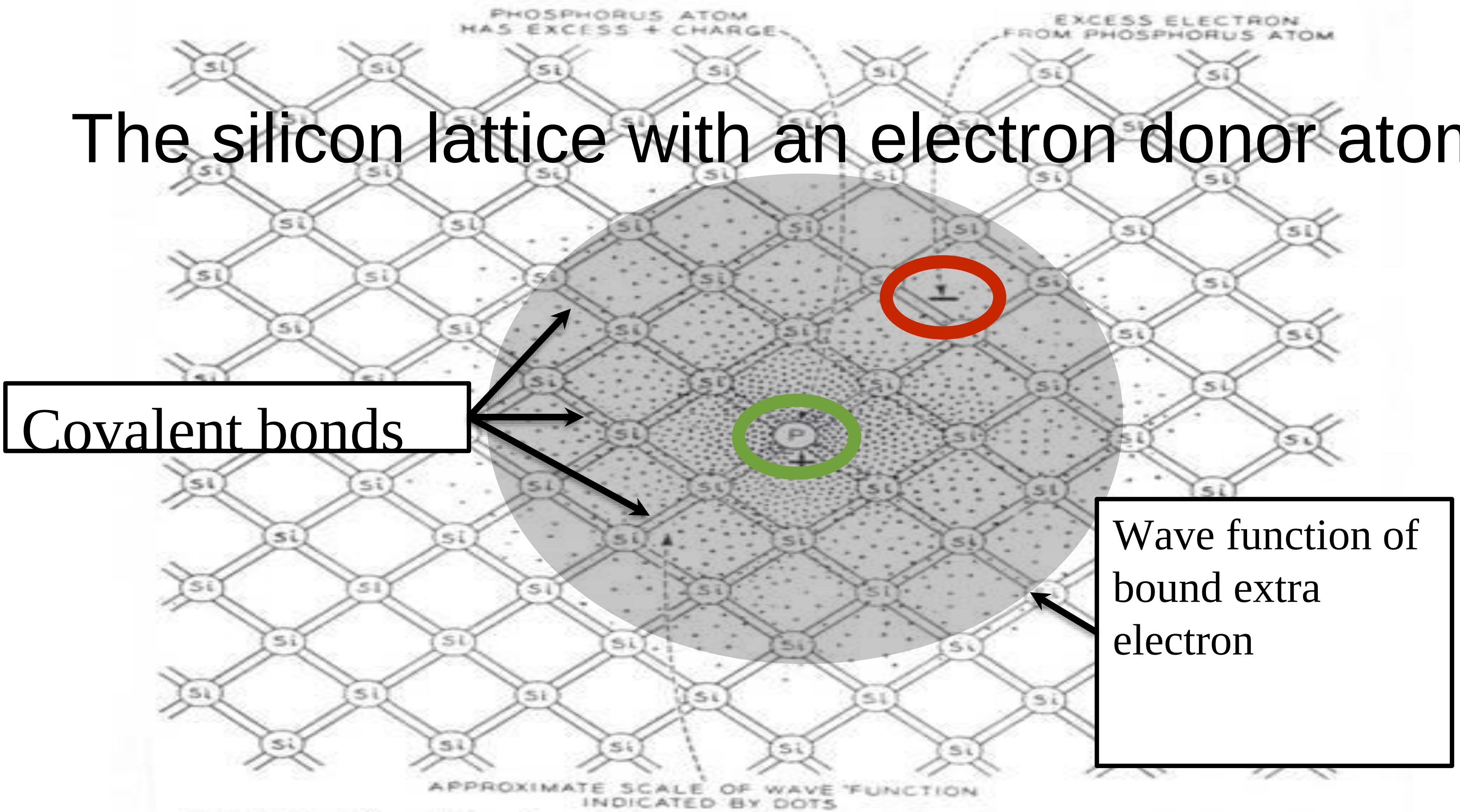
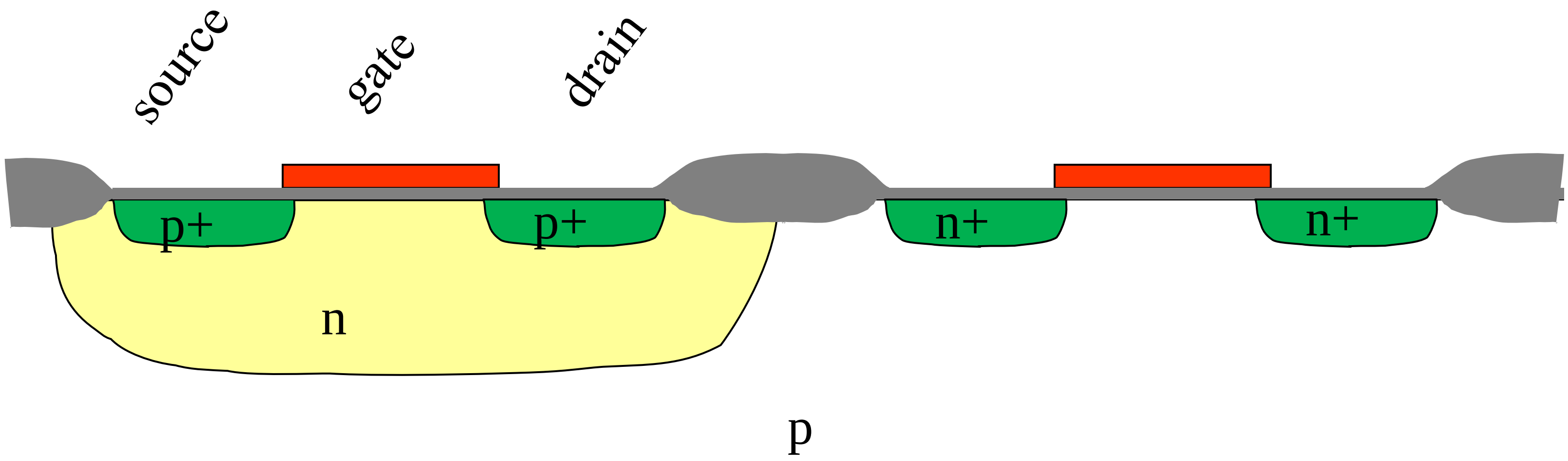
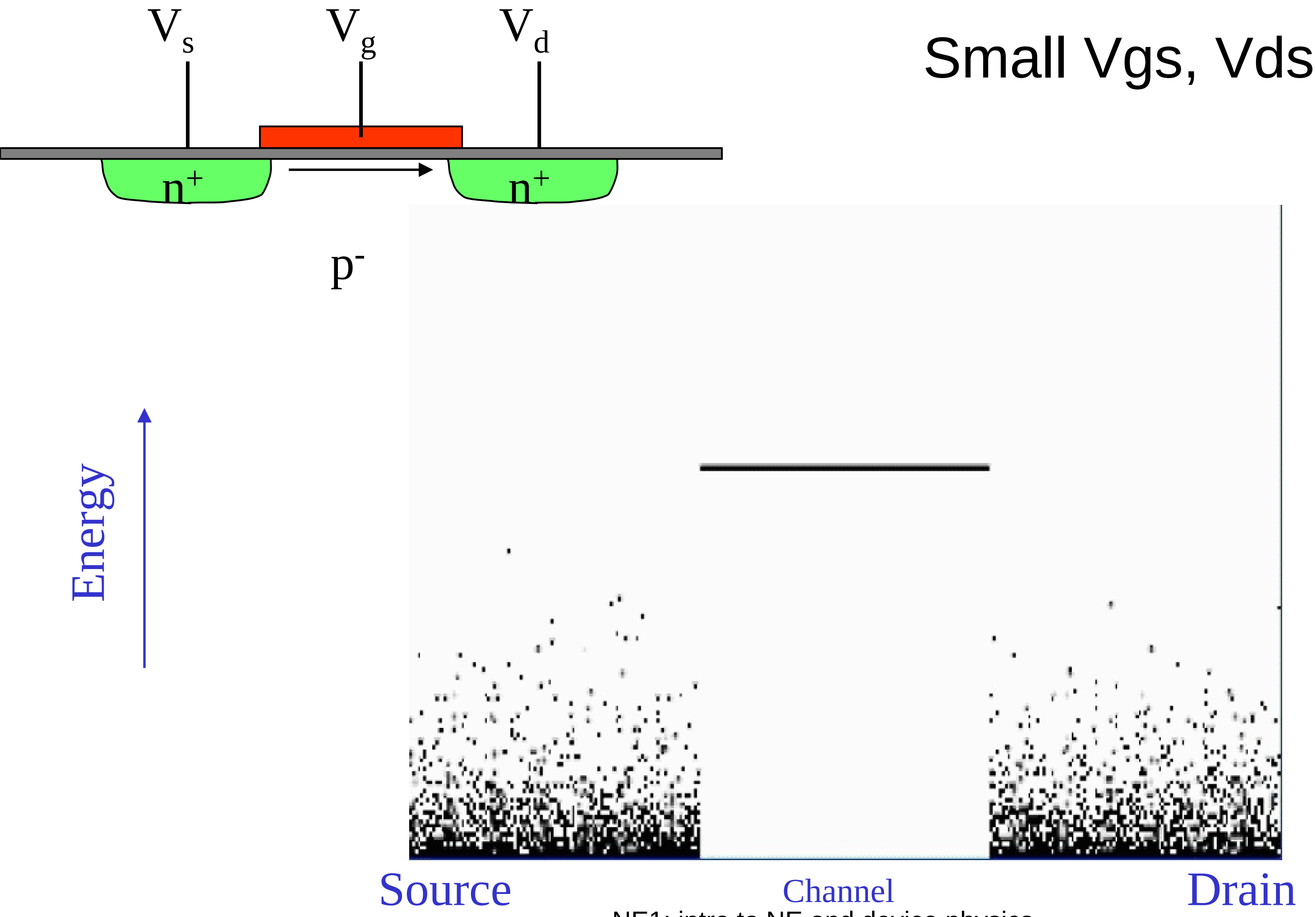


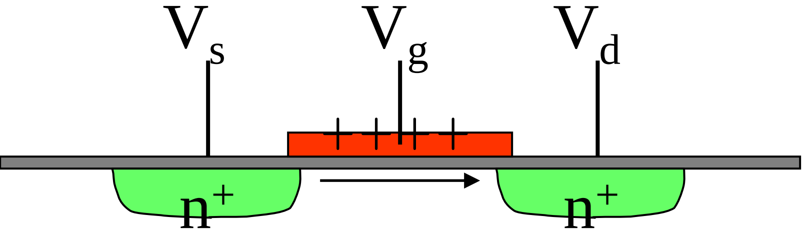
FIG. 1–14—Wave Function of Electron Bound to Phosphorous Atom in Silicon.

MOS transistors use insulated gates to control barrier energies at PN surface junctions at source and drain

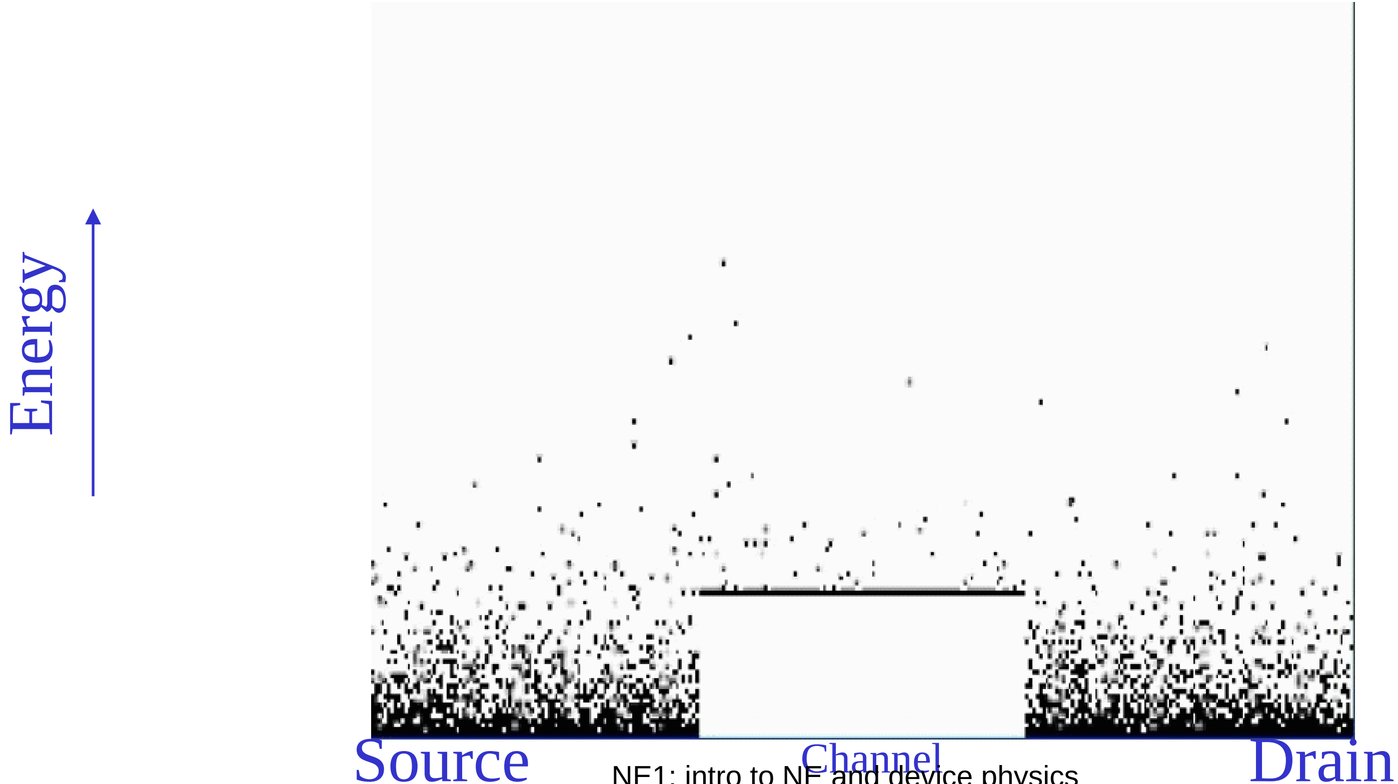


Small Vgs, Vds=0

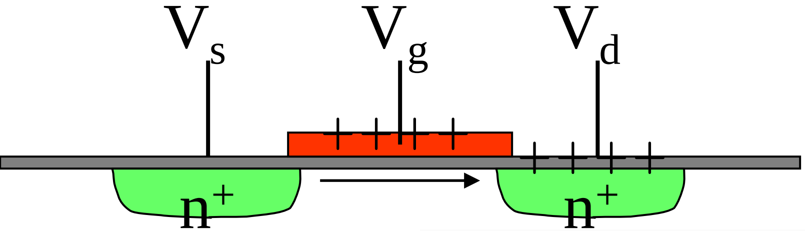


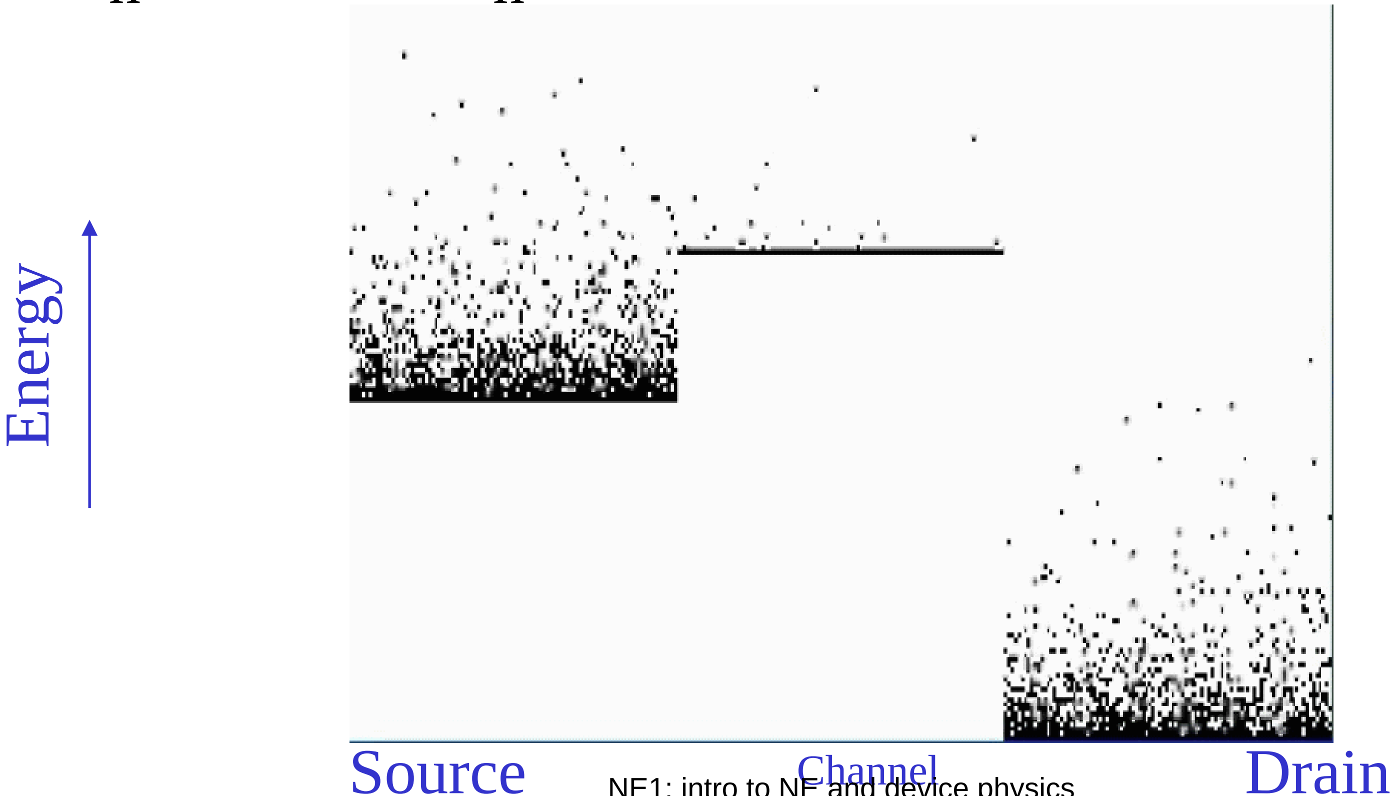


Larger Vgs, Vds=0



Larger Vgs, Large Vds



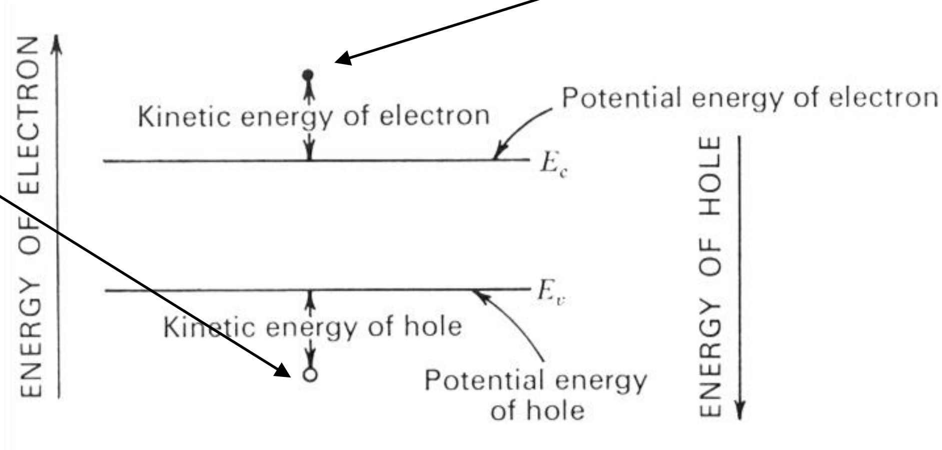


Electrons and *Holes*

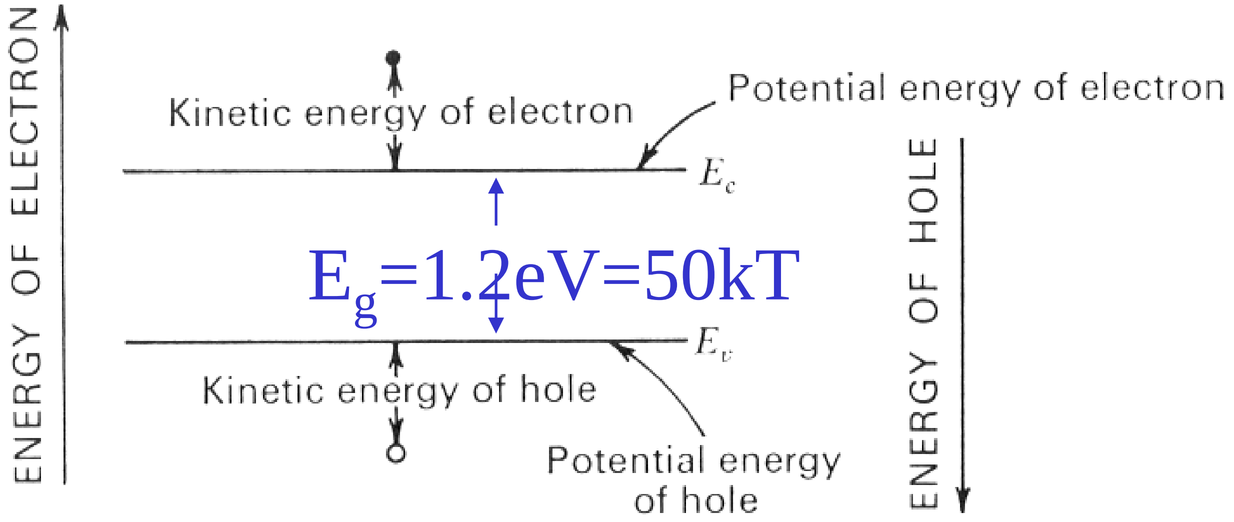
Holes are bubbles in the valence band

- The electrons move, but it is easier to talk about the vacancy (the hole) moving, just like it is easier to talk about a bubble moving than about the water around it moving
- Holes have positive charge and the *effective mass* in silicon is 2.5 times larger for a hole than for an electron

When electrons are broken loose from the lattice and enter the *conduction band*, they become *mobile*, and move almost as if in vacuum



The meaning of energy in the band diagram



The *band gap* of silicon is about 1.2eV at room temperature

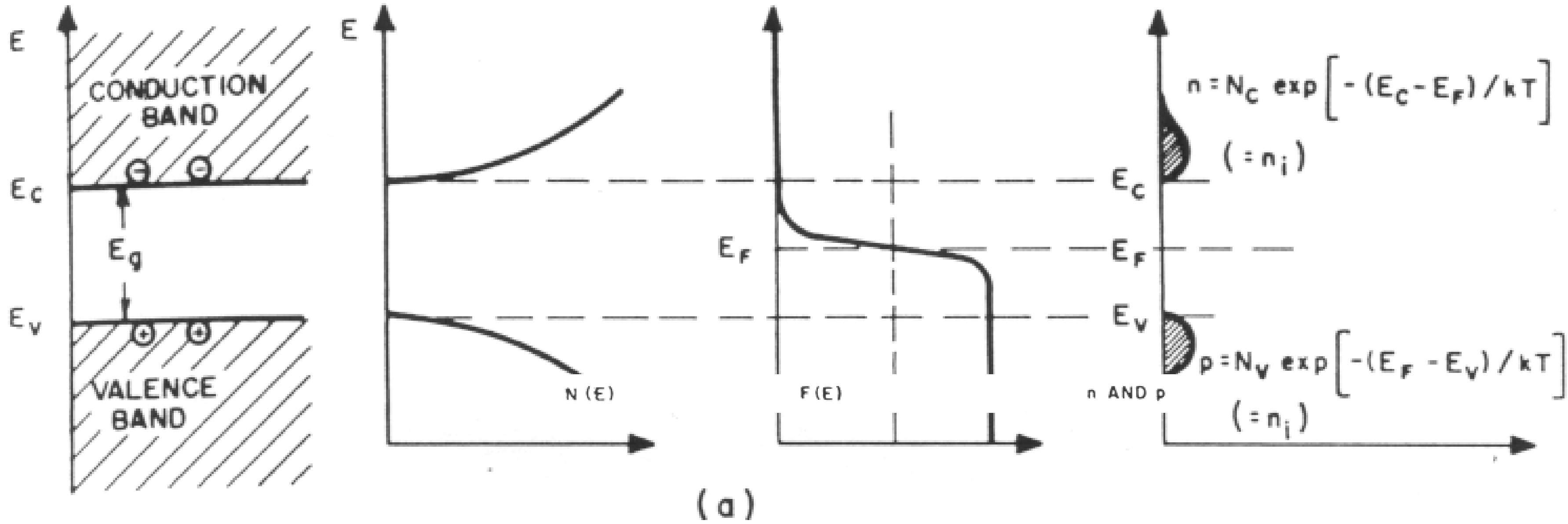
The *thermal energy*

- Each *degree of freedom* of a system in thermal equilibrium has average energy ***kT/2***, where ***k*=1.38 × 10^{-23} J/K** is **Boltzmann's constant** and ***T*** is absolute temperature. I.e. at 300C, *kT*=4.1 × 10^{-21} J
- The **<u>thermal voltage</u>** ***kT/q*** is the voltage a single charge falls through to pick up the thermal energy *kT*
- ***q*** *i*s the ***elementary charge*** 1.6 x 10^{-19} C
- **$U_T \equiv kT/q$=25mV**=1/40V at room temperature
- ***kT/q*** **is the natural scale of voltage for electronic systems in thermal equilibrium**

Intrinisic carrier density in silicon

- Concentration (density) of Si is about $10^{23}/\text{cm}^3$.
- n_i is the *intrinsic carrier density*
- At room temperature n_i is $10^{10}/\text{cm}^3$, or about $1/10^{13}$ Si atoms.
- n_i increases with temperature

An *intrinsic* (undoped) semiconductor



Band diagram

Density of states

Fermi-Dirac distribution

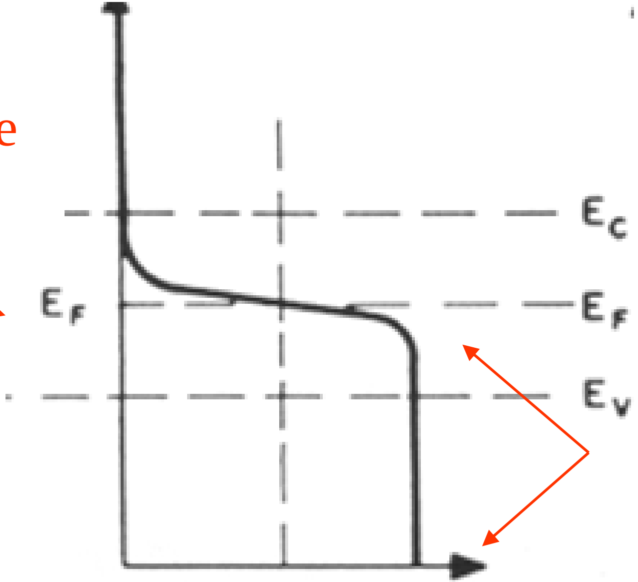
Carrier concentrations

Fermi-Dirac distribution

States above Fermi level are **occupied** with Boltzmann distribution

$$p(\text{occupied}) \approx e^{-(E-E_f)/kT}$$

States at the Fermi level are ½ occupied

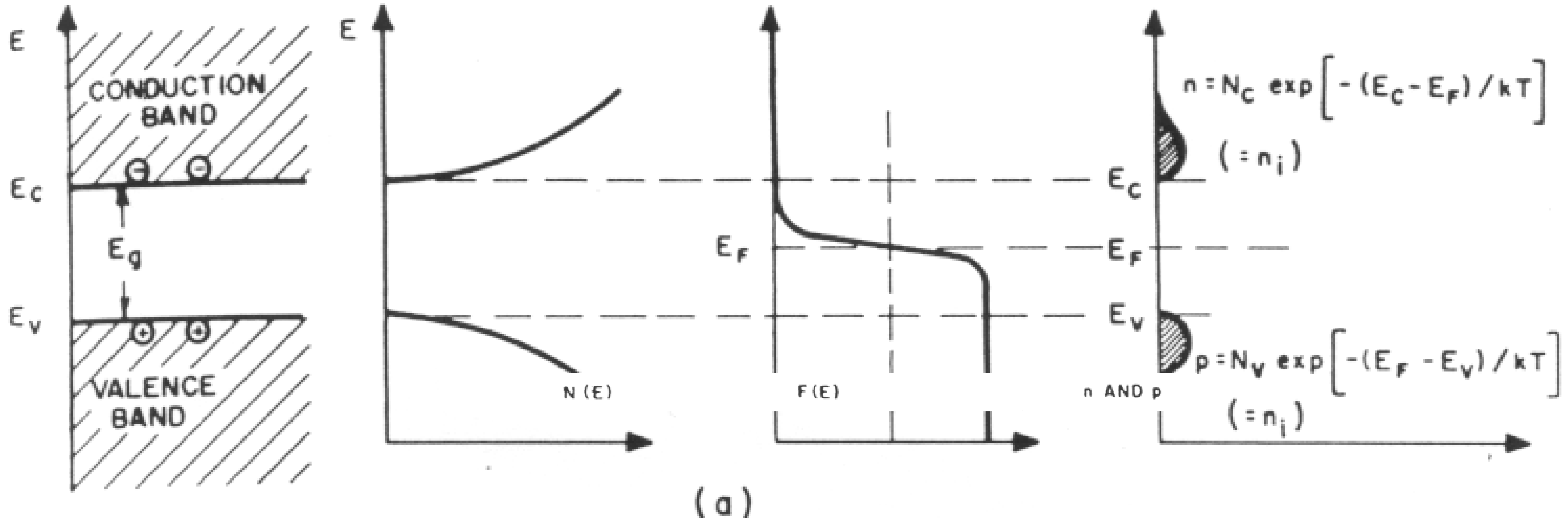


(a)

States below Fermi level are **unoccupied** with Boltzmann distribution

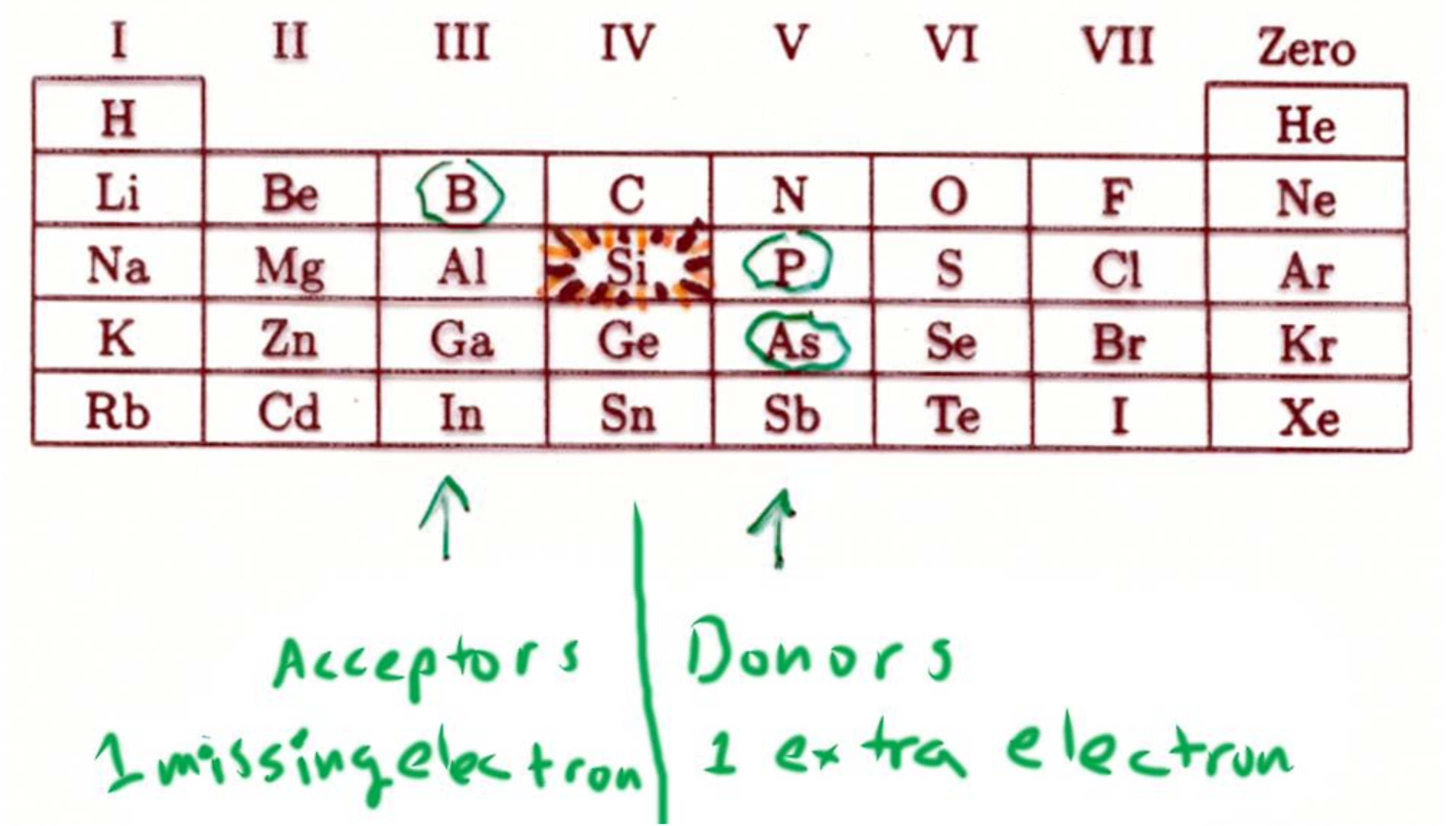
$$p(\text{unoccupied}) \approx e^{-(E_f-E)/kT}$$

An *intrinsic* (undoped) semiconductor



Band diagram | Density of states | Fermi-Dirac distribution | Carrier concentrations

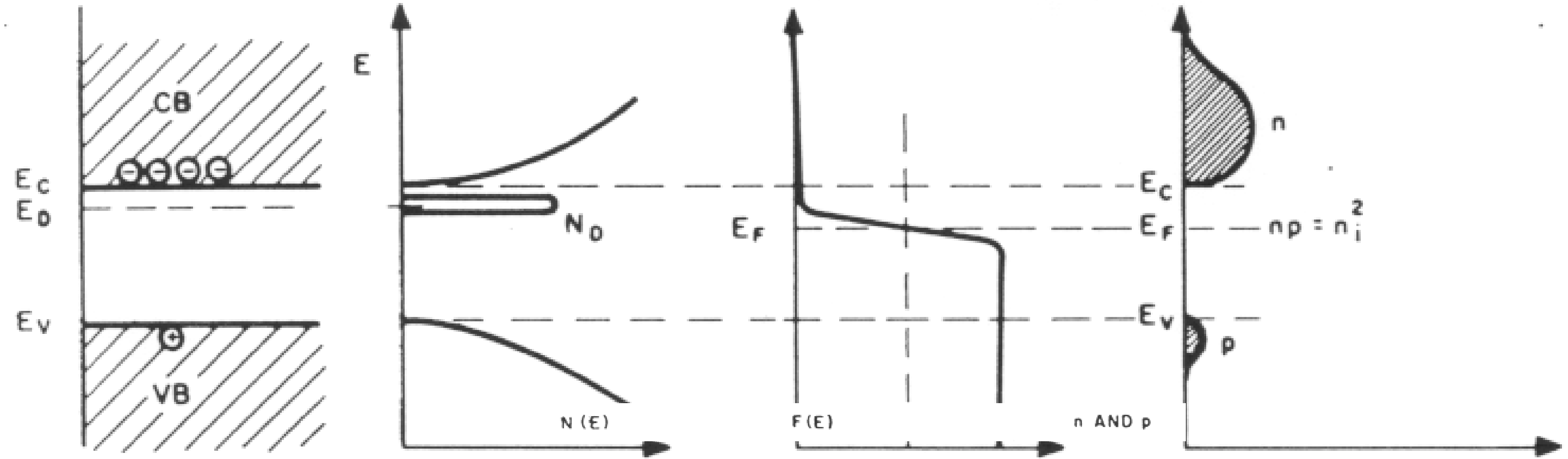
Donors and acceptors in the periodic table



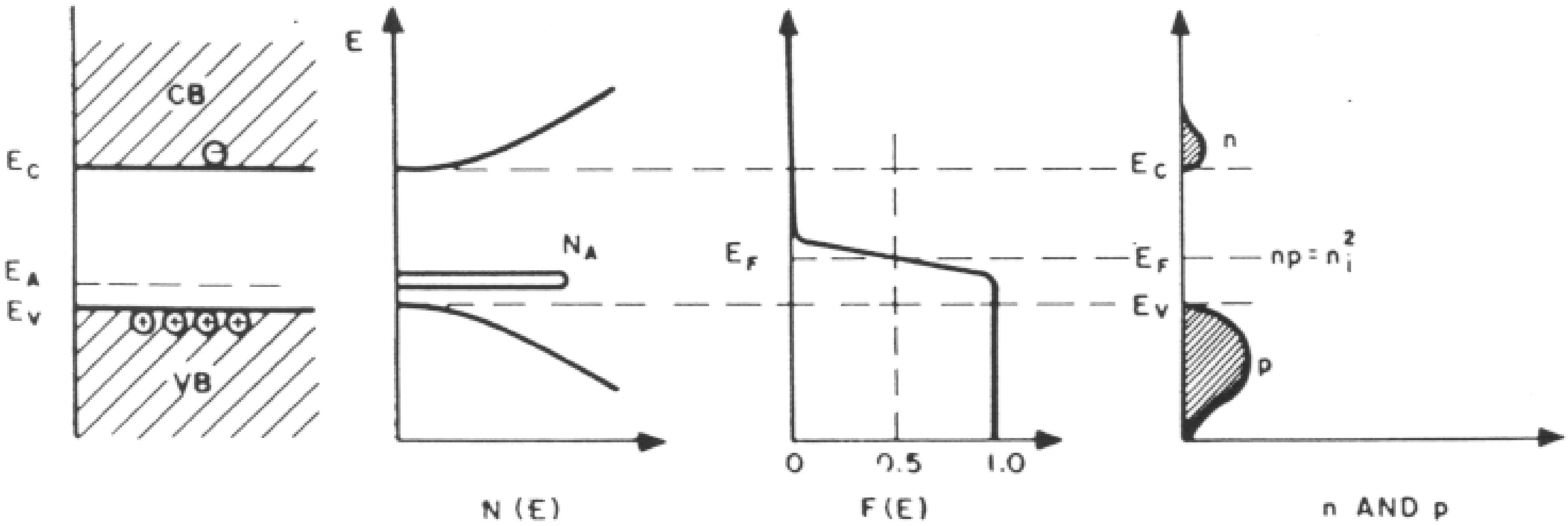
Doping levels

- Concentration (density) of Si is about $10^{23}/cm^3$
- Doping can vary from about $10^{15}/cm^3$ to $10^{19}/cm^3$
- These doping levels still represent only a tiny fraction of the total atoms, from 10^{-8} to 10^{-4}

An *n-type* semiconductor



A *p-type* semiconductor



Law of mass action: $\boldsymbol{np=n_i^2}$

- n_i is the *intrinsic carrier density*
- In equilibrium, more holes means less electrons, and vice-versa.

Electron transport

1. *Drift* and *Diffusion*
2. *Mobility*
3. The *Einstein relation*

An electric field causes carriers to <u>drift</u>

Velocity

$$J_{drift} = qn\upsilon = qn\mu(\xi)$$

Electric field

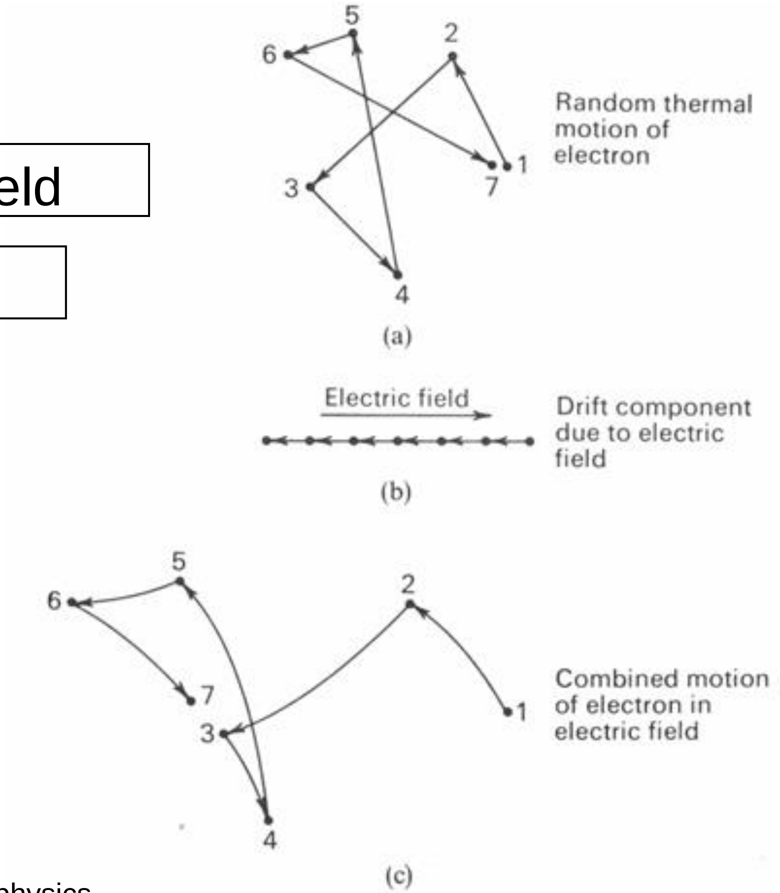
Mobility

Current flux

Charge density

$$J_{drift} \approx qn\mu\xi$$

for $\vec{\xi}$ that causes velocities much less than the thermal velocity of ≈ 100 km/s



Mobility is a function of electric field

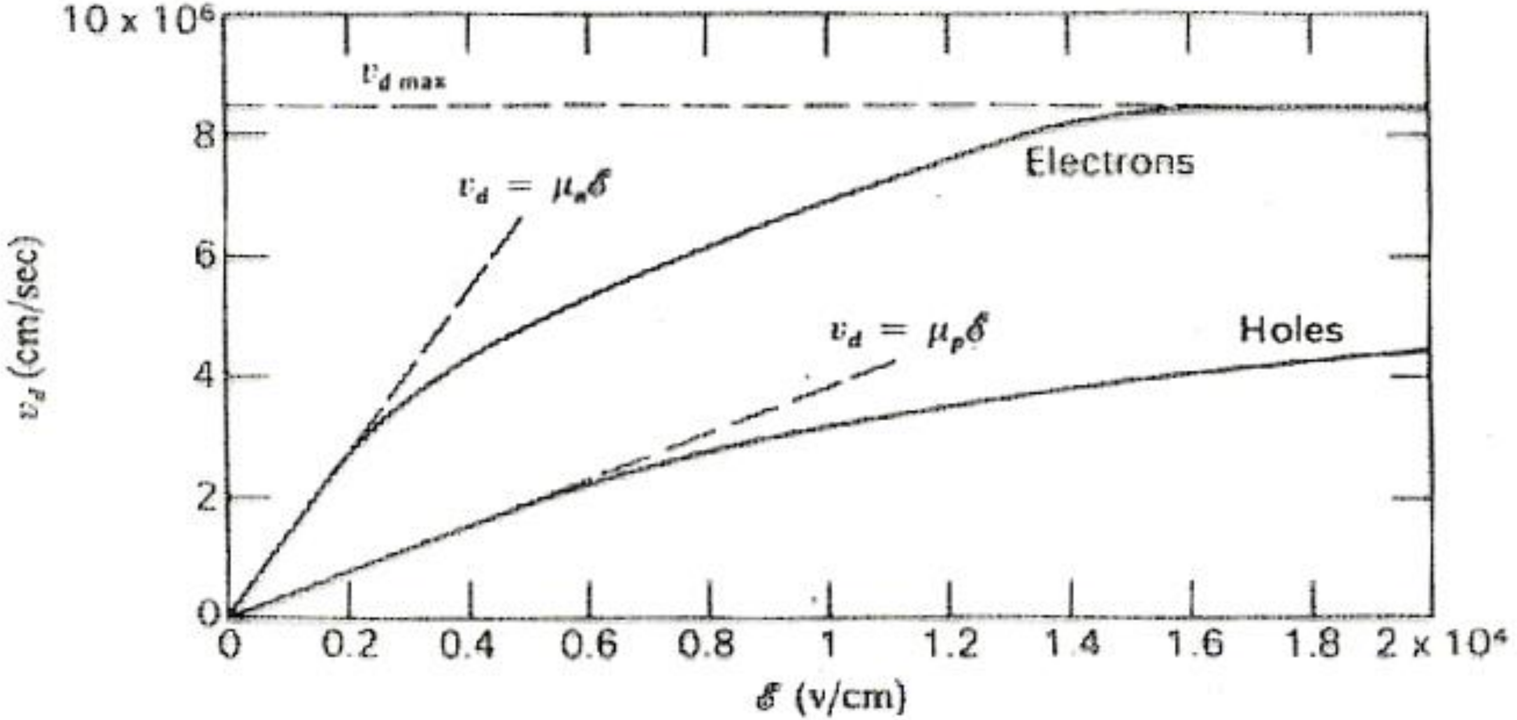
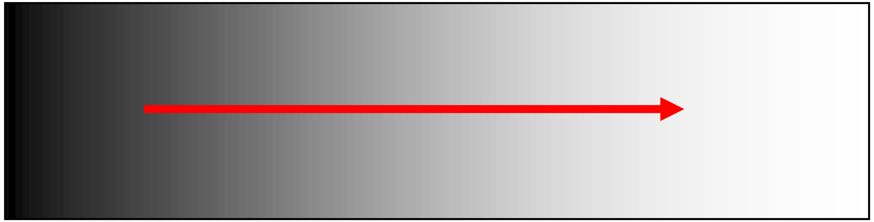


Fig. 4.10 Effect of electric field on the magnitude of the drift velocity of carriers in silicon.[3]

A density gradient causes carriers to <u>diffuse</u>



Diffusion current

$$J_{diff} = -Dq\nabla n$$

Current flux

Diffusion constant

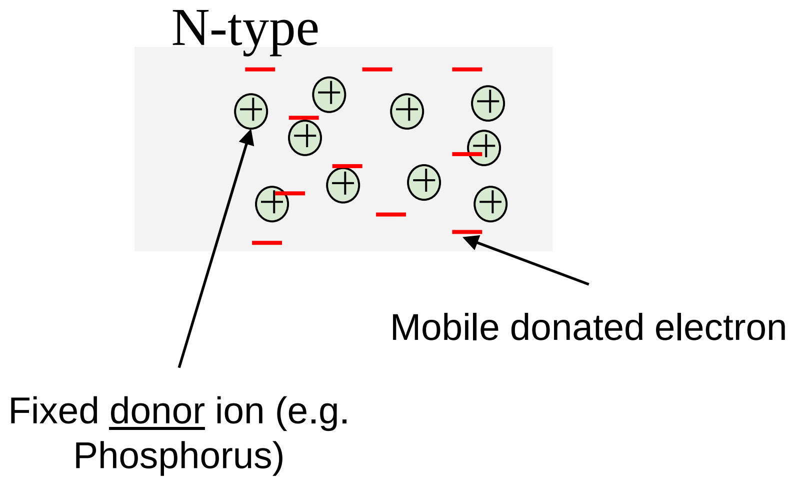
Spatial gradient of charge density

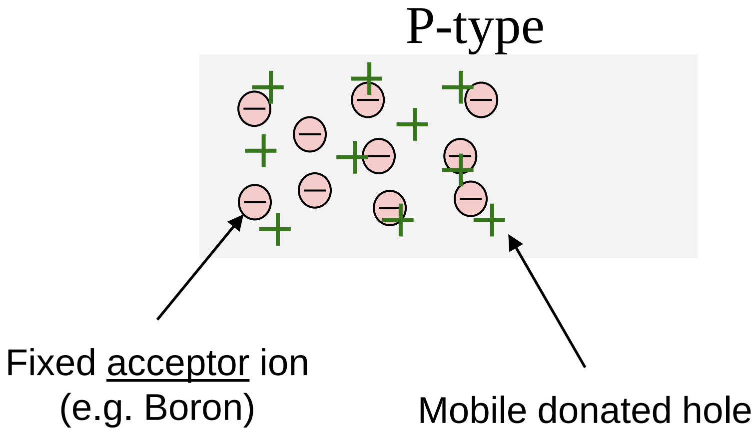
Drift and diffusion are related by the *Einstein Relation*

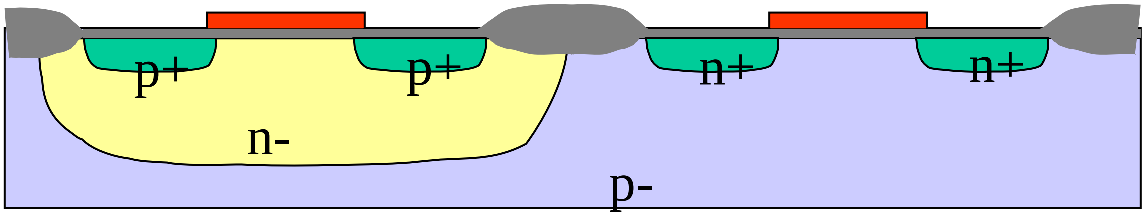
$$J_{diff} = -Dq\nabla n \qquad\qquad J_{drift} = qn\mu\xi$$

$$D = \frac{kT}{q}\mu$$

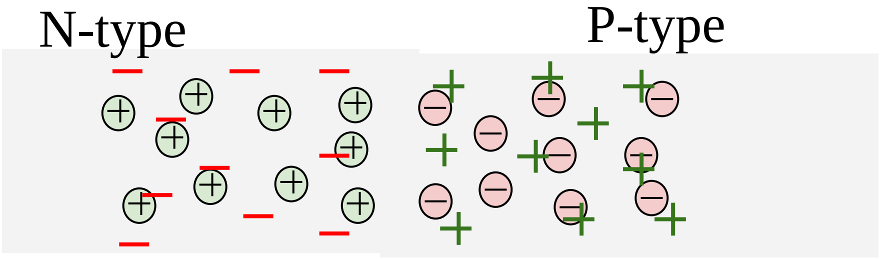
Charges, fields, and potentials in a PN junction







What happens at a junction between P and N?



Lots of mobile electrons

Lots of mobile holes

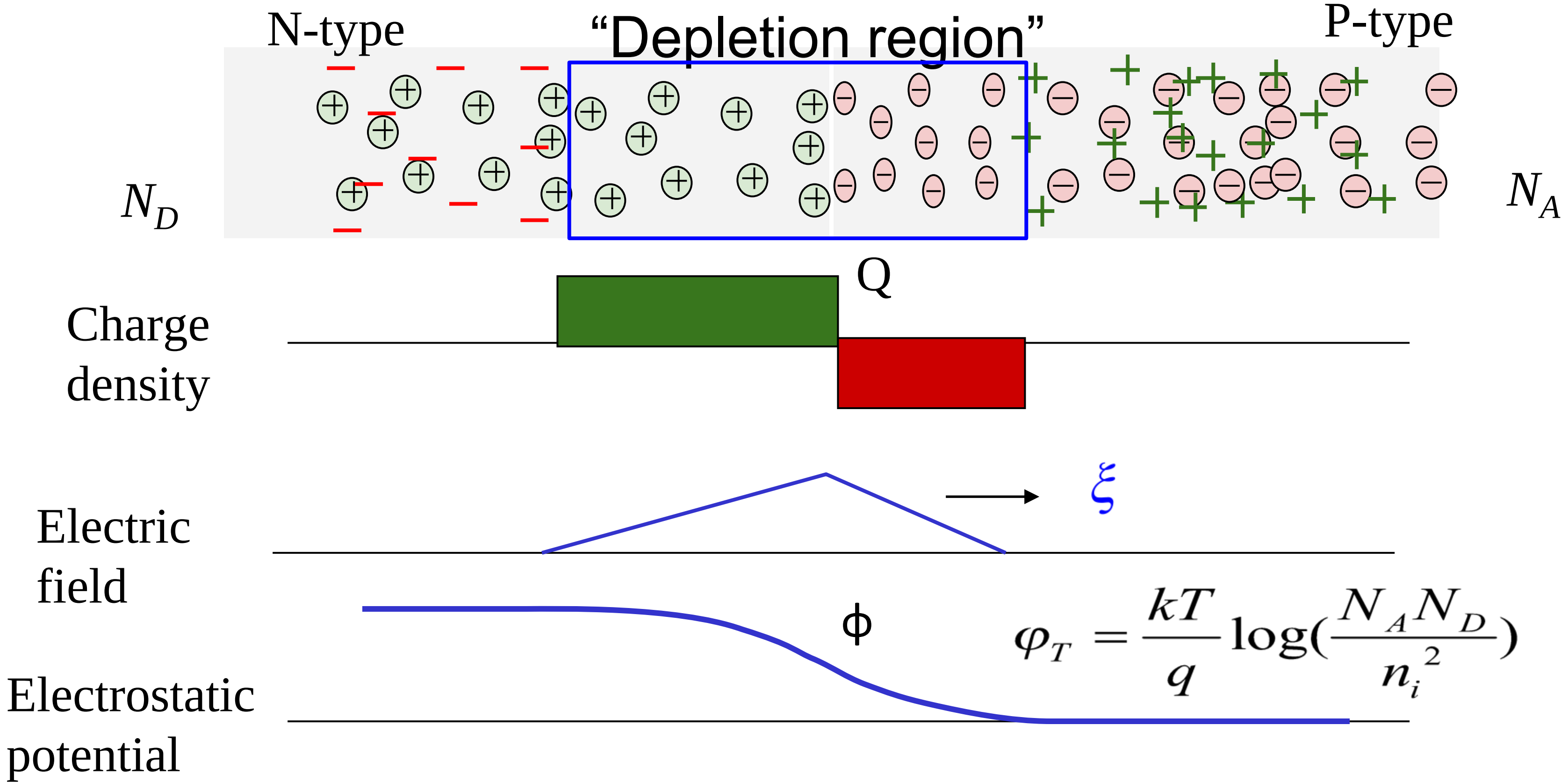
Electron density gradient:
Electrons diffuse rightwards

Hole density gradient:
Holes diffuse leftwards

The charge separation builds up an electric field to pull the carries “back home”

In a PN junction with no applied voltage, <u>drift and diffusion are balanced everywhere</u>

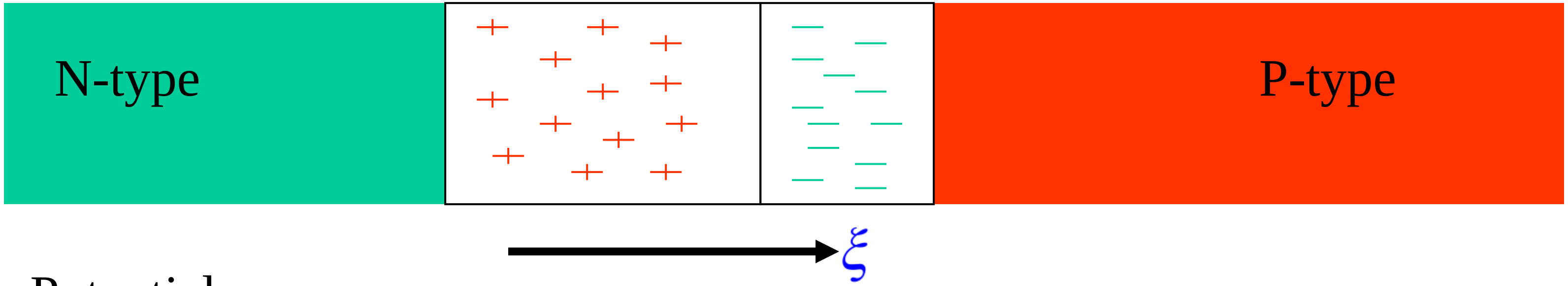
Charges, fields, and potentials in a PN junction



$$\varphi_T = \frac{kT}{q}\log\left(\frac{N_A N_D}{n_i^{\,2}}\right)$$

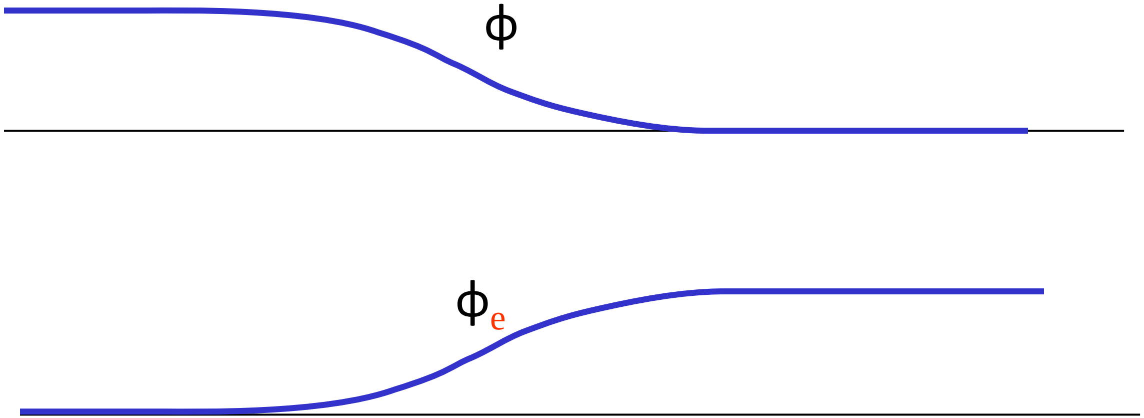
Typically, the *built-in voltage*, φ_T, is about 0.75V

Electrostatic potentials in a PN junction

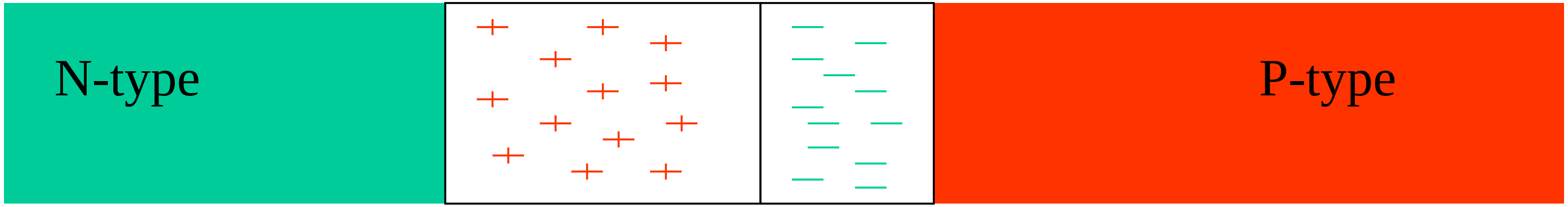


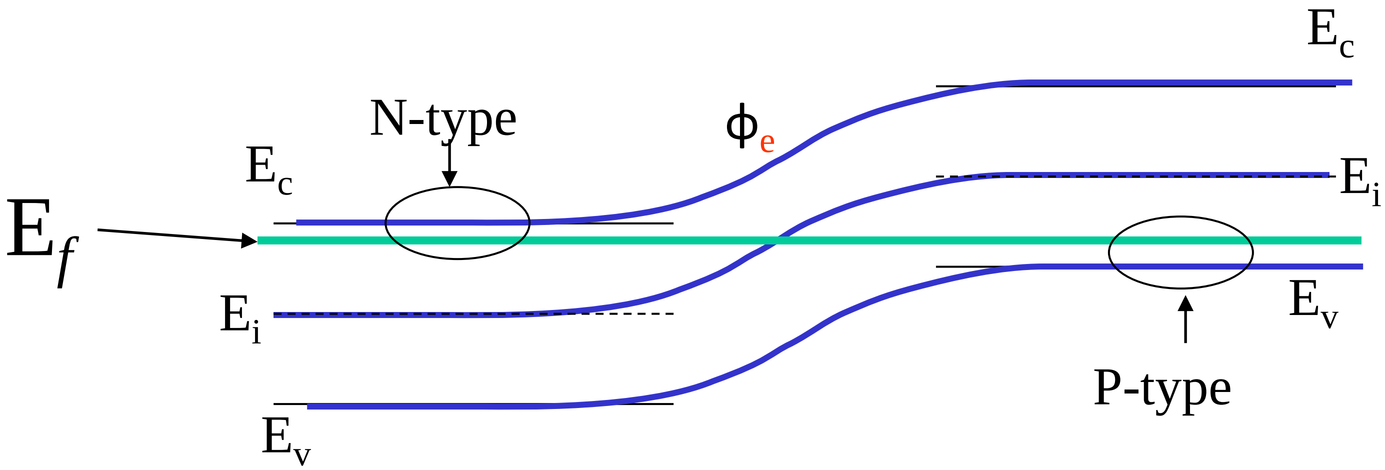
Electrostatic Potential: potential energy of positive charge

Potential energy of negatively charged electron

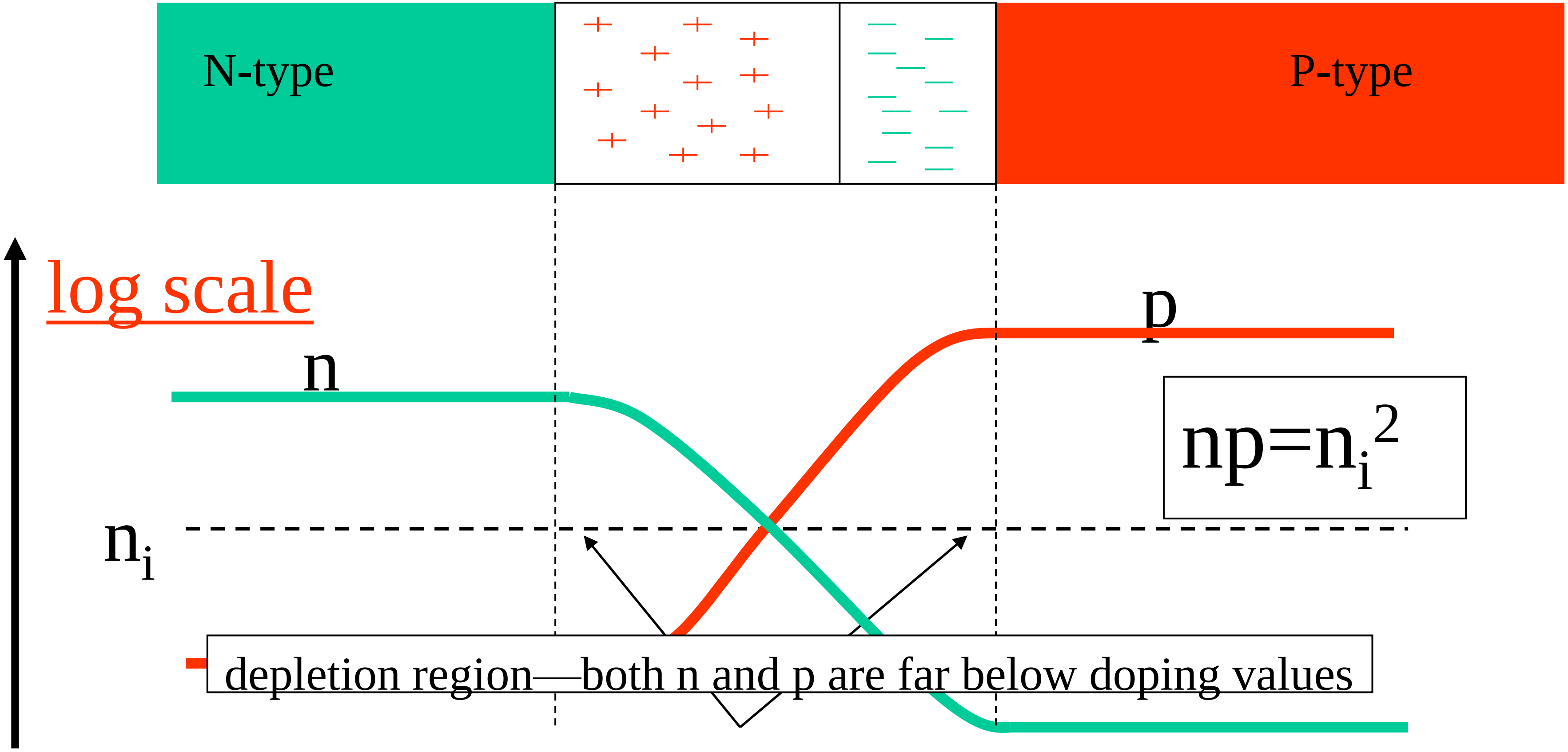


Band structure of a PN junction

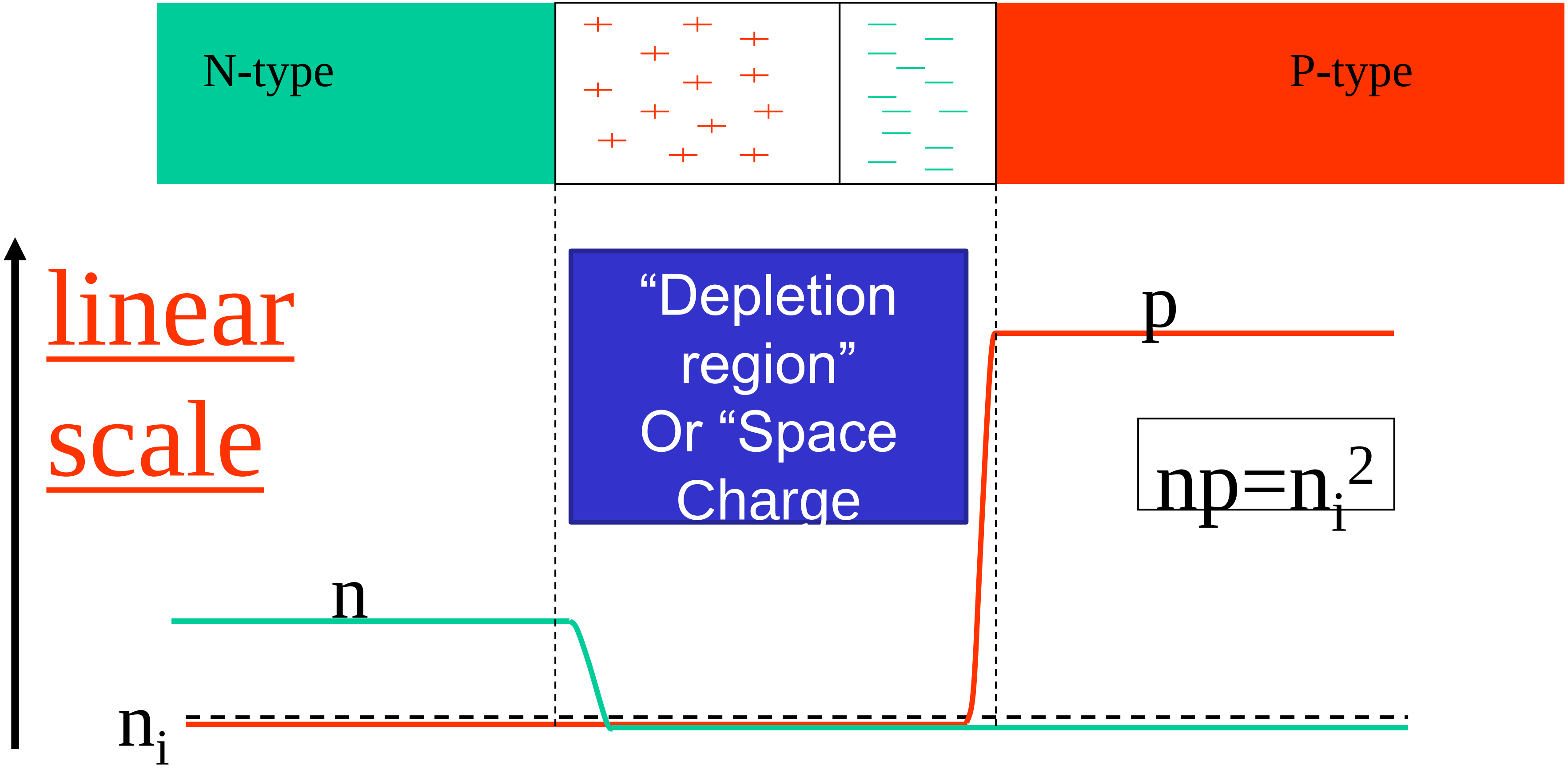




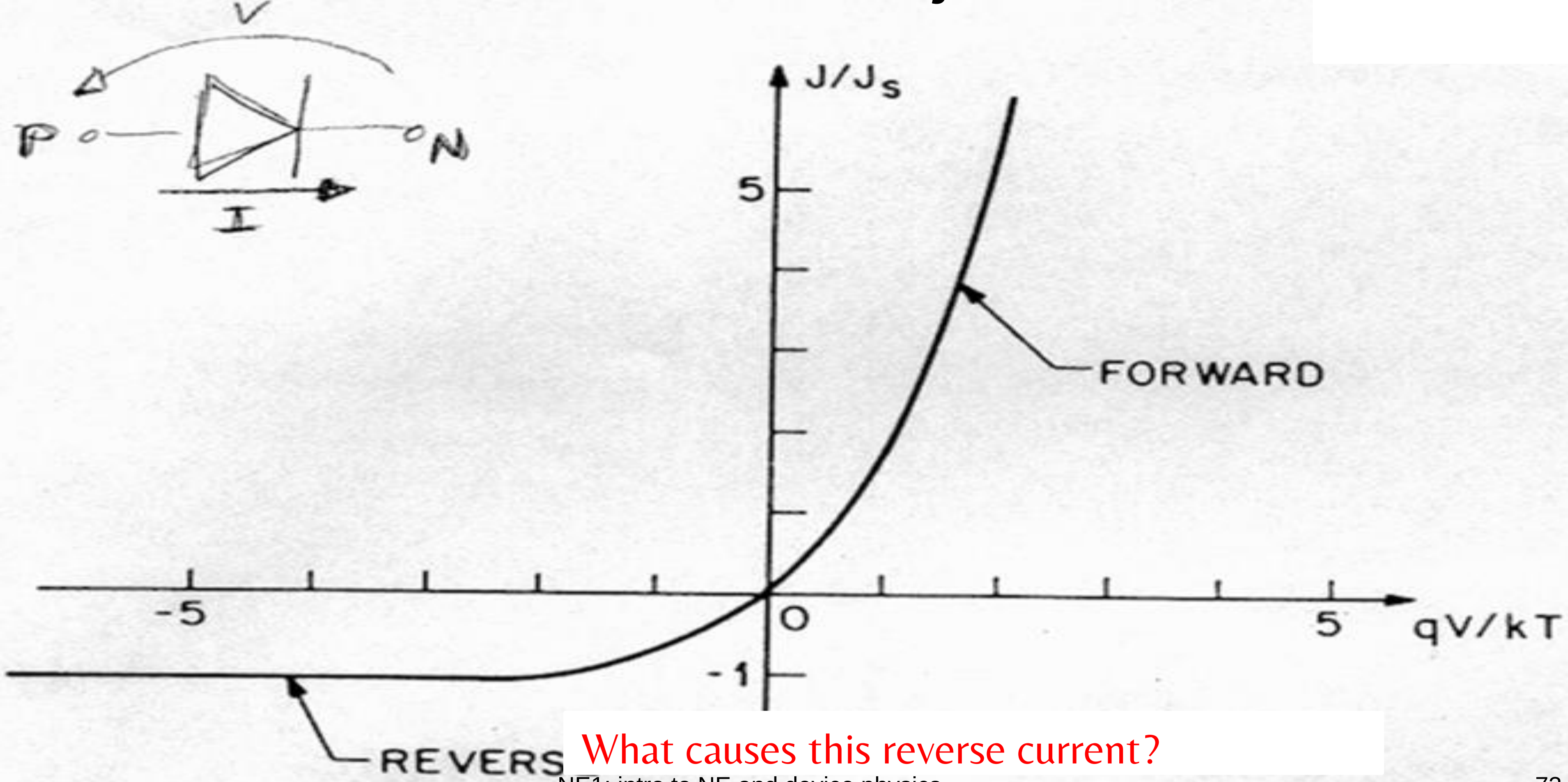
Carrier densities in a PN junction



Carrier densities in a PN junction

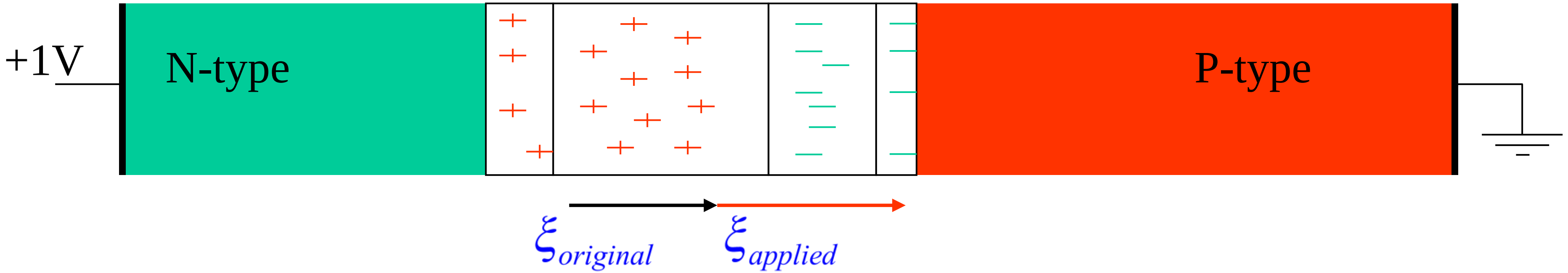


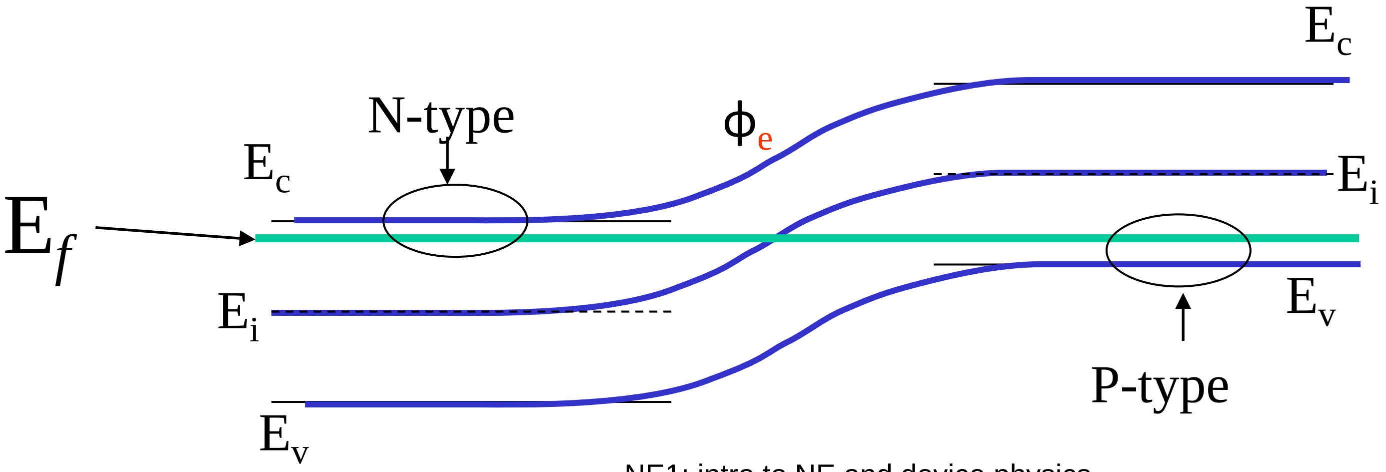
I-V characteristics of a PN junction “rectifier”



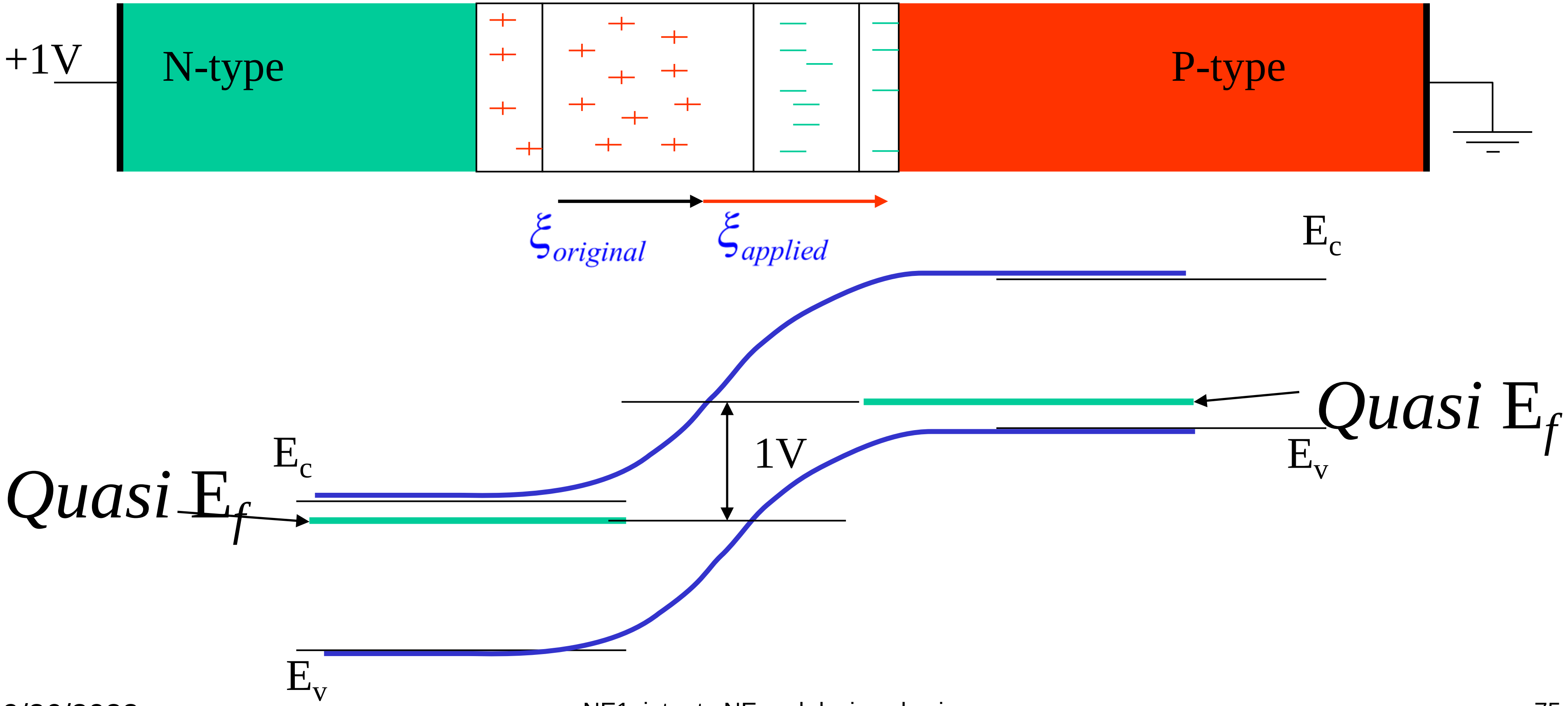
What causes this reverse current?

A reverse-biased PN junction

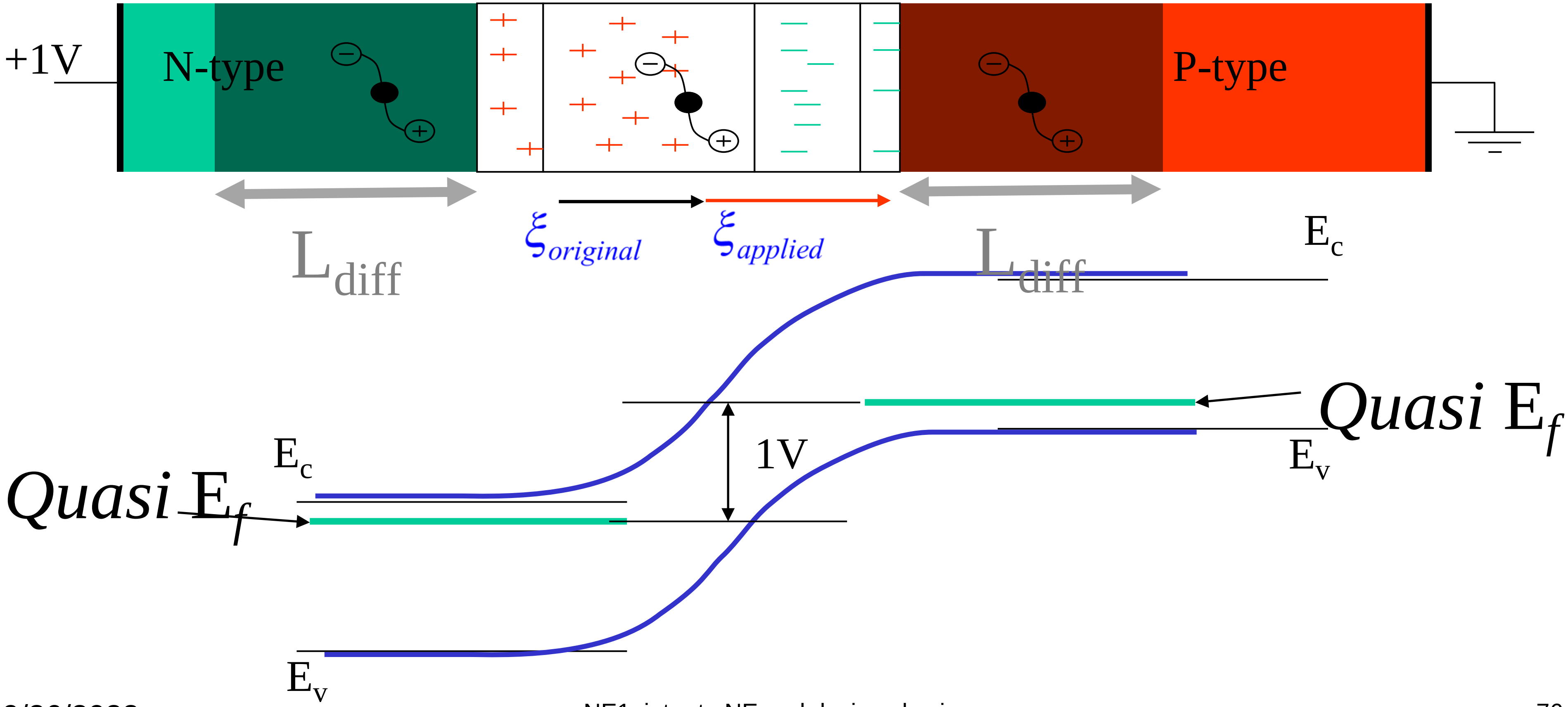




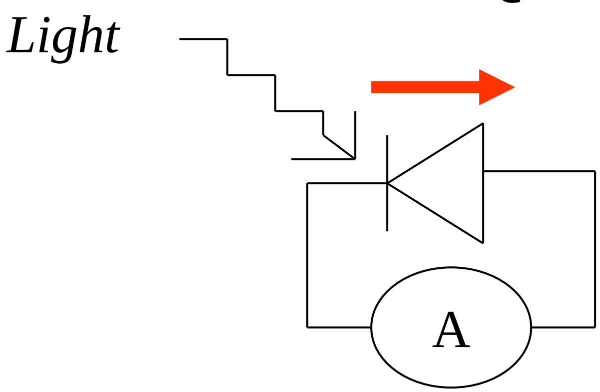
A reverse-biased PN junction



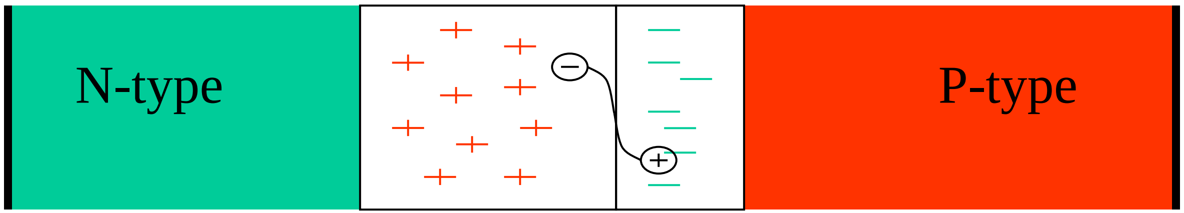
Reverse current comes from generated electron hole pairs in 3 regions



Question

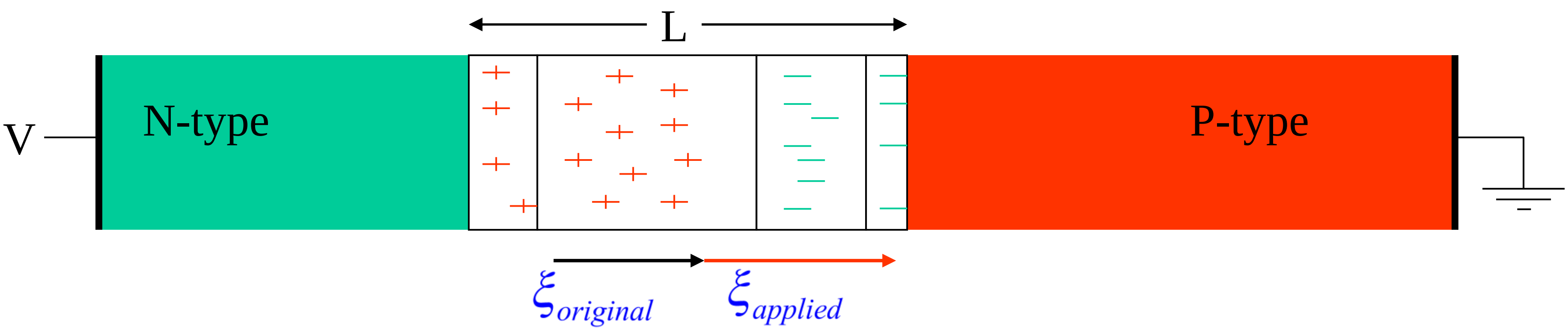


What happens when light shines on the junction?
Which way does current flow?



Answer: light tries to <u>forward bias</u> the junction.

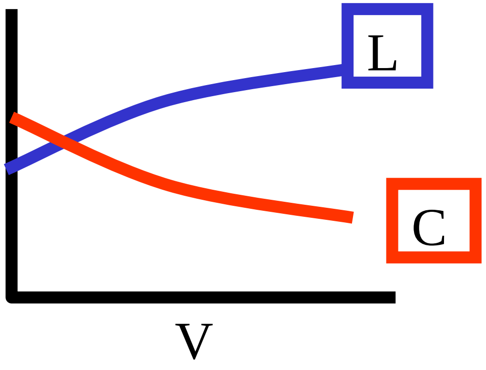
What is capacitance of reverse-biased PN junction?



$C = \varepsilon_{Si}/L$

As V increases, L increases.

So, as V increases, C decreases



What was covered

- Insulators, conductors, semiconductors
- Crystal structure of silicon
- Band structure (valence, conduction, and forbidden bands)
- Holes and electrons
- Mechanisms of charge transport (diffusion & drift)
- Doping with donors and acceptors
- Fermi-Dirac distribution
- Law of mass action ($np=n_i^2$)
- p-n junction
- Reverse biased junction and its capacitance in reverse bias

Next week:
Understanding how MOS transistors work in the subthreshold/weak inversion regime