SLIATE

SRI LANKA INSTITUTE OF ADVANCED TECHNOLOGICAL EDUCATION
(Established in the Ministry of Higher Education, vide in Act No. 29 of 1995)

Higher National Diploma in Information Technology

2nd Year, Second Semester Examination – 2016

IT 3002 - Computer Architecture

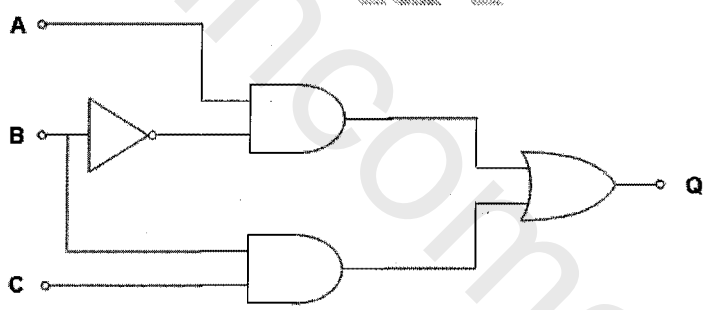
Model Answers

Instructions for Candidates:
Answer any 4 questions.

No. of questions : 05
No. of pages : 05
Duration : 2 hrs

Q1. (Total 25 marks)

(i). Consider the following logic circuit



a). **Draw the truth table for the circuit.** (04 Marks)

A	B	$\overline{B}$	C	$A.\overline{B}$	B.C	Q
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	1	1
1	0	1	0	1	0	1
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	1	1

b). **Give the Boolean expression for the above circuit.** (04 Marks)

$$Q = A.\overline{B} + B.C$$

(ii). **Simplify the following Boolean expressions using Boolean algebra. (Mention suitable laws in each steps)** (10 Marks)

a). X = C.(A+C')

X = C.(A+C')
X=C. A + C.C'
X=C.A + 0 (According to the complement theory)
X= A.C

(02 marks)

b). Y = A.C'+A.B.C'+ A'C'D' +A'C'D (02 marks)

Y=A.C' (1+B) + A'.C' (D'+D) (According to the complement theory)
Y=A.C'+ A'.C'
Y=C'(A+A')
Y=C'.1
Y=C'

c). Z = *AB+ A'C + BC* (06 marks)

= *AB* + *A'C* + *BC*(1) (Identity)
= *AB* + *A'C* + *BC*(*A* + *A'*) (Inverse)
= *AB* + *A'C* + (*BC*)*A* + (*BC*)*A'* (Distributive)
= *AB* + *A'C* + *A*(*BC*) + *A'*(*CB*) (Commutative)
= *AB* + *A'C* + (*AB*)*C* + (*A'C*)*B* (Associative)
= *AB* + (*AB*)*C* + *A'C* + (*A'C*)*B* (Commutative)
= *AB*(1 + *C*) + *A'C*(1 + *B*) (Distributive)
= *AB*(1) + *A'C*(1) (Null)
= *AB* + *A'C* (Identity)

(iii). **Apply DeMorgan's theorem to simplify** $\dfrac{\overline{A+\left(\overline{B+C}\right)}}{\overline{A+(\overline{B}.\overline{C})}}$ (02 Marks)

$$\overline{A}.(\overline{\overline{B}+\overline{C}})$$

$$\overline{A}.(B+C)$$

$$\overline{A}B+\overline{A}C$$

(iv). Simplify the following Boolean function F using K-Map

F = AB'C + AB'C' + A'B'C + A'B'C' (05 Marks)

C \ AB	00	01	11	10
v0	1	0	0	1
1	1	0	0	1

3 marks for K map table

1 marks for correct grouping

1 marks for answer

Minimized result is $\overline{B}$.

Q2. (Total 25 marks)

(i). Briefly explain the following:

a). PC (Program Counter)

A special register, determines the location in memory (memory address) from which the next instruction will be fetched.

b). MAR (Memory Address Register)

CPU register that either stores the memory address from which data will be fetched to the CPU or the address to which data will be sent and stored.

c). MBR (Memory Buffer Register)

Contains the data that was read or that is going to be written to the memory.

d). ALU (Arithmetic and Logical Unit)

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logical operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerful and complex ALUs. (2x4 Marks)

(ii). **Briefly explain Opcode and Operand in a machine instruction.** (04 Marks)

An opcode means 'Operation Code'. It is a single instruction that can be executed by the CPU. Opcode is a command such as MOV or ADD or JMP.

Eg: MOV, AL, 34h

According to the above example, the opcode is the MOV instruction. The other parts are called the 'operands', the operands are the register named AL and the value 34 hex.

(iii). Explain instruction pipelining and mention at least 4 stages of pipelining. (04 Marks)

Instruction pipelining is a technique that implements a form of parallelism called instruction-level parallelism within a single processor. It therefore allows faster CPU throughput (the number of instructions that can be executed in a unit of time) than would otherwise be possible at a given clock rate. The basic instruction cycle is broken up into a series called a pipeline. Rather than processing each instruction sequentially (finishing one instruction before starting the next), each instruction is split up into a sequence of steps so different steps can be executed in parallel and instructions can be processed concurrently (starting one instruction before finishing the previous one). (2 marks)

1. **Fetch instruction**
2. **Decode instruction**
3. Calculate operands (i.e., EAs)

4. Fetch operands
5. **Execute instructions**
6. Write result (3 essential stage or more stage 2 marks)

(iv). "Instruction pipelining increases the through put of CPU. But some of the problems appear, which are reduce the through put of CPU during pipelining." Identify and analyse three problems which are decrease the performance of pipelining.

Pipeline Hazards are situations that prevent the next instruction in the instruction stream from executing in its designated clock cycle

Hazards reduce the performance from the ideal speedup gained by pipelining

Three types of hazards

a). ***Structural hazards***
   i. Arise from resource conflicts when the hardware can't support all possible combinations of overlapping instructions(2 marks)

b). ***Data hazards***
   i. Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline

c). ***Control hazards***
   i. Arise from the pipelining of branches and other instructions that change the PC (Program Counter)

1 marks for every hazards and 2 marks for descriptions.

(3X3 Marks)

Q3. (Total 25 marks)

(i). Compare and contrast the Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM). (04 Marks)

a) SRAM is static while DRAM is dynamic

b) SRAM is faster compared to DRAM
c) SRAM consumes less power than DRAM
d) SRAM uses more transistors per bit of memory compared to DRAM
e) SRAM is more expensive than DRAM
f) Cheaper DRAM is used in main memory while SRAM is commonly used in cache memory

(ii). **Briefly explain "Seek Time", "Rotational Latency" and "Transfer Time" of a hard disk drive operation.** (06 Marks)

The seek time measures the time it takes the head assembly on the actuator arm to travel to the track of the disk where the data will be read or written.

Rotational latency (sometimes called rotational delay or just latency) is the delay waiting for the rotation of the disk to bring the required disk sector under the read-write head.

The transfer time for a disk operation is the time required to transfer the data from (or to) the disk surface to (or from) the computer once the start of the data is under the R/W head.

Transfer time is based on:

1 - Speed of rotation
2 - Density of data on the track
3 - Amount of data to be transferred

(iii). **Consider the following details of a Hard Disk:** (06 Marks)

Average seek time = 6 ms.
Disk rotation speed = 7600 rpm
512 bytes/sector
400 sectors/track (on average)
20,000 tracks/surface
Disk has 5 platters

a). Calculate the average rotational latency

$$= \frac{1}{2} X \frac{60}{7600} \; Sec$$

b). Calculate the capacity of this hard disk

=(sectors / track) × (sector size) × (cylinders) ×
(2 × number of platters)

=2 X 5 X 20000 X 400 X 512 Bytes

c). **Calculate the total time needed to read 300KB data file (assume the file is not fragmented)**

$$=6+(\frac{1}{2}X\frac{60}{7600}X1000)+(\frac{300X1024}{512}X\frac{1}{400}X\frac{60}{7600}X1000)\,ms$$

(06 Marks)

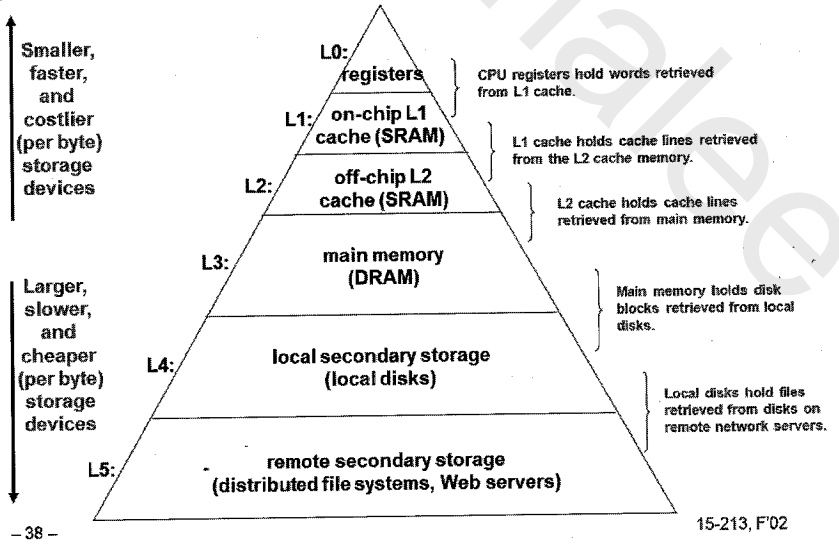
(iv). Explain function of Cache Memory.

Cache Memory: Cache memory, lies in between CPU and the Main memory. It is also called CPU memory that a computer microprocessor can access more quickly than it can access regular RAM. ... The main function of cache memory is to speed up the working mechanism of computer.

(02 Marks)

(v). Using memory hierarchy diagram, explain each type of memory in the hierarchy and their characteristics.

(Atleast 4 levels and 3 characteristics)



(07 Marks)

Q4. (Total 25 marks)

(i). Write down the three type of buses in the CPU system and briefly explain.

.(09 Marks)

(a) Data bus,

(b) Address bus,

(c) Control bus,

(1x 3 marks)

a) Data bus: A bus which carries a word or a data to or from memory is known as data bus. Data lines are bidirectional. One part of the data bus runs between RAM and the microprocessor. Another part of the data bus runs between RAM and various storage devices.

b) Address bus: The address bus carries memory address. It is unidirectional, the bits flow in only one direction.

c) Control bus: The control bus carries the control signals between the units of computers. The signals like READ/WRITE, START/HALT etc are carried by a control bus.

(2X3 marks)

(ii). State down any four (04) major functions of an Input/output Module.

Control & Timing.

CPU Communication.

Device Communication.

Data Buffering.

Error Detection.

Any four

(04 Marks)

(iii). Briefly explain the following techniques in I/O Module.

a). Programmed (polling).

Data are exchanged between the CPU and I/O module. CPU executes a program and issue command directly to the appropriate I/O. I/O module performs the requested action and set the appropriate bits in the I/O status register. No further action to alert the CPU. CPU waits for I/O

module to complete operation. Periodically checks the I/O status register. This wastes CPU time. To execute an I/O related instruction, CPU issues an address:

Identifies module (& device if more devices).

CPU issues an I/O command (Control,Test , Read, Write)

b). Interrupt driven.

With interrupt driven I/O: CPU-Issues an I/O command to a module, Continues to execute other instructions.

I/O module: Interrupts the CPU when completed the work. Requests service to exchange data with the CPU. CPU then executes the data transfer. This: Overcomes CPU waiting. No repeated CPU checking of device

I/O module: Receives a READ command from CPU. Proceeds to read data from the external device. Signals an interrupt to the CPU over control line: When the data are in the module's data register. Waits until its data are requested by the CPU. Places its data on the data bus: When the CPU request is made. Ready for another I/O operation.

CPU: Issues a READ command. Goes off and does other work. Checks for interrupt at the end of each instruction cycle. If interrupted: Save the context (PC and CPU registers) of current program. Process the interrupt:

Reads the data from the I/O module and stores it in memory. Restores the saved context and resumes interrupted program execution.

c). Direct Memory Access (DMA)

Direct memory access (DMA) is a method that allows an input/output (I/O) device to send or receive data directly to or from the main memory, bypassing the CPU to speed up memory operations.

DMA involves an additional (hardware) module on the system bus. DMA module can takes over control of the system from the CPU. To transfer data to and from memory over system bus.

To do this: DMA must use the bus only when the CPU does not need it or, DMA must force the CPU to suspend operation temporarily.

(03x2=06 Marks)

(iv). **"External devices are not generally connected directly into the computer bus structure." Briefly explain this statement.** (03 Marks)

Need I/ O modules,

Because of

- CPU speed is higher than others
- Different format of data transmission.
- Transmit different amount of data.
- Speed of devices are different.
- Increase the productivity of computer

(v). Give the advantage of single bus "Single-bus, integrated DMA-I/O" over "Single-bus, detached DMA"

DMA controller may support more than one device.

- May be a part of an I/O module.
- May be separate module that controls one or more I/Os.

Each transfer uses bus once:

DMA to memory.

CPU is suspended once.

(03 Marks)

Q5. (Total 25 marks)

(i). Let CPI= average cycles per instruction, I=number of instruction in a programme and T= clock cycle time,

a). Define CPU Execution Time in term of I, T and CPI (03 Marks)

Execution Time= I*CPI*T

According to the data given below;

Clock rate = 4 GHz

Average Cycles per instruction = 3

Number of instructions in a programme = 400

b). **Calculate clock cycle time?** (04 Marks)

$$T=\frac{1}{4\ X\ 10^9}\ Sec$$

c). Calculate CPU execution time of this programme. (04 Marks)

$$=400*3*\frac{1}{4\ X\ 10^9}\ Sec$$

(ii). **Briefly explain why process scheduling is important?** (02 Marks)

Be fair, Be efficient, Maximize throughput, Minimize response time, Maximize resource use etc.,

(iii). **What is preemptive and non-preemptive scheduling means?** (04 Marks)

Non-Preemptive scheduling: When a process enters the state of running, the state of that process is not deleted from the scheduler until it finishes its service time.

Preemptive scheduling: The preemptive scheduling is prioritized. The highest priority process should always be the process that is currently utilized.

(iv). **Using preemptive shortest job first algorithm, indicate the order of execution of each process in a time line and calculate the average waiting time for the processes given below.** (06 Marks)

Process	Arrival Time (in sec)	Service Time (in sec)
P1	8	3

P2	2	1
P3	1	3
P4	3	2
P5	4	4

Idle Time	P3	P2	P4	P5	P1
0 1	4	5	7	11	14

Process	Arrival Time (in Sec)	Service Time (In Sec)	Waiting time
P1	8	3	3
P2	2	1	2
P3	1	3	0
P4	3	2	2
P5	4	4	3

Average waiting time = (3+2+0+2+3) /5 = 10/5 = 2 sec

(v). **What is meant by deadlock** (02 Marks)

A deadlock is a situation in which two or more competing actions are each waiting for the other to finish, and thus neither ever does.

(02 Marks)