Marking Scheme

Q1)

I. What is the purpose Logic gates?

- A Logic gate is a device that performs a basic operation on electrical signals
- Gates are combined into circuits to perform more complicated tasks.

(02 marks)

II. Draw the truth tables for following Logic gates.

a. NAND

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

b. XOR

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

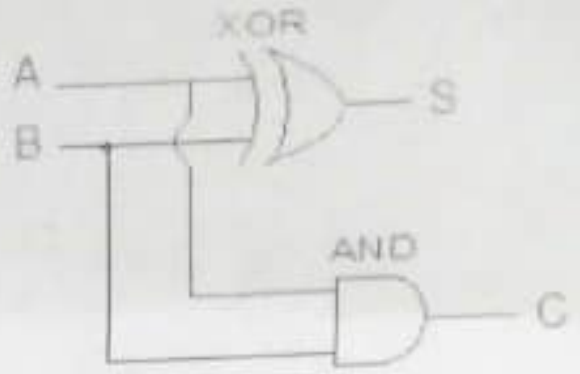
(Each Answer 02 marks, 02×2=04 marks)

III. Draw a circuit to represent half adder and draw the truth table.

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table

Schematic



Realization

(Correct Circuit 02 marks, truth table 02 marks, 02+02=04 marks)

IV. Write Boolean algebra equations for following Boolean Algebra laws.

a. Associative Law

Associative Law - This law allows the removal of brackets from an expression and regrouping of the variables.

$A + (B + C) = (A + B) + C = A + B + C$ (OR Associate Law)

$A(B.C) = (A.B)C = A.B.C$ (AND Associate Law)

b. Commutative Law

Commutative Law - The order of application of two separate terms is not important

$A.B = B.A$ The order in which two variables are AND'ed makes no difference

$A + B = B + A$ The order in which two variables are OR'ed makes no difference

(Each Answer 02 marks, 02×2=04 marks)

V. Simplify the following Boolean expression with Algebra law.

Apply the De Morgan's Law

$$\begin{aligned} Z &= \overline{(\bar{A} + C) \cdot (B + \bar{D})} \\ &= \overline{(\bar{A} + C)} + \overline{(B + \bar{D})} \\ &= (\bar{\bar{A}} \cdot \bar{C}) + (\bar{B} \cdot \bar{\bar{D}}) \\ &= A\bar{C} + \bar{B}D \end{aligned}$$

(Partial answers 02 marks, Complete answer 05 marks)

VI. Draw the Karnaugh map and simplify the following equation.

$$Z = \bar{A}B + B\bar{C} + BC + A\bar{B}\bar{C}$$

$$Z = B + A\bar{C}$$

(Correct Karnaugh map 02 marks, Group 02 marks, Final Answer 02 marks)
(02+02+02=06 marks)

(Total 25 marks)

Q2)

I. What is the purpose of an Instruction Set?

- The instruction set provides commands to the processor, to tell it what it needs to do.
- The instruction set consists of addressing modes, instructions, native data types, registers, memory architecture, interrupt, and exception handling, and external I/O.
- An example of an instruction set is the x86 instruction set, which is common to find on computers today.

(Any answer 02 marks)

II. Name four registers in the CPU.

Special Purpose Register

- Program Counter (PC)
- Memory Address Register (MAR)
- Memory Buffer Register (MBR)
- Instruction Register (IR)

General Purpose Register

- Accumulator (AX)
- Data Register (DX)
- Base Register (BX)
- Count Register (CX)

(Any 04 answers, 04 marks)

III. Briefly explain following CPU operations.

a. Instruction Fetch

- The processor reviews the program counter to see which command to execute next.
- The program counter gives an address value in the memory of where the next command is.
- The processor fetches the command value from the memory location.

(Any 02 answers, 02 marks)

b. Instruction Execute

It performs the function of the command. The ALU is utilised if the command involves arithmetic or logical operations.

(02 marks)

IV. Briefly explain CPU clocks

- Every computer contains an internal clock that regulates how quickly instructions can be executed.
- The clock also synchronizes all of the components in the system.
- Instruction performance is often measured in clock cycles

(Any 02 answer, 04 marks)

V. Write down the advantages and disadvantages of instruction pipelining.

Advantages

- It is a technique that implements a form of parallelism called instruction-level parallelism within a single processor.
- Pipelining increases instruction throughput by performing multiple operations at the same time.
- It allows faster CPU throughput (the number of instructions that can be executed in a unit of time)

(Any 02 answers, 03 marks)

Disadvantages

- It may increase latency due to additional overhead from breaking the computation into separate steps
- There are pipeline hazards

(Any 02 answers, 02 marks)

(03 marks+02 marks=05 marks)

VI. Briefly explain Pipeline hazard.

Structural hazards

Arise from resource conflicts when the hardware can't support all possible combinations of overlapping instructions

Data hazards
Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline

Control hazards
Arise from the pipelining of branches and other instructions that change the PC (Program Counter)

(Each answer 02 marks, 02×3=06 marks)

(Total 25 marks)

Q3)

I. Define the term CISC.

- The term CISC stands for ''Complex Instruction Set Computer''.
- It has a huge number of compound instructions, which takes a long time to perform.
- Hardware based
- CSIC processor has complex instructions that take up multiple clocks for execution.

(Any 02 answers, 02 marks)

II. Compare and contrast DRAM and SRAM.

	Tran. per bit	Access time	Persist?	Sensitive?	Cost	Applications
SRAM	6	1X	Yes	No	100x	cache memories
DRAM	1	10X	No	Yes	1X	Main memories, frame buffers

(Consider at least 04 points, 01×4=04 marks)

III. What is Non-volatile memory? Give two examples.

- It is a type of computer memory that has the capability to hold saved data even if the power is turned off

(02 marks)

ROM, PROM, EPROM, EEPROM, Flash Memory, Firmware

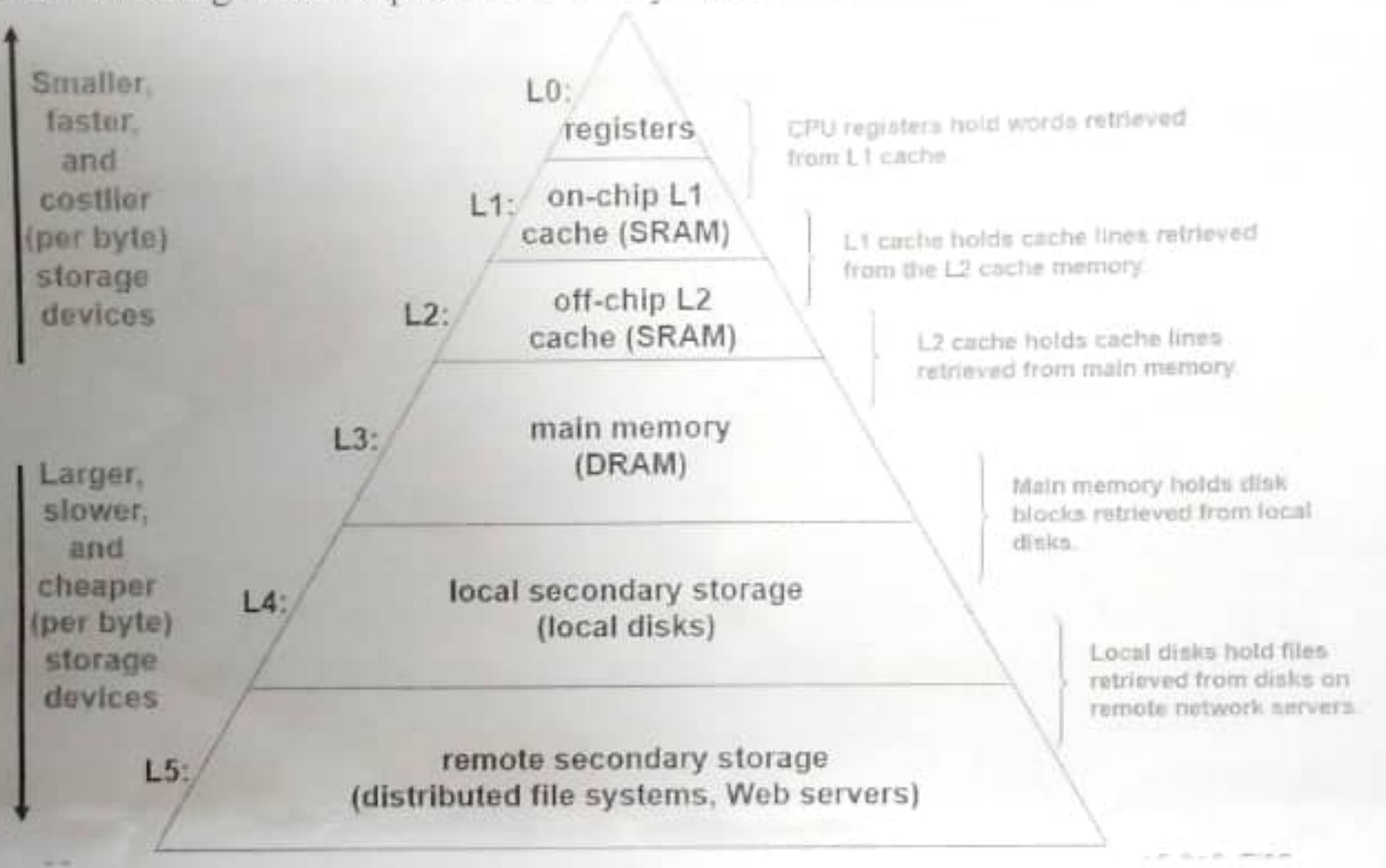
(Any 02 answers, 02 marks)
(02+02=04 marks)

IV. What are the functions of cache memory?

- A smaller, faster storage device that acts as a staging area for a subset of the data in a larger, slower device.
- There are two cache level L1 on chip and L2 off chip
- Use the cache hits and mises to find the block

(Any 02 answers, 04 marks)

V. Draw the diagram to represent memory hierarchy.



(Partial answers 03 marks, Correct diagram 05 marks)

VI. Consider the following details of hard disk.

Average seek time = 9ms
Disk rotation speed = 7200 rpm
Byte per sector = 512
Sectors per Track = 400
Tracks per Surface= 20000
Number of platters = 05
2 surfaces on each platter

a. Calculate capacity of the hard disk.

$$Hard\ Disk\ Capacity = Sector\ size \times \frac{Sectors}{Track} \times \frac{Tracks}{Platter} \times Platers \times 2$$

$$Hard\ Disk\ Capacity = 512 \times 400 \times 20000 \times 05 \times 2\ bytes$$

(02 marks)

b. Calculate the average disk rotational latency

$$Average\ disk\ rotational\ latency = \frac{1}{2} \times \frac{1}{RPM}$$

$$Average\ disk\ rotational\ latency = \frac{1}{2} \times \frac{1}{7200}$$

(02 marks)

c. Calculate the total time needed to read 200KB data file (Assume file is not fragmented)

$$Average\ disk\ access\ time = 9 + \frac{1}{2} \times \frac{1}{7200} + \frac{200 \times 1024}{512} \times \frac{1}{400} \times \frac{60}{7200} \times 1000\ milli\ seconds$$

(02 marks)

(Total 25 marks)

Q4)

I. What is Input/output module?

- External devices are not generally connected directly into the computer bus structure.
- It connected through the I/O module.
- It is the interface to CPU and Memory

(Any 02 answer, 02 marks)

II. Name four functions of I/O module.

- Control & Timing.
- CPU Communication.
- Device Communication.
- Data Buffering.
- Error Detection.

(Any 04 answers, 04 marks)

III. Briefly explain the operations of Interrupt driven I/O technique.

- Receives a READ command from CPU.
- Proceeds to read data from the external device.
- Signals an interrupt to the CPU over control line:
- When the data are in the module's data register.
- Waits until its data are requested by the CPU.
- Places its data on the data bus:
- When the CPU request is made.
- Ready for another I/O operation

(Any 04 answers, 04 marks)

b. Calculate the Average waiting time.

Process	Wait Time : Service Time - Arrival Time
P0	(0 - 0) + (12 - 3) = 9
P1	(3 - 1) = 2
P2	(6 - 2) + (14 - 9) + (20 - 17) = 12
P3	(9 - 3) + (17 - 12) = 11

Average Wait Time: (9+2+12+11) / 4 = 8.5

(03 marks)

(Total 25 marks)

Q5)

I. What is the purpose of System Busses?

- Bus is a subsystem that transfers data between computer components inside a computer or between computers.
- Abus can logically connect several peripherals over the same set of wires.
- Each bus defines its set of connectors to physically plug devices, cards or cables together.

(Any answer, 02 marks)

II. Name four types of disk interfaces.

- ATA – AT Attachment (named after IBM PC-AT)
- IDE – Integrated Drive Electronics (same as ATA)
- Enhanced IDE
- Encompasses several older standards (ST-506/ST-412, IDE, ESDI, ATA-2, ATA-3, ATA-4)
- Floppy disk
- SCSI – Small Computer Systems Interface
- ESDI – Enhanced Small Device Interface (mid-80s, obsolete)
- PCMCIA

(Any 04 answers, 04 marks)

III. Briefly explain following terms.

a. Ethernet

- It is interface to connect LAN
- Standard is IEEE 802.3
- 10 Mbits/s for Ethernet (10Base-T)
- 100 Mbits/s for Fast Ethernet (100Base-TX)

(Any 02 answers, 02 marks)

b. Serial Interface

- On PCs, a "serial interface" implies a "COM port", or "communications port"
- COM1, COM2, COM3, etc.
- Example RS232
- Point to point

(Any 02 answers, 02 marks)

IV. What is the concept of Deadlock?

- Deadlock is a situation where a set of processes are blocked because each process is holding a resource and waiting for another resource acquired by some other process.
- Deadlock can be occurred due to conditions Mutual exclusion, Hold and wait, Non-preemption and circular wait.

(Any 02 point, 04 marks)

V. Briefly explain following terms.

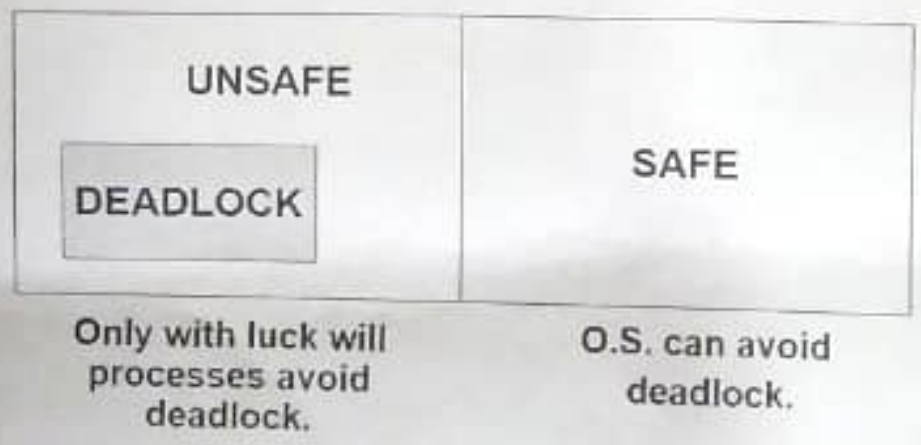
a. Resource Allocation Graph

- Resource Allocation Graph is use to represent deadlock detection.
- The resources are assigned to process
- If there is cycle then deadlock can be occurred.
- If resource types have multiple instances, then deadlock MAY exist.
- If each resource type has 1 instance, then deadlock has occurred.

(02 marks)

b. Deadlock Avoidance

- The system dynamically considers every request and decides whether it is safe to grant it at this point,
- The system requires additional priori information regarding the overall potential use of each resource for each process.
- Allows more concurrency.



(03 marks)

(02 marks+03 marks=05 marks)

VI. The following details are related to the computer performance.

Clock rate= 3GHz

Average Cycle per Instruction=4

Number of Instruction=500

a. Calculate the clock cycle time.

$$Clock\ Cycle\ Time = \frac{1}{4 \times 10^9}\ Seconds$$

(03 marks)

b. Calculate the CPU execution time of this program.

$$Execution\ Time = I \times CPI \times T$$

$$Execution\ Time = 500 \times 4 \times \frac{1}{4 \times 10^9}\ Seconds$$

(03 marks)

(Total 25 marks)

N.B.
Question number 03

Part iv) subpart a} give 02 marks for all students
Subpart c) give 02 marks for all students