SLIATE

SRI LANKA INSTITUTE OF ADVANCED TECHNOLOGICAL EDUCATION

(Established in the Ministry of Higher Education, vide in Act No. 29 of 1995)

Higher National Diploma in Information Technology

2nd Year, Second Semester Examination – 2018

HNDIT2401-Computer Architecture

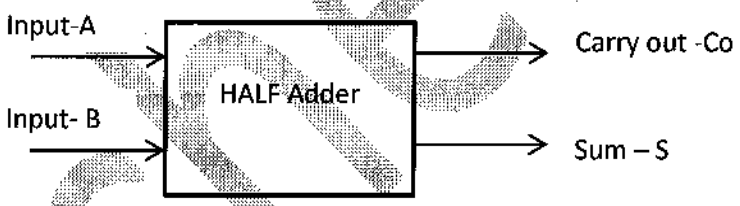
Marking Scheme

Question 01

1. State the two general categories of circuits. [2 Marks]
   - **Combinational circuits**
   - **Sequential circuits**

   [1x2 =2 Marks]

2. Consider the **half adder** to answer the following questions. [4 Marks]



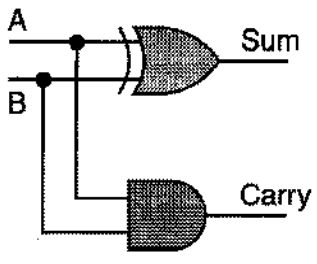
a. Create the truth table.

A	B		Sum-S	Carry out-Co
0	0		0	0
0	1		1	0
1	0		1	0
1	1		0	1

1 mark for correct sum column

1 mark for correct Carry out column

b. Construct a circuit diagram with minimum number of gates.



1 mark for each correct gate x2= 2 Marks

3. Draw the circuit diagram for the following Boolean expression only using **NAND** gates.

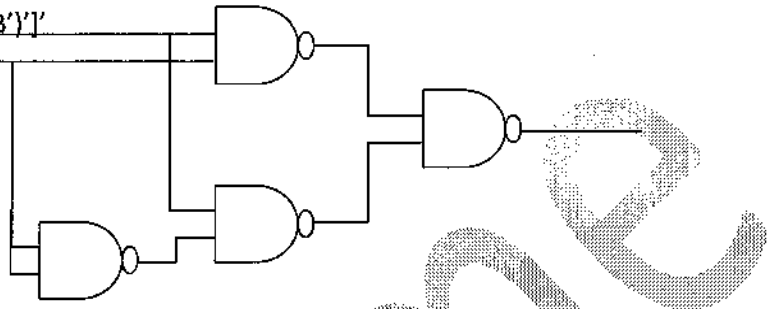
[5 Marks]

F (A, B) =AB+AB'

F(A,B)= [[AB+AB']']' **1 mark**

= [(A| A (AB')']'

B



1 mark for each gate x 4= 4 Marks

4. Simplify the following Boolean expression using Boolean algebra and its identities.

[6 Marks]

a. F(A,B)= A'B+AB'+(AB)'

A'B+AB'+A'+B'

A'(B+1) + B'(A+1)

A'+B' OR (AB)'

3 Marks

b. F(A,B,C)=A'B+ABC'+ABC

A'B+AB(C'+C)

A'B+ AB

B(A'+A)

B

3 Marks

5. Simplify the function F (A, B, C) =A'B'C'+AB'C+A'BC'+AB'C'+ABC' using K-Maps.

[8 Marks]

A \ BC	00	01	11	10
0	1	0	0	1
1	1	1	0	1

OR

C \ AB	00	01	11	10
0	1	1	1	1
1	0	0	0	1

5 marks for correct K-Map

1 marks for correct grouping

F(A,B,C)=C'+AB' **2 Marks**

Question 02

1. Briefly explain what **ALU** is. [2 Marks]

   The arithmetic logic unit (ALU) carries out the logic operations (such as comparisons) and arithmetic operations (such as add or multiply) required during the program execution

   2 Marks

2. State 4 Registers which resists inside the CPU [4 Marks]

   - **PC- Program Counter**
   - **MBR- Memory Buffer Register**
   - **MAR- Memory Address Register**
   - **IR –Instruction Register**
   - **ACC - Accumulator**
   - **Any other acceptable answer.....**

   Any four

   1 Mark x 4= 4 Marks

3. Describe the **instruction fetch** in instruction cycle. [5 Marks]

- **PC contains address of next instruction**
- **Address moved to MAR**
- **Address placed on address bus**
- **Control unit requests memory read**
- **Result placed on data bus, copied to MBR, then to IR**
- **Meanwhile PC incremented by 1**

[MAR] ← [PC]
PC=PC+1
[MBR]← Memory [MAR]
[IR] ←[MBR]

4. What are the three types of pipelining hazards briefly explain them. [6 Marks]

- ***Structural hazards***
  - **Arise from resource conflicts when the hardware can't support all possible combinations of overlapping instructions**
- ***Data hazards***
  - **Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline**
- ***Control hazards***
  - **Arise from the pipelining of branches and other instructions that change the PC (Program Counter)**

2 Marks for each x 3=6 Marks

5. To deal with branches and reduce the branch penalty in pipelining there are several ways. Briefly describe 4 of them. [8 Marks]

- **Prefetch Branch Target**
  Target of branch is prefetched in addition to instructions following branch
- **Loop buffer**
  This is a high speed cache type memory that is used for holding the most recently Fetched instructions. If a branch instruction is taken, first check the loop buffer to see if the instruction exists.
- **Branch prediction**
  Several methods of branch prediction are available
  - **Predict never taken**
    Assume that jump will not happen, Always (almost) fetch next instruction
  - **Predict always taken**
    Assume that jump will happen (at least 50%). Always fetch target instruction
  - **Predict by opcode**

This approach makes a prefetch decision based on the branch's opcode.

- **Taken/Not taken switch**

  Based on previous history

- **Delayed branching**

  The effect is to execute one or more instructions following the conditional branch before the branch is taken.

2 Marks for each type x 4= 8 Marks

Question 03

1. What is cache memory? [2 Marks]

   A small amount of faster, more expensive memory is used to improve the performance of recently accessed or frequently accessed data that is stored temporarily in a rapidly accessible storage media.

   2 Marks

2. Briefly describe two types of locality. [4 Marks]

   Temporal locality: Recently referenced items are likely to be referenced in the near future.
   Spatial locality: Items with nearby addresses tend to be referenced close together in time.

   2 Marks for each type x 2=4 Marks

3. What is nonvolatile memory? Give three examples for nonvolatile memory. [5 Marks]

   Nonvolatile memories retain values even if powered off while volatile memory not.
   Examples:

   - **Flash Memory**
   - **Hard Disk**
   - **Magnetic tape**
   - **Floppy disks**
   - **Optical Disk Drive**
   - **Any acceptable answer**

   2 marks for description
   1 mark for each example x 3= 3 Marks

4. Describe the terms **Seek Time, Rotational Latency, Transfer Time** in hard disk operation. [6 Marks]

- **Seek Time :- Time to position heads over cylinder containing target sector**
- **Rotational Latency :- Time waiting for first bit of target sector to pass under r/w head. Tavg rotation = 1/2 x 1/RPMs x 60 sec/1 min**
- **Transfer Time :- Time to read the bits in the target sector. Tavg transfer = 1/RPM x 1/(avg # sectors/track) x 60 secs/1 min.**

2 marks for each description x 3= 6 Marks

5. Answer the questions based on the following details of a hard disk. [8 Marks]
   512 bytes per sector
   300 sectors per track (on average)
   20000 tracks per surface
   Disk has 4 platters
   2 surfaces on each platter
   Disk rotation speed is 7600 rpm
   Average seek time is 9ms
   a. Calculate the capacity of the hard disk
      Capacity=512x300x20000x4x2
      24,576,000,000 bytes
      24.576 GB
      2 Marks
   b. Calculate the data transfer time.
      Transfer time= 60x1000/ (7600 x300) ms =0.026 ms
      2 Marks
   c. Calculate rotational latency.
      Rotational latency= 60 x1000/(7600x2) ms = 3.94 ms
      2 Marks
   d. Get the access time.
      Access time= 9 + (60x1000)/(7600x300)+ (60x1000)/(7600x2) ms
      9+ 0.026+3.94 ms
      12.96 ms
      2 Marks

Question 04

1. Define clock rate R with using clock cycle time T. [2 Marks]

   R=1/T

2. Find the CPU execution time of this program [4 Marks]
   Number of instructions in program (I) =300
   Average cycles per instruction (CPI) =3

Clock rate=4GHz

CPU time=I x CPI /R **2 Marks**

=300 x 3 / (4x10^9) S **2 Marks**

=225 x 10^{-9} S

3. Define the term deadlock with using an example. [5 Marks]

A deadlock is a situation in which two computer programs sharing the same resource are effectively preventing each other from accessing the resource, resulting in both programs ceasing to function.

3 Marks for description

2 Marks for Any suitable example

4. Briefly describe the three general strategies to handle a deadlock. [6 Marks]

- ***Ignore Deadlocks*** **2 Mark**
- **Ensure deadlock never occurs using either**

  Prevention **Prevent any one of the 4 conditions from happening.**

  Avoidance **Allow all deadlock conditions, but calculate cycles about to happen and stop dangerous operations.**

  2 Marks

- **Allow deadlock to happen. This requires using both:**

  Detection **Know a deadlock has occurred.**

  Recovery **Regain the resources.**

  2 Marks

5. Computing Systems are classified into four major categories in **Flynn's Taxonomy**. Briefly describe them. [8 Marks]

- **Single-instruction, single-data (SISD) systems**

  An SISD computing system is a uniprocessor machine which is capable of executing a single instruction, operating on a single data stream.

- **Single-instruction, multiple-data (SIMD) systems –**

  An SIMD system is a multiprocessor machine capable of executing the same instruction on all the CPUs but operating on different data streams.

- **Multiple-instruction, single-data (MISD) systems –**

An MISD computing system is a multiprocessor machine capable of executing different instructions on different PEs but all of them operating on the same dataset.

- **Multiple-instruction, multiple-data (MIMD) systems –**

An MIMD system is a multiprocessor machine which is capable of executing multiple instructions on multiple data sets

2 Marks for each x4=8 Marks

Question ~~05~~ 04

1. State two techniques for Input Output operations. [2 Marks]

   - **Polling**
   - **Interrupt driven**
   - **DMA**

   Any 2 answers

2. Give 4 major functions of I/O module. [4 Marks]
   - **Control and timing**
   - **CPU communication**
   - **Device communication**
   - **Data buffering**
   - **Error detection**

   Any 4

3. Differentiate Preemptive and Non-preemptive scheduling in CPU scheduling. [4 Marks]

   Preemptive: - The resources are allocated to a process for a limited time and then is taken away, and the process is again placed back in the ready queue if that process still has CPU burst time remaining.
   Non Preemptive: - Once resources are allocated to a process, the process holds it till it completes its burst time or switches to waiting state.

   2 Marks for each x 2=4 Marks

4. State 5 criteria that can be used for performance evaluation of a scheduling algorithm. [5 Marks]

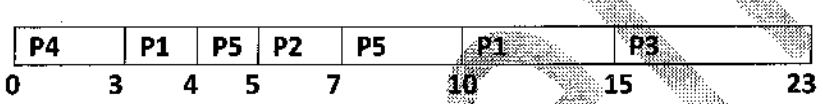
   - **Utilization**
   - **Throughput**

- **Service time**
- **Queuing time**
- **Residence time**
- **Response time**
- **Think time**

Any 5

5. Using preemptive shortest job first algorithm represents the order of execution of the process given below in a time line. Calculate the waiting time of each process and get the average waiting time. [10 Marks]

Process	Arrival Time (seconds)	service Time (seconds)
P1	2	6
P2	5	2
P3	1	8
P4	0	3
P5	4	4



Process	Waiting time
P1	(3-2)+(10-4)=7
P2	5-5=0
P3	15-1=14
P4	0
P5	(4-4)+(7-5)=2

Avarage waiting time= (7+0+14+0+2)/5=4.6

5 marks for the correct time line

5 marks for calculating waiting time for each process