Assignment 3

Fundamentals of Digital System Design

Due Date: November 16, 2024

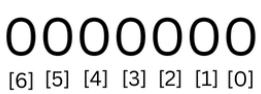
This assignment is based on the previous assignment on designing the traffic light system

1. Write the system verilog code for the state diagram created for assignment 2.

The completed assignment should be submitted as a .sv file **on or before 11.59pm, November 16, 2024**. If you also create a testbench which is optional, submit both as a .zip file.

Please use the following variable names for inputs and outputs when writing the code. You do not need to create a timer for this assignment. Just make timer_done a binary input given by the user.

Index	Description
0	traffic_B
1	timer_done



Index	Description
0	red_light_A
1	amber_light_A
2	green_light_A
3	red_light_B
4	amber_light_B
5	green_light_B
6	amber_timer_en