Assignment 4

Fundamentals of Digital System Design

Due Date: November 16, 2024

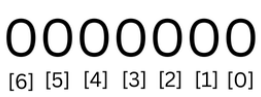
This assignment is based on the previous assignments (Assignment 2 and 3) on designing the traffic light system.

1. Write the system verilog code for a nested down counter to count 7.5 seconds. This is the " external timer module is present to ensure that the traffic light shows the 'Amber' colour for a required amount of time" described in Assignment 2. Make sure to create hierarchical design.

The completed assignment should be submitted as a .zip file **on or before 11.59pm, November 16, 2024**. The .zip file should contain the all the modules (i.e. traffic light module and the timer modules).

Please use the following variable names for inputs and outputs when writing the code. You have to create timer module considering the clock pulse delivered is 100ms. The timer module should be a nested counter consisting of two down counters. one for milliseconds and the other for seconds. Once the counter is done, it should make the timer_done flag true. Next combine the timer module with the traffic light system and ensure that it works as described in Assignment 2

Index	Description
0	traffic_B
1	timer_done



Index	Description
0	red_light_A
1	amber_light_A
2	green_light_A
3	red_light_B
4	amber_light_B
5	green_light_B
6	amber_timer_en