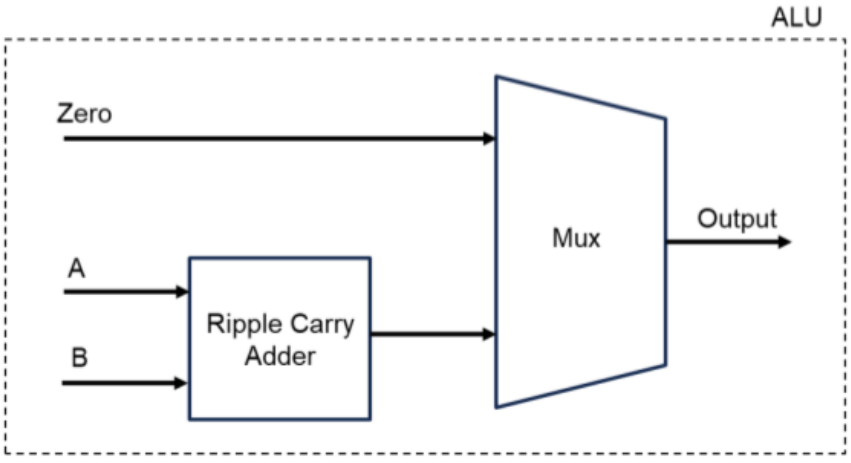
Fundementals of Digital System Design - Assignment 01

DUE: 11:59PM, Sunday, October 13, 2024

Create a simple **ALU (Arithmetic Logic Unit)** with the following functionalities. Use the image given below as a reference. .

1. Able to add two 4 bit numbers
2. Output zero
3. Use a SELECT bit to select the multiplexer output. SELECT bit 0 gives zero as output. SELECT bit 1 gives the addition as output.



Make sure to use a ripple carry adder.
Write the system verilog code with a test bench for this design.
Submit the testbench and design file included in a zip file.