Indian Institute of Technology Hyderabad

Electrical Engineering
Indian Institute of Technology Hyd
CMOS VLSI Design

August 29, 2025

Deadline: 05 Sep 2025 | *Assignment # 2* | Maximum Marks: TBD

Instructions:

1. Use LT Spice for the simulations.

Constant values (use if not specified in question) - Planck's constant (h) = 6.626×10^{-34} Jule-sec, Boltzmann constant (k) = 1.38×10^{-23} Jule/K, Room Temperature = 300 K, Thermal voltage (v_t) at room temp = 26mV, Speed of light (c) = 3×10^{8} m/s, Intrinsic concentration (n_i) at room temperature (cm^{-3}) = 1.5×10^{10} for Si, dielectric constant of vacuum $\epsilon_0 = 8.85\times10^{-14}$ F-cm^{-1}, $\epsilon_{Si} = 12\epsilon_0$, $\epsilon_{Sio_2} = 4\epsilon_0$, Mean life time of charge carriers (τ = 1 ns), $\mu_n C_{ox}$ for 180nm CMOS tech node silicon nMOST = $300\mu A/V^2$, $\mu_p C_{ox}$ for 180 nm CMOS tech node silicon pMOST = $60\mu A/V^2$. $|V_{th,p}| = V_{th,n} = 0.5$V (if required), Oxide thickness $t_{ox} = 10\ nm$, VDD = 3V

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1. Draw the I-V (Ids-Vds) characteristics of an NMOS and PMOS Device for different VGS varing from 0 to 3 Volts (take a step of 0.5V).

2. Design a CMOS inverter for equal rise and fall time. Find its rise time, fall time, and delay with and without load capacitance of 10 pF. Plot its VTC and IV characteristics of this inverter with no load condition.

3. Design a static CMOS NAND and NOR Gates for equal rise and fall time. Find its rise time, fall time, and delay with and without load capacitance of 10 pF.

Student's roll number: Ended here