



Electrical Engineering
Indian Institute of Technology Hyd
CMOS VLSI Design

September 22, 2025

Deadline: 29 Sep 2025

Assignment # 3

Maximum Marks: TBD

Instructions:

1. Use Cadence (with GPDK) for the simulations.

1. Make schematic and layout of a static CMOS Inverter with proper DRC + LVS + Antenna Error clean. Run the RC extraction of the same and compare with schematic result. Find the maximum switching frequency for both cases.
2. Repeat Q1 for 3 input NAND and NOR gate with proper sizing.
3. Repeat Q1 and Q2 for a load capacitance of 1 pF.
4. Repeat Q3 for delay optimization with a chain of inverters. Find the optimum number of stages.
5. Repeat Q3 with Pseudo and dynamic gate (with footer + with/without keeper) architecture for delay optimization with a chain of inverters with the optimum number of stages. Change the topology of the gate design to get the delay improvement.