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4 Characterization of Silicon/Insulator Interface

1. Electrical methods are commonly used to investigate interface charges in Si/SiO_2 interface
2. Electrical methods measure parameters that are of direct interest to semiconductor devices such as capacitance, threshold voltages, insulator quality and electrical charges
3. The most dominant electrical measurement technique is the capacitance-voltage or C-V method, which provide a large amount of information about insulator /semiconductor properties
4. The basic structure used to make the measurement is a MOS capacitor, consisting of a metal or doped polysilicon gate electrode, a dielectric film (Oxide) and a semiconductor substrate connected to a sweeping DC voltage with a small superimposed AC capacitance measurement voltage as shown in Fig.12

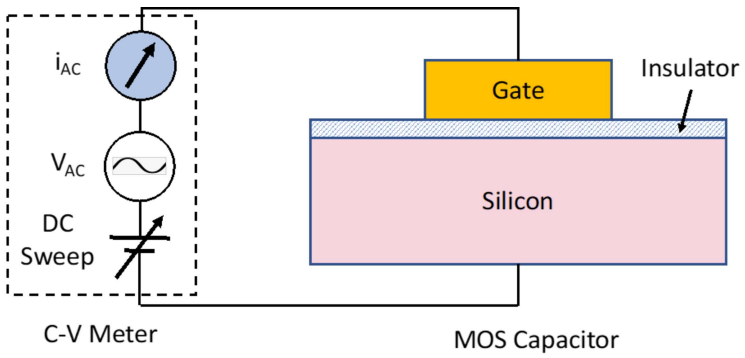

Figure 12: MOS Structure - CV measurement set up

5. The capacitance measured is the change in charge w.r.t to change in voltage

$$\boxed{C \equiv \frac{\Delta Q}{\Delta V}} \tag{18}$$

6. C-V measurements are done by using two series voltage sources, the small AC voltage source and a DC voltage that is swept in time
7. The purpose of the DC voltage is to allow the capacitance to be sampled at different depths in the device. The AC signal allows the capacitance to be measured at each depth
8. The sweep rate is slow enough to approximate a series of steady state or equilibrium measurements at a range of DC voltages
9. The defect density is assumed to be small in the oxide to start with.
10. Consider an n-type Silicon substrate with a positive voltage $+V_G$ on the gate as shown in fig.14.

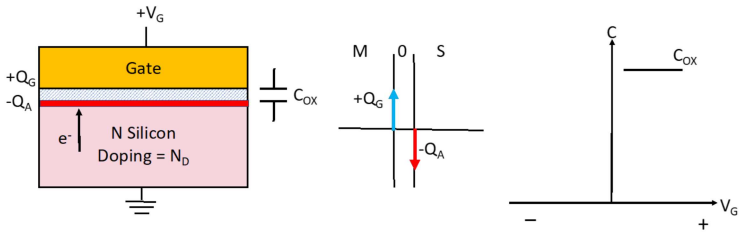

Figure 13: PMOS - Accumulation

11. **Accumulation**: In n-type material, the dominant carriers are electrons which are negatively charged and therefore attracted to the surface if they see the positive voltage applied to the metal. The electrons form an accumulation layer at the silicon surface.

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12. **Depletion**

    - Applying a negative DC voltage or bias to n-type substrate repels the majority carriers
    - Any negative charge on the gate must be balanced by corresponding positive charge in the substrate to maintain charge neutrality as shown in Fig.**??**
    - The positive charge is provided by the substrate donor atoms that have a net positive charge because of the depletion of the electrons
    - At the same time, **thermally generated** minority carriers from the bulk get attracted towards the surface. They do not contribute to charge balancing
    - The structure can be visualized as a series of two capacitors, the oxide capacitance and depletion capacitance

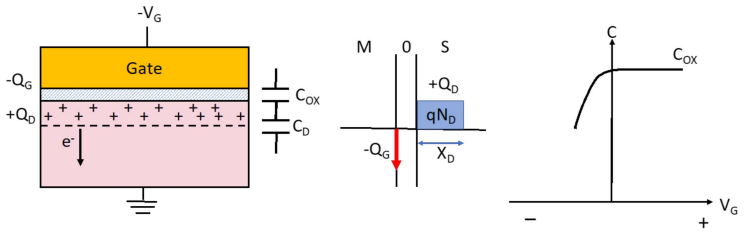

Figure 14: PMOS - Depletion

13. The gate charge is balanced by the depletion charge as

$$\boxed{|Q_G| = |Q_D| = N_D x_D} \tag{19}$$

14. $|Q_G|$ and $|Q_D|$ are charge densities, N_D is the doping concentration, x_D is the thickness of the depletion region

15. The first order approximation of depletion capacitance is given by

$$\boxed{C_D = \frac{\varepsilon_s}{x_D}} \tag{20}$$

16. The over all capacitance decreases as the voltage is made more negative and is given by

$$\boxed{\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_D}} \tag{21}$$

17. The rate at which the capacitance decreases depends on how fast the depletion layer changes with the applied bias, which in turn is a function of doping concentration. Hence the concentration information can be extracted from this plot

18. **Inversion:**

    - Once the voltage applied is equal to the threshold voltage, the surface concentration of holes is equal to the bulk concentration of electrons.
    - At inversion, the depletion layer thickness reaches its maximum value as shown in Fig.**??**

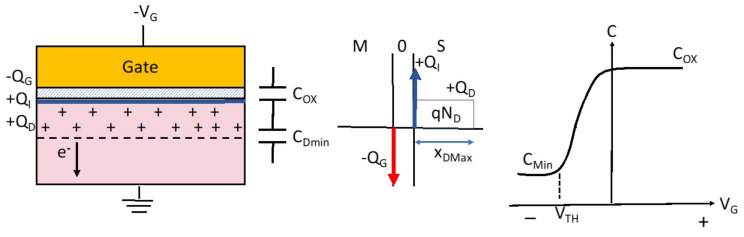

Figure 15: PMOS - Inversion

19. The charge balance equation at inversion can be written as

$$\boxed{Q_G = N_D x_D + Q_I} \tag{22}$$

20. Q_I is the charge density of the inversion layer

21. Whether the capacitance remains at a minimum with increasing negative bias or reverts to oxide capacitance value depends on the frequency of the measurement

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22. **Low Frequency:**

    - At low frequency the differential charge on the gate ΔQ_G is balanced by the holes in the inversion layer ΔQ_I
    - The capacitance can be treated as a parallel plate capacitor with the oxide being the dielectric
    - The capacitance returns to its original value C_{ox} as shown in the Fig.16

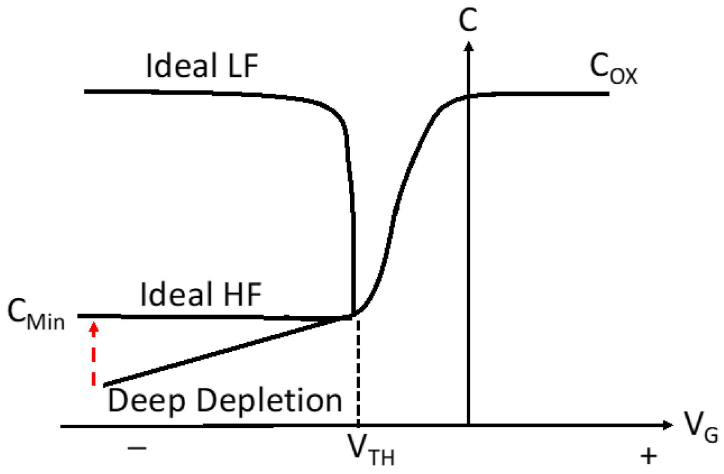

Figure 16: CV curve, low frequency and high frequency

23. **High Frequency**

    - At high frequency the differential charge on the gate ΔQ_G icannot be balanced by the holes in the inversion layer ΔQ_I
    - The process of hole generation is thermal generation, which is inherently slow
    - The holes cannot contribute to the charge balancing at high frequency
    - The depletion width varies differentially according to the differential charge(voltage) applied
    - The capacitance stays constant at a minimum value C_{min}
    - The capacitance returns to its original value C_{ox} as shown in the Fig.16

24. The point at which both the low frequency and the high frequency curve intersect is the threshold voltage

25. **Deep Depletion: This occurs when the sweeping rate of DC voltage is fast**

26. As the DC voltage is swept at higher rate, the thermal generation process of holes becomes a limiting step. The depletion width increases beyond x_{Dmax} to balance the charge resulting in reduction of capacitance beyond C_{min}

27. The typical DC sweep voltage rate is 0.1 V/sec

28. **Non idealities and their effect on CV:**

    - Fixed charge shifts the CV curve laterally as it impacts the threshold voltage as shown in Fig.6

- Similarly, work function difference shifts the CV curve laterally as it impacts flat band voltage which is the component of the threshold voltage
- Distorted or stretched curve happens due to interface traps
- Non-repeatable CV curves is an indication of presence of mobile carriers
- A U shaped curve is an indicative of interface traps

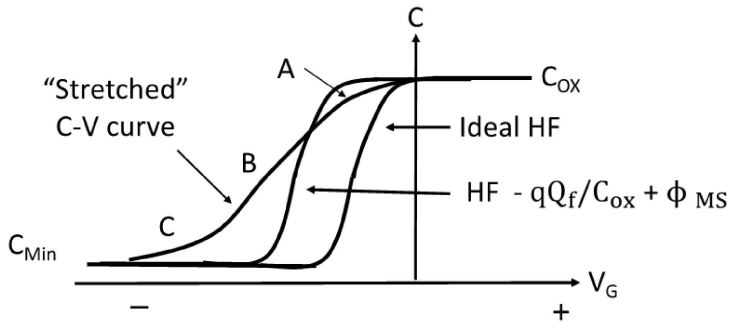

Figure 17: Non ideal CVs