EE1501 - Digital Systems Lab

Assignment - 2

Please submit a report which includes the code, its testbench, results, and your approach.

Q1) Design a sequence detector for the sequence “10010” (non-overlapping). Include the state graph and state table in your report, and write behavioral verilog code corresponding to the FSM coding guidelines. The testbench should generate a stream of bits with at least 3 instances of the sequence.

Q2) Design a floating point adder (IEEE 754 format). Testbench should contain 2 test cases.
Reference: IEEE-754 Floating-Point Conversion from Floating-Point to Hexadecimal (cuny.edu)
Example testcase:
A = 6.25 = 32’h40C80000
B = 0.5= 32’h3F000000
O = A+B = 6.5 = 32’h40D00000