EE2510. Productivity Tools for IC Design. Autumn 2024-25.
Dept. of CSE/EE, IIT Hyderabad
RTL Synthesis - Execution and Reporting

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The objective of this assignment is to make you familiar with one of the IC design tools (RTL synthesis tool), execute synthesis for various designs, parse reports or log files and generate various summaries.

You are free to use any of the taught automation techniques, which you think is best for the specific requirement.

Synthesize various RTL designs/benchmarks from
https://drive.google.com/drive/folders/1ktDfiGGp8ZAIvM8X_gGRl9t-h0Rx9btJ

1. ISCAS-85: 1 design
2. CEP: 2 designs
3. ITC99: 2 designs
4. UART: 3 designs
5. CUSTOM: 2 designs ~~(will be added later)~~ **(Added 2 custom designs)**

Synthesis corners/libraries (available in the PDK_DIC folder):

1. slow
2. fast
3. fast_hvt
4. slow_hvt
5. fast_lvt
6. slow_lvt

Create a separate folder for each of these 10 benchmarks, create tcl and/or constraint files for them within the folder, execute synthesis using scripts, and prepare the following summary in a report pdf. You can apply your creativity in how to present the results in terms of table/csv/plots/etc.

Use 2 different frequency options (100 MHz and 400 MHz) during synthesis. The duty cycle can be 50% for each.

1. Comparison of area/timing/power for different library corners for each design
2. **Comparison of area/timing/power as per each frequency**
3. Identify the count of each cell type by reading the generated netlist
4. Identify the most power consuming sub-block within each benchmark
5. Identify the sub-block with highest area within each benchmark

Your report should also include your approach to automating the execution and processing of tool reports/log files. Also, include any specific observations from the experiments, and your key learnings from this exercise.
For ease of development, do the assignment in 3 steps.

1. Step-1 (~45 marks): 8 benchmarks (without custom), with only fast and slow libraries
2. Step-2 (~25 marks): 8 benchmarks (without custom), with all 6 libraries
3. Step-3 (~30 marks): All 10 benchmarks, with all 6 libraries

IMPORTANT:

1. The document can get updated with more clarifications/modifications based on queries from students
2. Please use moodle forum to ask queries so that everyone can see the queries and answers to them
3. Any updates done in this document will be marked in red color

Submission instructions:

1. Submission should include a zip file containing your scripts and the setup, as well as the pdf report file containing various summaries/plots as described above.
2. Your zip file should not include the large sized outputs generated by the tool - this is to minimize the size of the submitted file. But your reports and other outputs should be on the server which we can look at if needed.
3. The zip file should be named ROLLNUM1_ROLLNUM2_groupNUM.zip (e.g., EE22BTECHXXXXX_EE22BTECHYYYYY_02.zip). groupNUM is your group number.
4. The submission should be strictly your own work and not copied from any other group or from the web. The results should be genuine ones and not any arbitrary numbers.
5. Each group makes only 1 submission.