

# EE1101: Circuits and Network Analysis

## Lecture 11: Dependent Sources

August 22, 2025

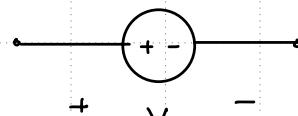
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### Topics :

1. Dependent Sources
  2. Three Terminal Circuit Elements
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## Dependent Sources

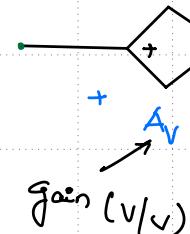
So far: Voltage | Current Source  
(independent sources)



Voltage across is not  
dependent on external ckt

Dependent Sources: → Value is determined based on Voltage | Current in an External ckt element.

### ① Voltage Controlled Voltage Source

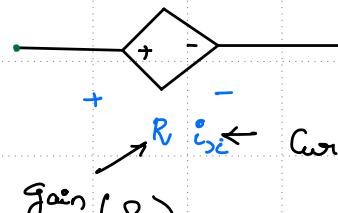


$$V_s = A_v V_{xc}$$

$A_v V_{xc}$  ← Voltage across an ext. ckt elem  
(or)  
Gain (V/V)      controlling parameter: Voltage.

used to model an  
Operational Amplifier  
(OPAmp)

### ② Current Controlled Voltage Source



$$V_s = R_i i_x$$

$R_i i_x$  ← Current through an ext. ckt elem  
(or)  
Gain (S)      controlling parameter: Current

can be constructed using  
an OPAmp

## Dependent Sources

### ③ Voltage Controlled Current Source



$$i_s = G v_x$$

$G v_x$  ← Voltage across an ext. cut elem  
(or)  
controlling parameter: Voltage.

model MOSFET

### ④ Current Controlled Current Source



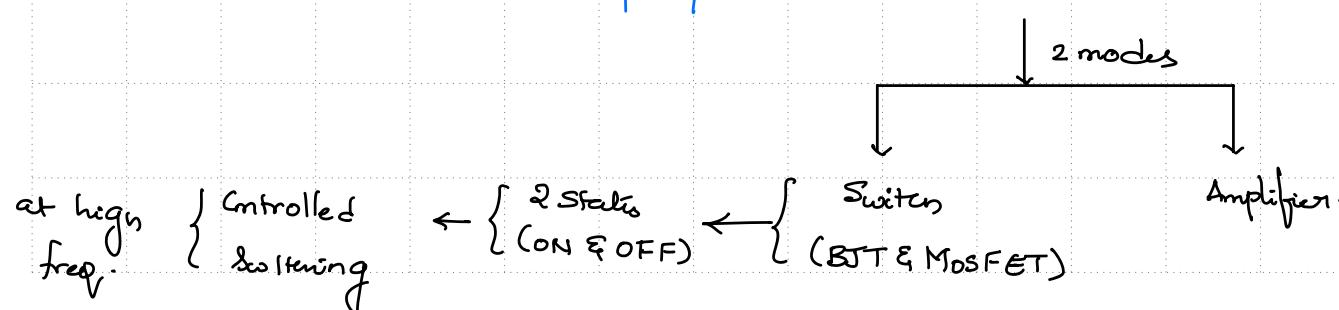
$$i_s = A_i i_x$$

$A_i i_x$  ← Current through an ext. cut elem  
(or)  
controlling parameter: Current

model a BJT

BJT, MOSFET & OpAmp  $\rightarrow$  3-terminal devices.

2 modes



## Three Terminal Circuit Elements (as a switch)

Example: A 3 Terminal CKT elem operating as a switch.

Control Port is

b/w A & C.

if  $V_{AC} > 0$  : ON state

$B \in C \rightarrow$  Short  
( $R \rightarrow 0$ )

if  $V_{AC} < 0$ :

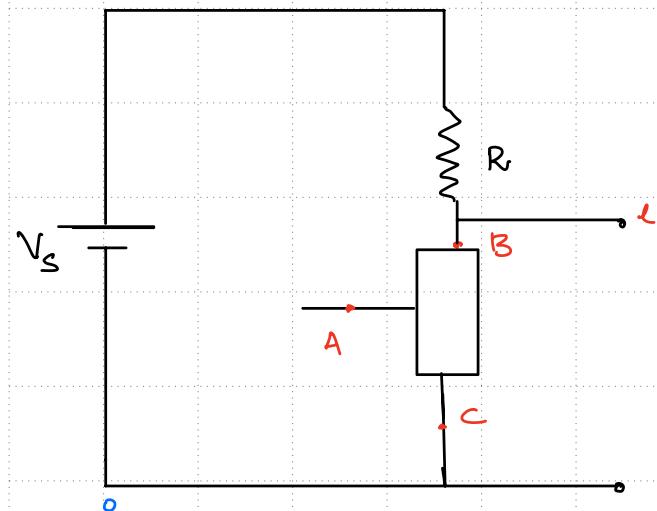
$B \in C \rightarrow$  Open

( $R \rightarrow \infty$ ) for any 3-terminal element

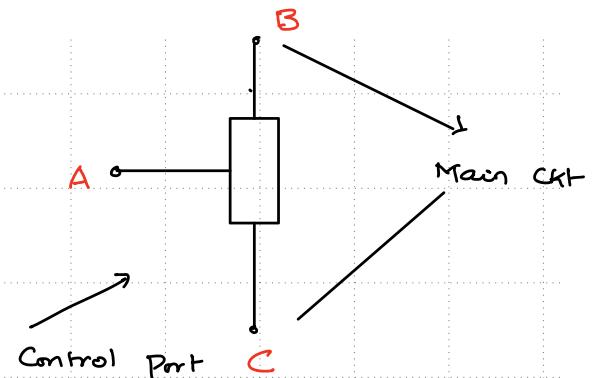
a) def Control Port & main CKT  
(A-C) (B-C)

b) Conditions on Control port  
( $\in$  main CKT)

- (i) Switch (ON & OFF)
- (ii) Amplifier short. open



$$V_L = \begin{cases} 0 & \text{(assuming ideal) when } V_{AC} > 0 \\ V_s & \text{when } V_{AC} < 0 \end{cases}$$



determines the current/voltage  
across the other two  
terminals.

## Three Terminal Circuit Elements (as a switch)

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Control Port is

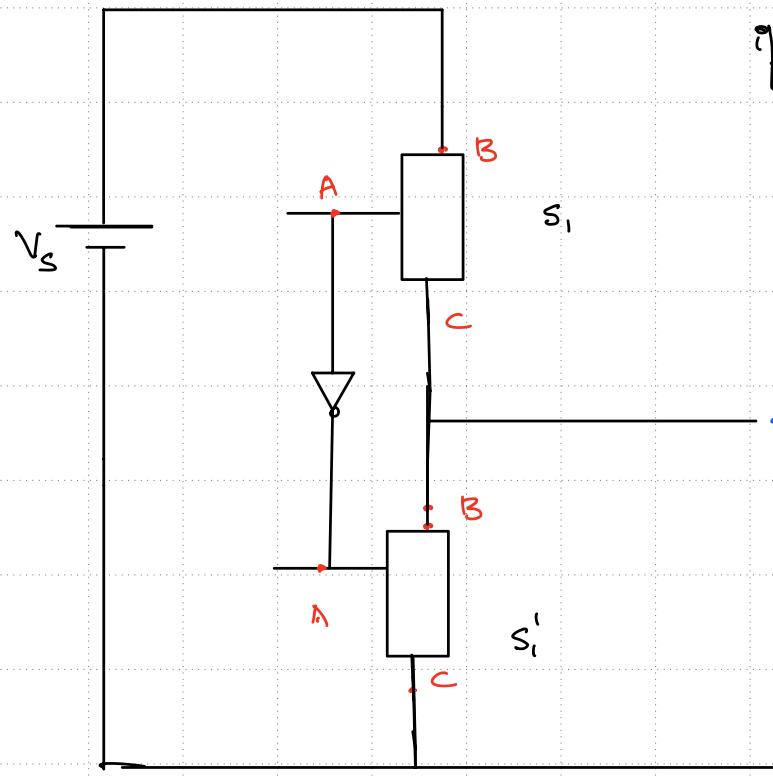
b/w A & C.

if  $V_{AC} > 0$  : ON state

$B \in C \rightarrow$  Short  
( $R \rightarrow 0$ )

if  $V_{AC} < 0$  :

$B \in C \rightarrow$  Open  
( $R \rightarrow \infty$ )



when  $V_{AC} > 0$  ( $S_1$ )  $\Rightarrow V_{AC} < 0$  ( $S_1'$ )

$$V_L = V_s$$

when  $V_{AC} < 0$  ( $S_1$ )  $\Rightarrow V_{AC} > 0$  ( $S_1'$ )

$$V_L = 0$$

$V_L$

