COURSE TITLE: INTRODUCTION TO CMOS PROCESSING
COURSE CODE: EE2520
Textbook: Integrated Circuit Fabrication (Science and Technology)
Authors: James D Plummer and Peter B. Griffith

Introduction

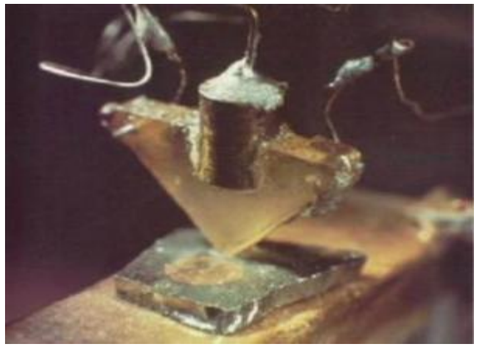
(Lecture1)

KEY CONCLUSIONS

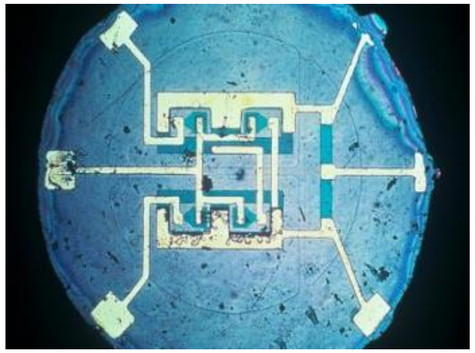
By the end of Introduction Lecture(s), you should be familiarized with

- History of Integrated Circuits
- Planar Process
- Moore’s Law
- Dennard Scaling
- Technology Node
- Unit Processes
- Course Objectives

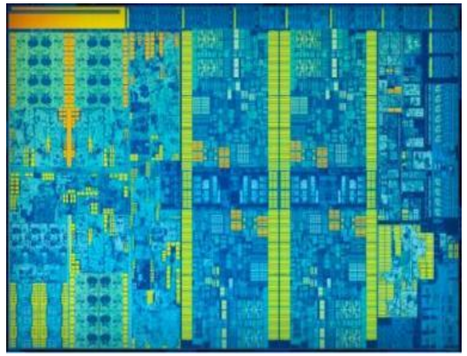
1948 - Present



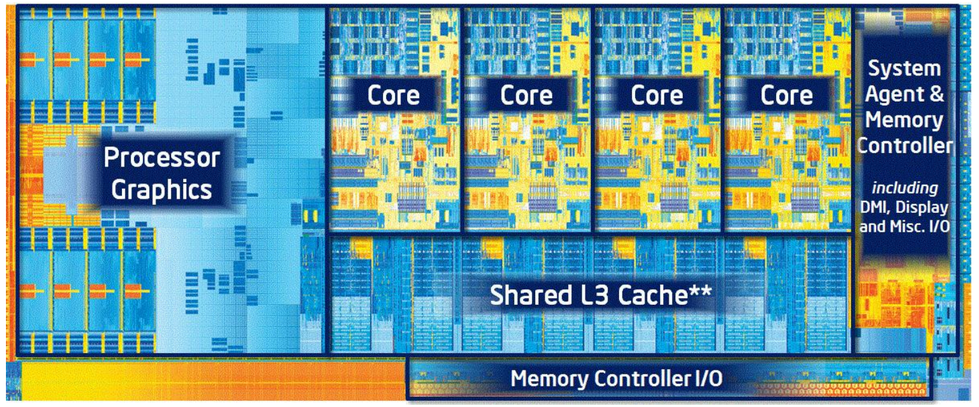
First Solid State Device



First Integrated Circuit

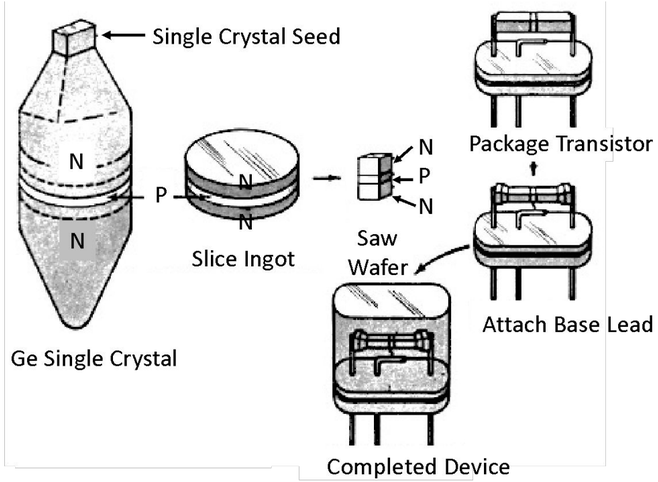


Latest Microprocessor

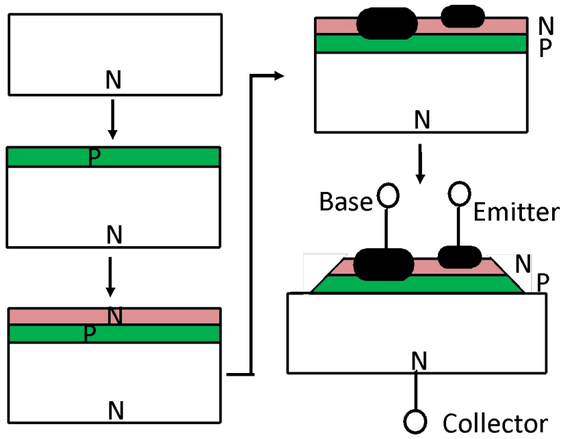


A Complex Chip (i7 processor)

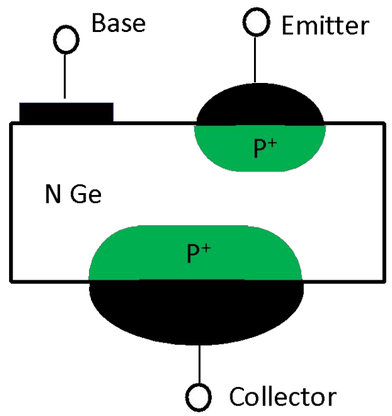
Bulk Vs Planar

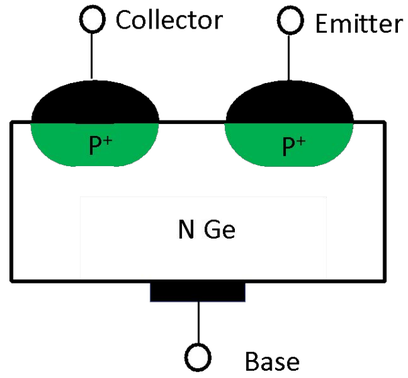


Grown junction transistor technology of the 1950s

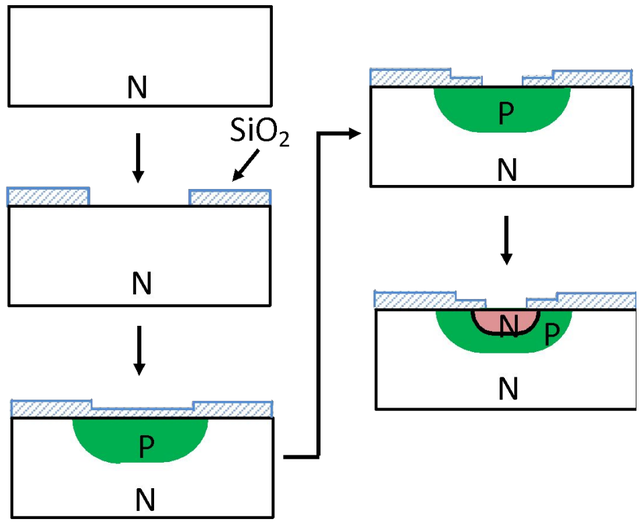


Double diffused transistor technology of the 1950s



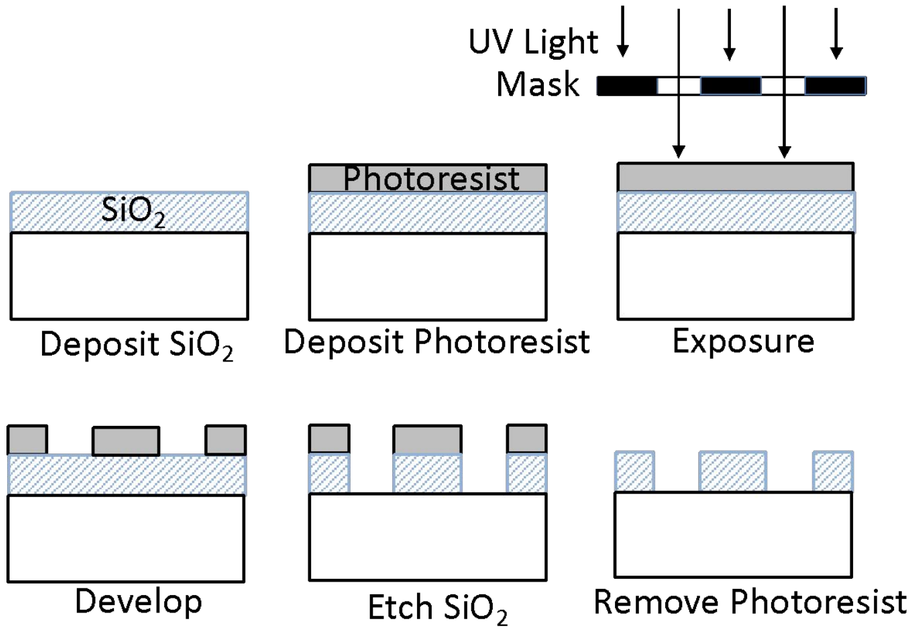


Alloy junction technology of the 1950s.

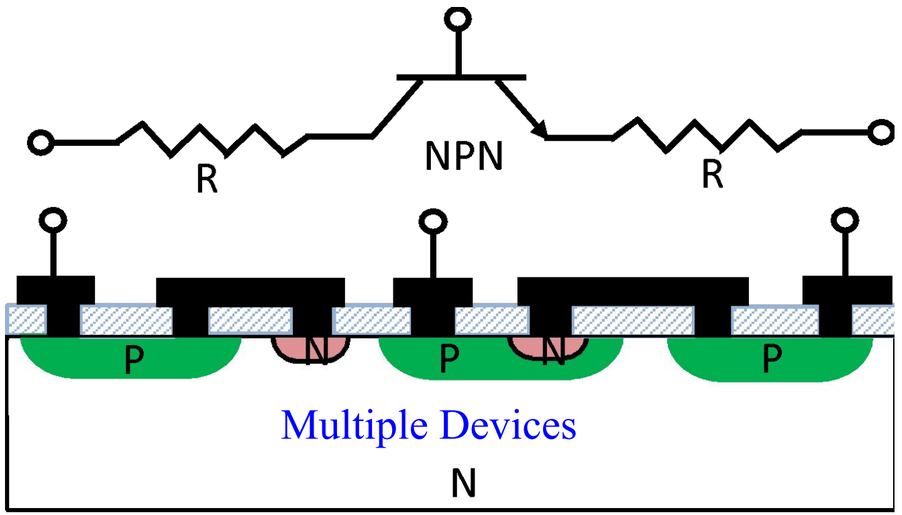


The planar process (Hoerni - Fairchild, late 1950s).

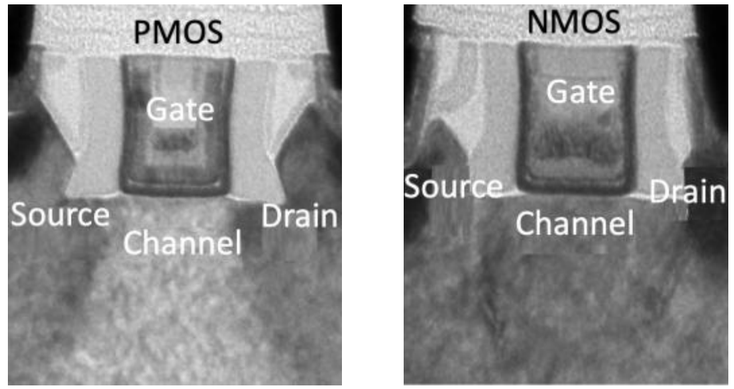
Planar Process



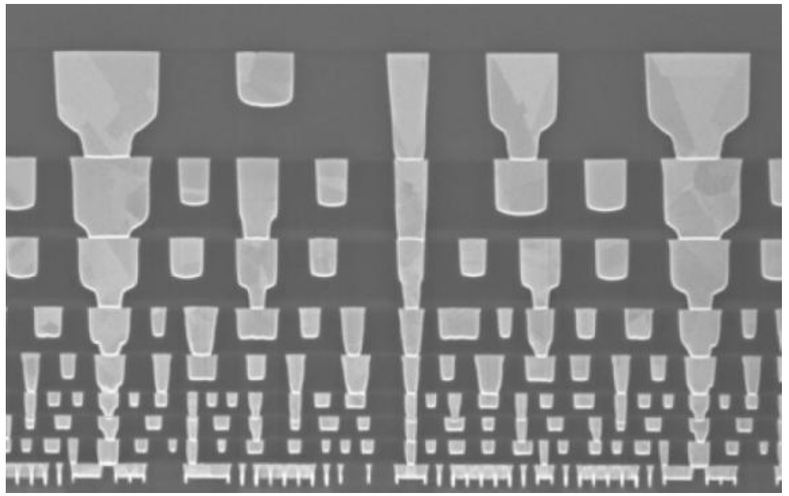
Basic lithography process



Multiple Devices

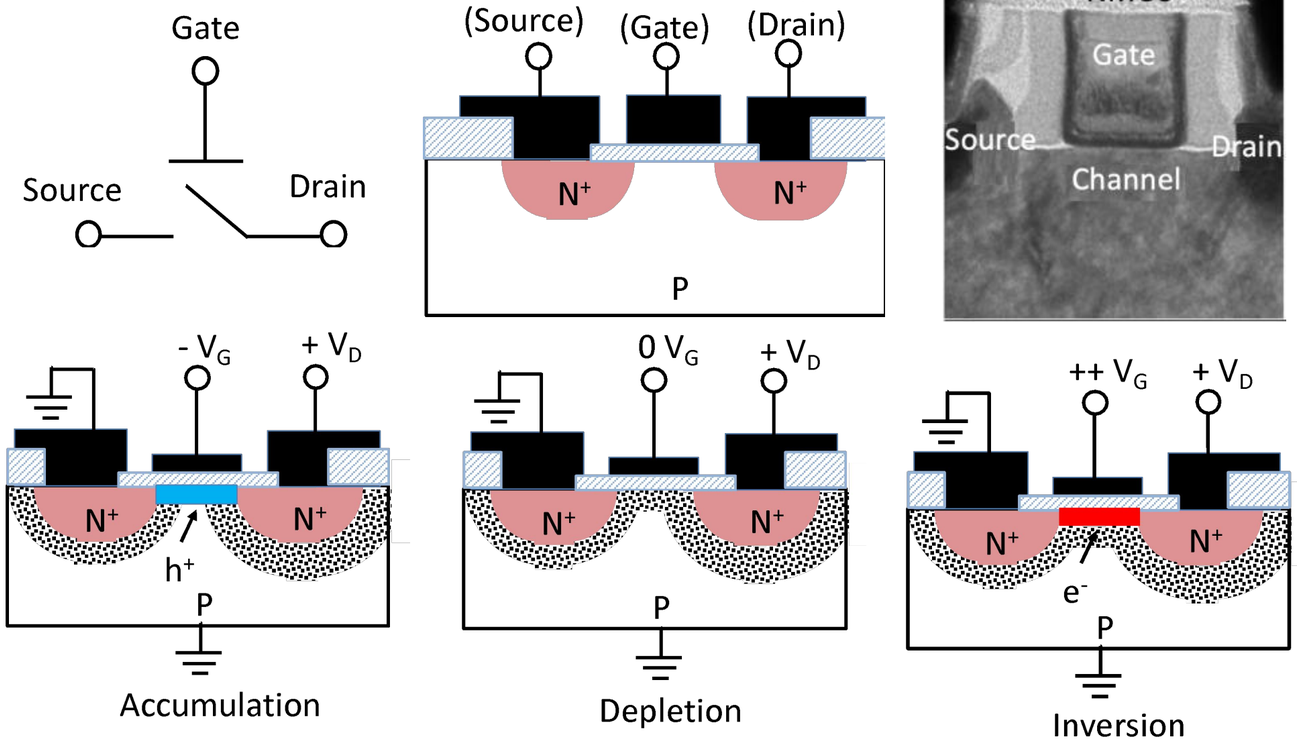


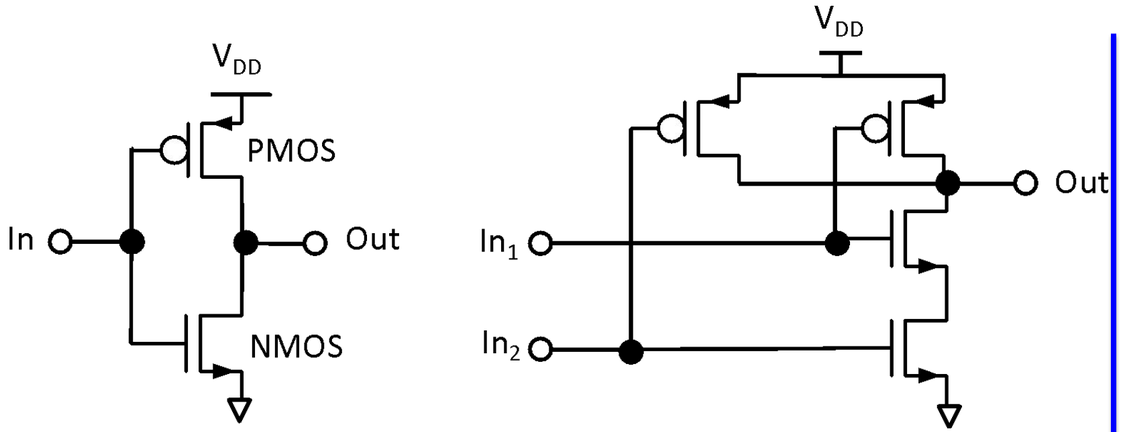
The Sub Micron Transistor

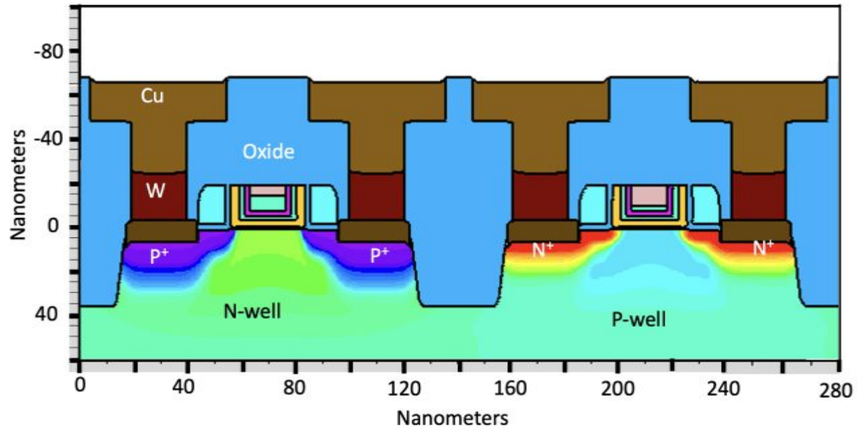


CMOS Transistors with Metal Interconnects

MOS Vs CMOS



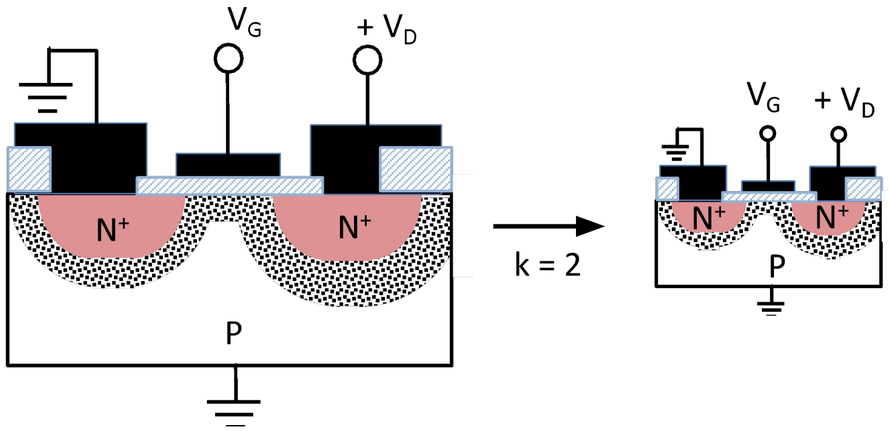




CMOS allows:

- High input impedance.
- 0 DC power dissipation.
- 0 and 1 voltage levels at Gnd and V_{DD}.
- High I_{ON}, low I_{OFF}.
- Highly flexible circuit/system design

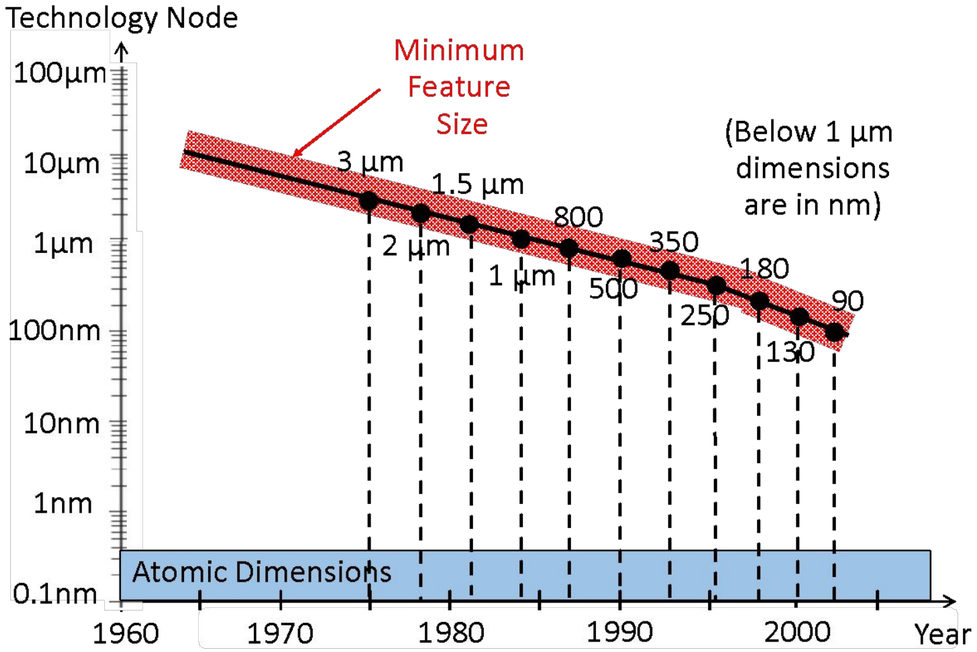
Dennard Scaling



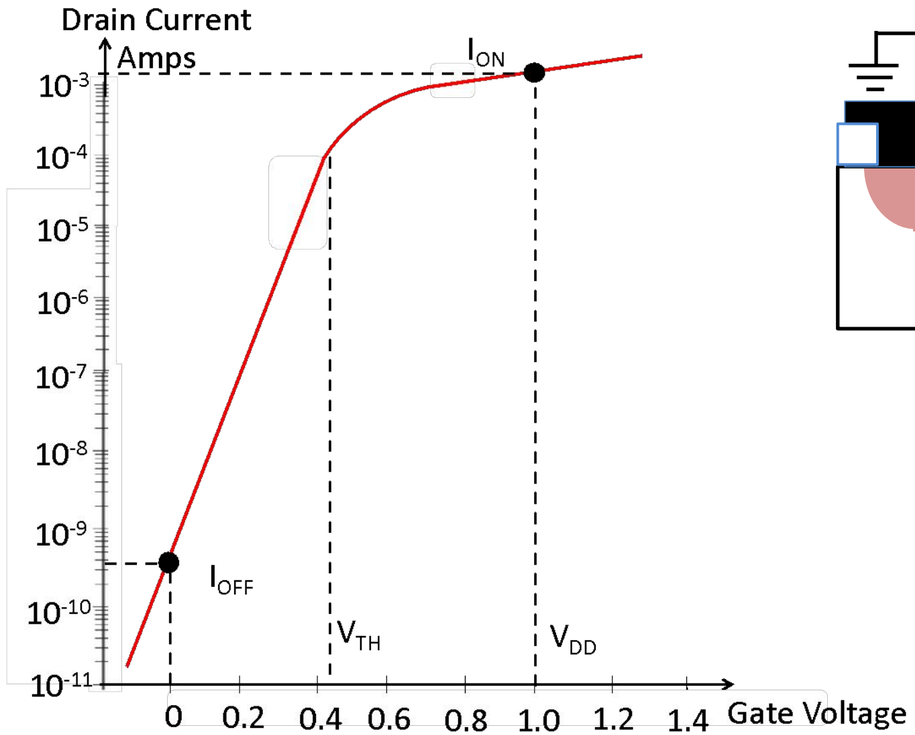
ITRS - 2003 version

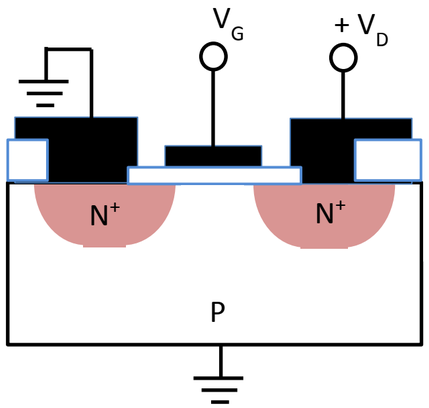
Device or Circuit Parameter	Scaling Factor
Device Dimension, t_{ox}, L, W	1/k
Doping Concentration	k
Voltage V	1/k
Current I	1/k
Capacitance $\varepsilon A/t_{ox}$	1/k
Delay time VC/I	1/k
Power Dissipation VI	$1/k^2$
Power Density VI/WL	1

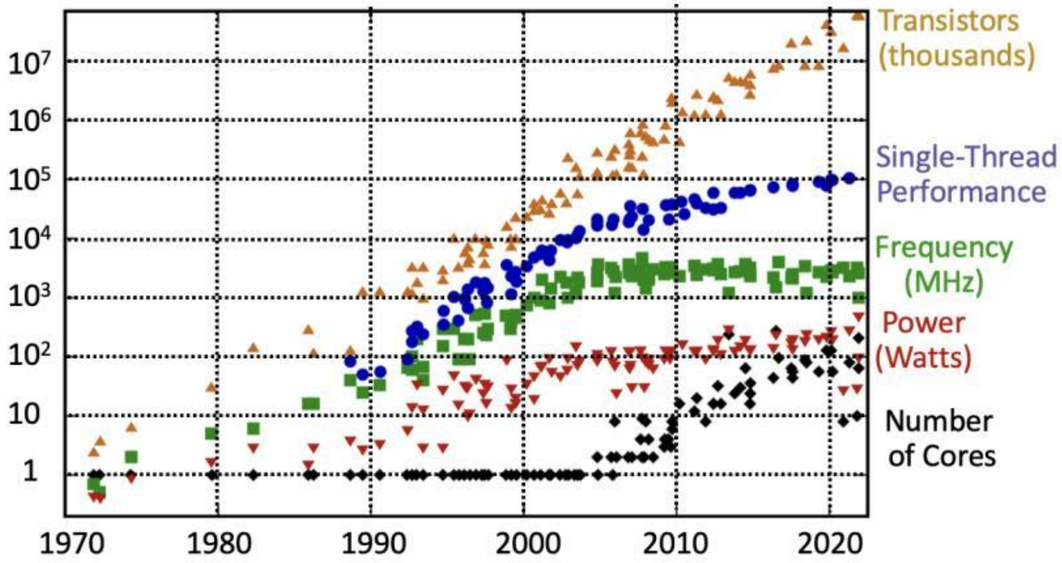
Year of Production	2000	2002	2004	2007	2010	2013	2016	2018
Technology Node (nm)	180	130	90	65	45	32	22	14
MPU Gate Length	100	70	53	35	25	18	13	10
DRAM Bits/Chip (GB)	.512	1	4	16	32	64	128	128
MPU Transistors (10^6)			550	1100	2200	4400	8800	14000
Supply Voltage (V)	1.5-1.8	1.2-1.5	0.9-1.2	0.8-1.1	0.7-1.0	0.6-0.9	0.5-0.8	0.5-0.7



Non Ideal Scaling

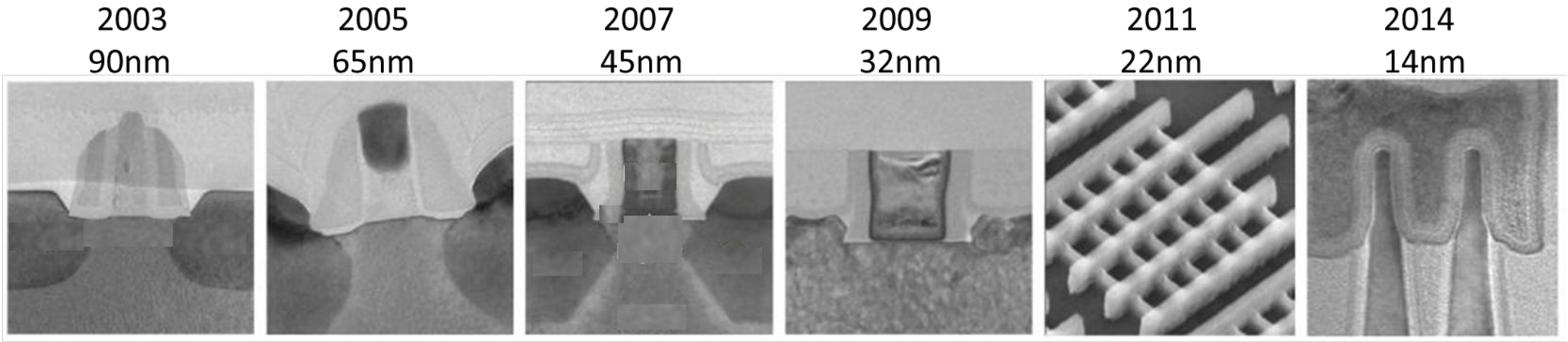


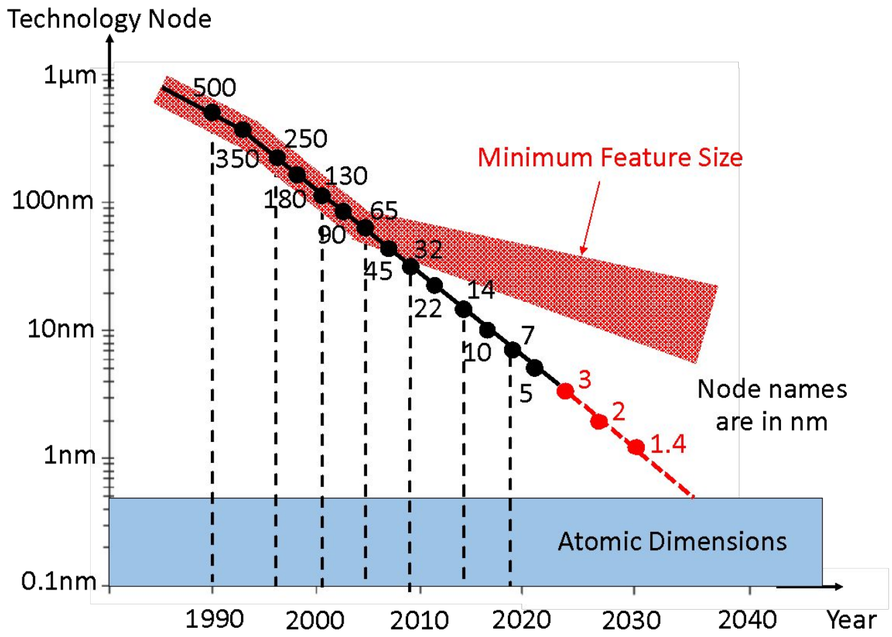




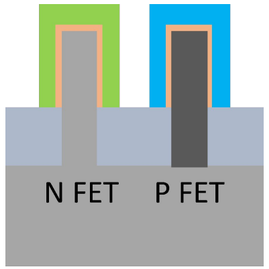
$$\text{Inverse slope} = \frac{kT}{q}\ln(10) = \frac{60\text{mV}}{\text{decade current (I)}}$$

Beyond Ideal Scaling - Innovations

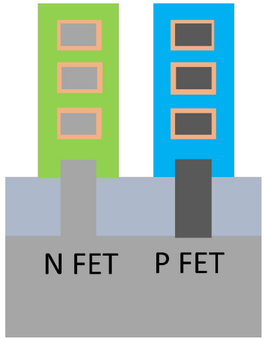




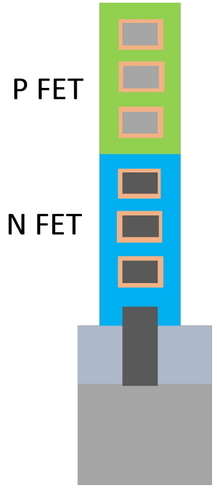
The two limited Regimes



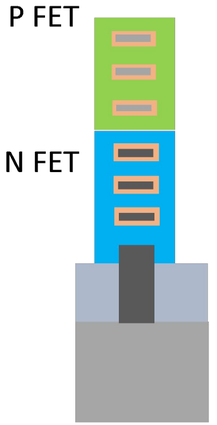
FinFET



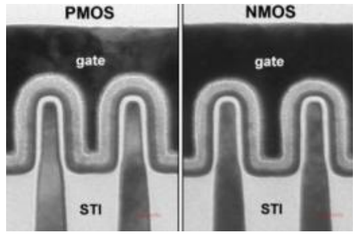
GAA FET

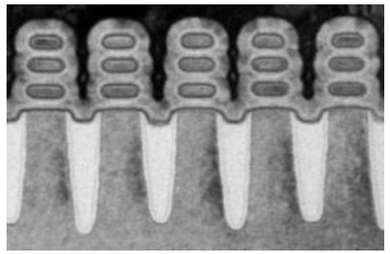


Stacked
GAA FET

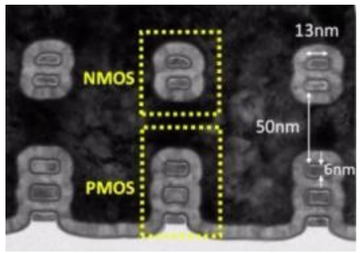


2D Channel
GAA FET





TSMC



Intel