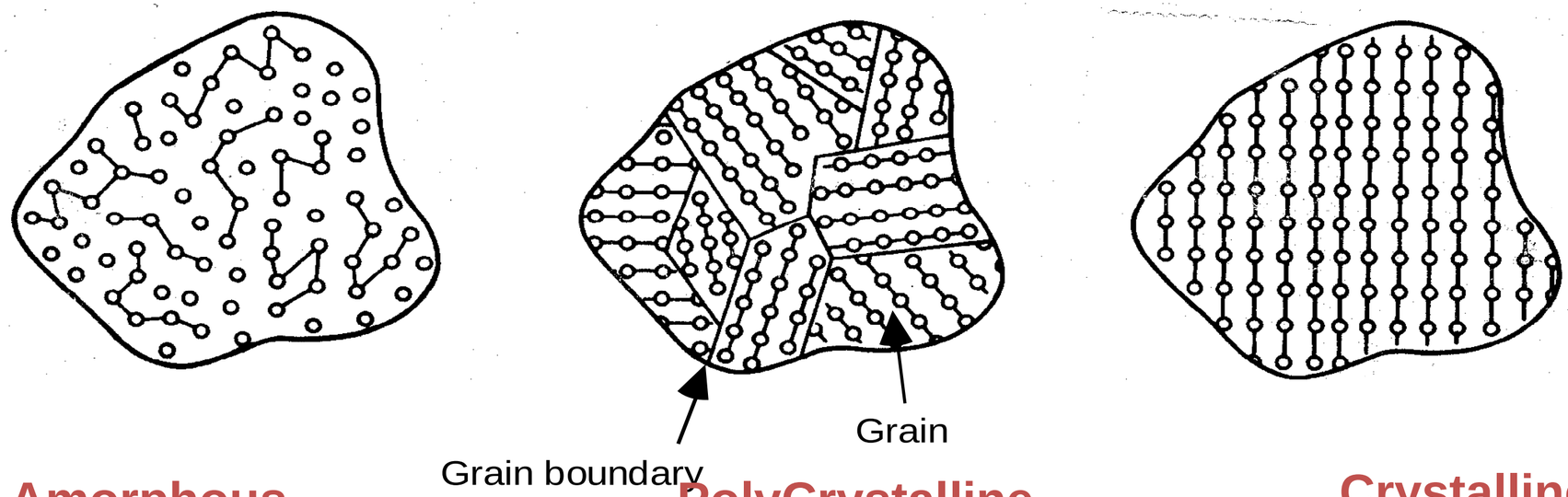
Silicon Substrate

(Wafer Preparation)

KEY CONCLUSIONS

Crystallanity



Amorphous

No Well Defined Order

Ex: Gate oxide of MOSFET

PolyCrystalline

Medium range order

Grains – Crystallinity

Grain Boundaries - Defects

Crystalline

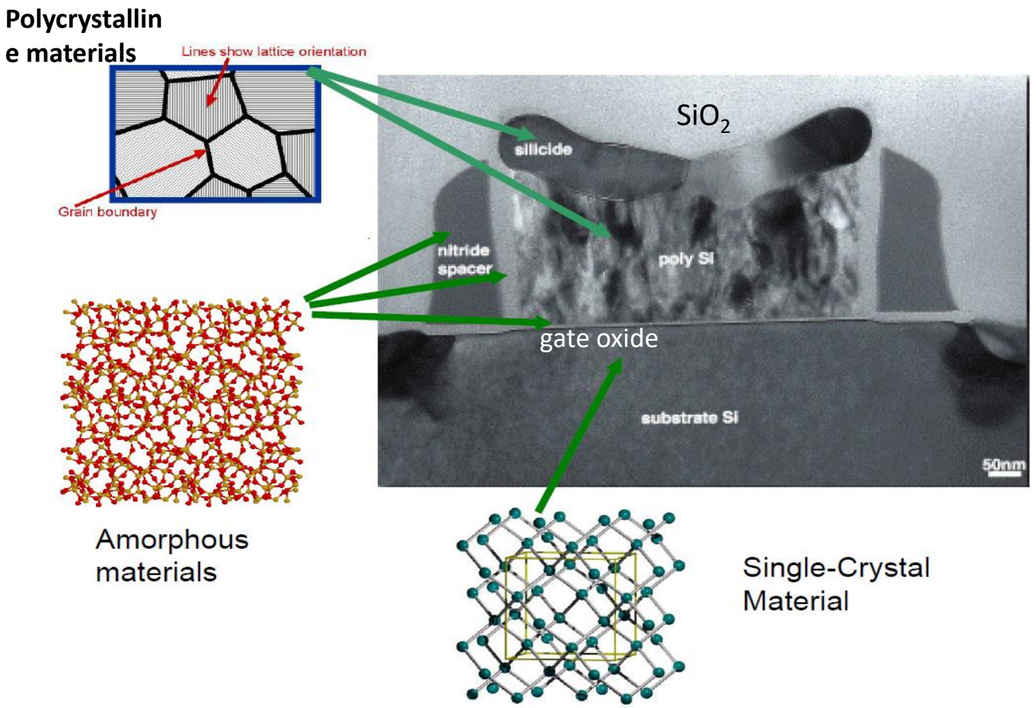
Long range order

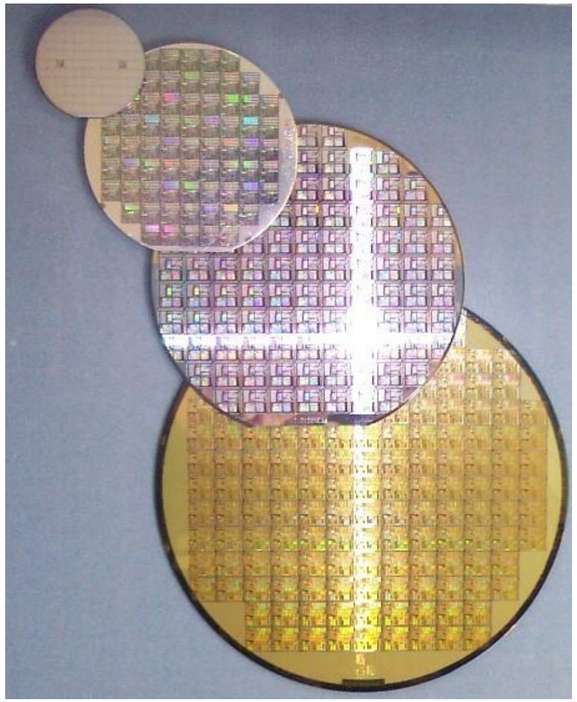
Unit Cell

Substrate:

- Single Crystal
- Better Control of Electronic Properties

Crystallanity

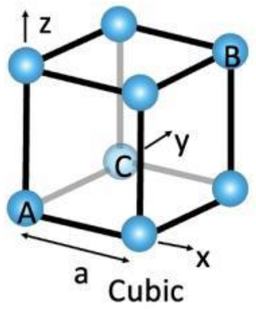


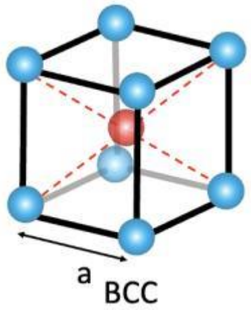


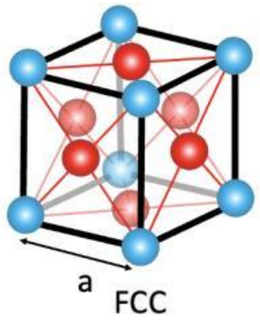
- Wafers are thin substrates on which micro fabrication is done
  - Usually 200-2000 um thick
  - Thickness decided by mechanical considerations
- Square or circular in shape
- Usually polished to mirror shine

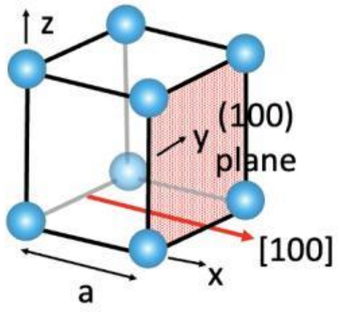
- Extremely pure
- Trace impurities in Si < 1 ppb, i.e. Better than 99.9999999% purity

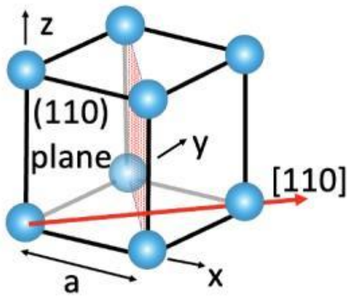
Cubic Crystallanity

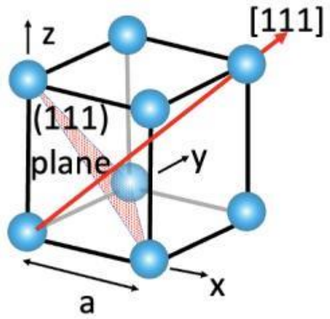






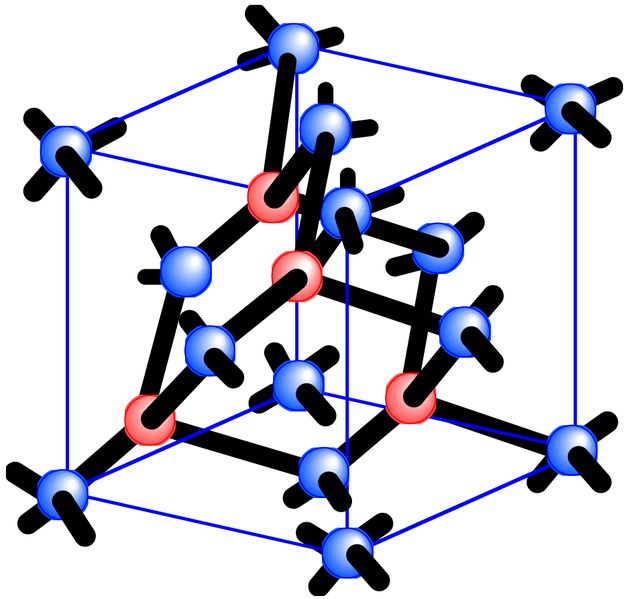






- Cartesian Coordinate System
- Miller Indices – - reciprocals of the intercepts of the plane with the x, y and z axes.
- [hkl] – Direction
- <hkl>: Set of all directions
- (hkl) – Plane
- {hkl} – Family of planes
- [hkl] is perpendicular to (hkl)

Single Crystal Silicon - Wafer

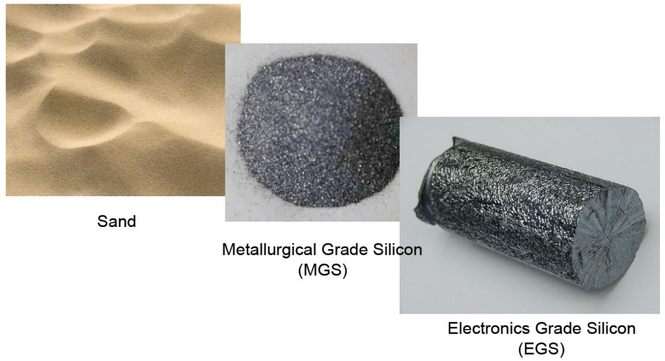


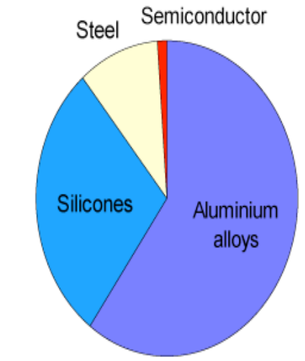
- Diamond Structure
- SP3 Hybridization
- Two merged FCCs offset by a/4 in x,y,z

	Possible values
Size	1”, 2”, 3”, 4”, 6”, 8”, 12”, 14”
Orientation	(110), (100), (111)
Grade	Prime > Solar > Test > Mechanical
Method	Float-zone (FZ), Czochralski (CZ)
Thickness	Usually 300 -800um, but can be 10-2000 µm
Resistivity	<0.005 Ωcm to 10^5 Ωcm
Finish	Single or double-side polish (SSP or DSP)
Processing	(Optional) oxide coating, epitaxy coating, etc.

	Si	Steel	Aluminium
Young’s Modulus (GPa)	130-190	210	70
Yield Stress (MPa)	5000	250-1500	15-20
Density (g/cm^3)	2.33	7.8	2.7
Thermal Conductivity (W/mK)	149	50.2	205

Silicon Wafer – Pre - preparation





Total production ~ 900 000 tonnes/p.a.

Element	Concentration (ppma)
Al	1200-4000
B	37-45
P	27-30
Ca	590
Cr	50-140
Cu	24-90
Fe	1600-3000
Mn	70-80
Mo	<10
Ni	40-80
Ti	150-200
V	100-200
Zr	30

Metallurgical Grade Silicon

- Quartzite (sand, SiO_2) is placed in a hot (~1800^{o}C) furnace with carbon releasing materials to form metallurgic grade silicon (MGS)
- Over 50% MGS is used to make Al alloys.
- The fraction used for semiconductors is very small.

$$2SiO_2(solid) + 2C(solid) \rightarrow Si(liquid) + 2CO(gas)$$

Electronic Grade Silicon

- Si -> liquid form ($SiHCl_3$) -> Si
- High temperature Reactions
- $Si + 3HCl \rightarrow SiHCl_3(g) + H_2(g)$
- $SiHCl_3$- liquid *at room temperature*, boiling point 32^{o}C.
- Distillation
- Hydrogen Reduction
- $SiHCl_3(g) + H_2(g) \rightarrow Si(s) + 3HCl(g)$
- Electronic Grade Silicon

Wafer Preparation steps

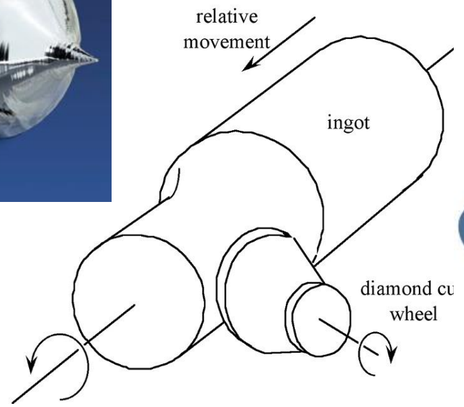
aescarbon.com

1. Polysilicon feed stock 99.999%

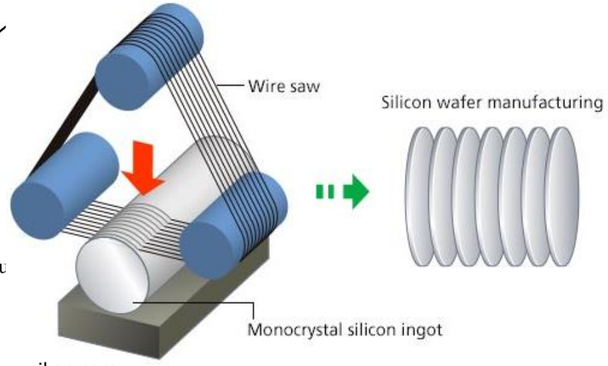
sifex.com

2. Ingot

3. Shaping



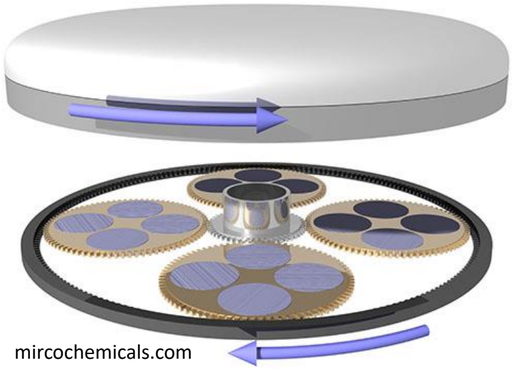
cnx.org



nikon.cpm

4. Slicing

5.Etching & 6. Polishing

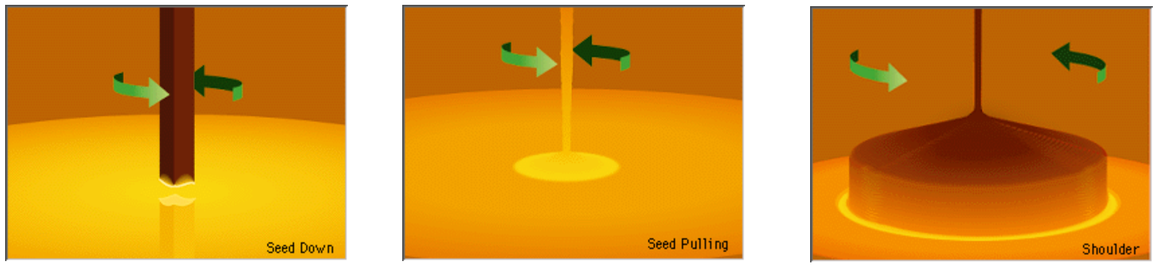


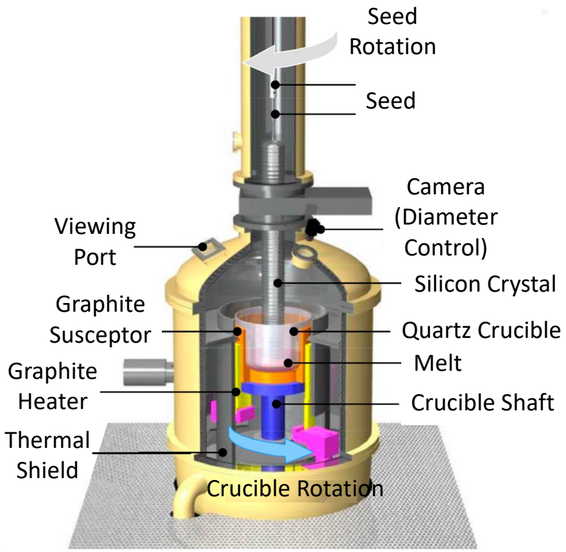
mircochemicals.com

- Ingot Preparation
- Grinding
- Slicing
- Polishing

Ingot Preparation – Czochralski method

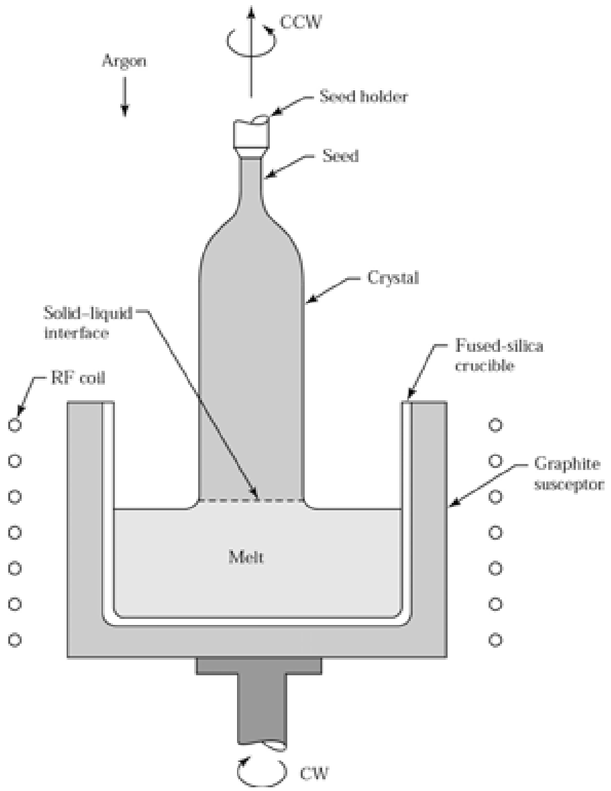
- Developed by Jan Czochralski in 1918
- Most common method to fabricate Si wafers
- Small pieces of EGS in an SiO2 crucible
- Heated above 1417 ˚C in inert ambience
- Dopants are added in the melt
- Insertion of single crystal seed and slow pull up
- Crystal orientation and wafer diameter determined by seed orientation and pull rate)
- Melt flows up the seed and cools as crystal begins to grow.
- Seed rotated about its axis to produce a circular cross-section crystal.





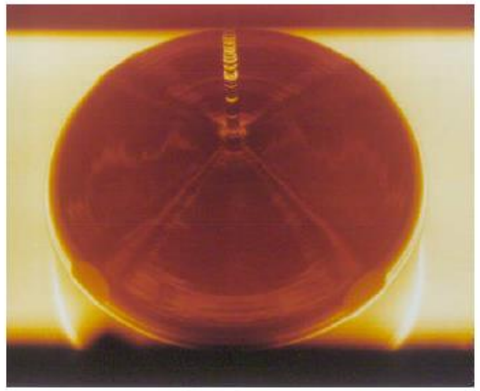
Si ingot or boule
Purity >99.9999999% possible

Czochralski method

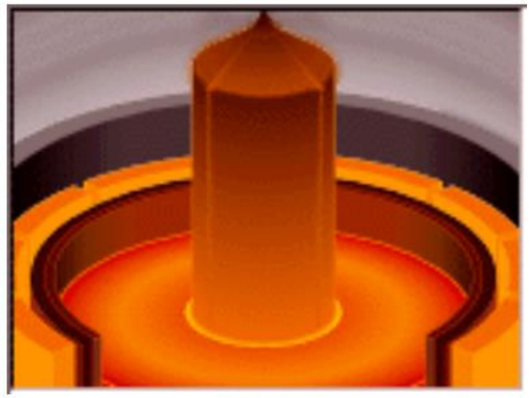


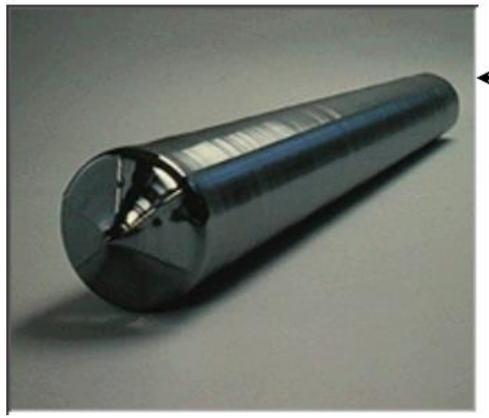
A commercial CZ puller

Early in the growth process



Later in the growth

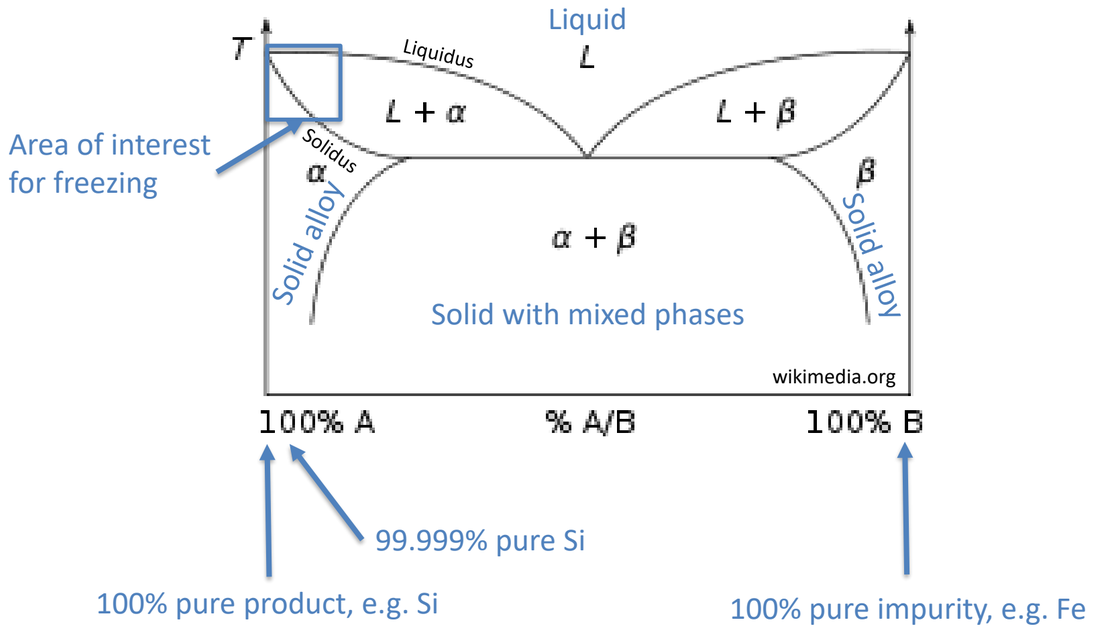


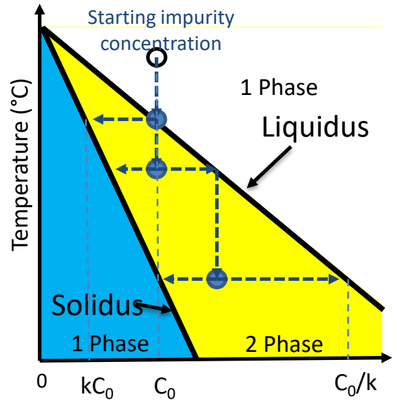


finished boules

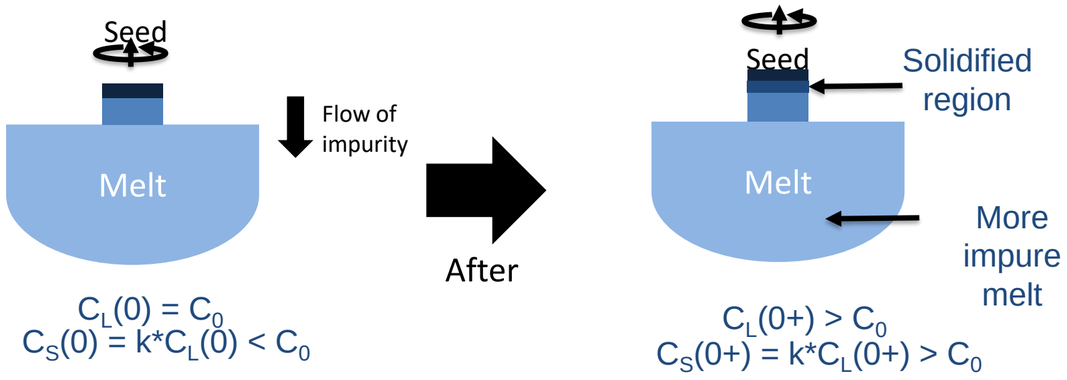
CZ silicon - Characteristics

- Growth is easiest with (111) orientation
- Surface energy of (111) < surface energy (100) < surface energy (110)
- Oxygen get incorporated in to the crystal
  - 10^{16}-10^{18} cm^{-3}
  - Mostly by etching of SiO_2 crucible
  - Makes the crystal stronger
- Zone refining and purification process is inherent !!!
- Distribution coefficient (k) for any impurity is:
  - $k = \frac{C_S}{C_L}$
  - C_S is the concentration of impurity in solid
  - CL is the concentration of impurity in liquid





Impurity and Doping Profile



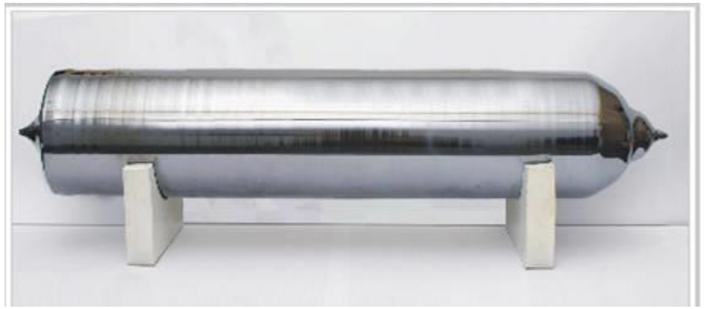
$C_L(0) = C_0$
$C_S(0) = k*C_L(0) < C_0$

Solid is purer than solution!

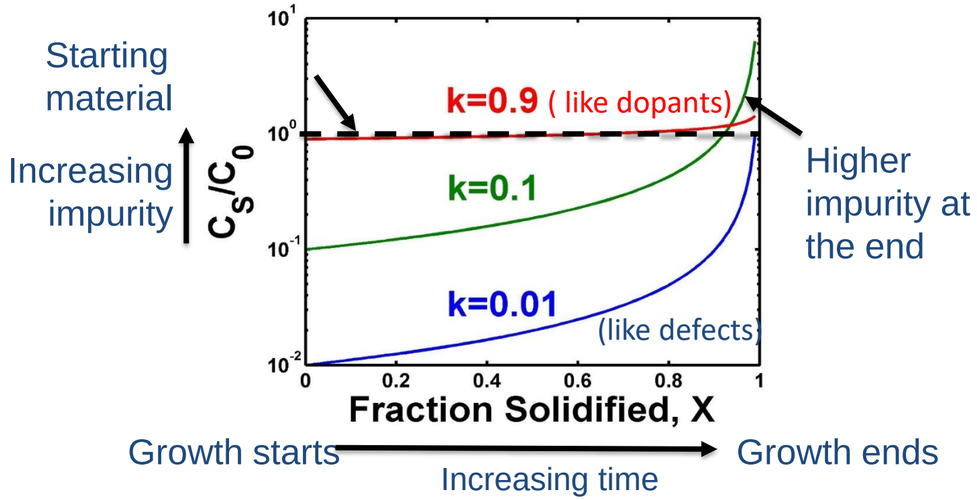
$C_L(0+) > C_0$
$C_S(0+) = k*C_L(0+) > C_0$

Liquid becomes more impure
Subsequent solid will also be more impure

Start
More pure
Less doped

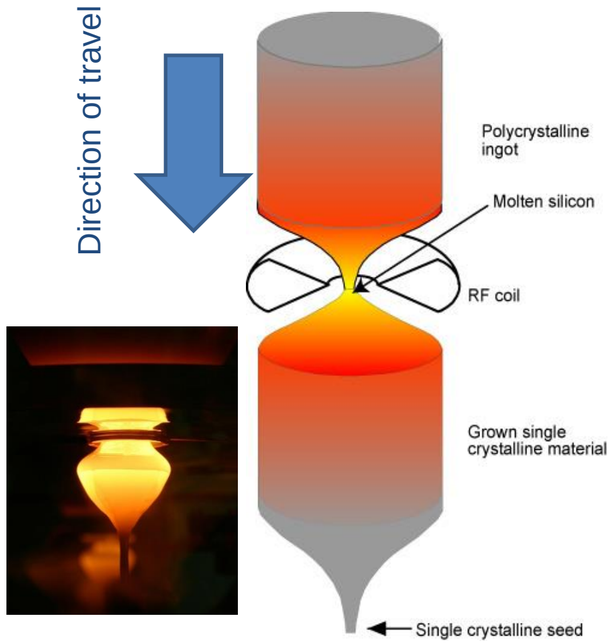


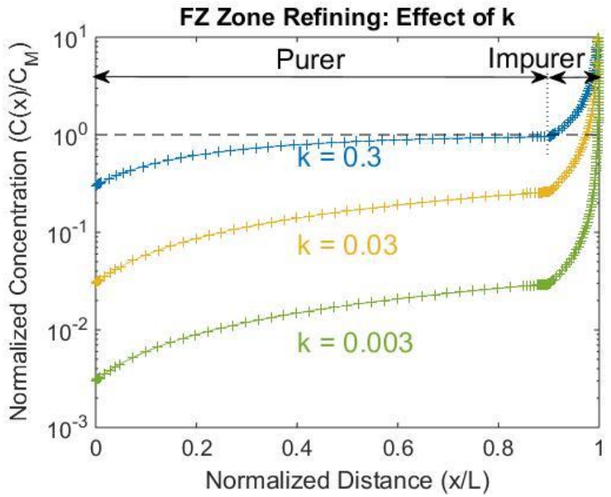
End
Less pure
More doped

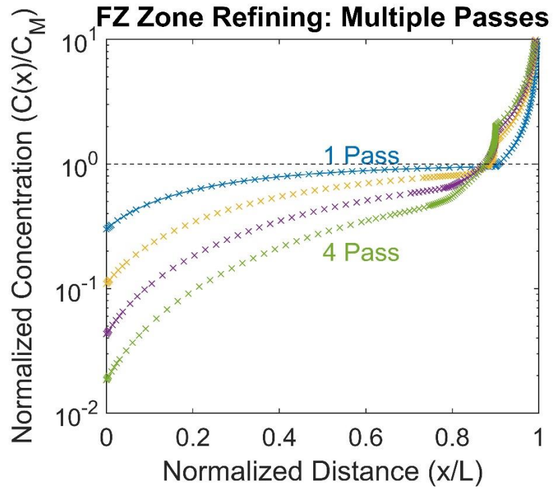


Impurity	Segregation Coefficient
As	0.3
Bi	7×10^{-4}
C	0.07
Li	10^{-2}
O	0.5
P	0.35
Sb	0.023
Al	2.8×10^{-3}
Ga	8×10^{-3}
B	**0.8**
Au	2.5×10^{-5}

Float Zone method

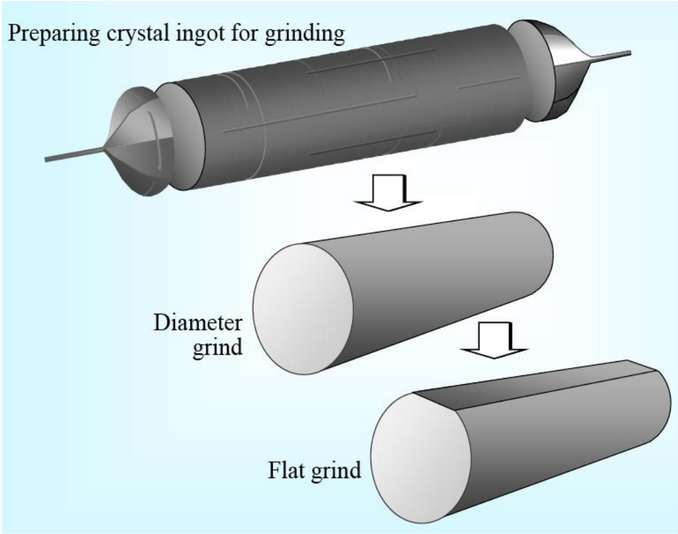


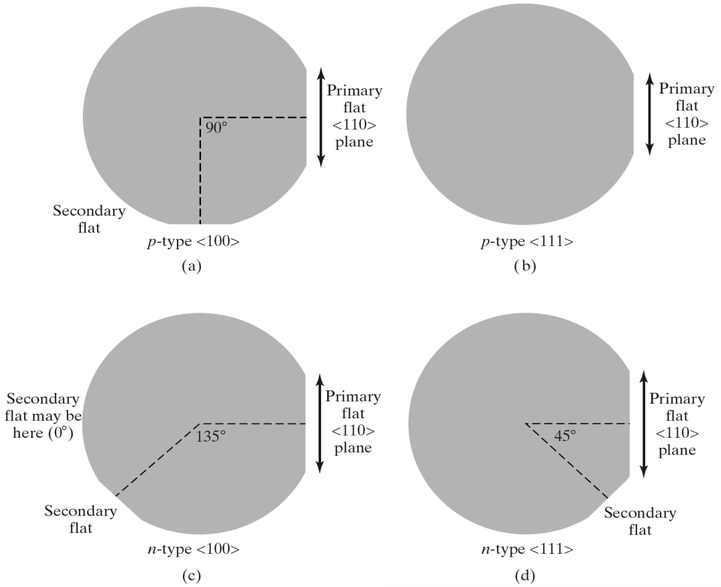


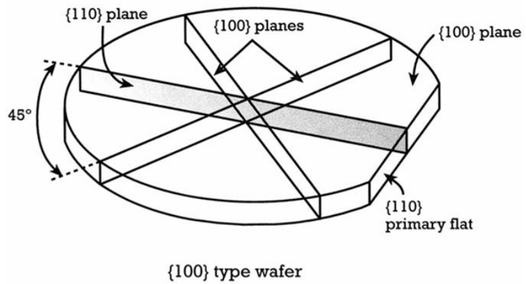


- Grows higher purity material than CZ
  - Very low doping levels possible
    - Resistivity >10^5 Ohm cm
  - Very low Oxygen
    - < 10^{15} cm^{-3}
  - Lower defect contamination
    - 10x lower
- Starts with a solid rod
  - Not a melt. Typically CZ ingot.
- More expensive (upto 5-10x)
- Zone refining can be done multiple times

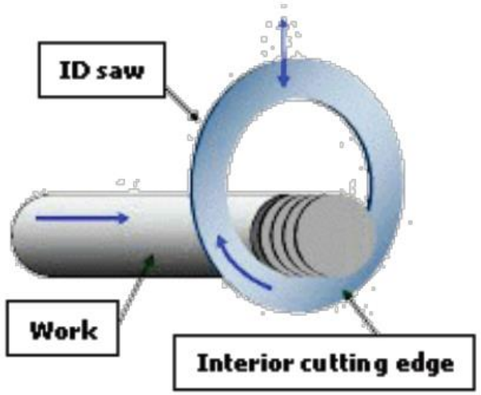
Wafer Preparation steps

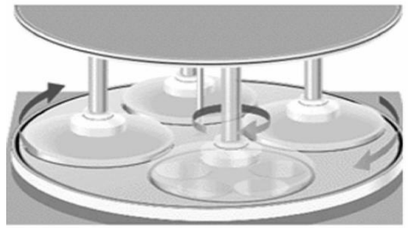


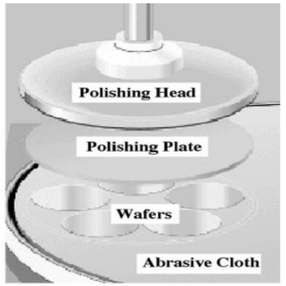




{100} type wafer







THANK YOU