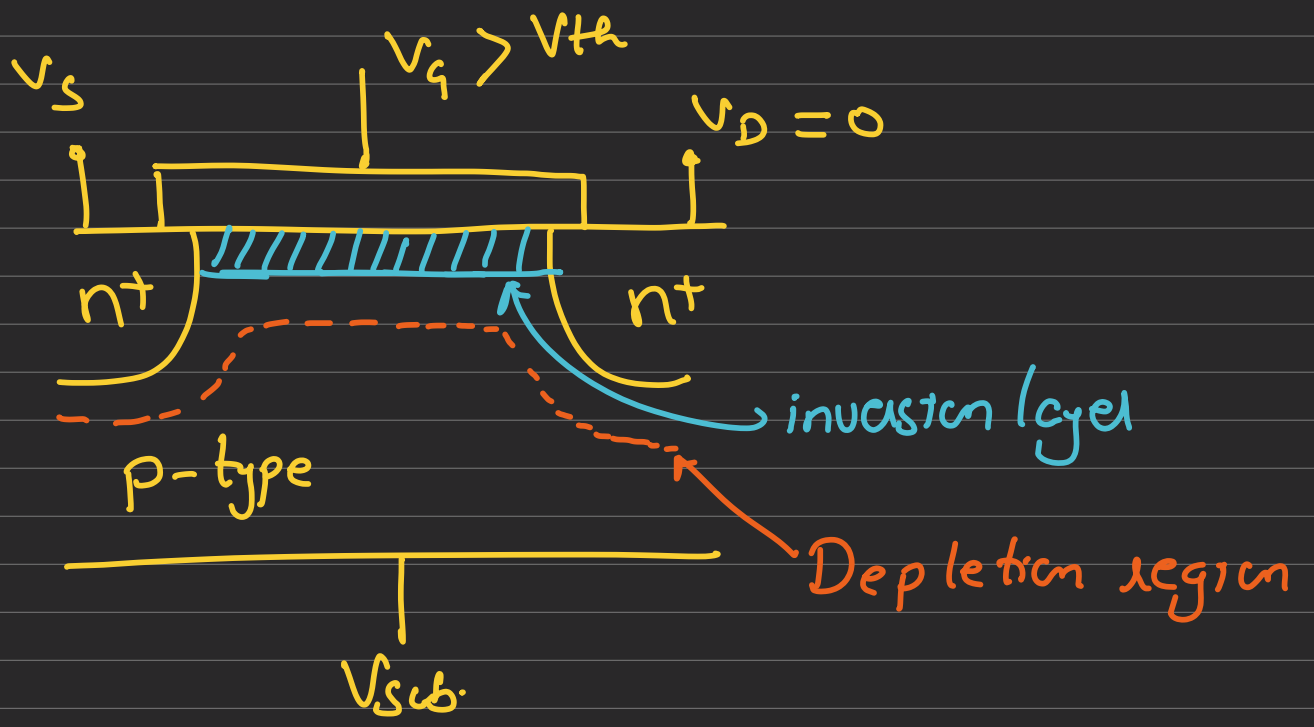
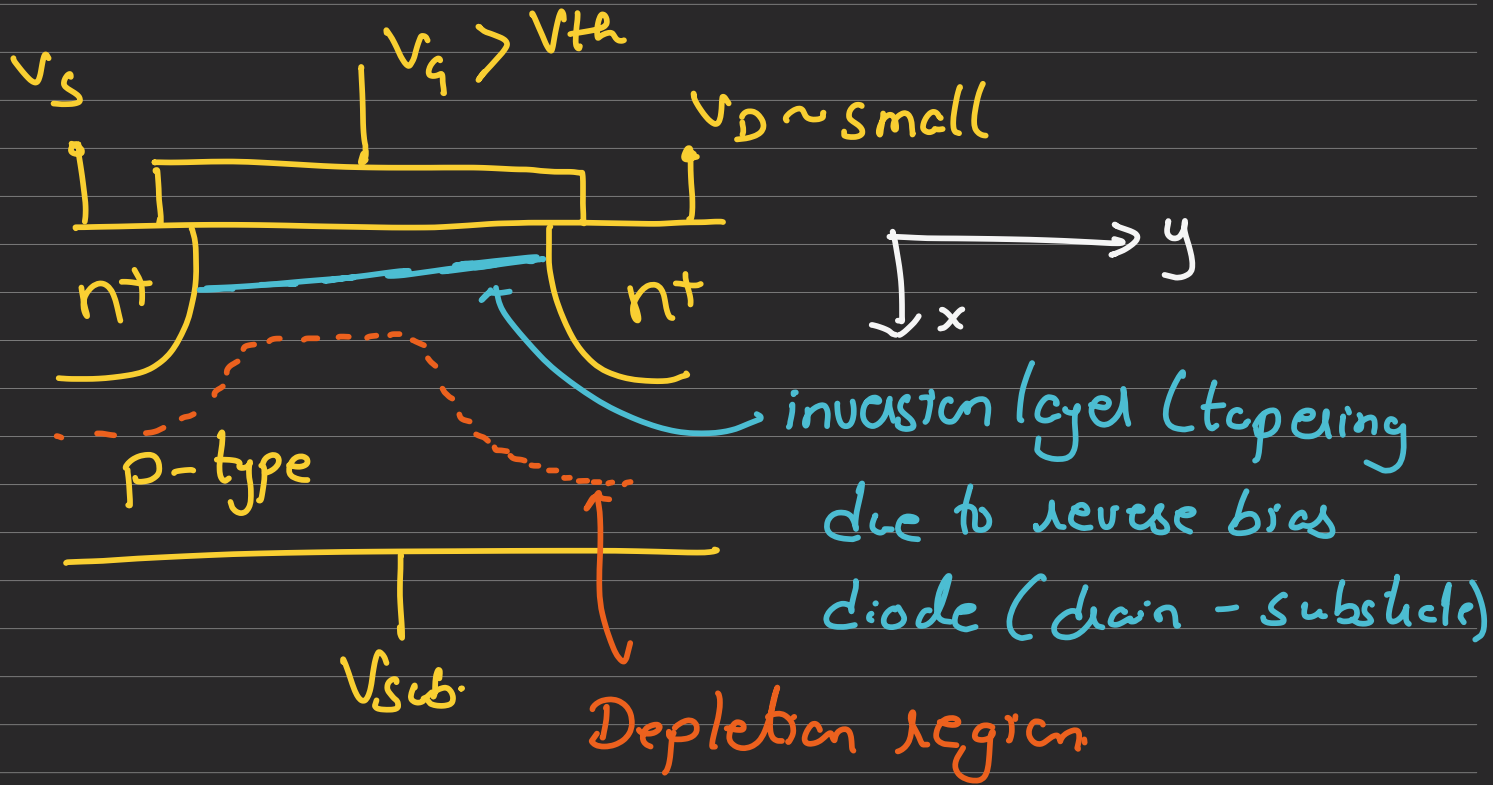
MOSFET



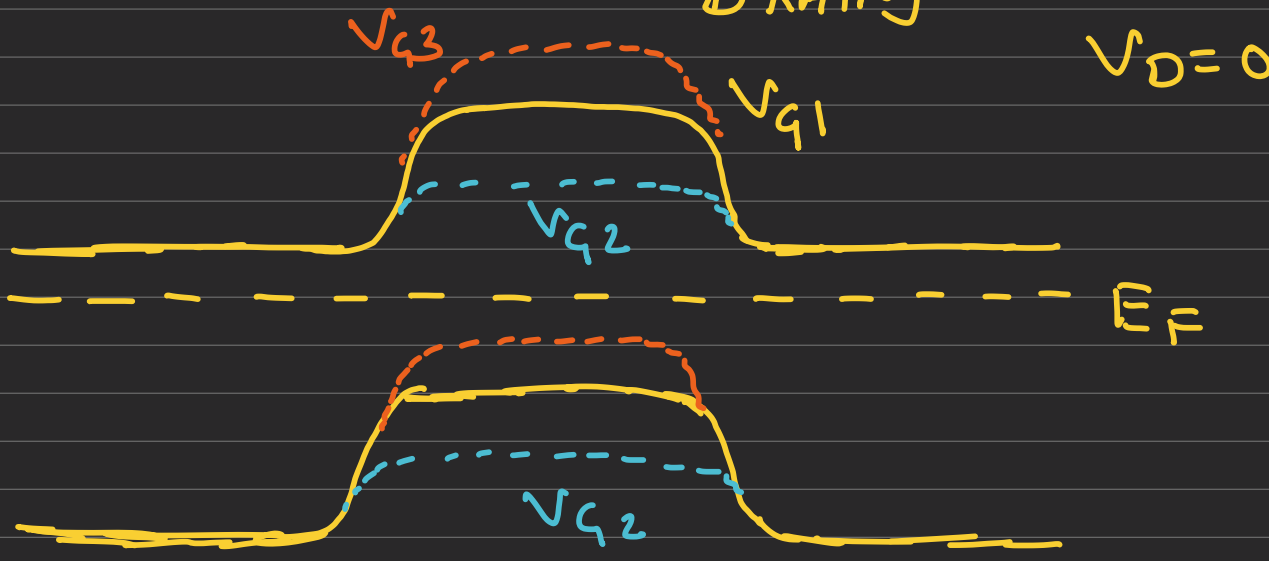


ASSUMPTIONS IN THE FOLLOWING ANALYSIS

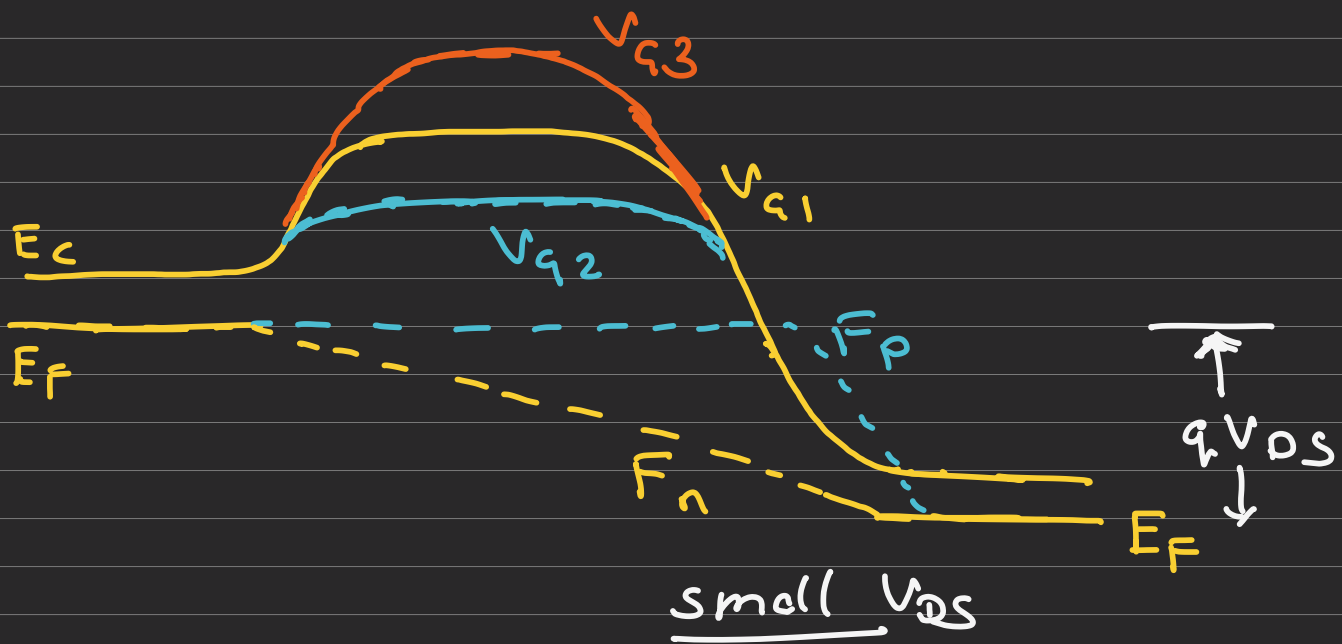
(1) GRADUAL CHANNEL APPROXIMATION [$\bar{E}_x \gg \bar{E}_y$]

(2) Charge sheet approximation [inversion charge exist only at the oxide-semiconductor interface]

Lateral Band diagram [SOURCE - CHANNEL - DRAIN]



$V_{G2} < V_{G1} < V_{G3}$



small V_{DS}

ON-state I-V characteristics [current flow mechanism - drift]

$$Q_{inv} = C_{ox}[V_{GS} - V_T - V(y)]$$

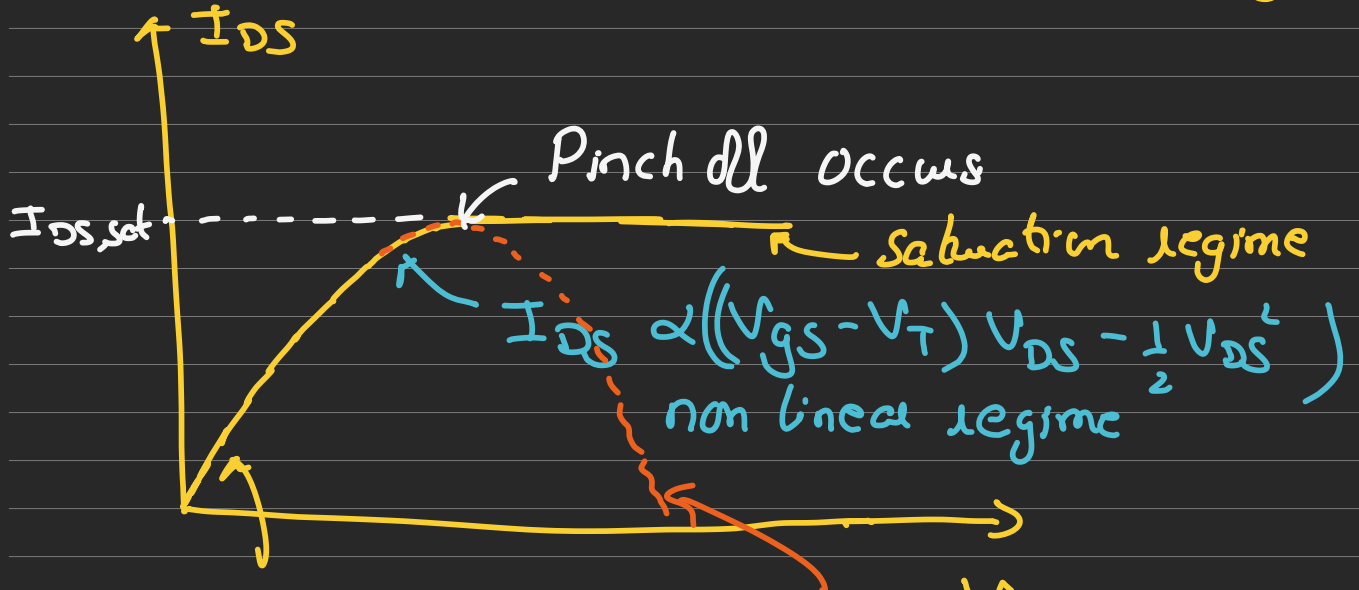
$I = q Q_{inv} \mu \mathcal{E}$ $\quad$ $W \rightarrow$ width of MOSFET

$= W q \mu C_{ox} \left[V_{GS} - V_t - V(y) \right] \frac{dV}{dx}$

$$\int_0^L I \, dy = \int_0^{V_{DS}} q \mu C_{ox} \left[V_{GS} - V_t - V(y) \right] dV$$

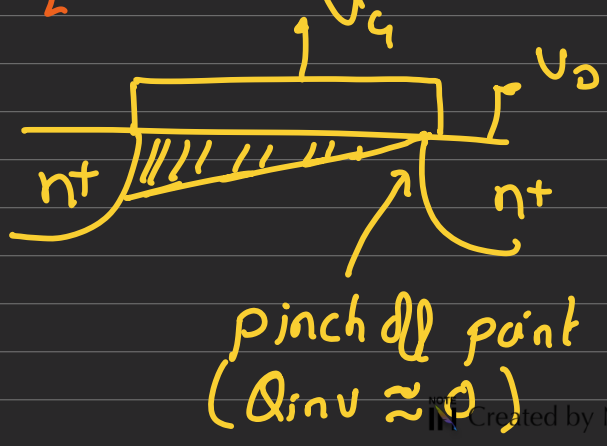
$$I L = q \mu C_{ox} W \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_{DS} = q \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] *$$



$I_{DS} \propto \left((V_{GS} - V_T) V_{DS} \right)$
(linear regime)

E_L *



More correct form of eq.

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{m}{2}V_{DS}^2\right]$$

$m = 1 + \frac{C_D}{C_{ox}}$ $\quad C_D \rightarrow$ depletion capacitance

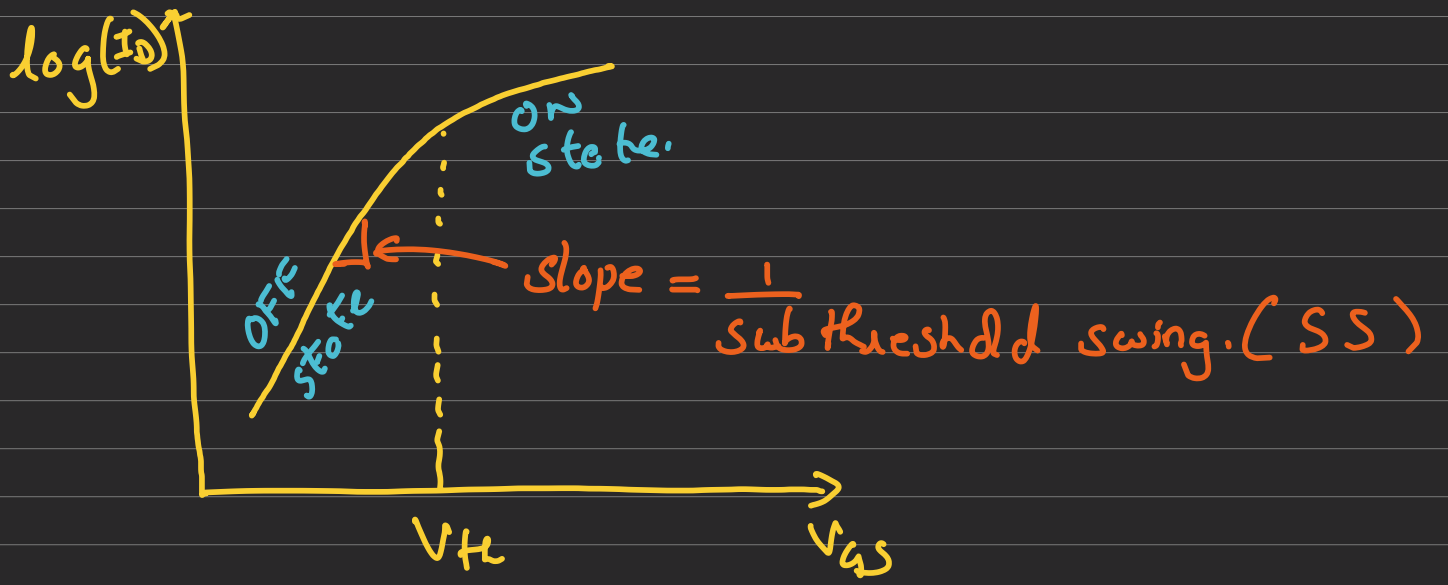
$C_{ox} \rightarrow$ Oxide capacitance ε_{ox}/t_{ox}

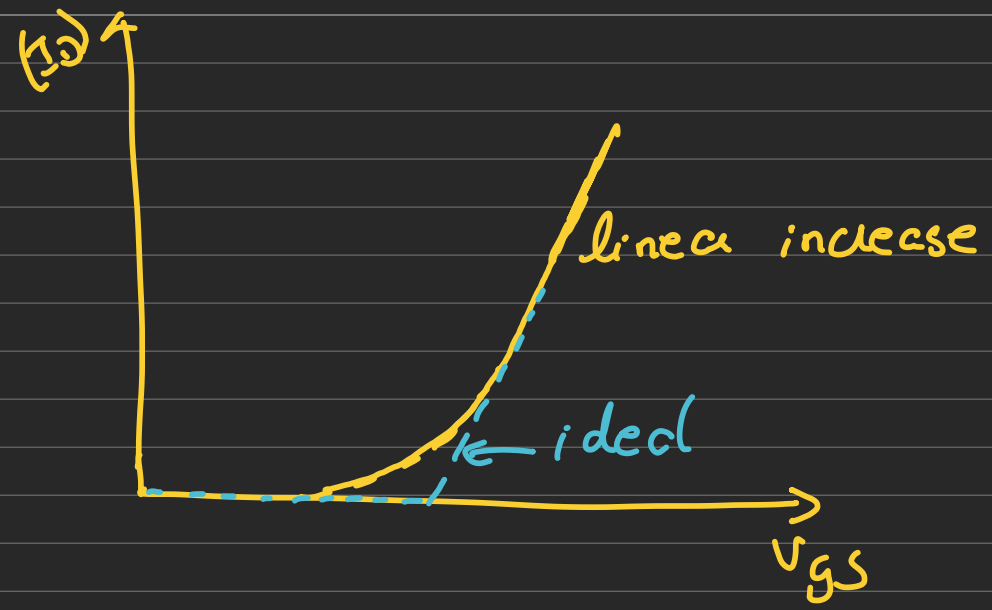
Saturation occurs (max of I_{DS}) when

$$V_{DS} = \frac{V_{GS} - V_T}{m}$$

$$I_{DS}^{(sat)} = \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2m}$$

Transfer Characteristics





OFF state characteristics (low V_{DS})

Current flow mechanism Diffusion

$$I_{DS} \propto \frac{n(0) - n(L)}{L}$$

$$n(0) = n_{p0} \exp\left[\frac{\Psi_S}{V_T}\right] \qquad V_T = \frac{k_B T}{q}$$

$$n(L) = n(0) \exp\left[\frac{-V_{DS}}{V_T}\right]$$

Ψ_S surface potential

$$I_{DS} \propto n_{p0} \exp\left[\frac{\Psi_S}{V_T}\right]\left[1 - \exp\left[\frac{-V_{DS}}{V_T}\right]\right]$$

V_{DS} is larger than $k_B T/k$ $\quad \exp\left[\frac{-V_{DS}}{V_T}\right] \approx 0$

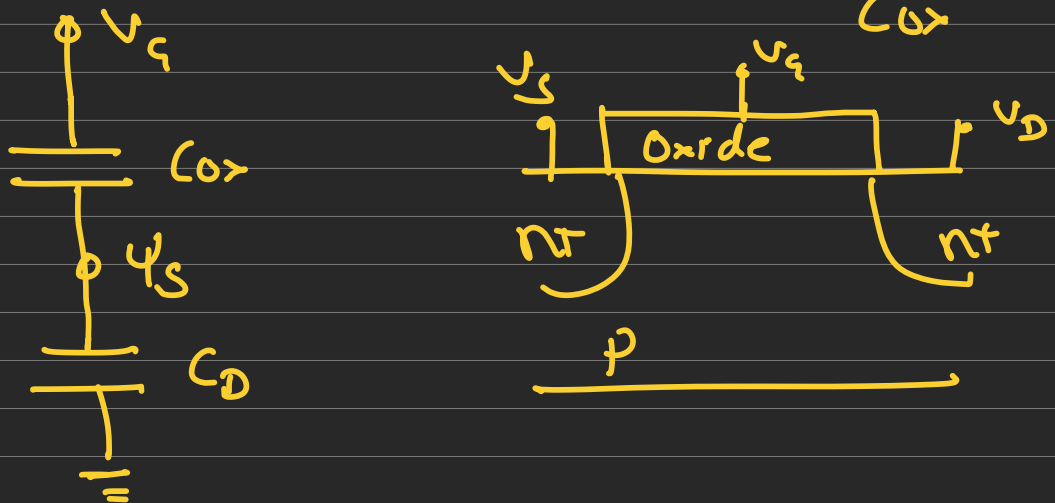
$$I_{DS} \propto \exp\left[\frac{\Psi_S}{V_T}\right]$$

$$\log(I_{DS}) \propto \frac{\psi_s}{V_T} \log(e) \propto \frac{\psi_s}{V_T \ln(10)}$$

$$\frac{\partial \log(I_{DS})}{\partial V_{GS}} = \text{slope} = \frac{1}{SS} = \frac{1}{V_T \ln(10)} \frac{\partial \psi_s}{\partial V_{GS}}$$

$$SS = \frac{\partial V_{GS}}{\partial \log(I_{DS})} = V_T \ln(10) \underbrace{\left(\frac{\partial V_{GS}}{\partial \psi_s}\right)}_{m}$$

$$= 1 + \frac{C_D}{C_{ox}}$$



$$m = \frac{\Delta V_G}{\Delta \psi_s} \Rightarrow \Delta V_G = \left(1 + \frac{C_D}{C_{ox}}\right) \Delta \psi_s$$

Interpretation of body factor m

$$SS = V_T \ln(10) \left[1 + \frac{C_D}{C_{ox}}\right]$$

$$60 \left[1 + \frac{C_D}{C_{ox}}\right] \text{ mV/dec.}$$

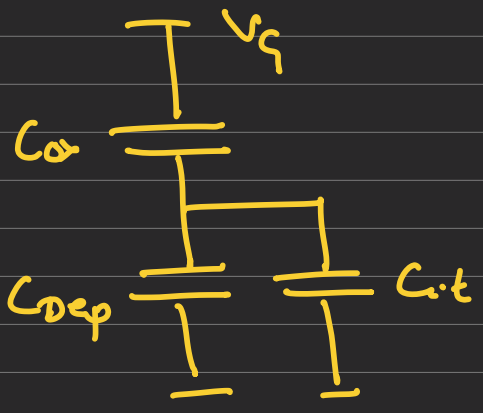
$m > 1$

SS → amount of change in the gate bias that is required to change the drain current by a factor of 10 [decade] $SS = \frac{\Delta V_{GS}}{\Delta \log(I_{DS})}$

$\min[SS] \rightarrow 60$ mV/dec [when $C_D \ll C_{ox}$]

With traps at the interface

$$SS = 1 + \frac{C_D + C_{it}}{C_{ox}}$$



presence of interface traps increases the subthreshold swing

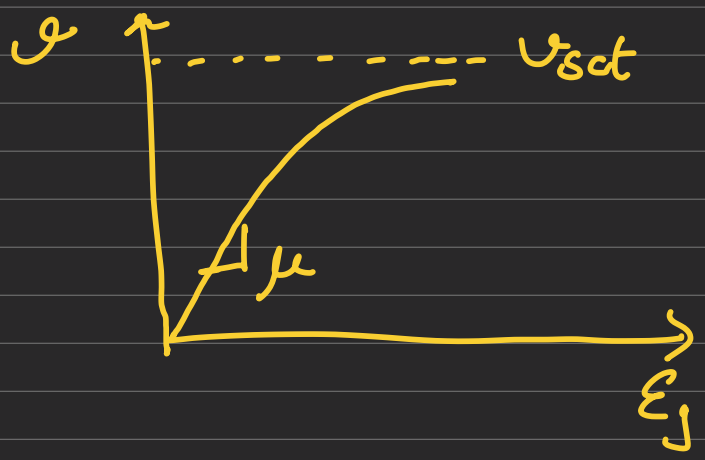
(Part of the channel charge is trapped in the interface traps)

— X — X —

In the earlier ON state analysis we had assumed constant mobility (effective mobility)

$$\mu = \frac{\int n(x)\,\mu(x)\,dx}{\int n(x)\,dx}$$

In practical devices there is degradation in the mobility due to multiple reasons. Two important ones are (1) Due to lateral electric field $\mathcal{E}_y$



$$\mu^{HF} = \frac{\mu^{LF}}{\left[1 + \left(\frac{\mathcal{E}_y}{\mathcal{E}_c^{\parallel}}\right)^{\alpha}\right]^{1/\alpha}}$$

(2) Normal electric field $\bar{\mathcal{E}}_x$

large $\bar{\mathcal{E}}_x$ pulls the carriers closer to the interface (oxide - semiconductor) which makes their movement along 'y' difficult

→ think in terms of Friction

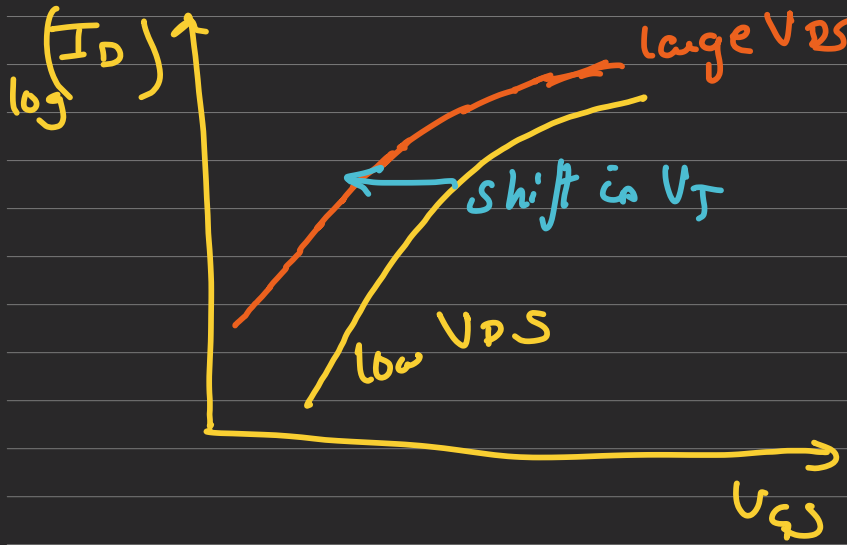
$$\mu^{N,HF} = \frac{\mu^{HF}}{\left(1 + \left(\frac{\mathcal{E}_x}{\mathcal{E}_c^{\perp}}\right)^{\beta}\right)^{1/\beta}}$$

$\mathcal{E}_c^{\parallel}$ & $\mathcal{E}_c^{\perp}$ are the critical electric fields along y & x respectively. These are treated as fitting parameters

Scaling of MOSFET channel length increases the second order effects (also called as short channel effects, SCE)

DRAIN bias also starts to effect the SWITCHING ON & OFF of the device in short channel devices

($L_C \sim W_{DEP,S} + W_{DEP,D}$)



To mitigate SCE, increase the gate coupling i.e. reduce t_{ox}, increase ε_{ox} (high-x gate oxide)

finally limited by the gate current

Ultimately increase the number of gates
- → Double gate
- → FinFET

Other historical efforts
- → use of III-V semiconductors
- → materials like Graphene / CNTs etc.

Another way to improve the gate control is to reduce the channel thickness i.e. going from bulk planar transistor to SOI to DG