EE1501 - Digital Systems Lab

Assignment - 3

Please submit a report which includes the code, its testbench, results, and your approach.

Q1) y = x0*h0 + x1*h1 + x2*h2 + x3*h3 + x4*h4 + x5*h5 + x6*h6 + x7*h7 + x8*h8 + x9*h9 (x0, h0… are all numbers, bit width of your choice)

Compute y assuming you have only 2 Multipliers and 1 Adder. Note that the above operation is a dot product.

Q2) Write Verilog code to divide any clock frequency by 3.