**Instructions:**

1. Use Cadence (with GPDK) or LT Spice + Electric software for the simulations.
2. Download the software from
https://www.staticfreesoft.com/productsFree.html

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1. Make schematic and layout of a static CMOS Inverter with proper DRC + LVS + Antenna Error clean. Run the RC extraction of the same and compare with schematic result. Find the maximum switching frequency for both cases.
2. Repeat Q1 for 3 input NAND and NOR gate with proper sizing.
3. Repeat Q1 and Q2 for a load capacitance of 1 pF.