.

EE1101: Circuits and Network Analysis

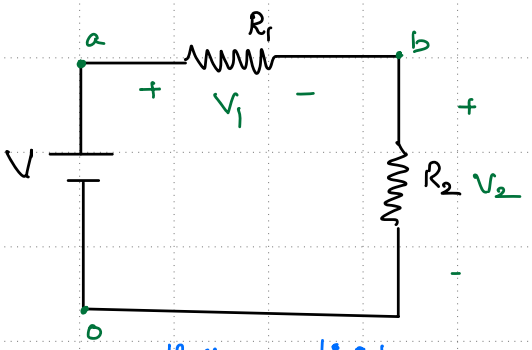
Lecture 05: DC Circuit Analysis

August 5, 2025

Topics :

1. Voltage and Current Divider Circuits
2. Port and its characteristics

Voltage and Current Divider Circuits



Voltage divider → what happens when $R_2 \to \infty$ (open circuit)

$$V_1 = \frac{R_1}{R_1+R_2} V.$$

and $$V_2 = \frac{R_2}{R_1+R_2} V.$$

$$\frac{V_1}{V_2} = \frac{R_1}{R_2}.$$

$I \to 0$

$V_1 \to 0$

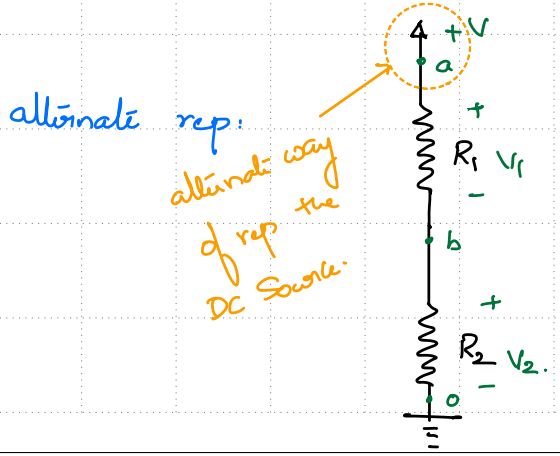
$V_2 \to V$

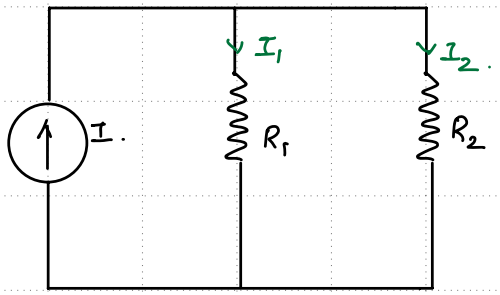
what happens if $R_2 \to 0$ (Short circuit)

$V_1 \to V$

$V_2 \to 0$

$I \to \frac{V}{R}$





Current divider

$$I_1 = \frac{R_2}{R_1+R_2} I \qquad I_2 = \frac{R_1}{R_1+R_2} I.$$

$$\frac{I_1}{I_2} = \frac{R_2}{R_1}$$

In a Current divider ckt

what happens if $R_2 \to 0$ (Short circuit)

$I_2 \to I$ and $I_1 \to 0$.

$V \to 0$.

what happens when $R_2 \to \infty$ (open circuit)

$I_1 \to I$, $I_2 \to 0$

$V \to IR_1$

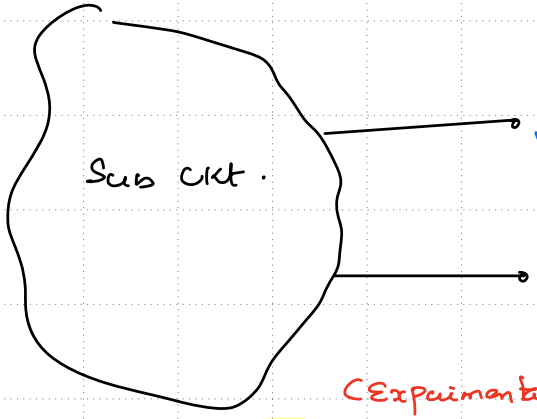
Port and its Characteristics (v-i characteristic)

→ Any pair of terminals in a n/w : rep (node 1 – node 2) or 1-1' or 2-2'

↓ one of these two scenarios

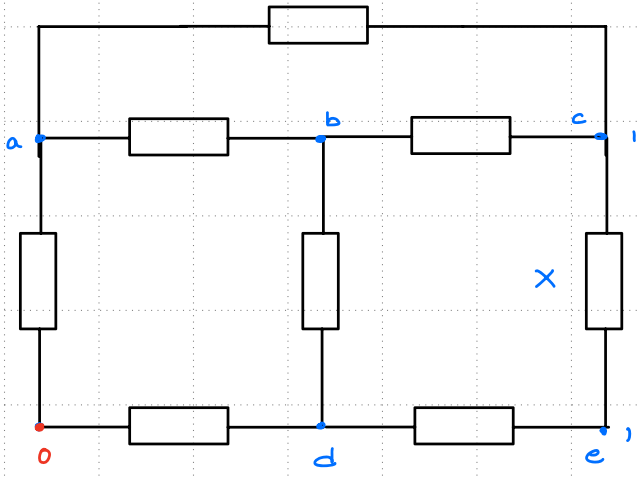
Aim: to derive its characteristics such that when you interface the port to an external n/w, one can easily study the behaviour of the sub ckt behind the port.

Scenario 1



(Experimental means when sub ckt is not known)

Scenario 2



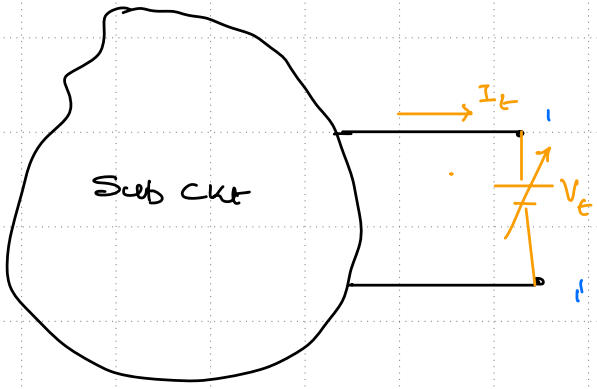
Port c-e.

goal:- to derive the v-i characteristic of a sub ckt (refer to as characteristic of a port)

if an elem is connected b/w the terminals of a port → remove it and consider the rest of the ckt as a sub ckt

claim:- using the v-i characteristic of a port and the " " of the elem connected across the port → one can find the operating point.

Port and its Characteristics (v-i characteristic)



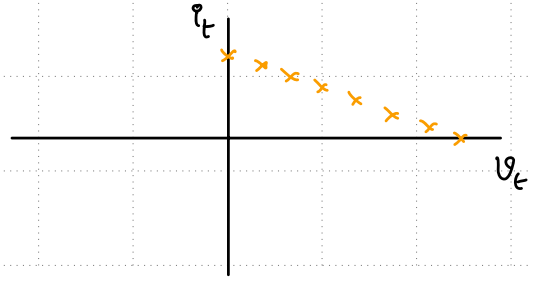
Scenario 1

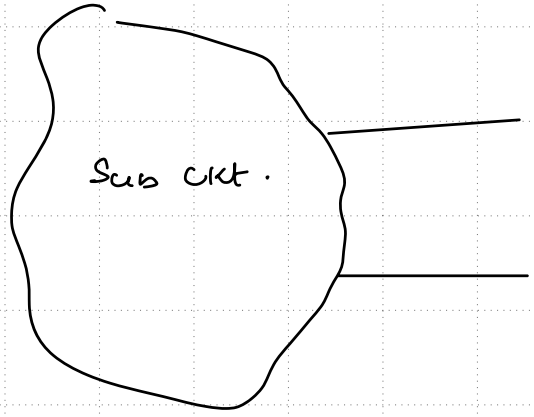
(when the components/ models of the sub circuit is not known)

⇓

Terminal characteristics of port can be obtained experimentally

For example, Connect a Variable Voltage Source and plot the (V_t, i_t) for various values of V_t





if the sub CKt is known

We use analysis techniques to Plot the terminal characteristic

for linear sub circuits

a) open circuit voltage (V_{oc})

b) short circuit current (I_{sc})

c) Equivalent Resistance (R_{eq})

↓

(i) Null the other sources in the CKt

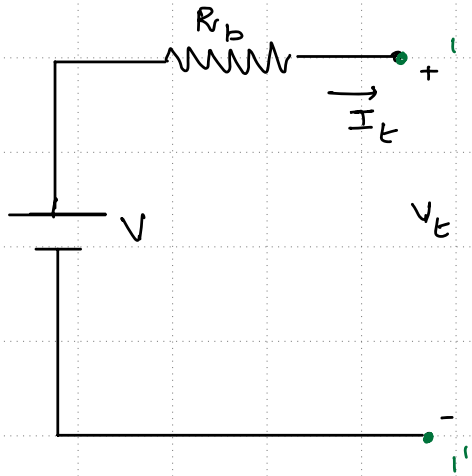
(ii) Connect a V/I Source at port

(iii) Measure I/V

(iv) $R_{eq} = V/I$.

can give the v-i characteristic of a port.

Example 01 - Terminal characteristics of a practical voltage source



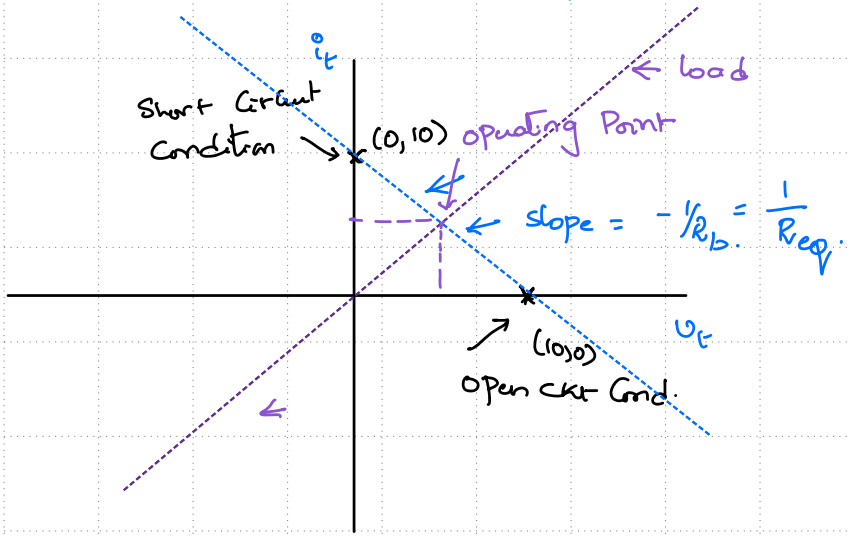
Open ckt voltage : $V_t = V$ and $I_t = 0$

Short ckt Current : $I_t = V/R_b$ and $V_t = 0$

Eq. resistance — Short the V source, open the I Source } Nulling the other Sources.

$$R_{eq} = \frac{V_t}{I_t} = -R_b.$$

(↑ bec of sign convention.)



Example: $V = 10V$ $R_b = 1\Omega$. line through (0, 10) and (10, 0)

when we connect a load of 1Ω (R_l). $V_t = 5\Omega$.

Example 02

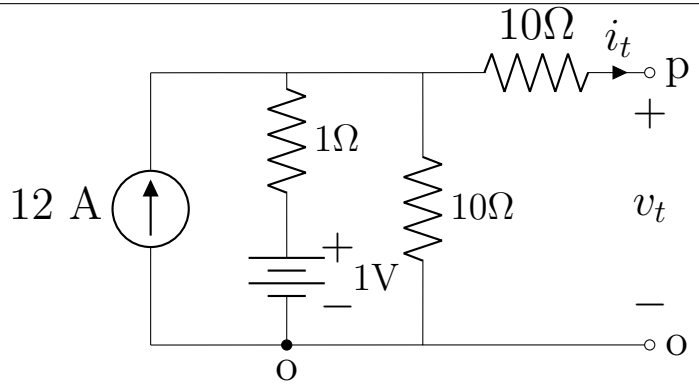


Fig. 1: Circuit for Example 02

Open ckt voltage : $130/11$ V.

SC Current : $13/12$ A

Eq. Resistance : $120/11$ Ω.