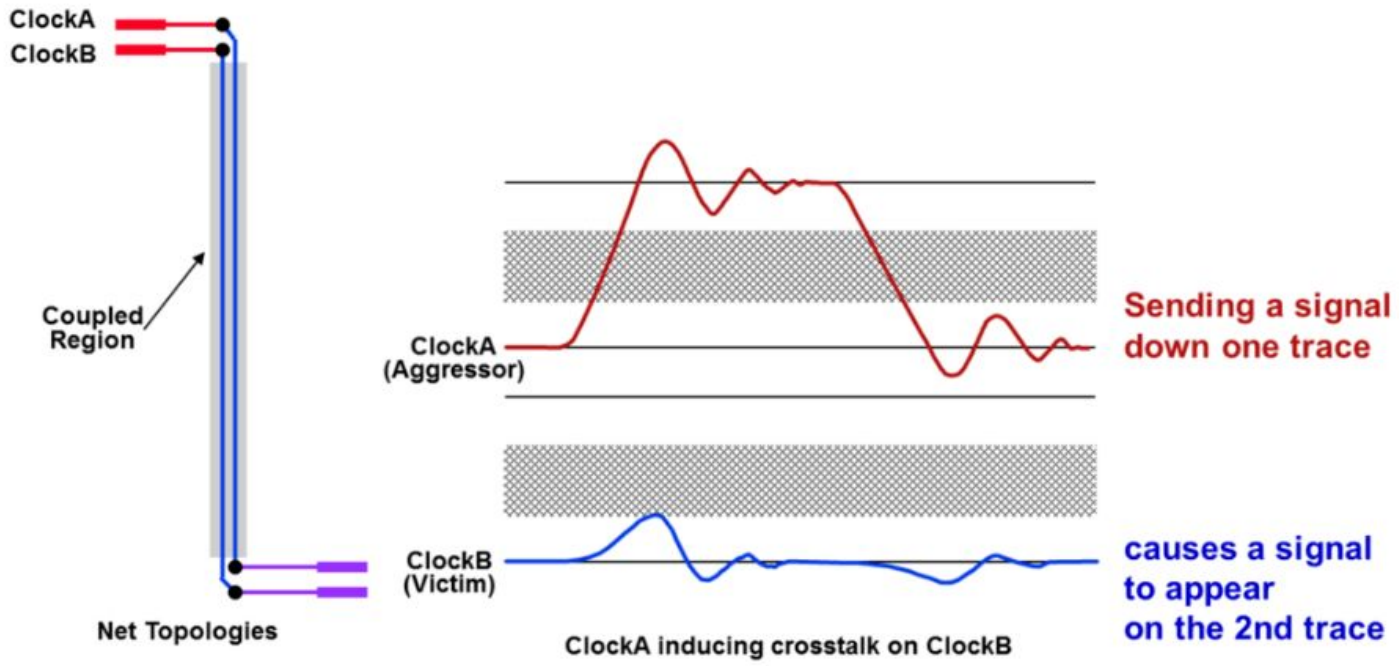

ClockA
ClockB
Coupled
Region
Net Topologies
ClockA
(Aggressor)
ClockB
(Victim)
Sending a signal
down one trace
causes a signal
to appear
on the 2nd trace
ClockA inducing crosstalk on ClockB

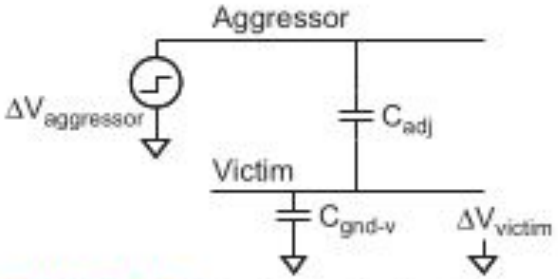


FIGURE 6.17 Coupling to floating victim

$$\Delta V_{\text{victim}} = \frac{C_{\text{adj}}}{C_{\text{gnd}-v} + C_{\text{adj}}} \Delta V_{\text{aggressor}}$$

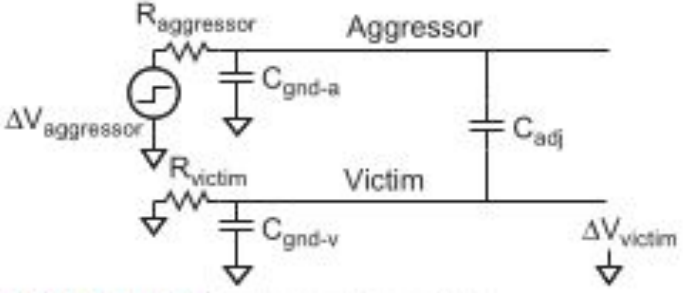


FIGURE 6.18 Coupling to driven victim

$$\Delta V_{\text{victim}} = \frac{C_{\text{adj}}}{C_{\text{gnd}-v} + C_{\text{adj}}} \frac{1}{1+k} \Delta V_{\text{aggressor}}$$

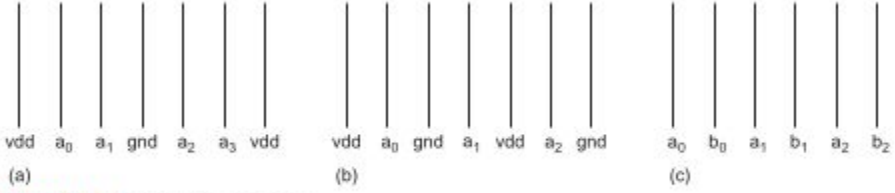
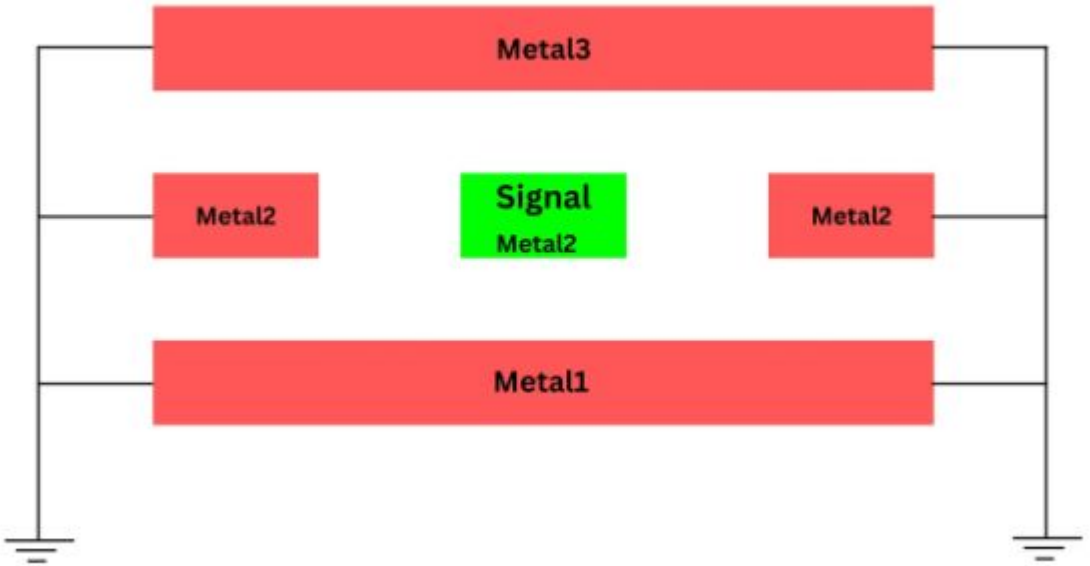


FIGURE 6.28 Wire shielding topologies



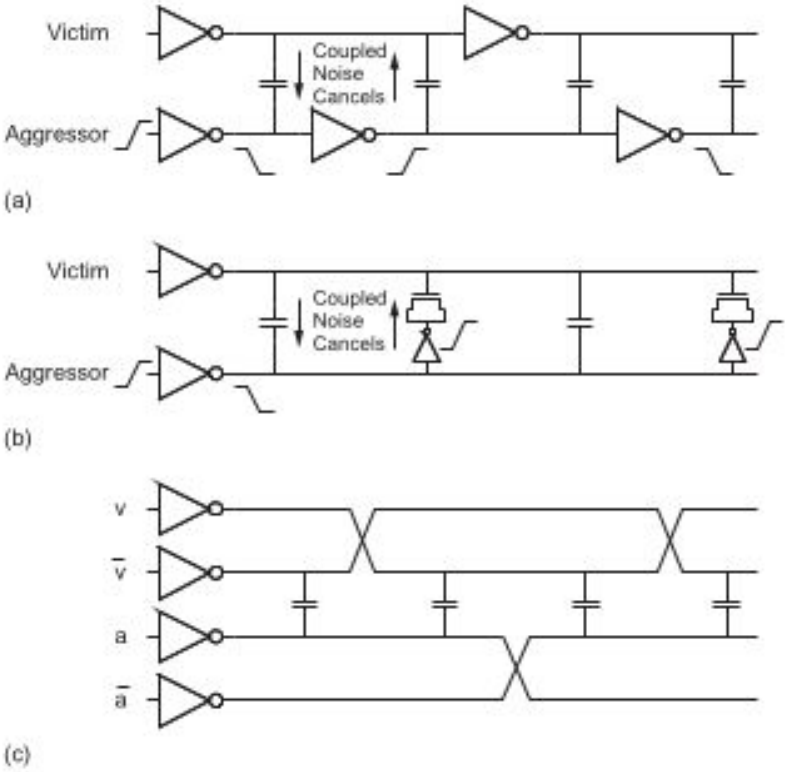
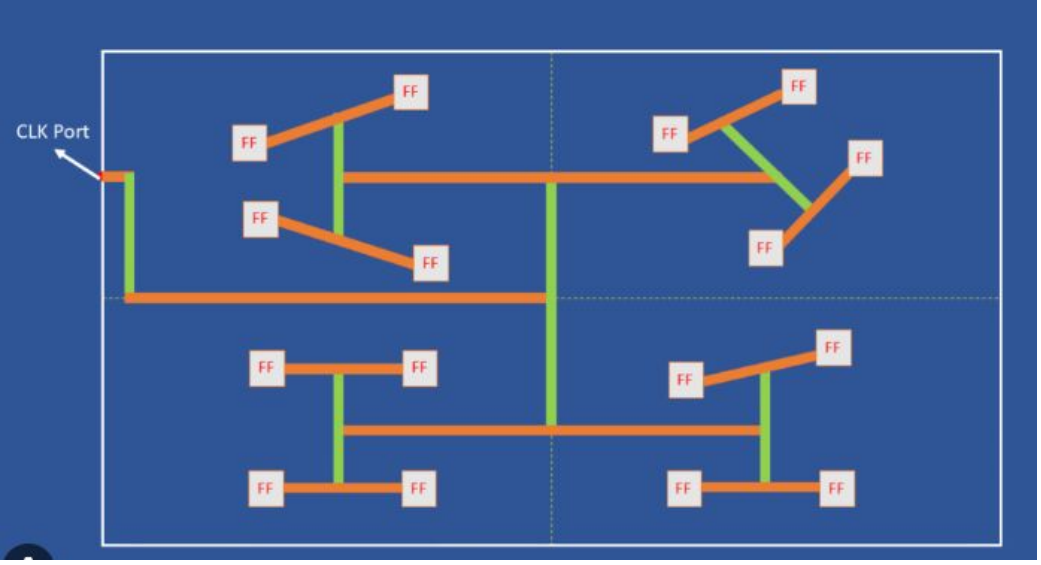
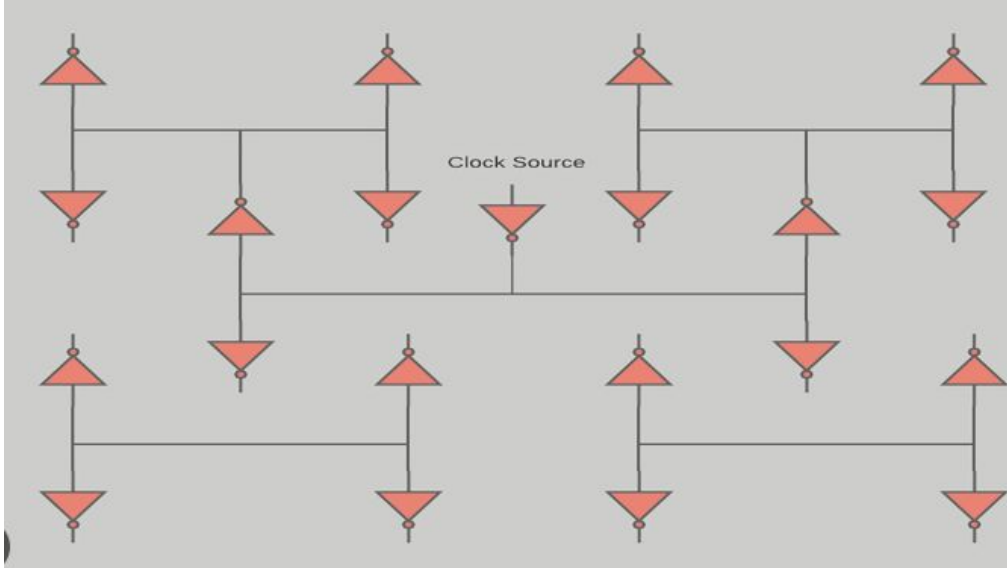
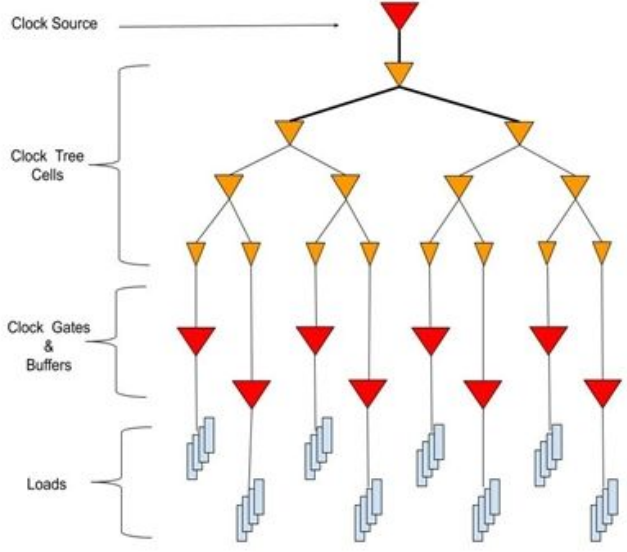
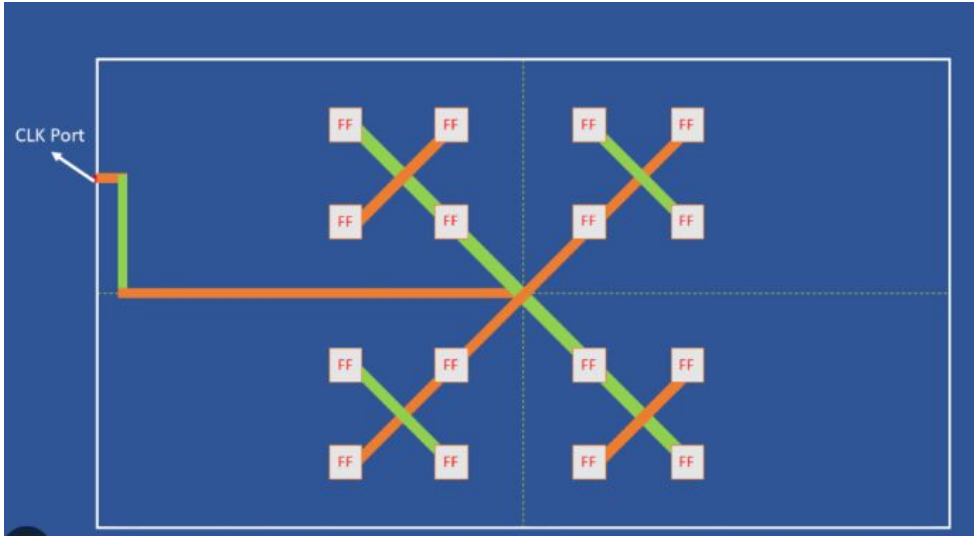


FIGURE 6.29 Crosstalk control schemes


CLK Port
FF


Clock Source


Clock Source
Clock Tree Cells
Clock Gates & Buffers
Loads


CLK Port
FF

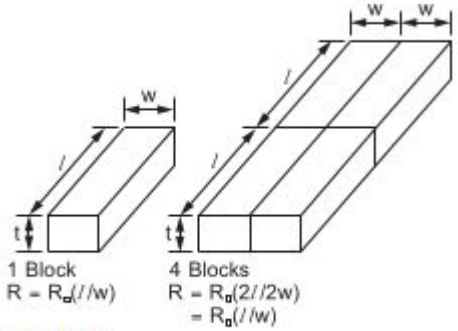


FIGURE 6.6
Two conductors with equal resistance

TABLE 6.2 Bulk resistivity of pure metals at 22 °C

Metal	Resistivity ($\mu\Omega \cdot$ cm)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Molybdenum (Mo)	5.3
Titanium (Ti)	43.0

Compute the sheet resistance of a 0.22 μm thick Cu wire in a 65 nm process. Find the total resistance if the wire is 0.125 μm wide and 1 mm long. Ignore the barrier layer and dishing.

SOLUTION: The sheet resistance is

$$R_{\square} = \frac{2.2 \times 10^{-8}\ \Omega \cdot \text{m}}{0.22 \times 10^{-6}\ \text{m}} = 0.10\ \Omega/\square \tag{6.4}$$

The total resistance is

$$R = (0.10\ \Omega/\square)\frac{1000\ \mu\text{m}}{0.125\ \mu\text{m}} = 800\ \Omega \tag{6.5}$$

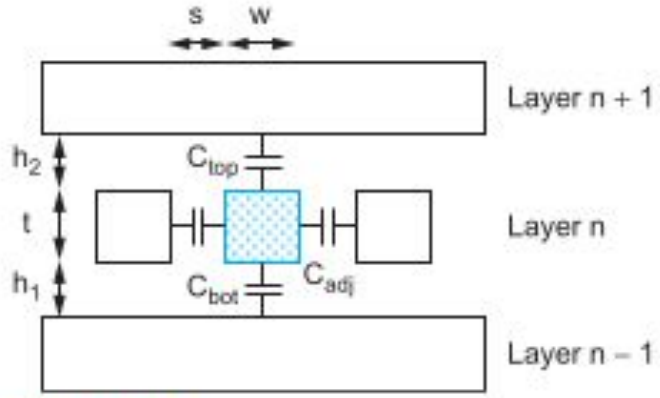


FIGURE 6.11 Multilayer capacitance model

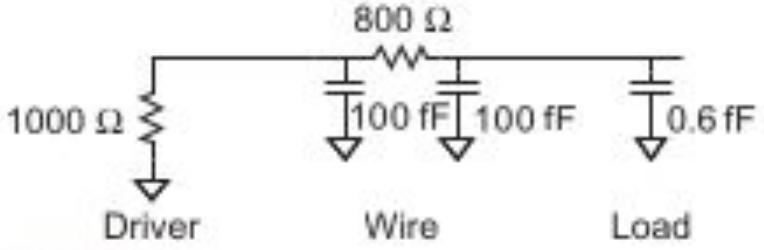


FIGURE 6.14 Equivalent circuit for example

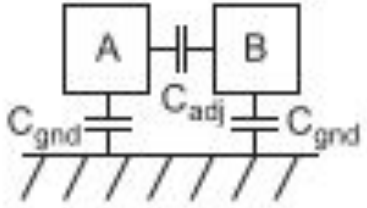


FIGURE 6.16 Capacitances to adjacent neighbor and to ground

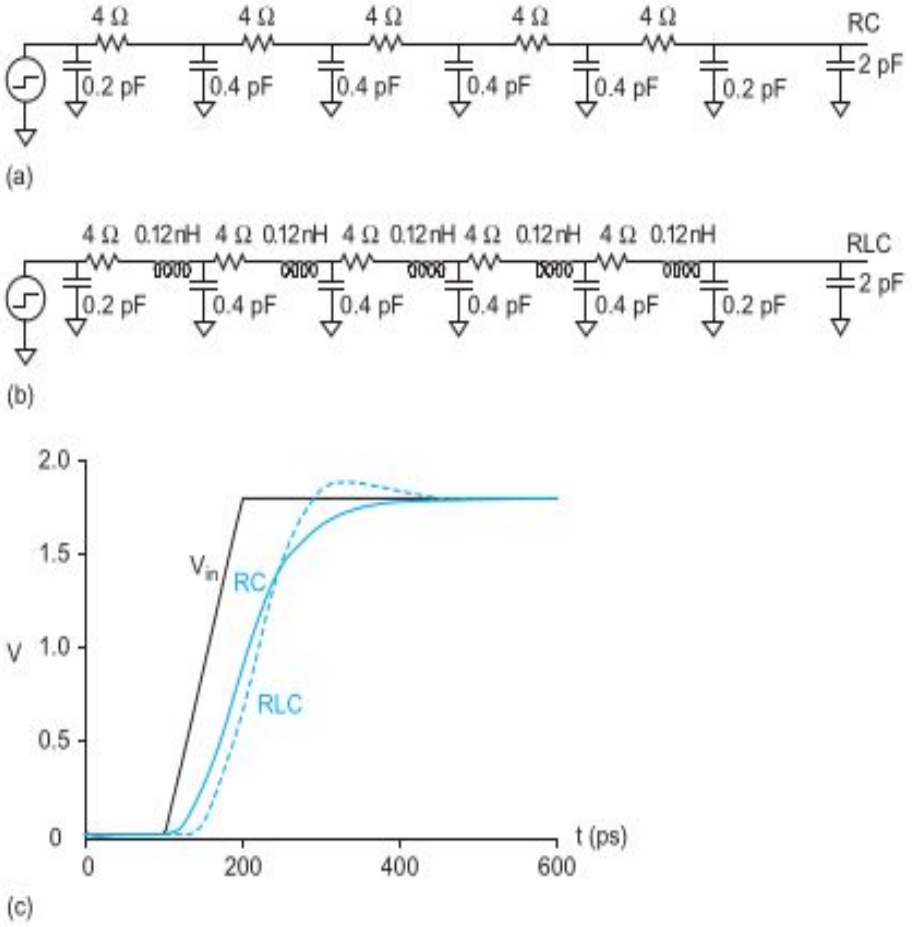


FIGURE 6.21 Wide clock line modeled with and without inductance

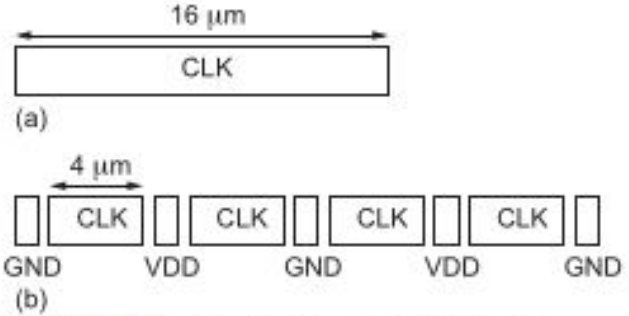


FIGURE 6.22 Wide clock line interdigitated with power and ground lines to reduce inductance

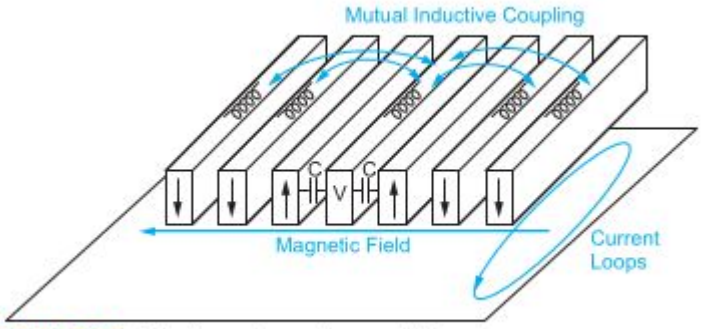


FIGURE 6.23 Inductive and capacitive crosstalk in a bus

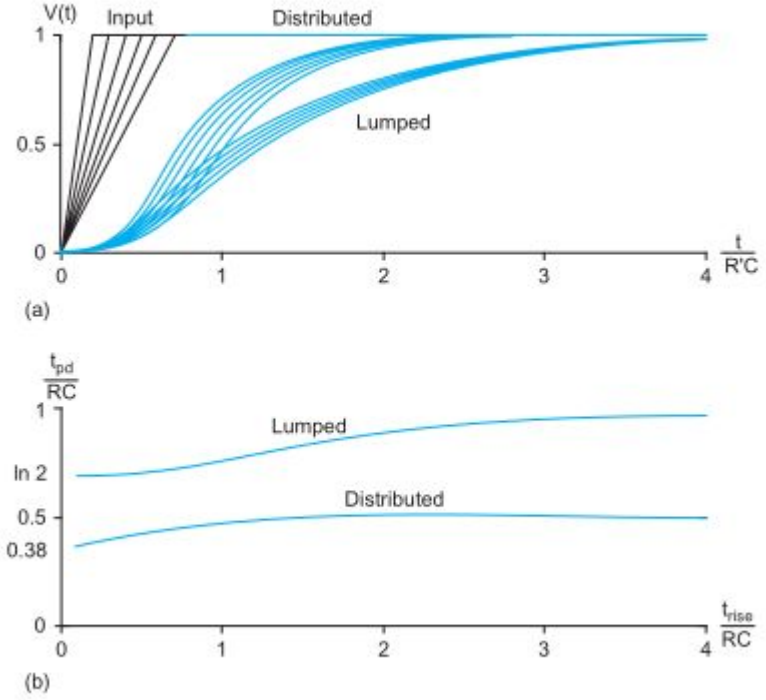


FIGURE 6.25 Effect of rise time on lumped and distributed RC circuit delays

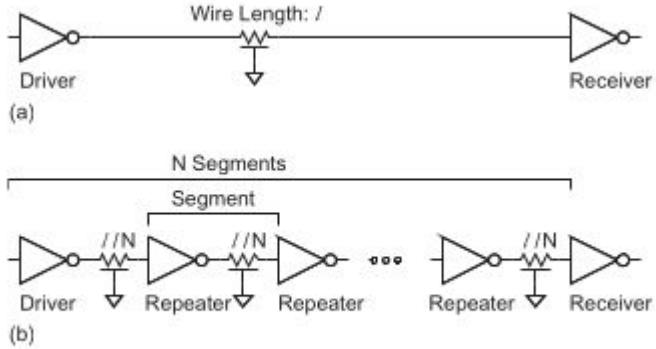


FIGURE 6.26 Wire with and without repeaters

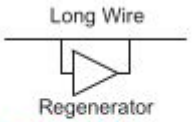


FIGURE 6.31
Regenerator

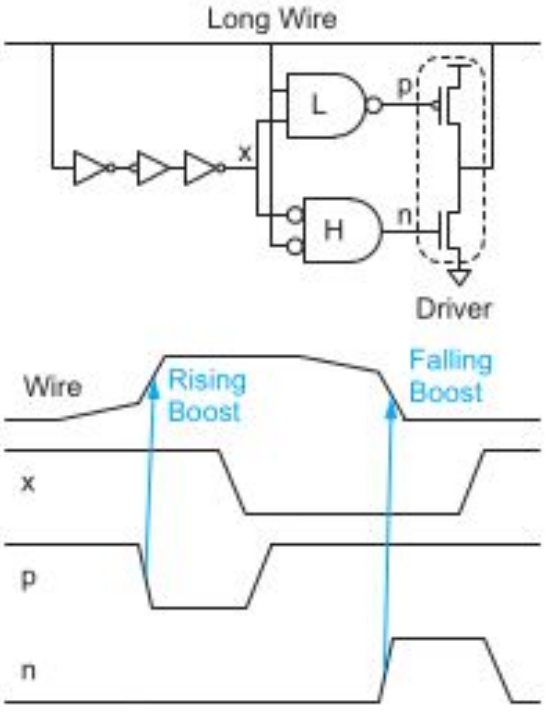
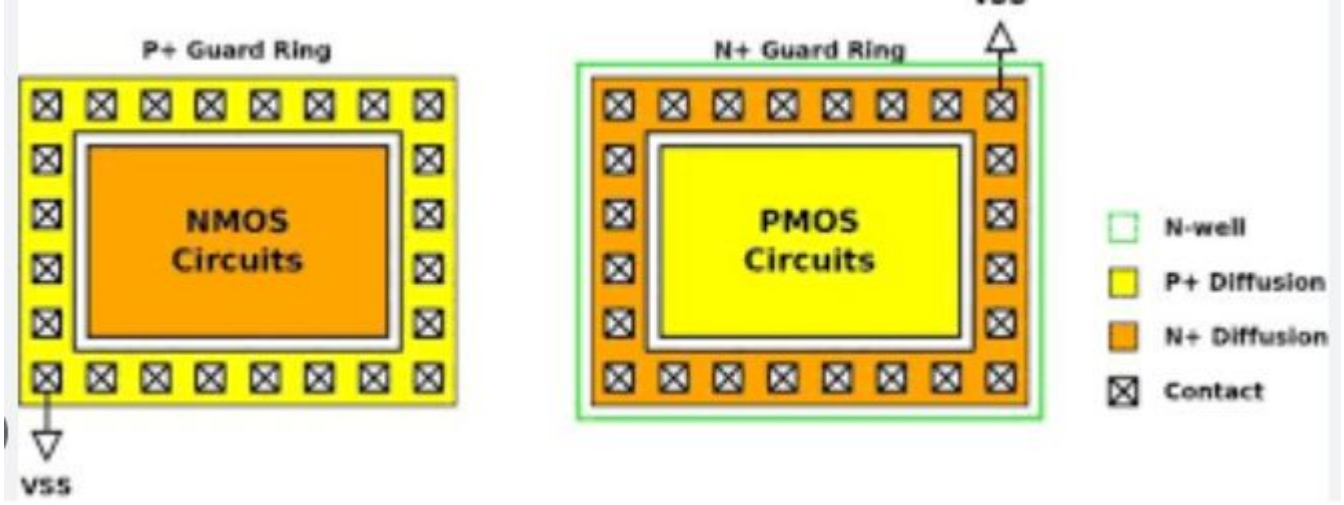
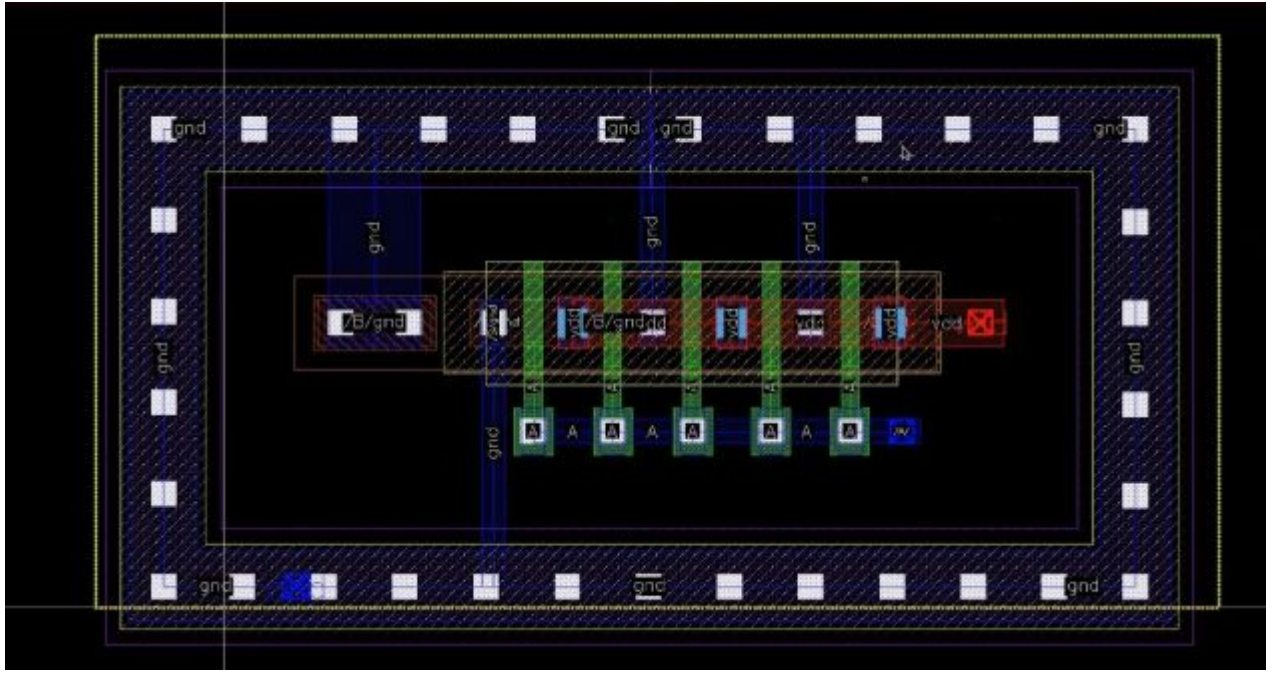
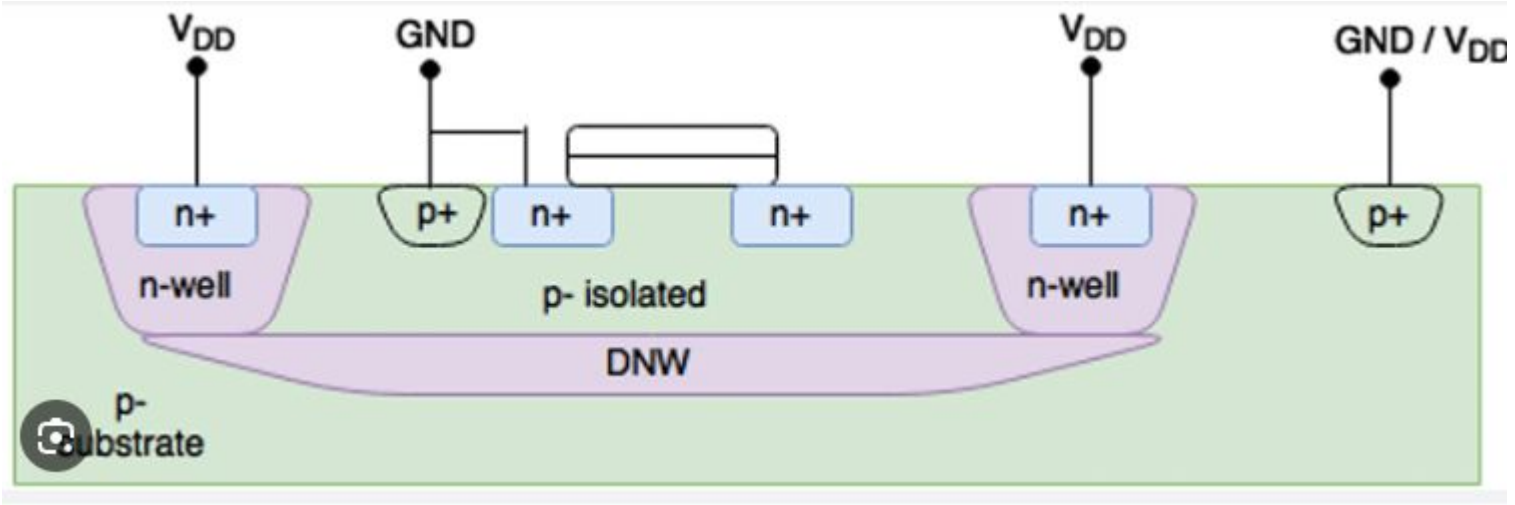
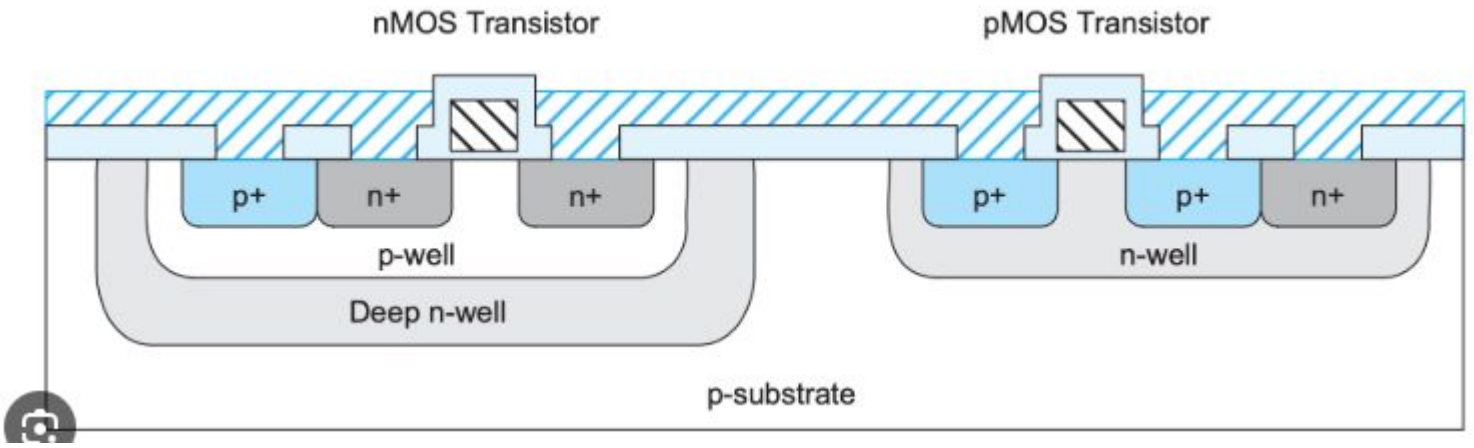


FIGURE 6.32 Regenerator


P+ Guard Ring
N+ Guard Ring
NMOS
Circuits
PMOS
Circuits
N-well
P+ Diffusion
N+ Diffusion
Contact
VSS


gnd
vdd
A


V_{DD}
GND
V_{DD}
GND / V_{DD}
n+
p+
n+
n+
n+
p+
n-well
p- isolated
n-well
DNW
p-
substrate


nMOS Transistor
pMOS Transistor
p+
n+
n+
p+
p+
n+
p-well
n-well
Deep n-well
p-substrate

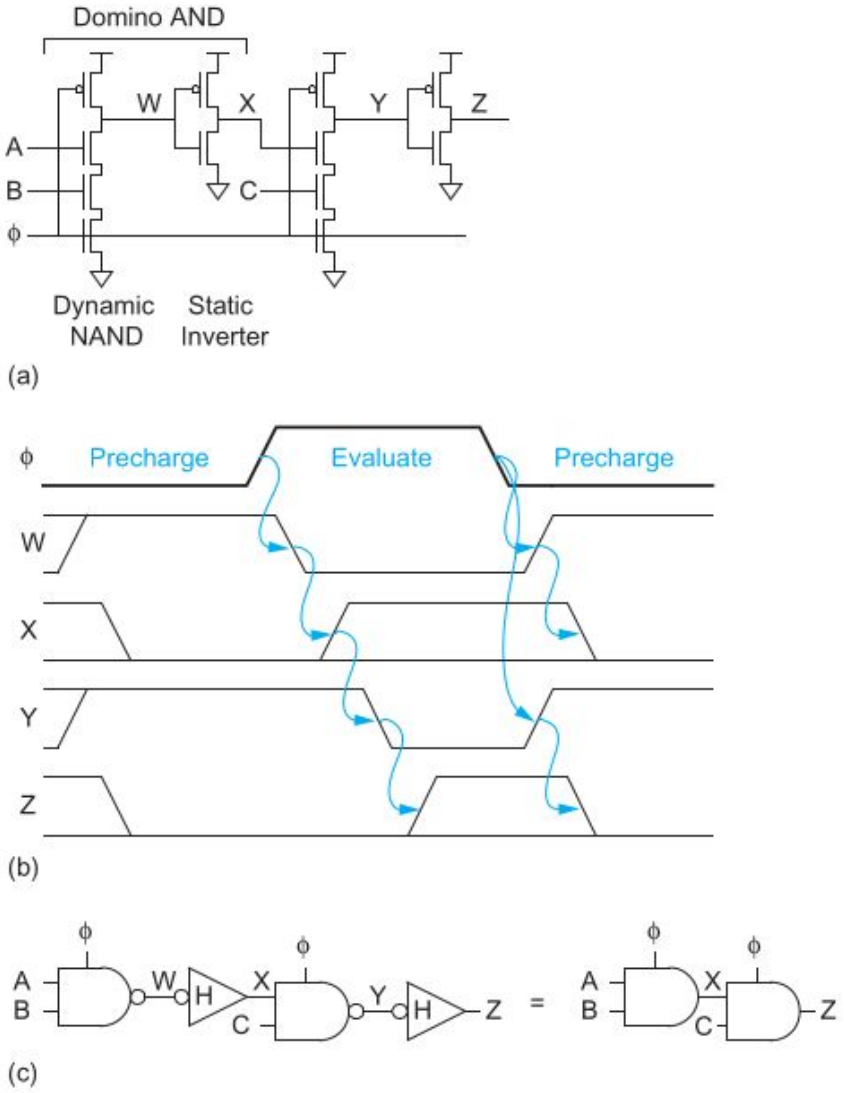
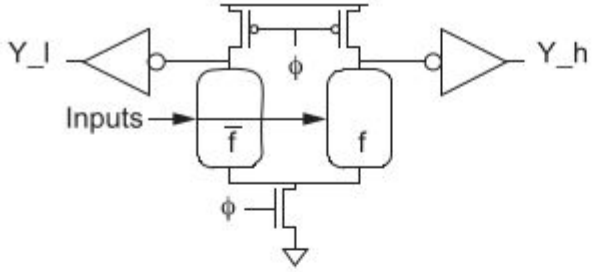
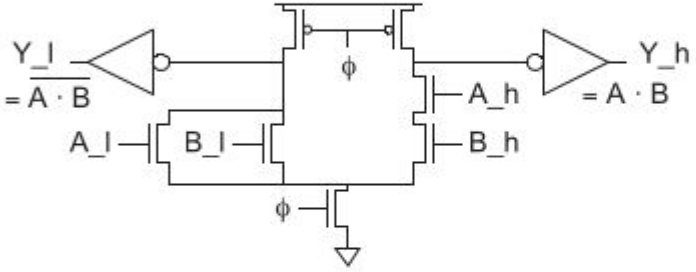


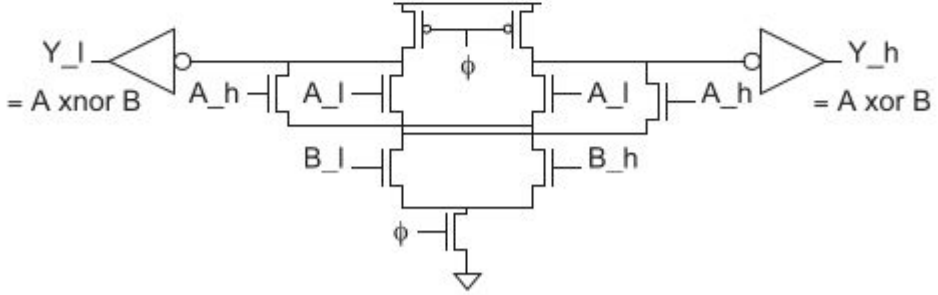
FIGURE 9.28 Domino gates



(a)



(b)



(c)

FIGURE 9.30 Dual-rail domino gates

TABLE 9.2 Dual-rail domino signal encoding

sig_h	*sig_l*	Meaning
0	0	Precharged
0	1	'0'
1	0	'1'
1	1	Invalid

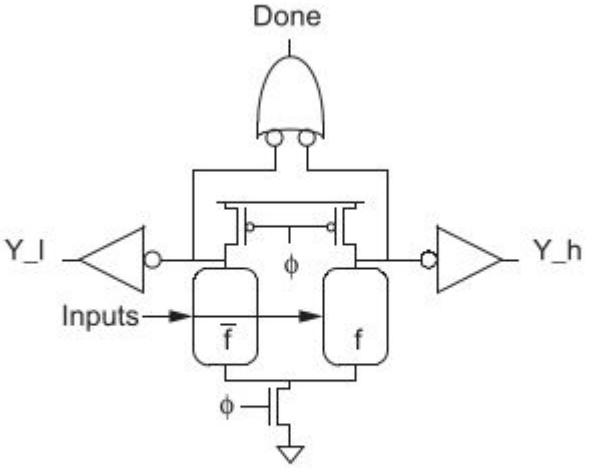


FIGURE 9.31 Dual-rail domino gate with completion detection

Multiple-Output Domino Logic (MODL)

$$c_1 = g_1 + p_1 c_0$$
$$c_2 = g_2 + p_2\left(g_1 + p_1 c_0\right)$$
$$c_3 = g_3 + p_3\left(g_2 + p_2\left(g_1 + p_1 c_0\right)\right)$$
$$c_4 = g_4 + p_4\left(g_3 + p_3\left(g_2 + p_2\left(g_1 + p_1 c_0\right)\right)\right)$$

$$g_i = a_i b_i$$
$$p_i = a_i \oplus b_i$$

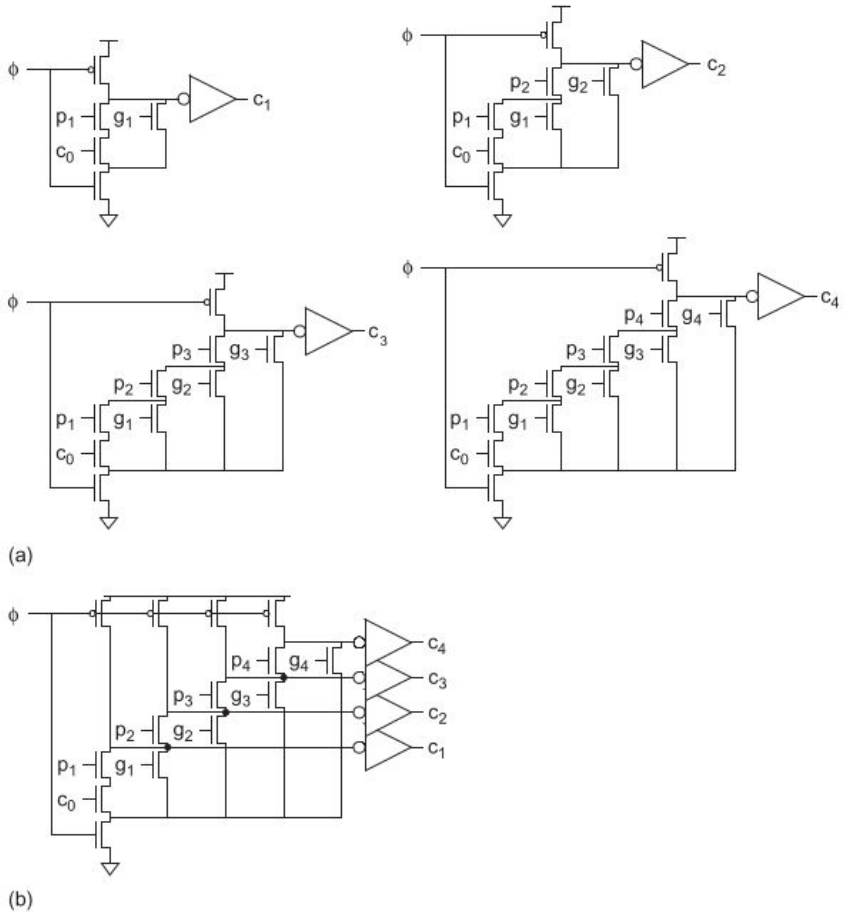


FIGURE 9.44 Conventional and MODL carry chains

Circuit Pitfalls

- Threshold drops
- Ratio failures
- Leakage
- Charge sharing
- Power supply noise
- Coupling
- Minority carrier injection
- Back-gate coupling
- Diffusion input noise sensitivity
- Race conditions
- Delay matching
- Metastability
- Hot spots
- Soft errors
- Process sensitivity

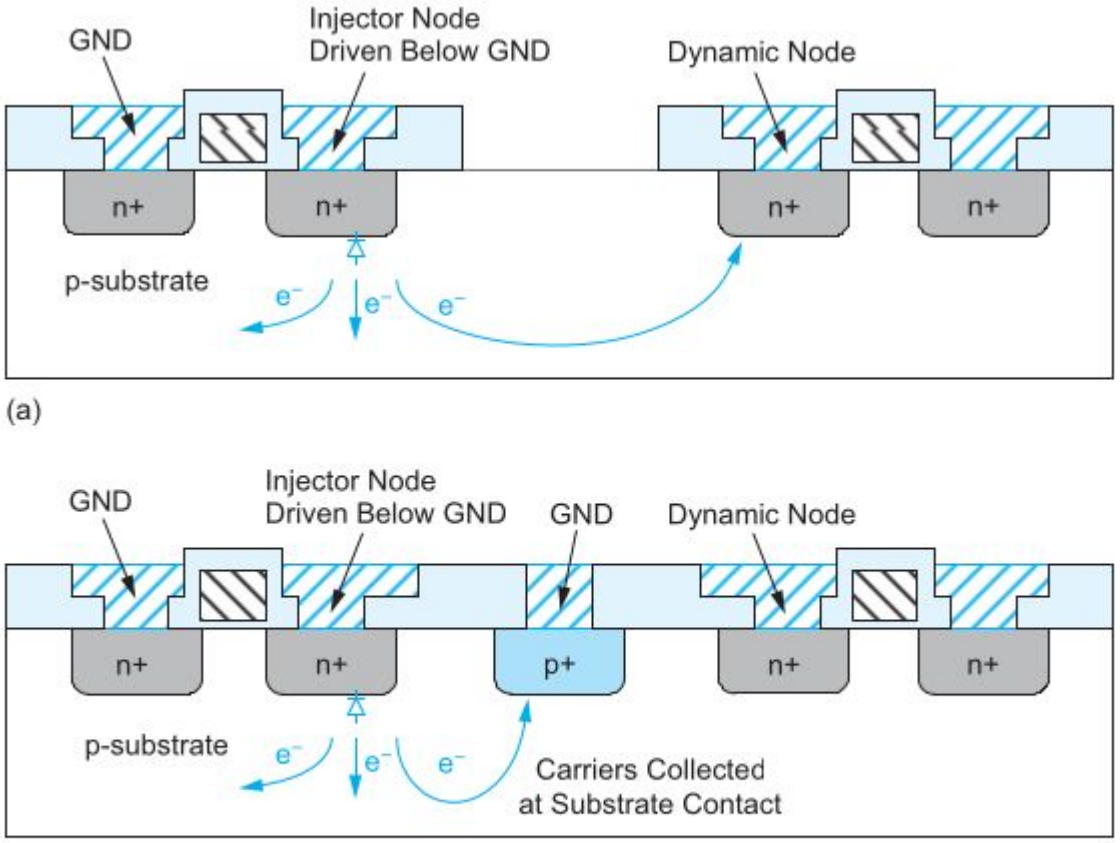


FIGURE 9.58 Minority carrier injection and collection

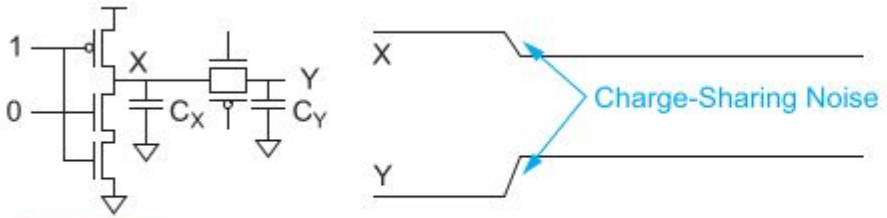


FIGURE 9.56 Charge sharing on dynamic gate driving pass transistor

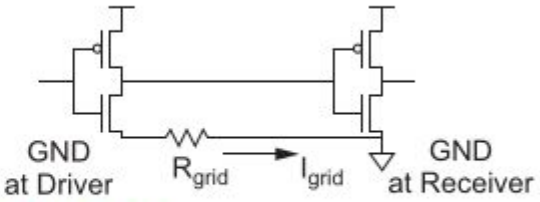


FIGURE 9.57 Power supply IR drops

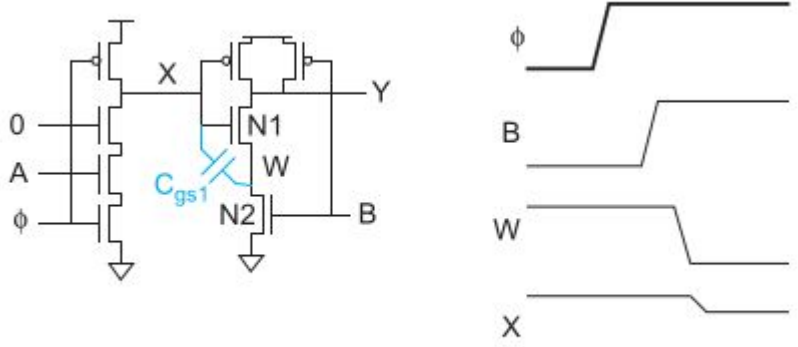


FIGURE 9.59 Back-gate coupling

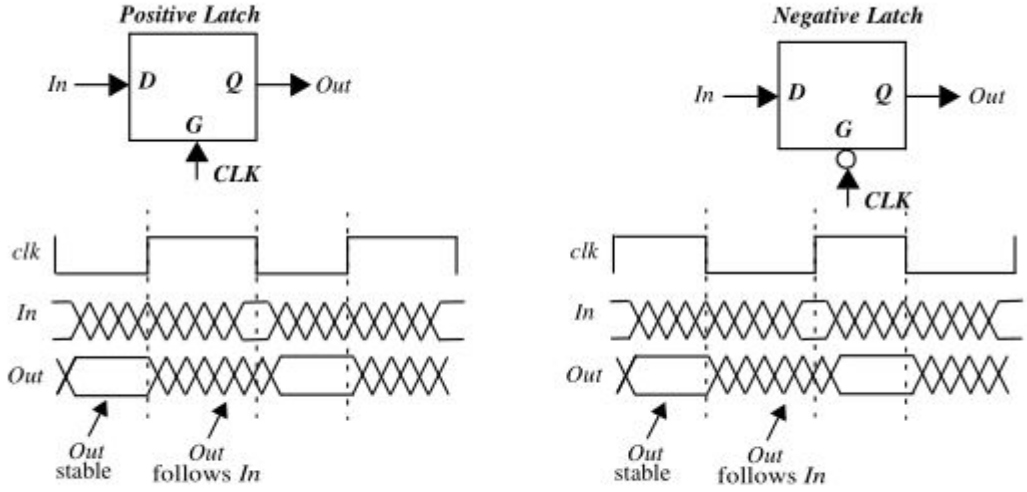


Figure 7.3 Timing of positive and negative latches.

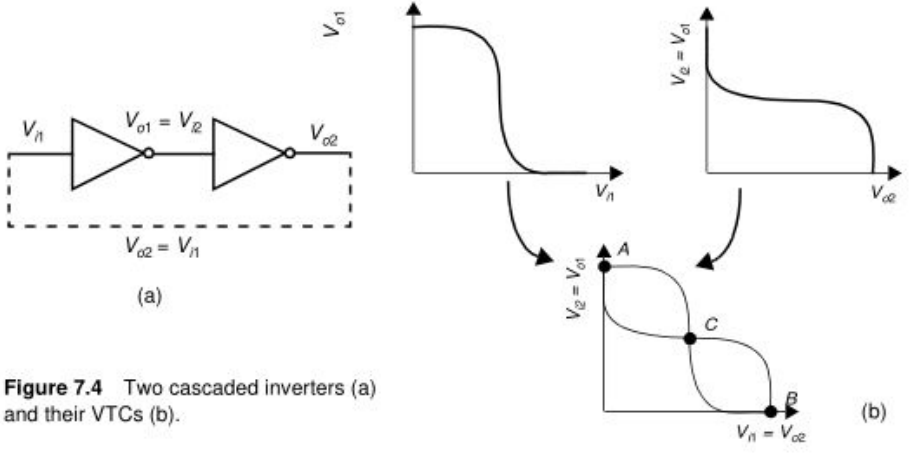
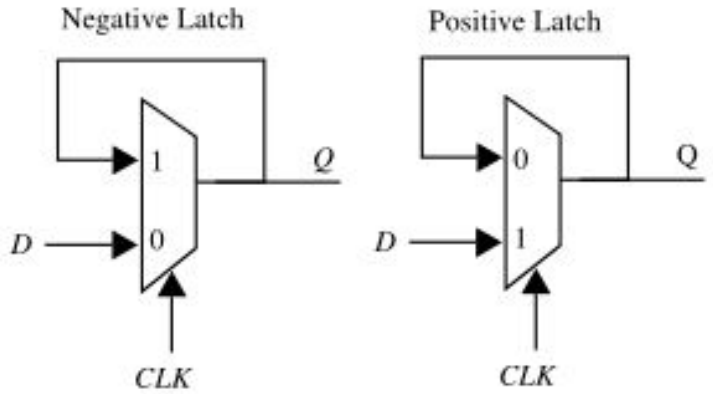


Figure 7.4 Two cascaded inverters (a) and their VTCs (b).



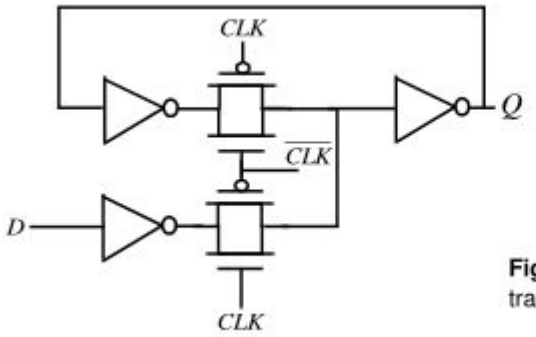
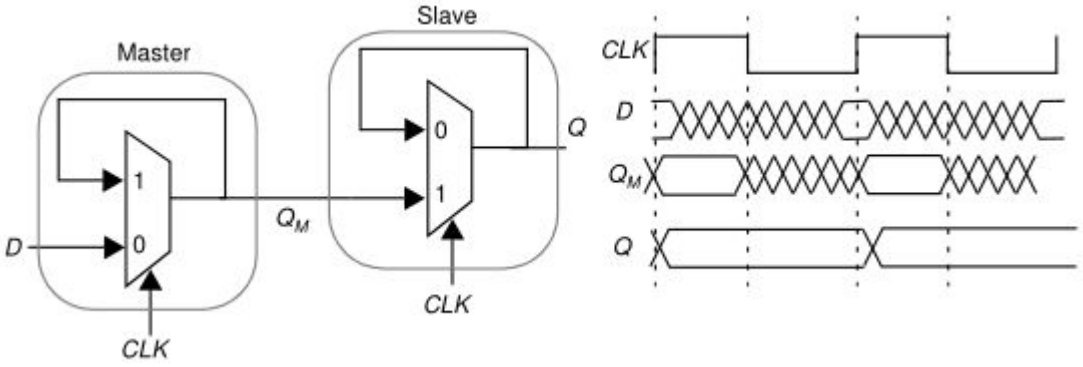


Figure 7.12 Positive latch built using transmission gates.



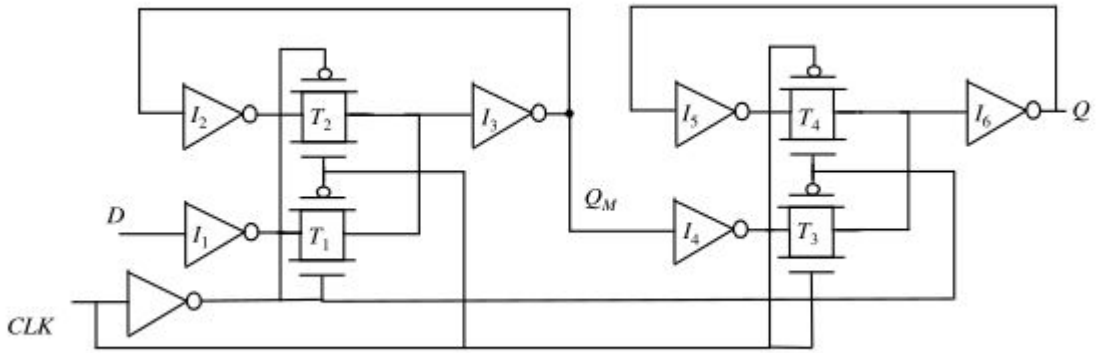


Figure 7.15 Master-slave positive edge-triggered register using multiplexers.

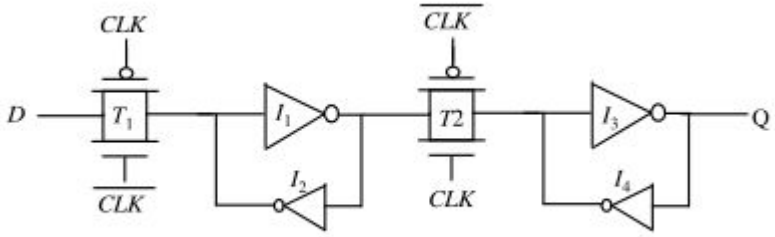


Figure 7.18 Reduced load clock load static *master-slave* register.

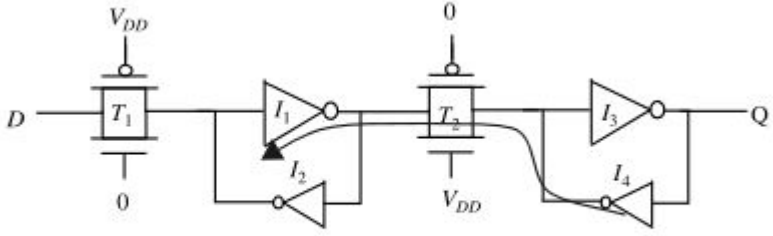
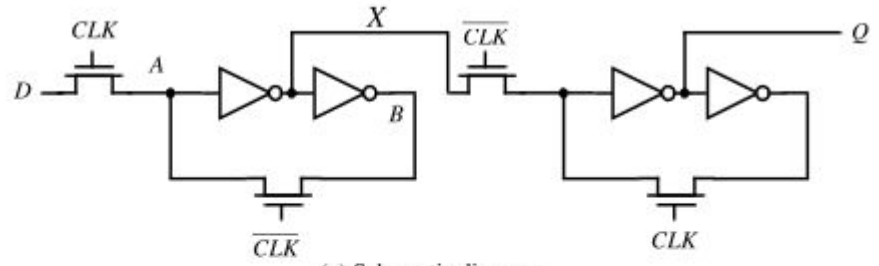
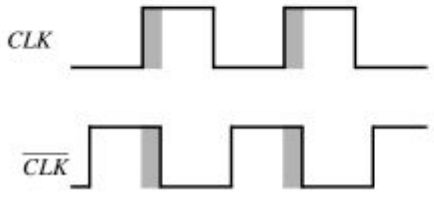


Figure 7.19 Reverse conduction possible in the transmission gate.



(a) Schematic diagram



(b) Overlapping clock pairs

Figure 7.20 *Master-slave* register based on NMOS-only pass transistors.

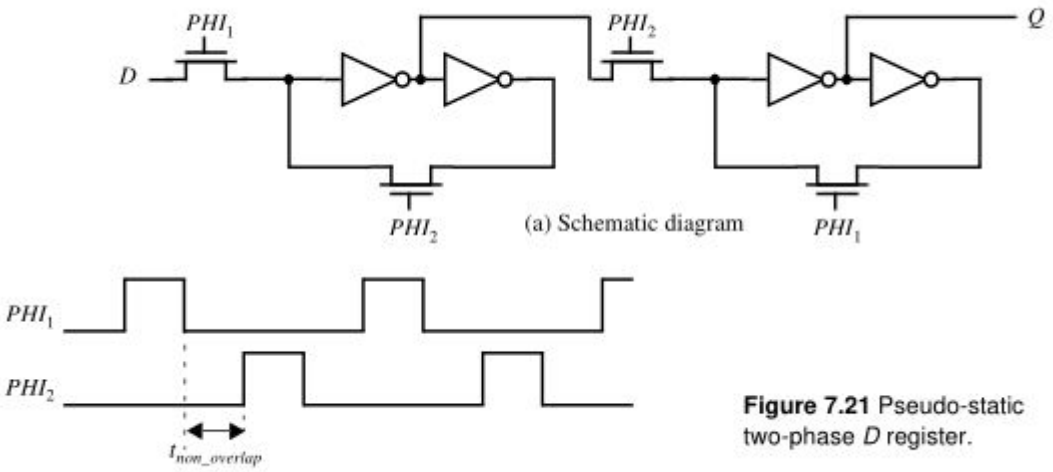


Figure 7.21 Pseudo-static two-phase *D* register.

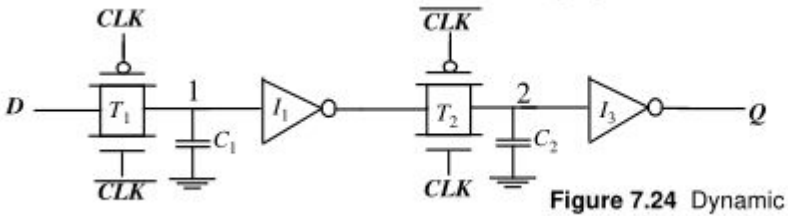


Figure 7.24 Dynamic *edge-triggered* register.

$$t_{overlap0-0} < t_{T1} + t_{I1} + t_{T2}$$

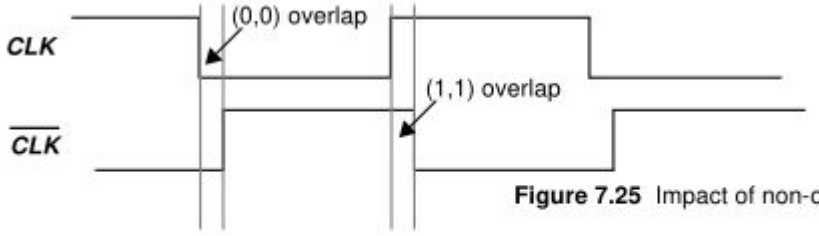
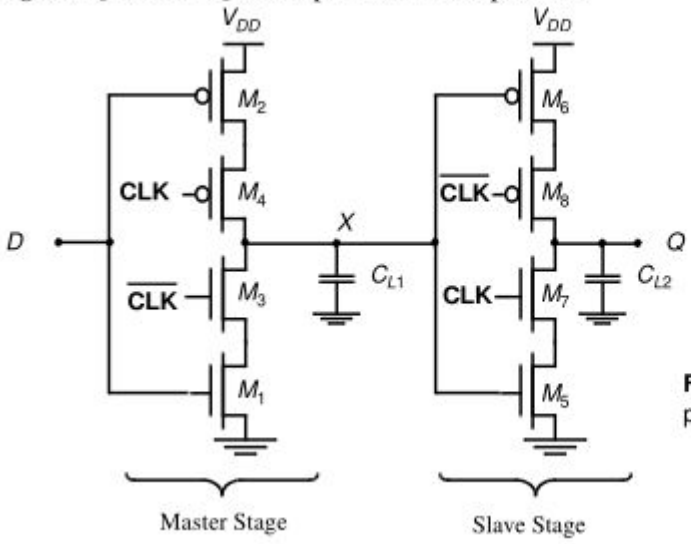
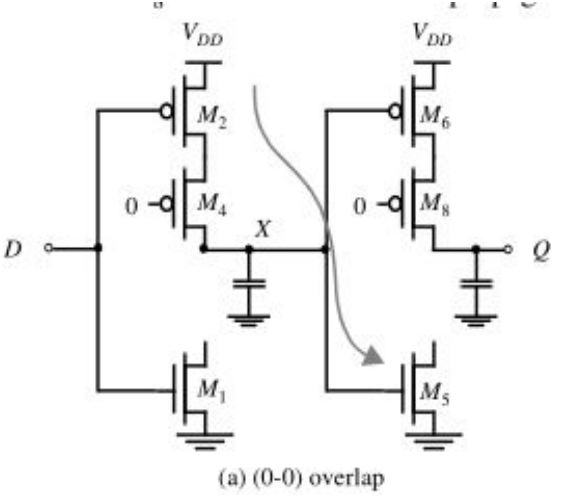


Figure 7.25 Impact of non-overlapping clocks.

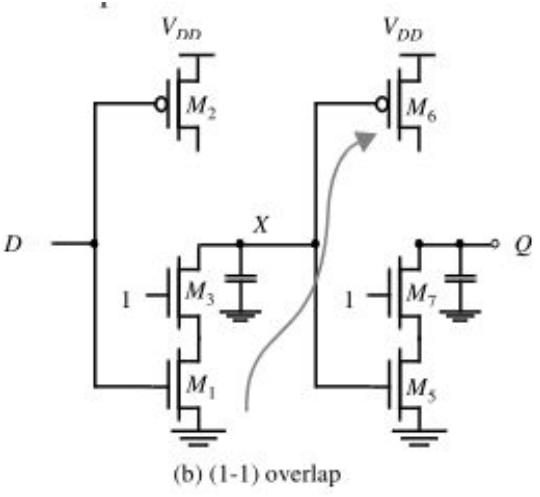
Similarly, the constraint for the 1-1 overlap is given as:

$$t_{hold} > t_{overlap1-1}$$





(a) (0-0) overlap



(b) (1-1) overlap

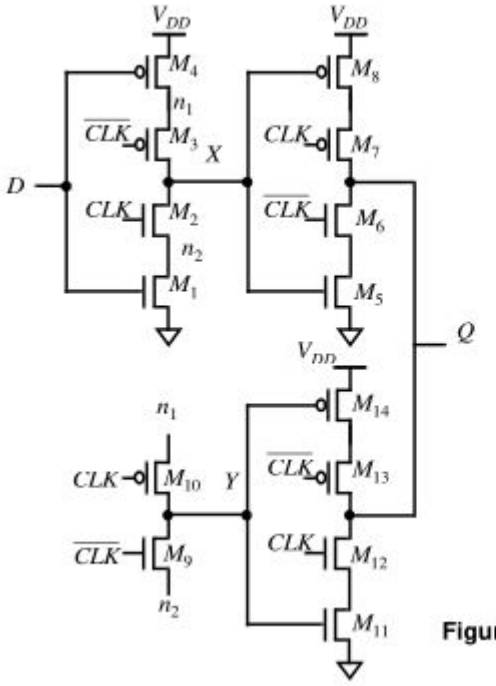


Figure 7.29 C^2MOS based dual-edge triggered register.

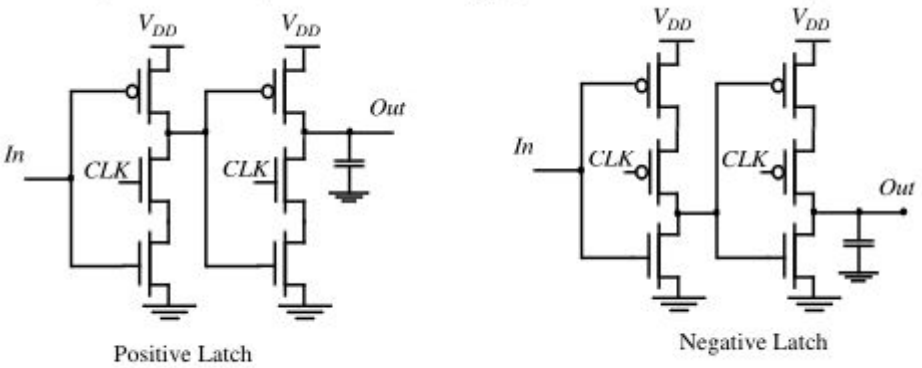


Figure 7.30 True Single Phase Latches.

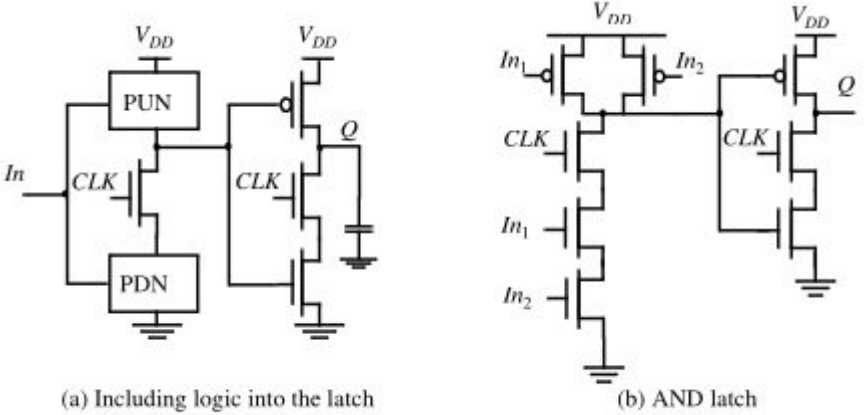


Figure 7.31 Adding logic to the TSPC approach.

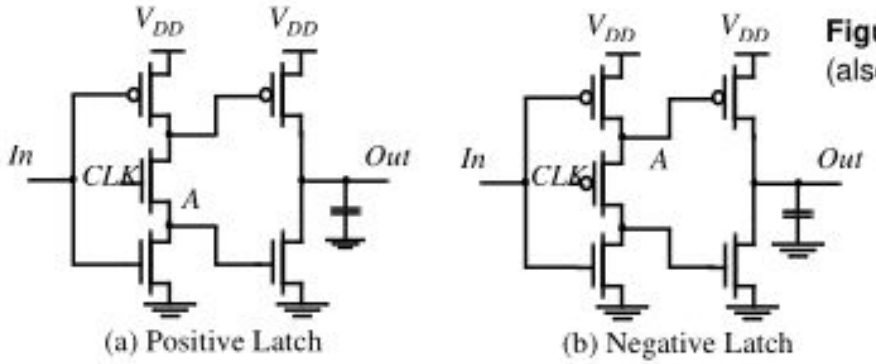


Figure 7.32 Simplified TSPC latch (also called split-output).

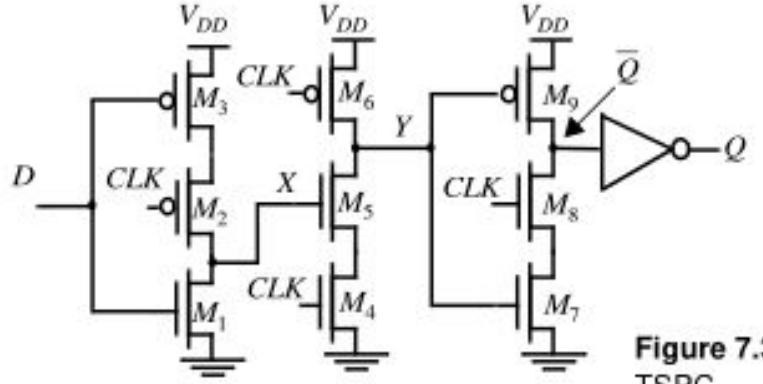


Figure 7.33 *Positive edge-triggered* register TSPC.

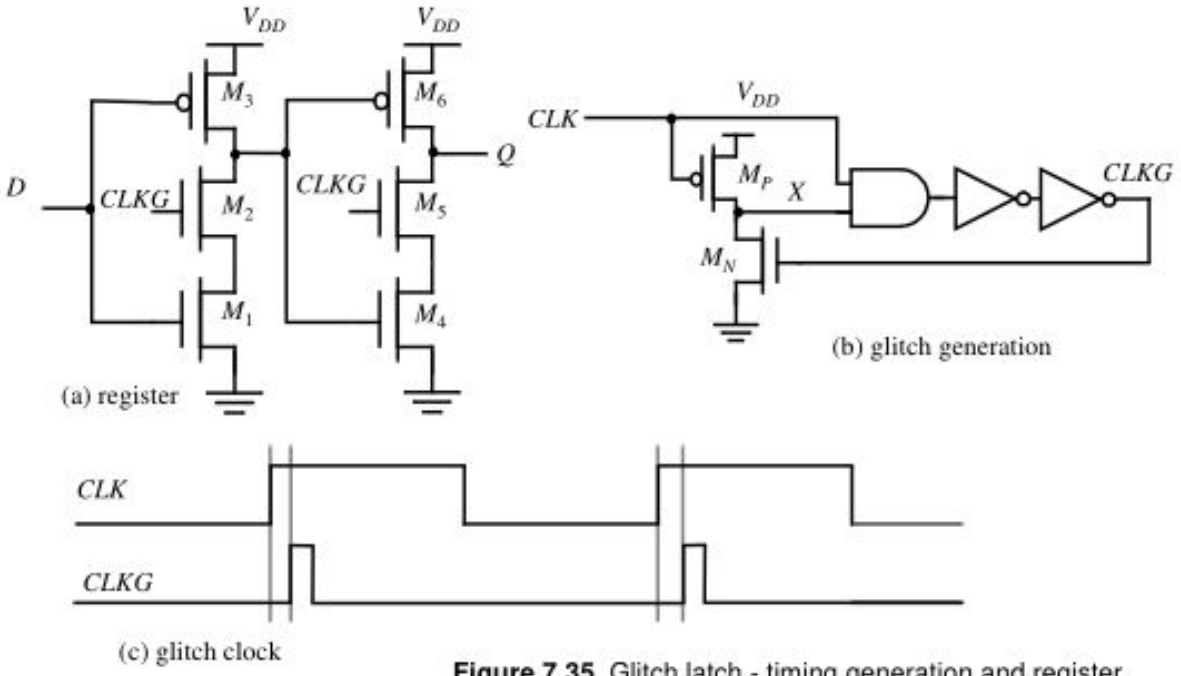


Figure 7.35 Glitch latch - timing generation and register.