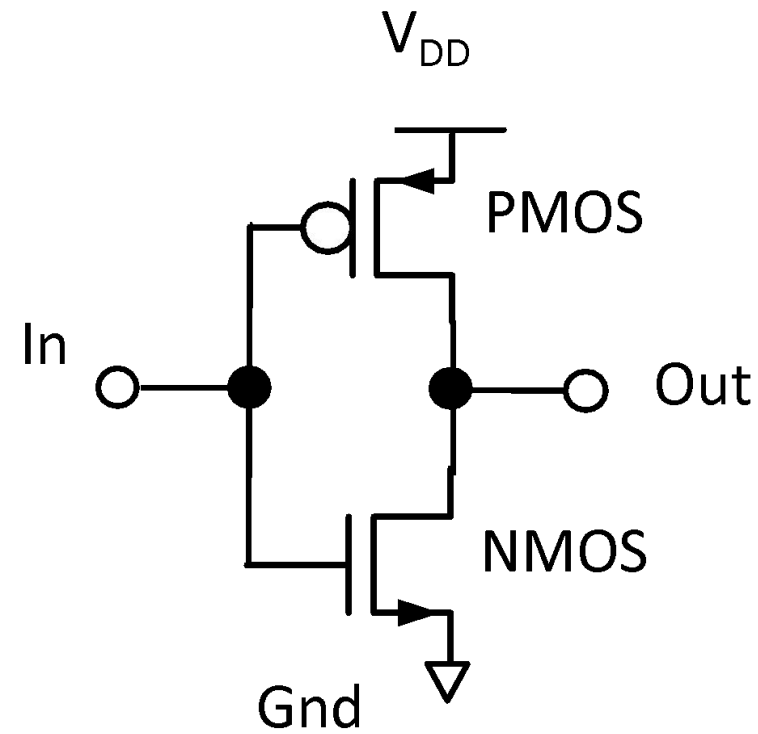


# Modern CMOS Processing

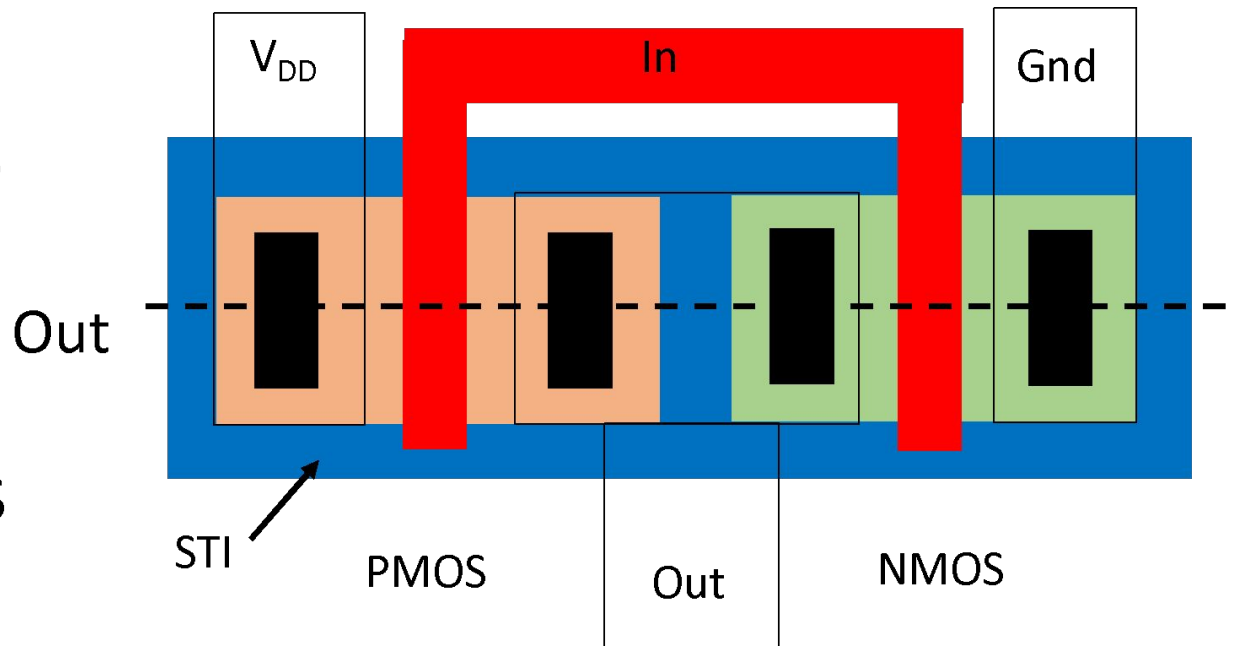
# KEY CONCLUSIONS

1. The Main advantage of CMOS is lack of static power dissipation
2. When NMOS is in the ON state PMOS is in the off state. When there is no switching action, there is no direct path between supply and ground
3. Si/SiO<sub>2</sub> is the best

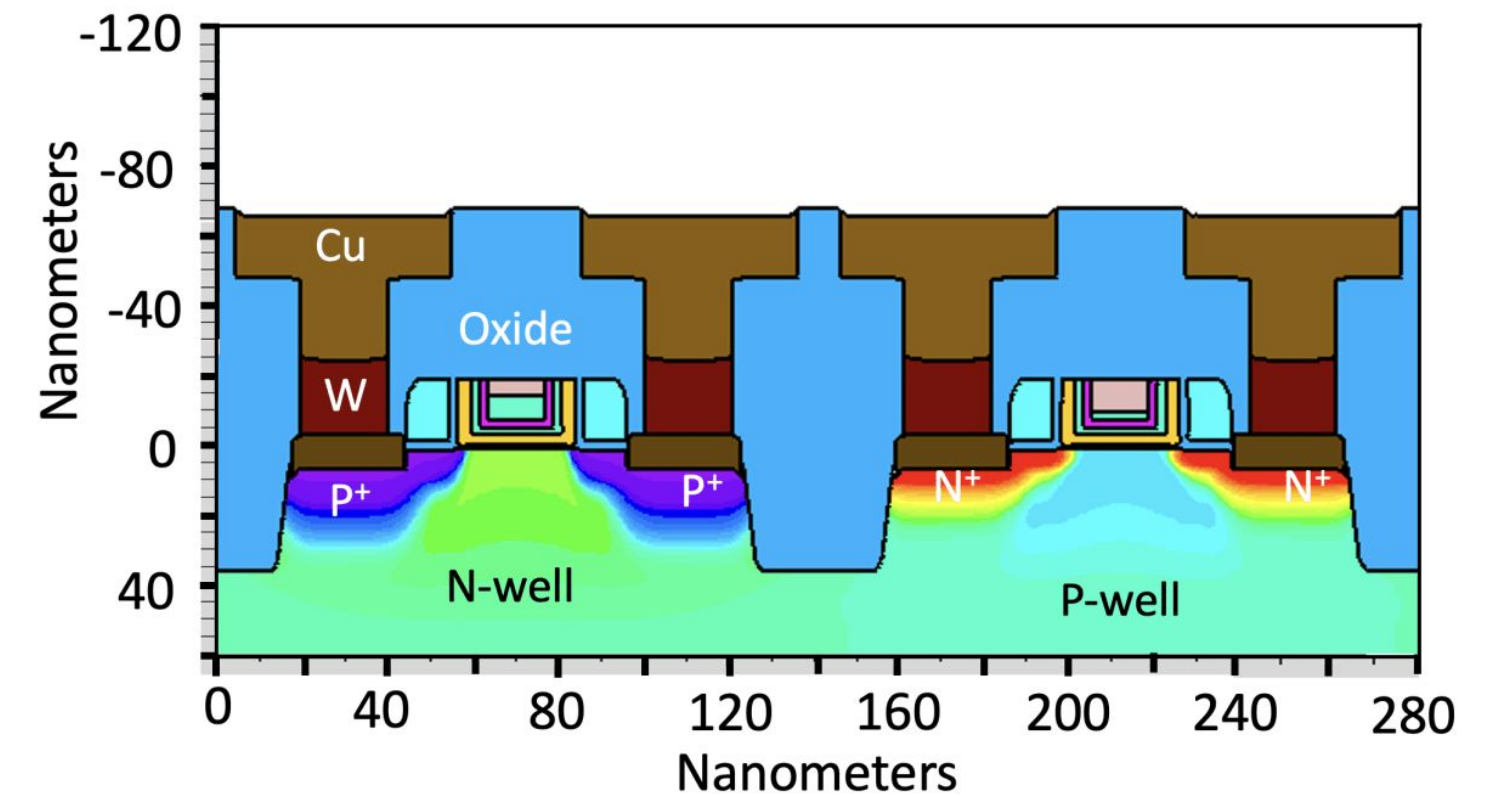
# CMOS INVERTER



Schematic



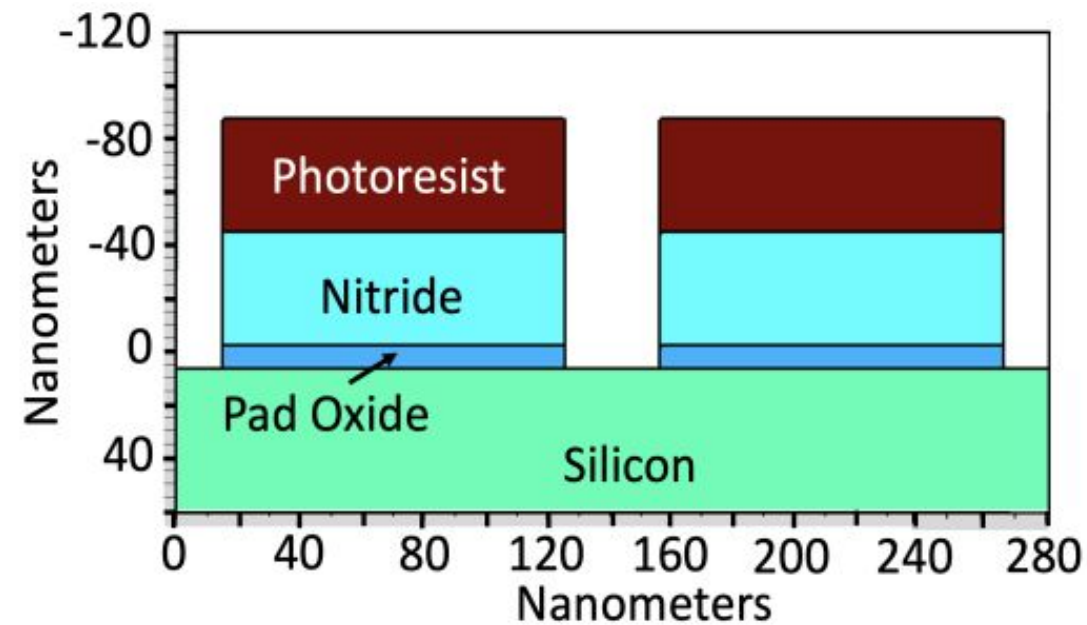
Layout



Simulated Device

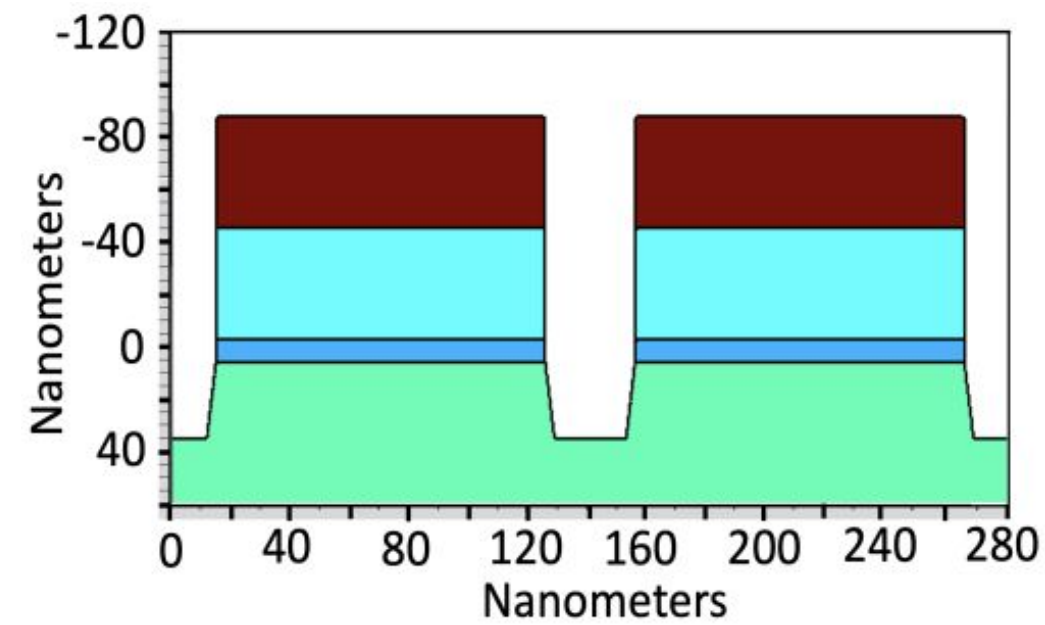
- Twin Well Process
- 28 nm Technology
- 16 Mask Process

# ISOLATION

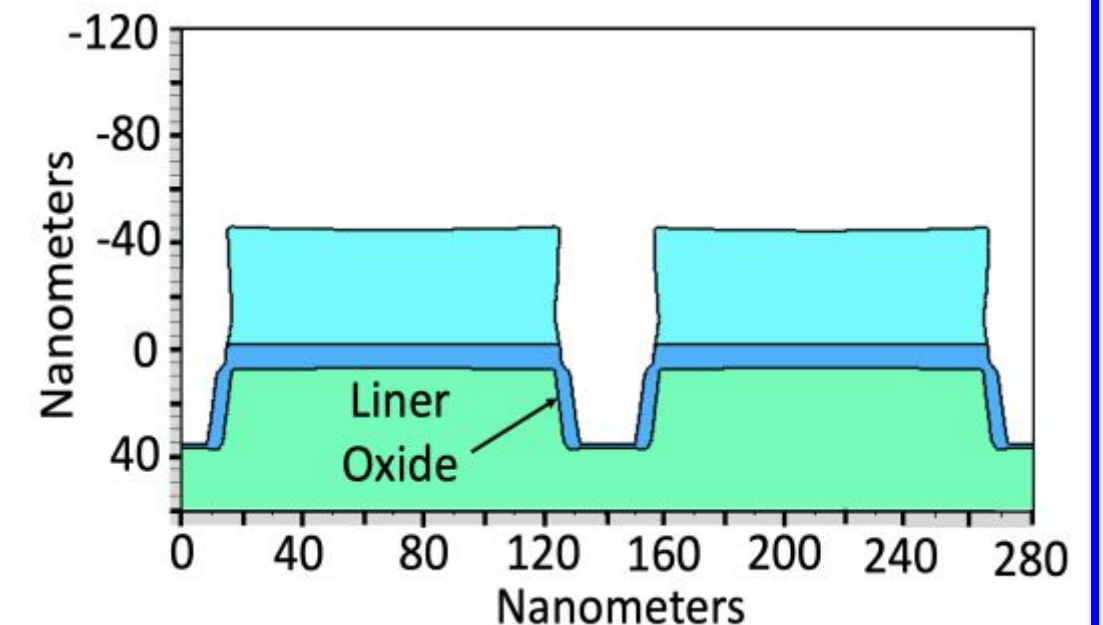


- Substrate P type Moderately doped
- Wafer Clean (SC1, SC2, HF)
- Thermal growth  $\text{SiO}_2$  (10 nm)
- LPCVD Nitride Deposition (50 nm)
- Photoresist (PR) Spin Coat
- Plasma Etch Nitride and Oxide

**MASK1**

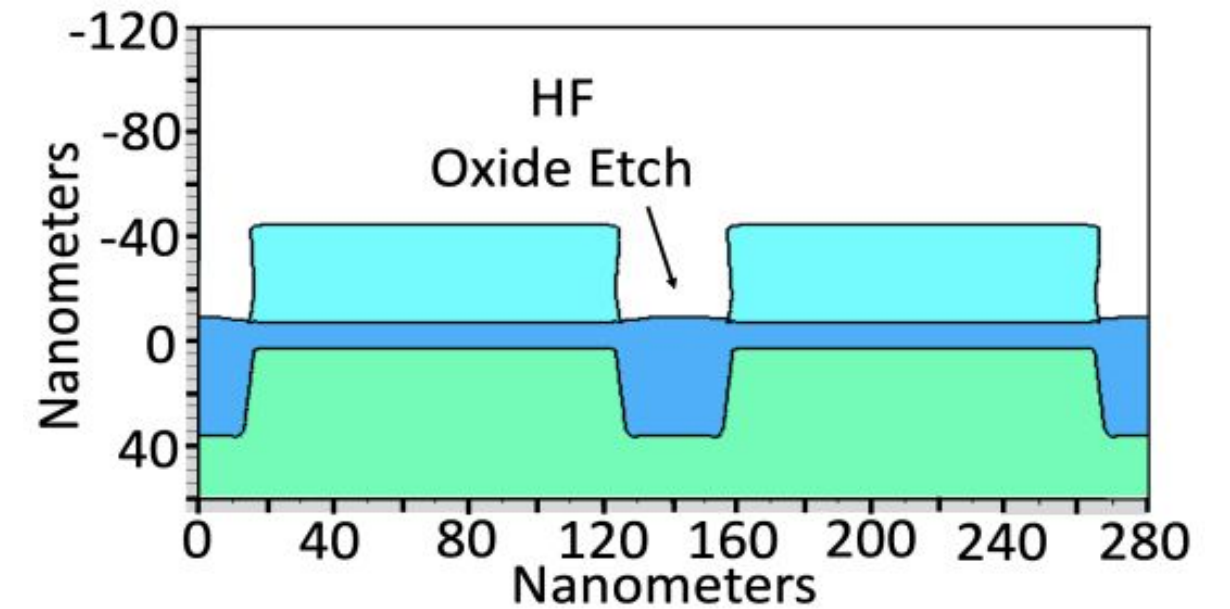
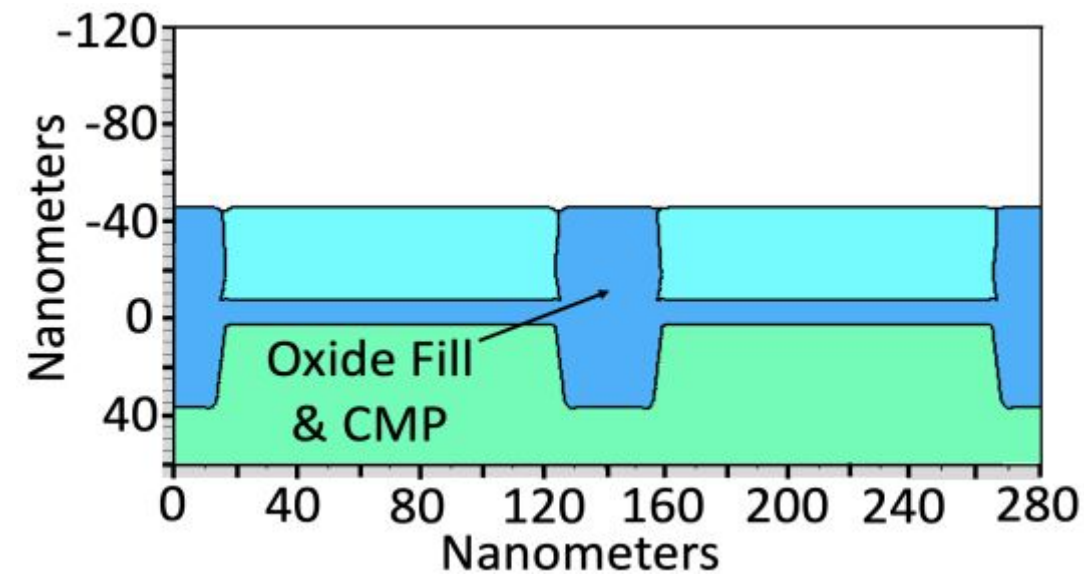
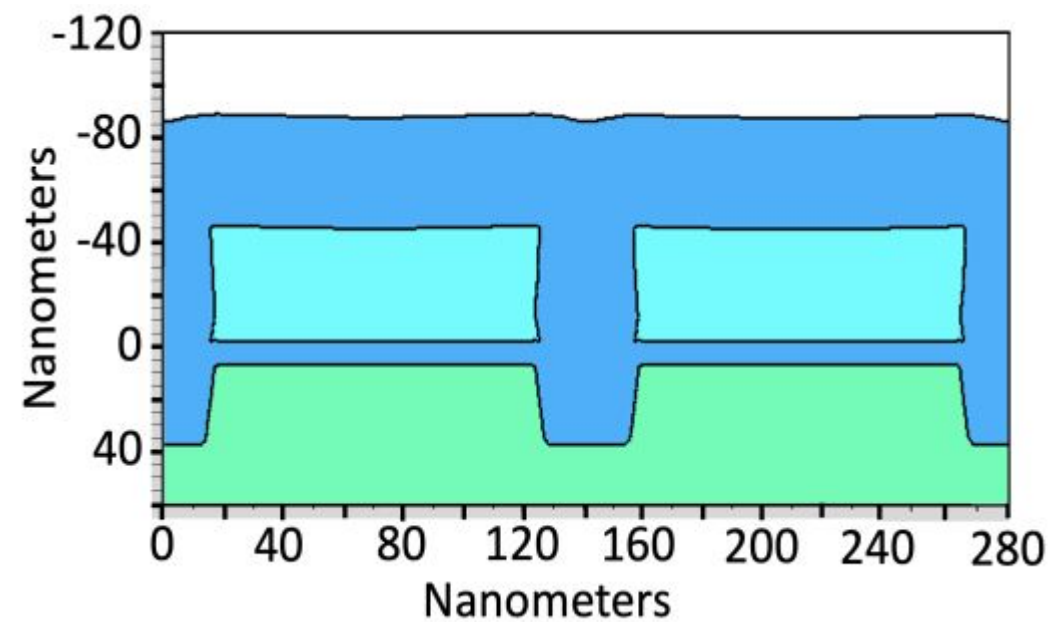


- Silicon Etching
- Tapered Etch (35 nm deep 85 ° angle)
- PR Removal



- Liner Oxide Deposition 30 min at 800°C (5 nm)
- Oxide does not grow below nitride

# ISOLATION CONTD

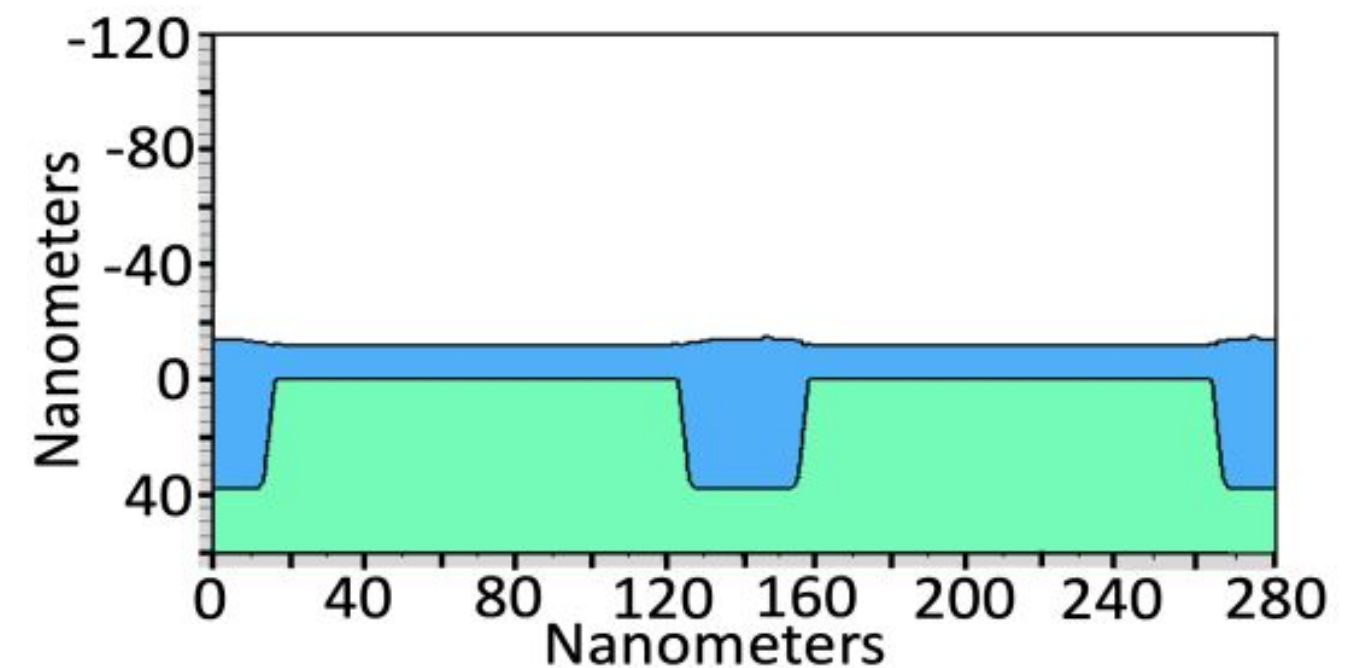


- **LPCVD SiO<sub>2</sub> (Conformal)**
- Void and gaps avoided using processing conditions

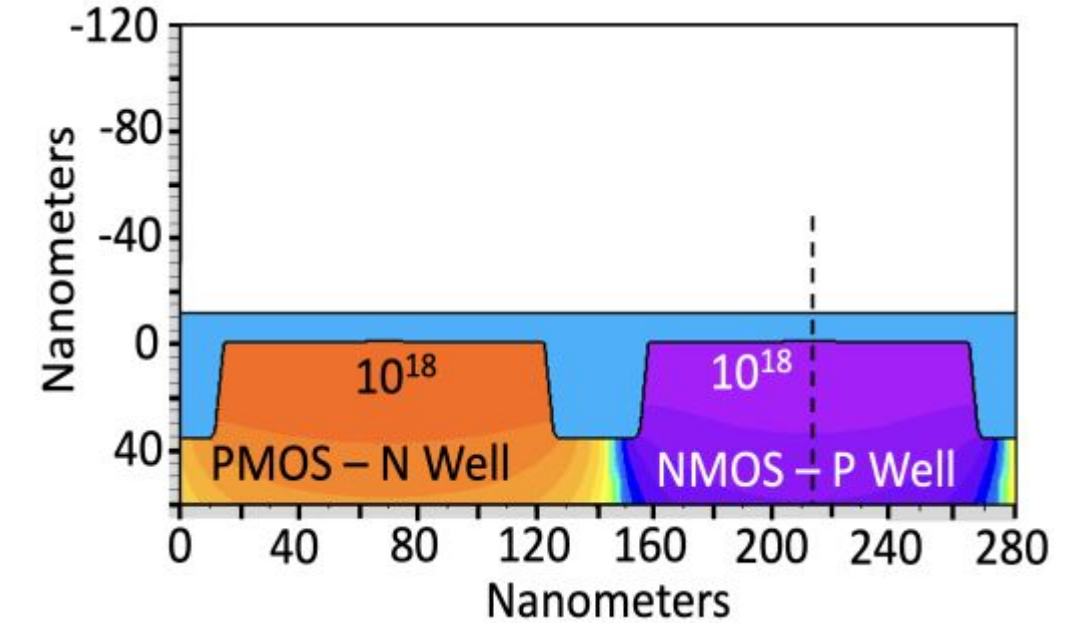
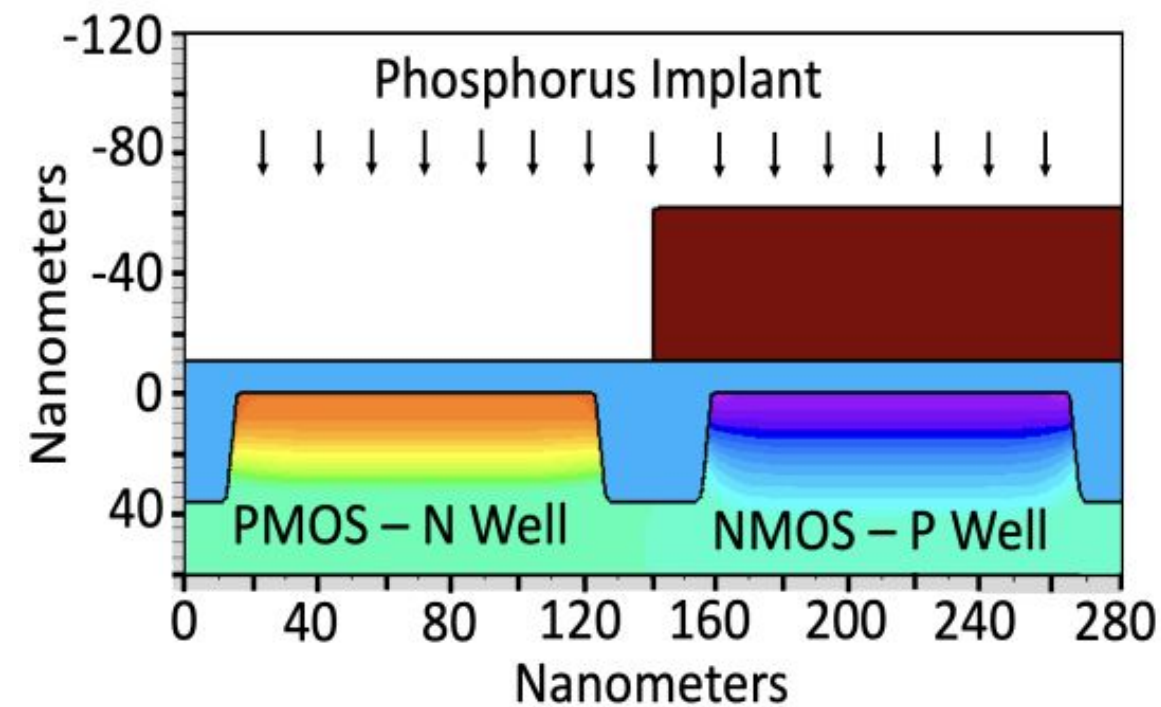
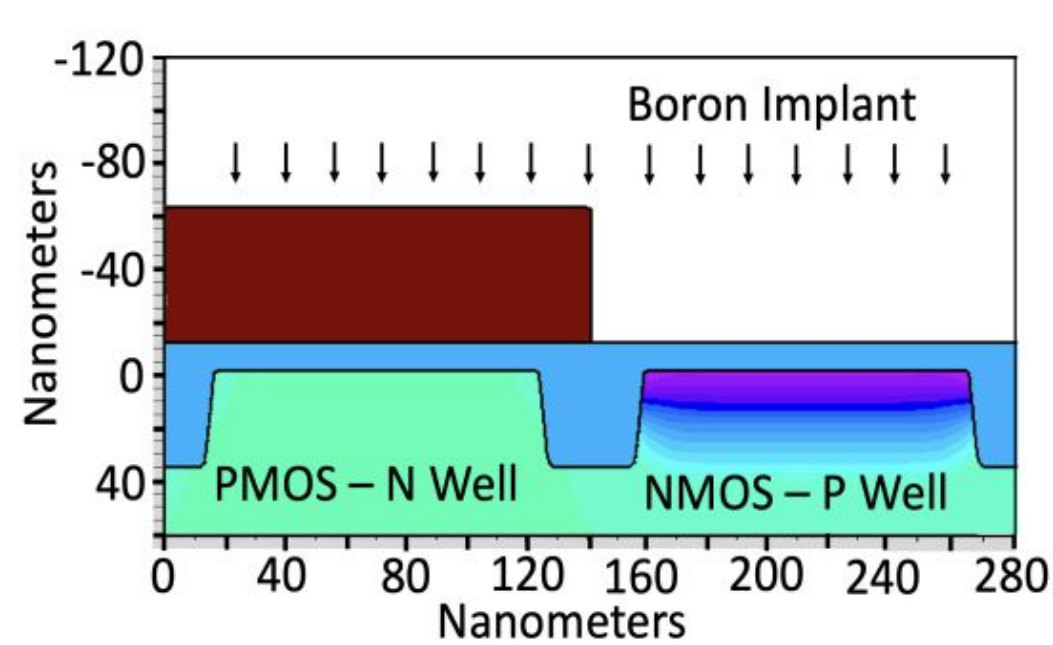
- Chemical Mechanical Polishing
- Hard Si<sub>3</sub>N<sub>4</sub> serves as a polishing stop

- **SiO<sub>2</sub> etch using HF**
- Nitride acts as a mask

- **Removal of Nitride in Phosphoric acid**
- Highly selective towards nitride and does not etch oxide



# p-Well and n-Well formation



- **Boron Implantation- P type**
- Photoresist acts as a mask

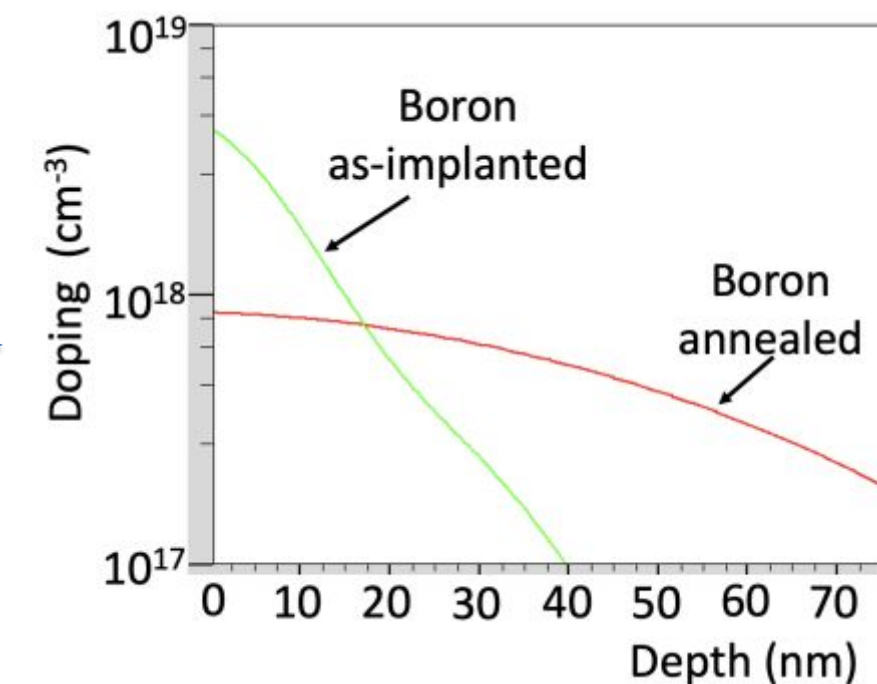
MASK #2

- **Phosphorous Implantation – N type**
- Photoresist acts as a mask

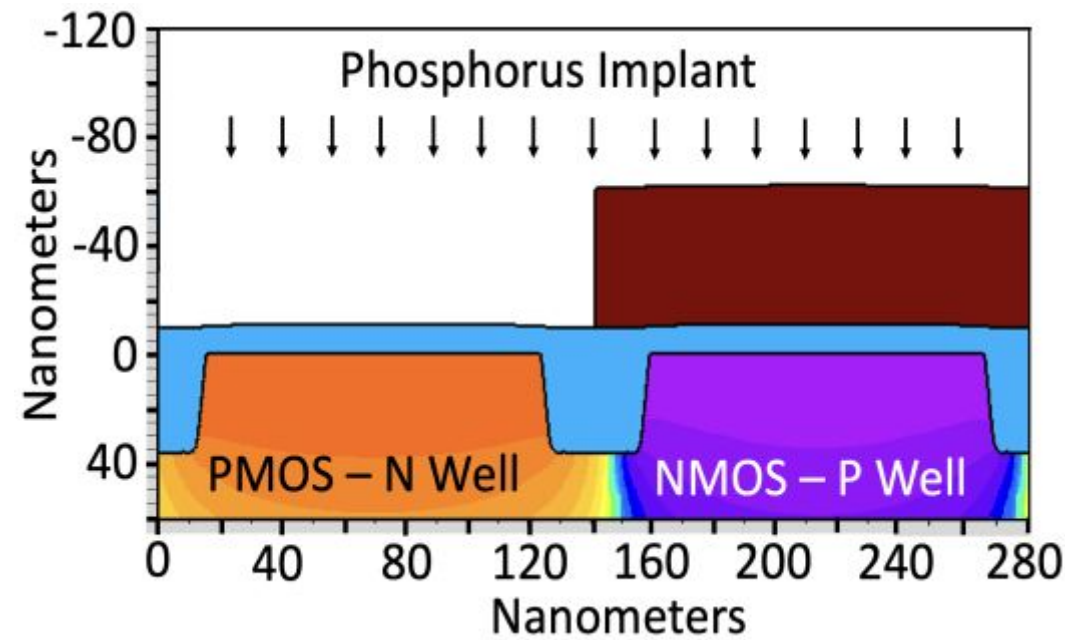
MASK #3

- **Annealing at 1000 °C, 10 min**
- **Repairs Ion Implantation damages**

- Doping Profile before and after anneal
- Gaussian Profile (approximate)



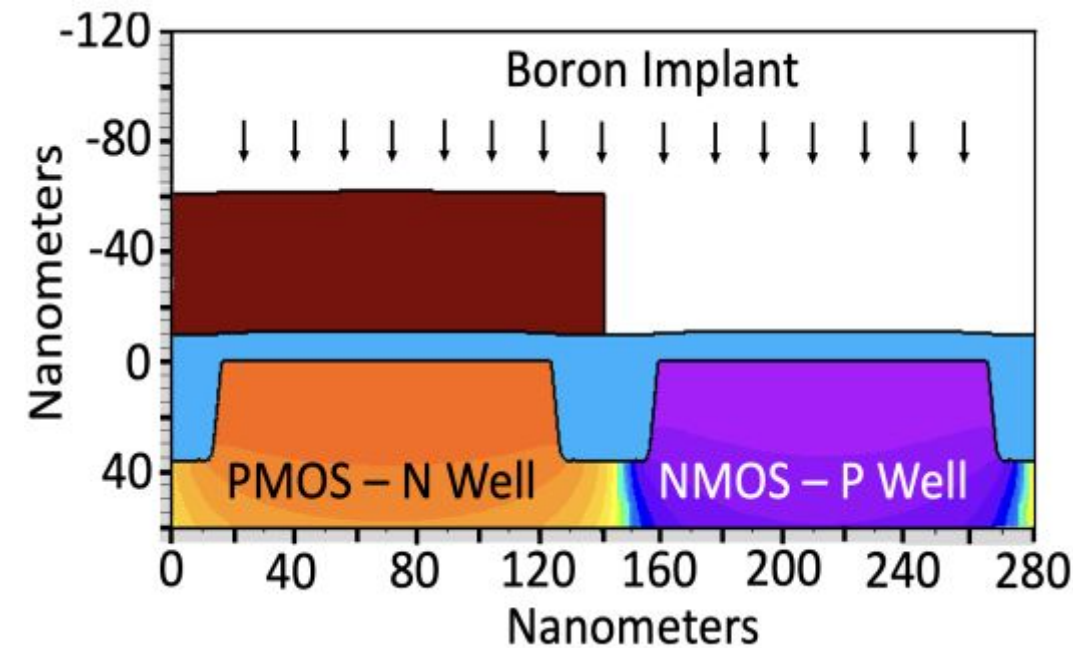
# Theshold adjust and Poly Si Gate formation



- **Threshold adjust implant**
- **Creates different VT nMOS**

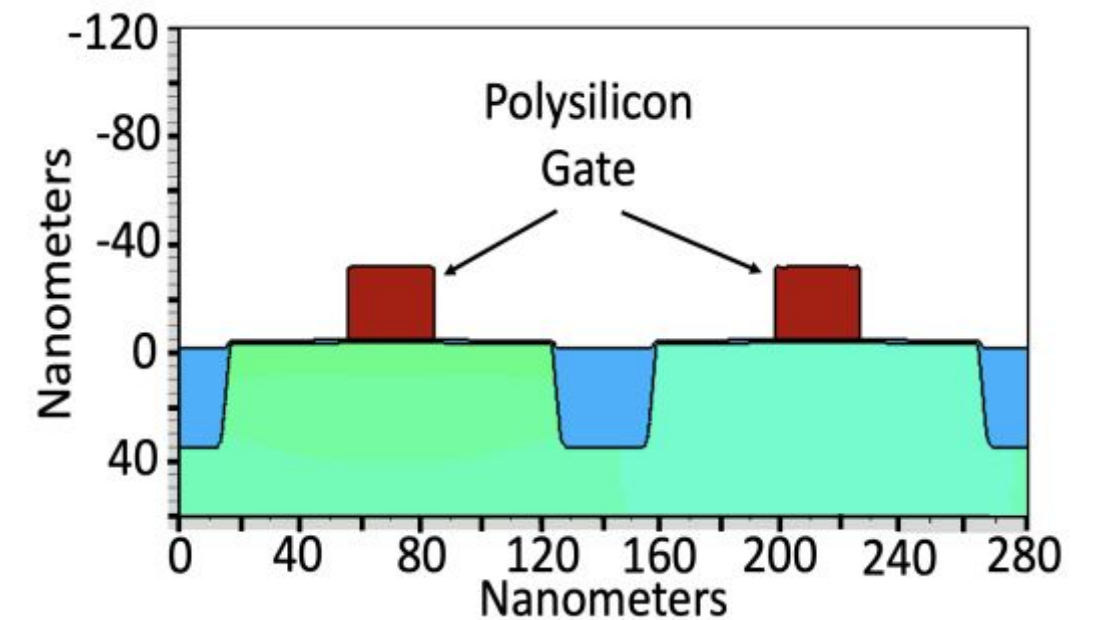
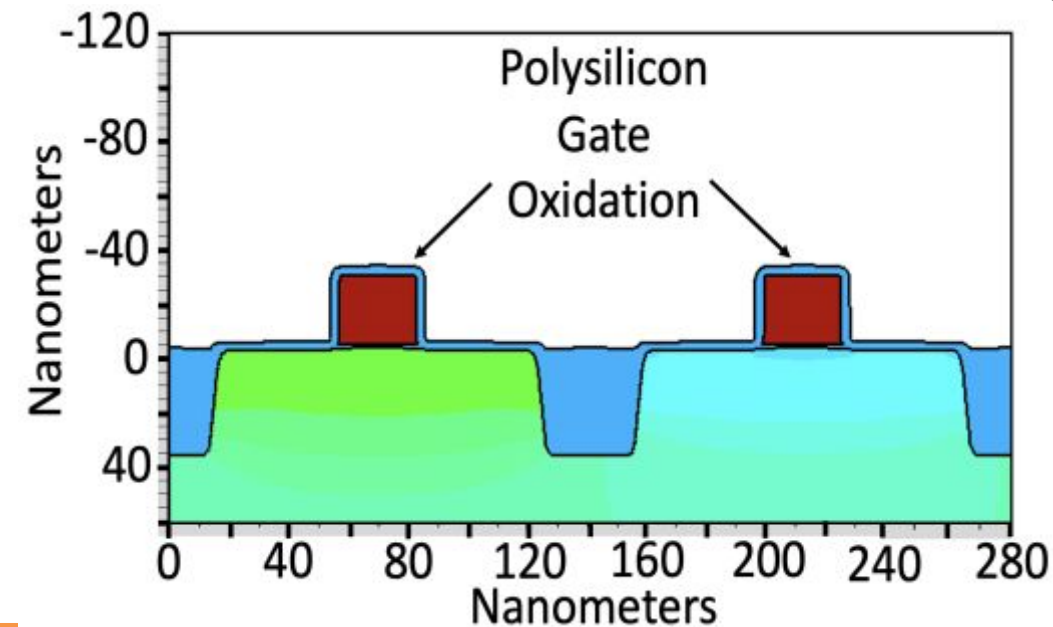
MASK #4

- **Gate Oxide growth**
- **800 °C, 5 nm**



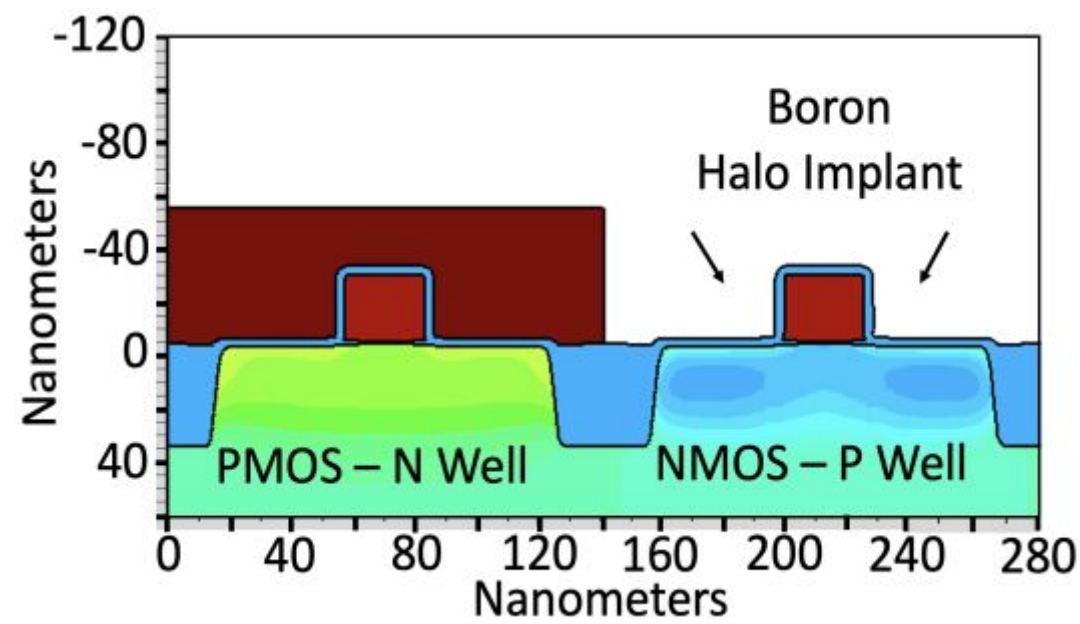
- **Threshold adjust implant**
- **Creates different VT PMOS**

MASK #5



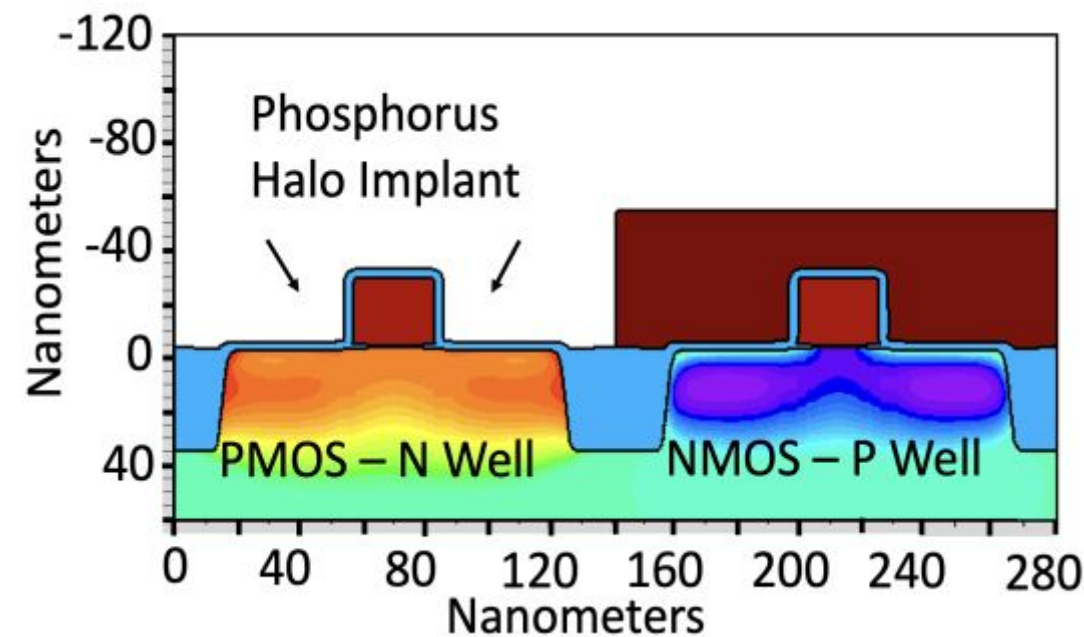
- **Etch oxide**
  - **Grow Polysilicon (Temporary Gate)**
  - **Etch Poly Silicon**
  - **Anisotropic plasma etching**
- MASK #6

# Halo Implants and Lightly doped drain

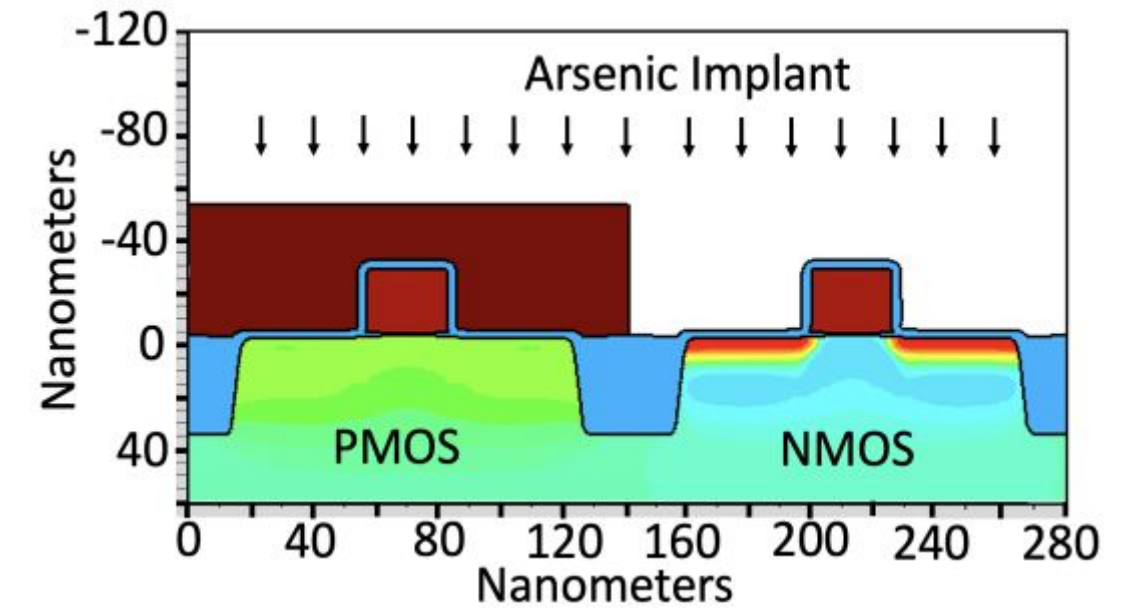


4

- Halo implant
- Tilted implant at  $25^\circ$
- Prevent Punch through  
MASK #7



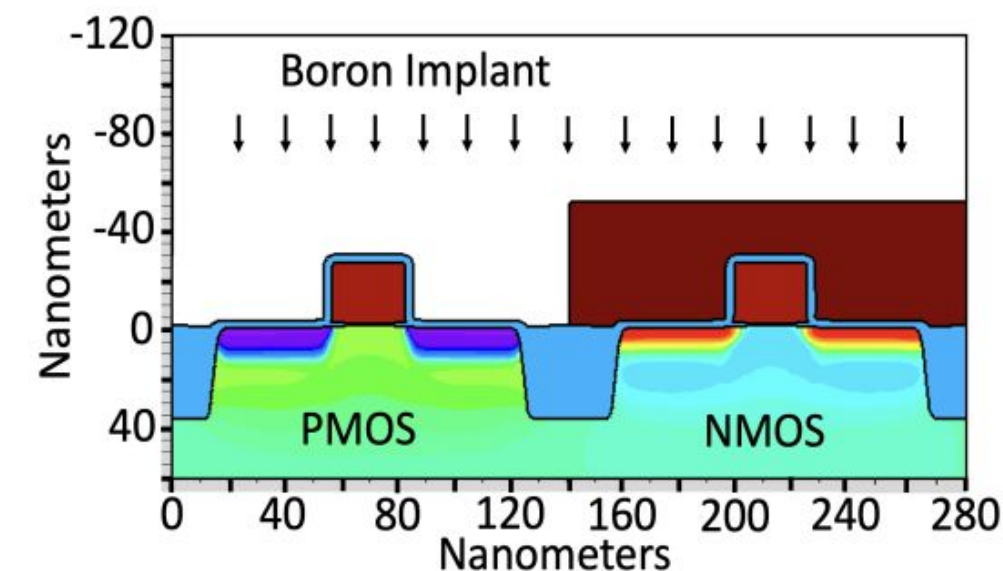
- Halo implant
- Tilted implant at  $25^\circ$
- Prevent Punch through  
MASK #8



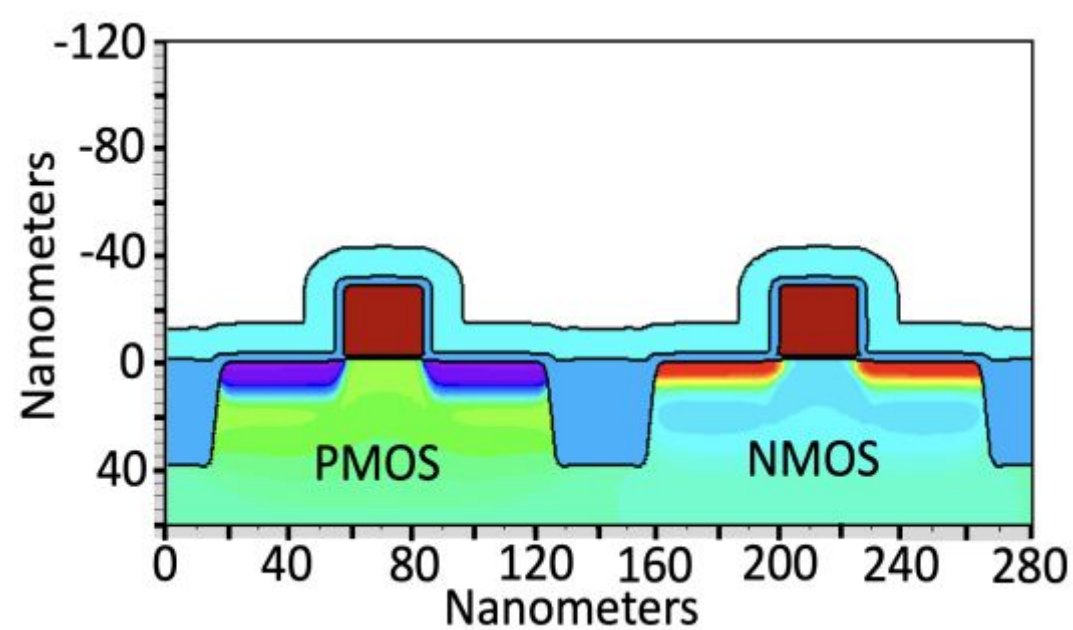
- Lighty Doped Drain
- Mitigates high fields in the channel

MASK #9

- Lighty Doped Drain
- Mitigates high fields in the channel  
MASK #10

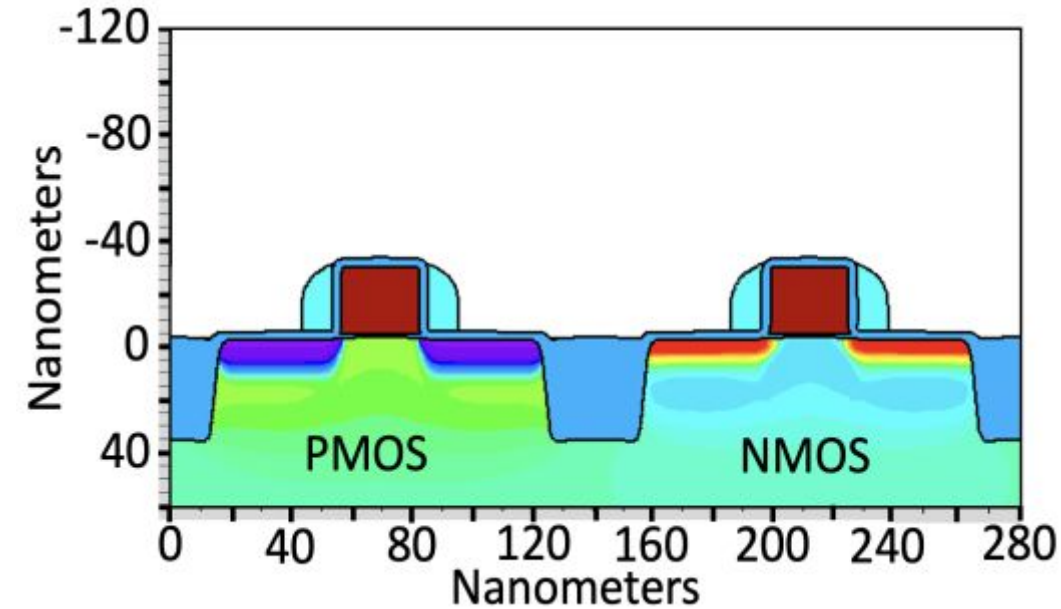


# Side Wall Spacers; Self aligned S/D formation

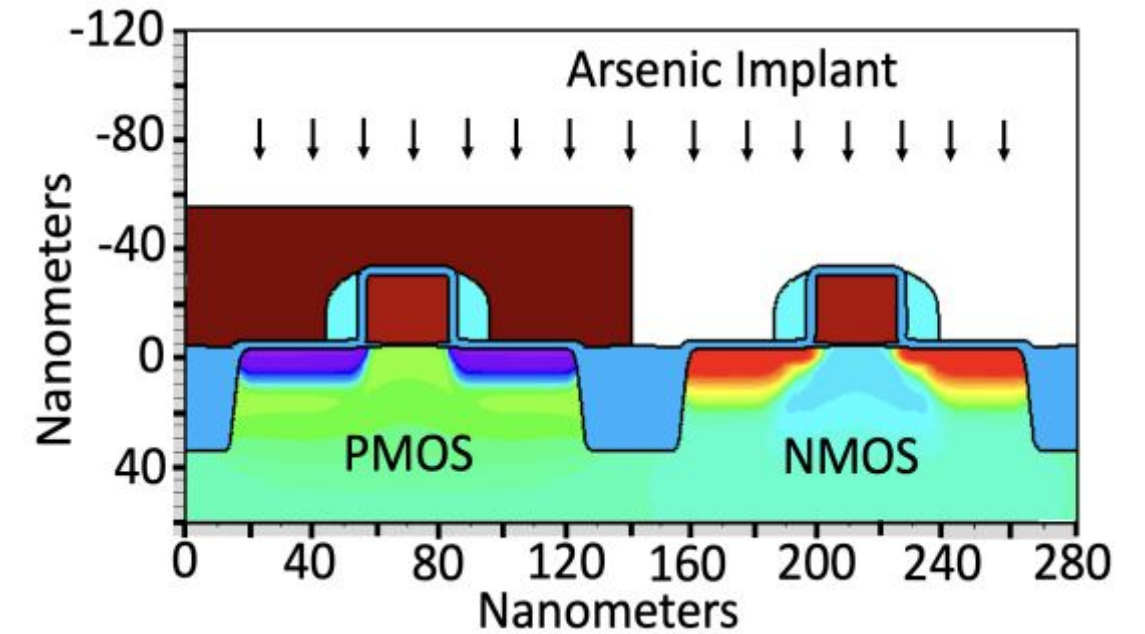


4

- Side Wall Spacer Deposition
- Confomal
- CVD



- Side wall etch
- Anisotropic
- Retains side walls
- No masking

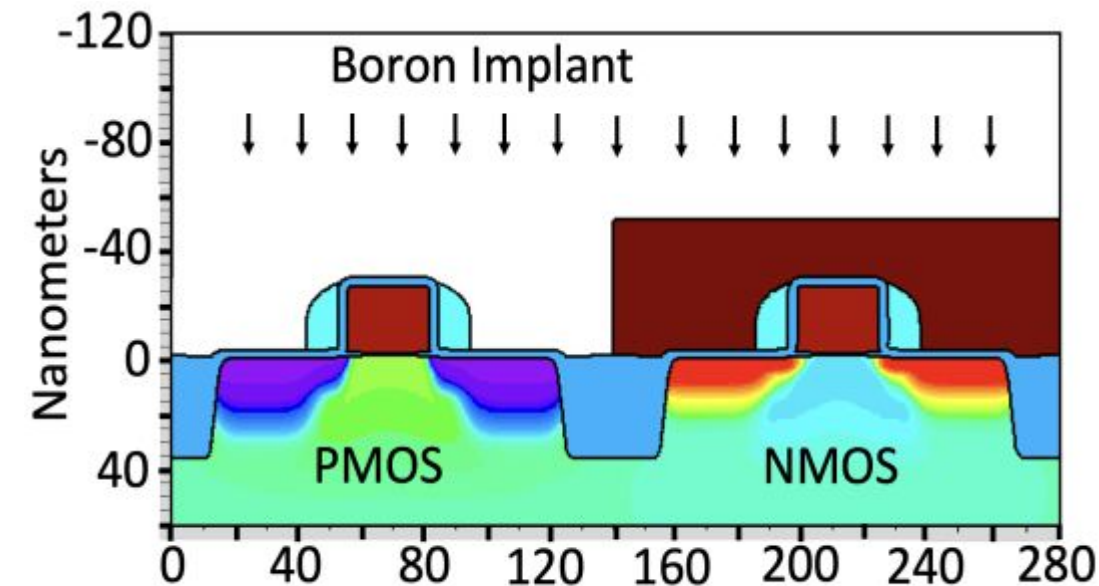


- Implantation of source/drain
- Implant Masked by polysilicon and spacer

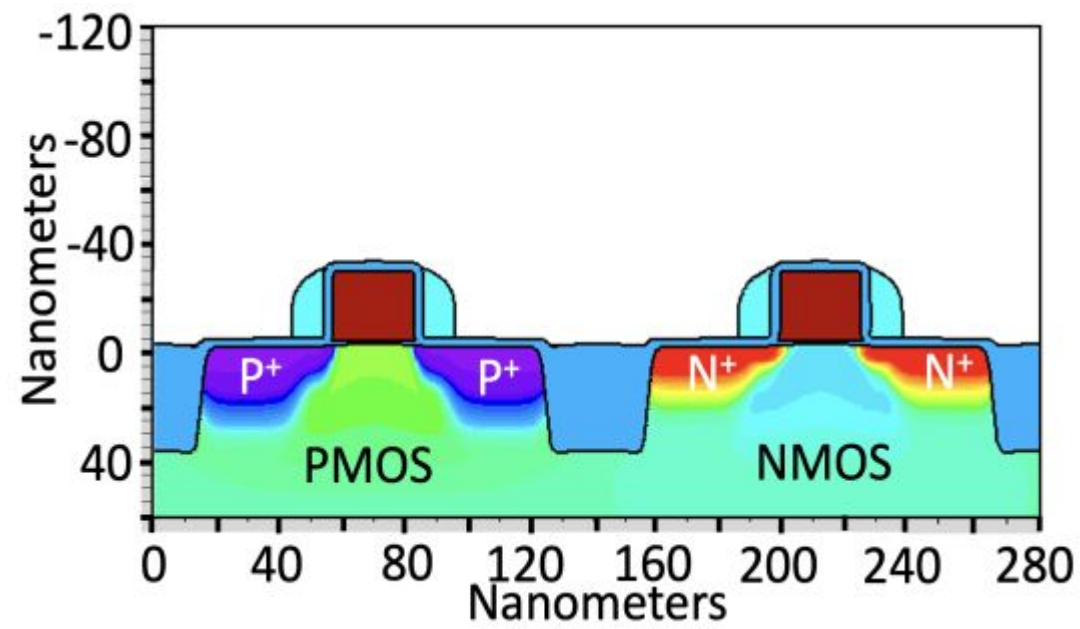
MASK #11

- Implantation of source/drain
- Implant Masked by polysilicon and spacer

MASK #12

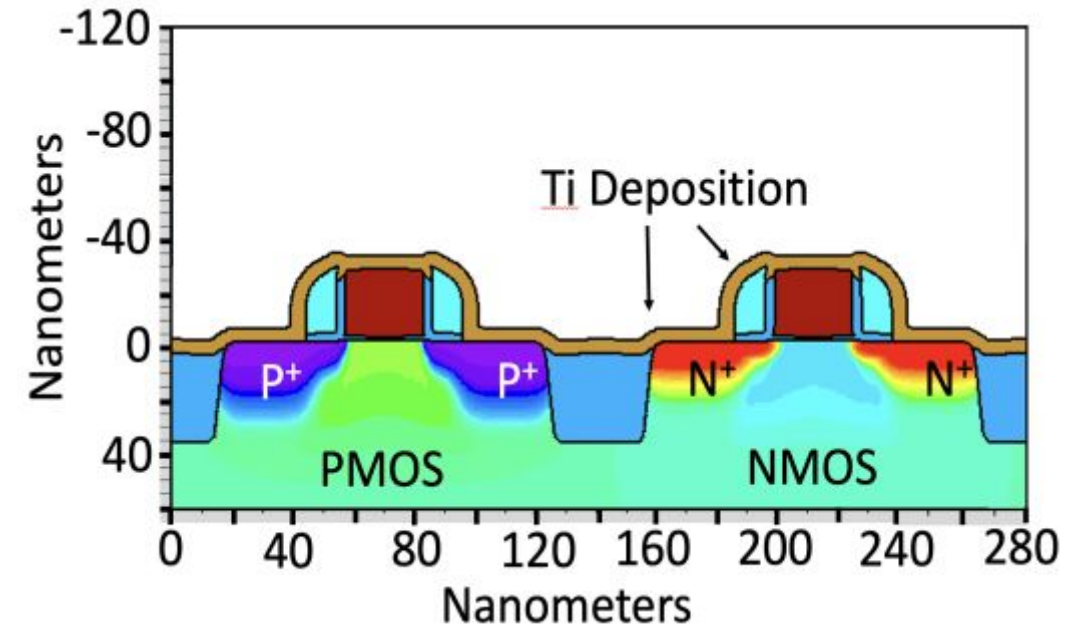


# Source Drain Interconnects

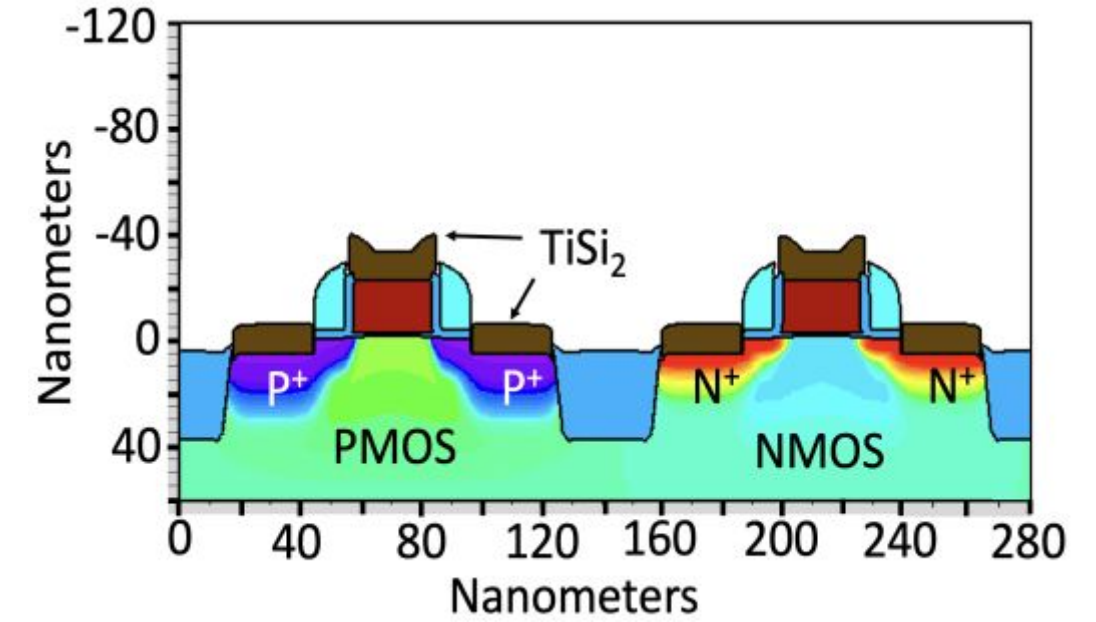


4

- **Rapid Thermal Anneal**
- Damage rectification and precise control of doping

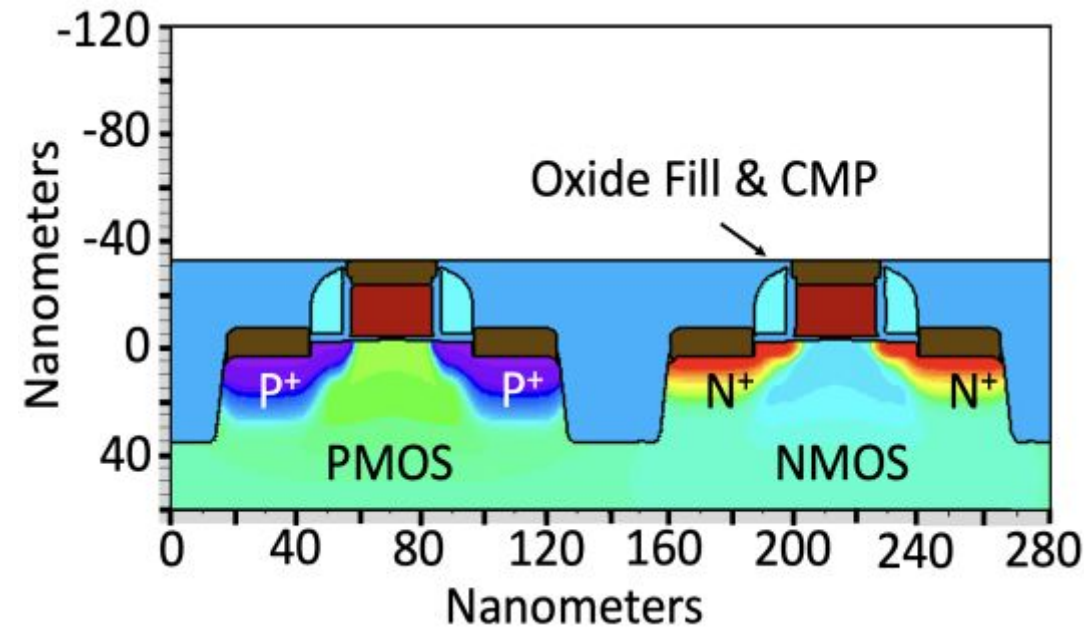


- **Titanium Deposition**
- 5 nm



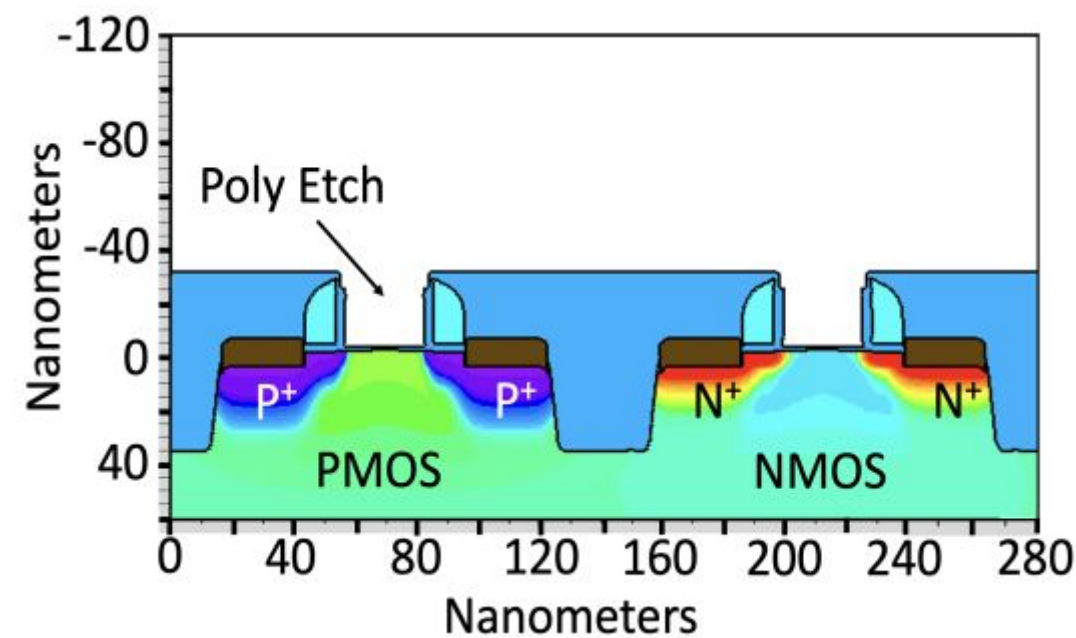
- **Titanium silicidation**
- Nitrogen Ambience, Causes TiN at the top

# Gate Last Process

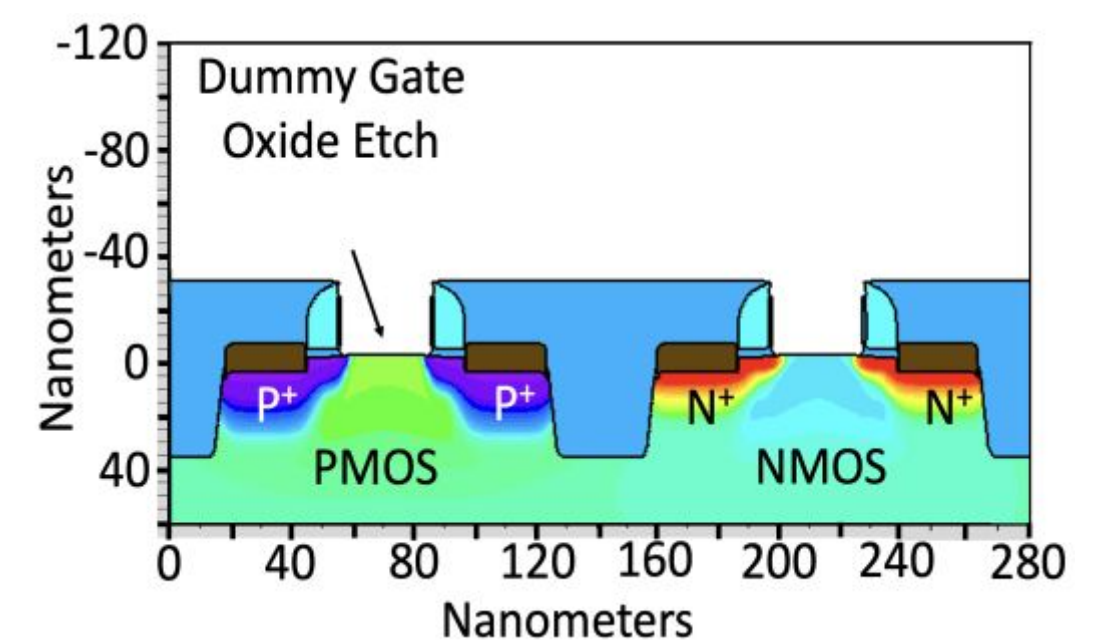


4

- **Conformal Oxide Deposition**
- **CMP**

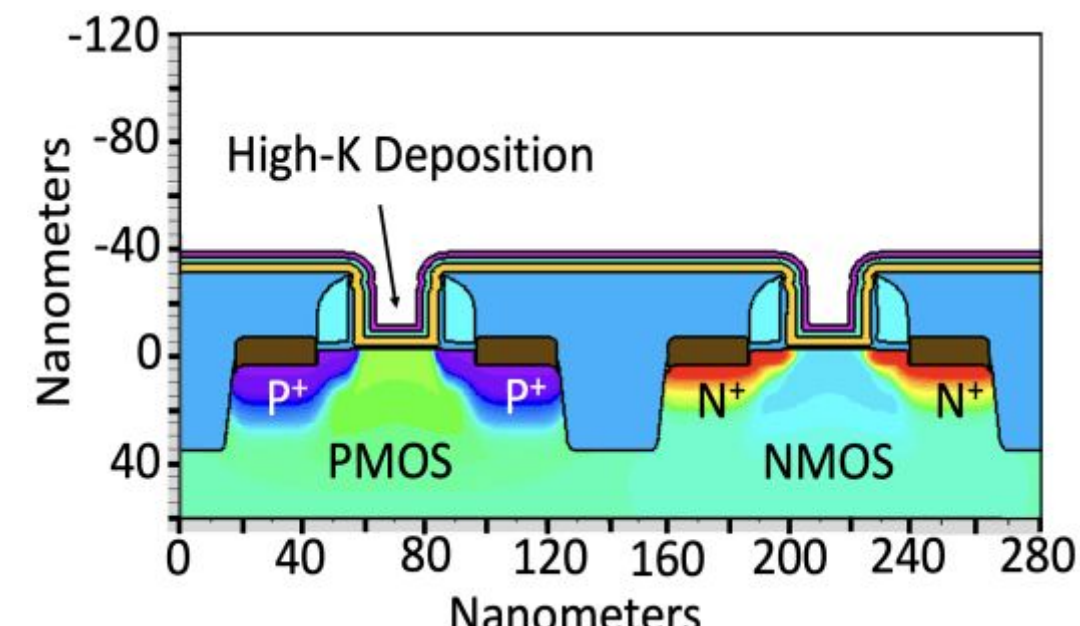


- Polysilicon etch for paving way for high K dielectric
- **Source and Drain Contacts**

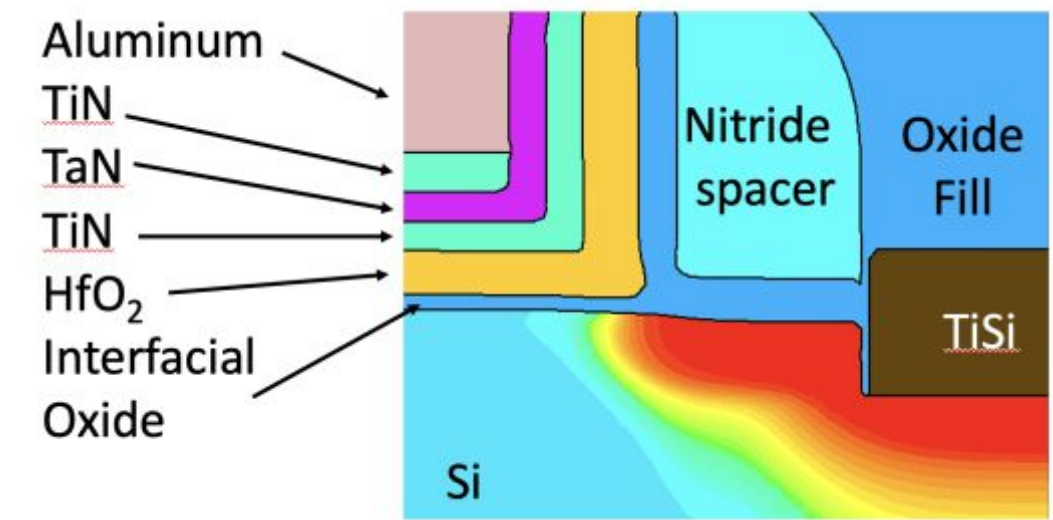
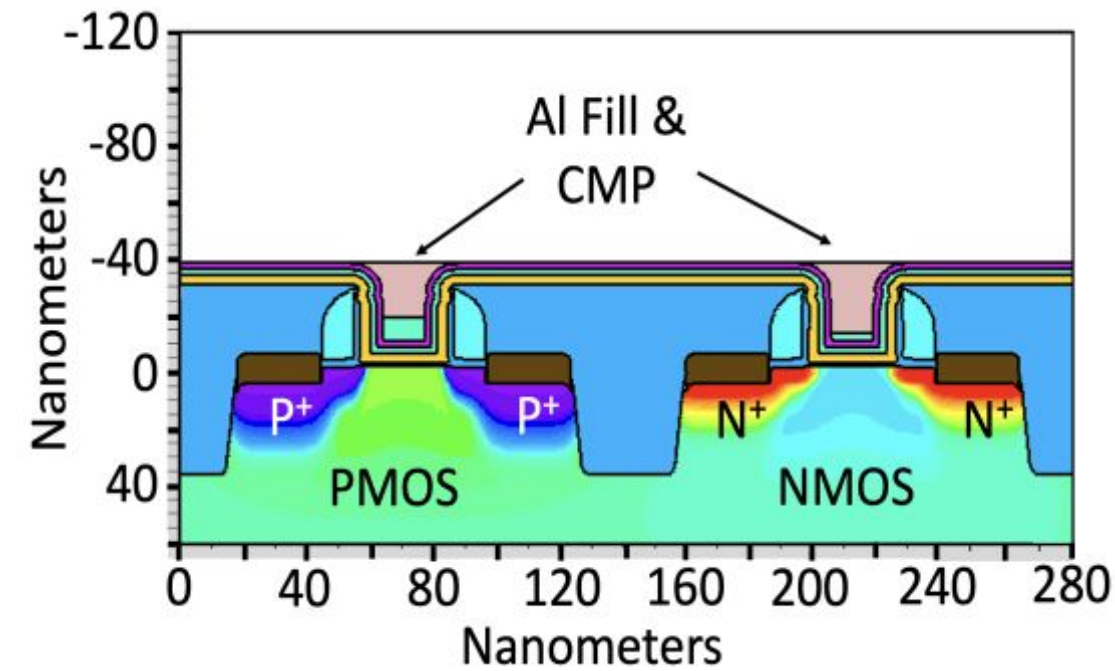
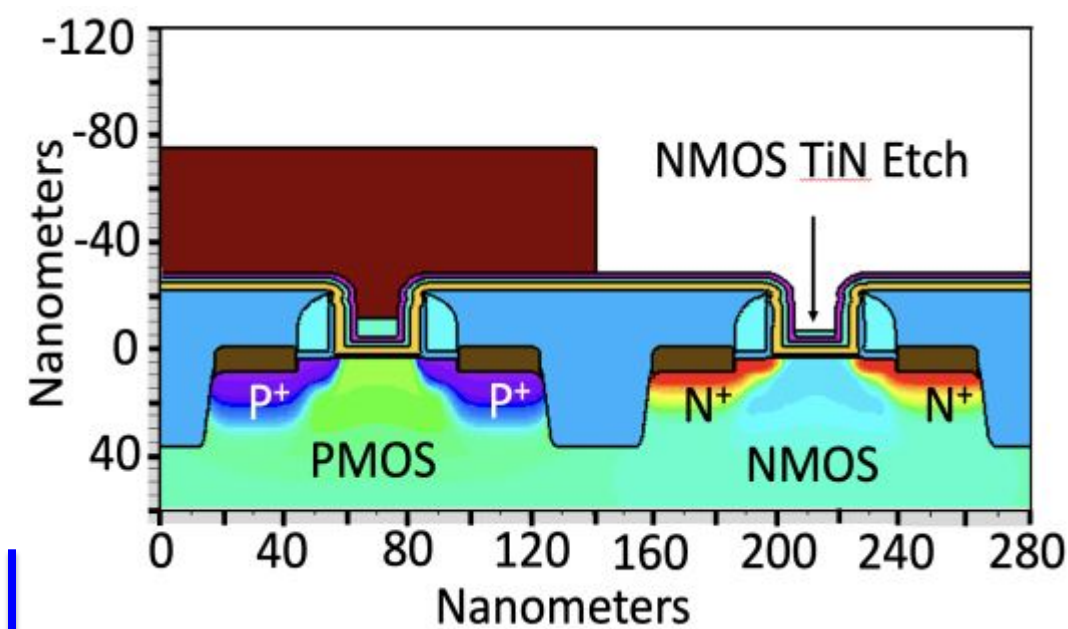


- Gate oxide etch
- **1 nm chemical stable oxide growth**

- **Hafnium Oxide deposition**
- **Atomic Layer Deposition (ALD)**



# Metal Stack Deposition



• Metal Stack Deposition

• Metal Stack Deposition

• Metal Stack Deposition

• 90 nm and 45 nm Transistors

