# Thermal Growth of Silicon Dioxide

EE 2520

Jan - June 2024

## 1 Introduction

**Slide #3**

1. The perfect and well studied interface between Si and its oxide is the primary cause for dominance of CMOS technology

2. $SiO_2$
   - Can be selectively etched
   - Can act as a good masking material against diffusion of dopants
   - Is an excellent insulator due to its very wide band gap (8.9 eV)
   - Can tolerate very high electric fiels

3. The interface between Silicon and its oxide is virtually perfect on the atomic scale, has very few mechanical or electrical defects and is stable over time

4. $SiO_2$ is used in various steps of CMOS processing. It can be used as a spacer mask against implant, as an isolation oxide in shallow trench and as an insulator between metal layers in back end processing but the primary use till 45 nm technology node. Various applications oxides as well as dielectrics is shown in Fir.1

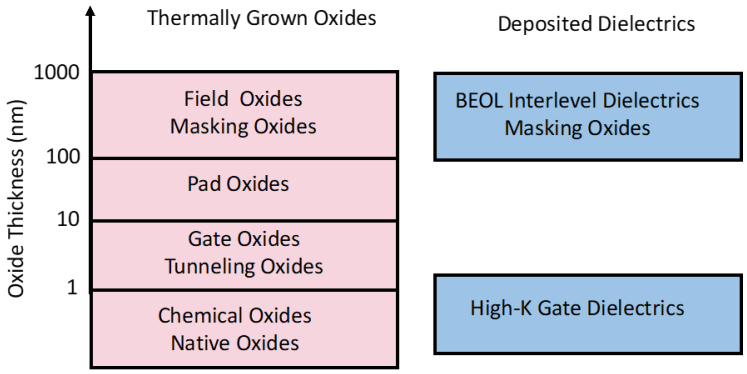


Figure 1: Oxide and dielectric thickness in CMOS

5. Formation of native oxide on Silicon is inevitable even at the room temperatures. The thickness is of the order of 1-2 nm and is mostly non uniform. This oxide needs to be removed

before any processing can be done on Silicon wafer. This removal is done by standard cleaning procedure consisting of SC1, SC2 and HF dip

6. Gate oxides typically are less than 10 nm
7. Slightly thicker thermal oxides in the range of 10 - 50 nm are used under silicon nitride layer as a stress relief or a "pad" oxide
8. Thicker oxides often serve as masks for gas phase doping steps
9. It is possible to deposit oxide layers using chemical vapor deposition (CVD) techniques. These depositions usually occur at smaller thermal budget
10. The interface between deposited oxide and the underlying silicon is not as perfect electrically as that formed by a thermal oxide
11. It is possible to anneal a deposited oxide to improve its properties and approach that of a thermal grown oxide. The simplest way is to expose the deposited oxide to oxygen or water vapor at high temperatures. The oxidant to diffuse to the interface, oxidizes the interface while high temperature densifies the oxide thereby improving the properties
12. Deposition of oxide is required for Back End of the Line process (BEOL)

## 2 Basic Model for Oxide Growth

**Slide #4**

1. Fig.2 shows a horizontal furnace with Si wafers stacked side by side in the furnace
2. The oxidant gases are introduced at the rear of the furnace
3. $O_2$ is for dry oxidation; Steam ($H_20$) or pyrophoric mixture of $H_2 + O_2$ is for wet oxidation

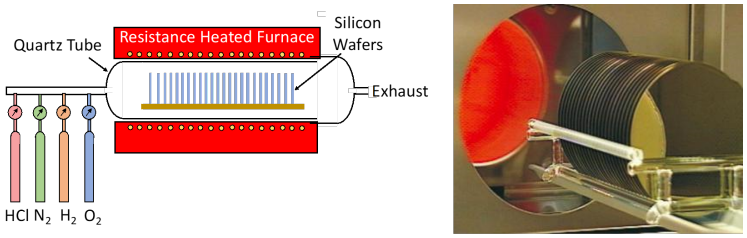


Figure 2: Typical Oxidation furnace

4. In Silicon Oxidation, the oxygen or water vapor diffuses through the oxide to the silicon/oxide interface where the net growth occurs
5. Silicon oxidation occurs by the inward diffusion of the oxidant rather than the outward diffusion of silicon

6. Oxygen atoms diffuse towards $Si/SiO_2$ interface, breaks the Si-Si bonds and forms the Si-O bonds

7. This process involves volume expansion because of the room needed for the oxygen atoms. An expansion of 30% is necessary in all the directions to accomodate oxygen atoms.

8. The Silicon substrate constraints oxide on two sides as depicted in Fig.3. The only option is for the oxide to expand both down into the silicon as it grows and above the silicon to accomodate the volume expansion

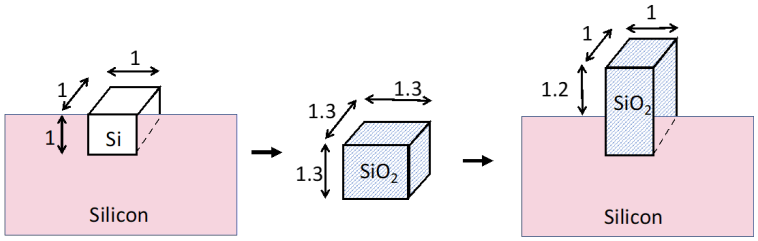


Figure 3: Silicon Dioxide Growth Mechanism

**Slide #5**

9. **LOCOS**:

   - LOCOS stand for LOC oxidation of Silicon
   - In the LOCOS process, the nitride acts a diffusion layer to the $O_2$ or $H_2O$ oxidant and prevents oxidation underneath the $Si_3N_4$ layer. Thus the silicon is oxidized locally. This process was used for isolating devices and is replaced by Shallow Trench Isolation
   - As shown in the cross section image Fig.4, the volume expansion on the planar surface is accommodated by the oxide both growing down and twors the silicon interface and expanding upwards beyond the original interface for the 2.2 times volume expansion
   - Nitride does not act as a perfect mask for the oxidation.
   - The oxidant diffuses and reacts laterally under the mask edge thereby lifting the nitride to produce the characteristic "bird's beak" shape

10. The growth of oxide on crystalline silicon is amorphous primarily due the lattice mismatch.

11. A central silicon atom is tetrahedrally coordinated to four oxygen atoms, each of which is shared by an adjancent silicon atom. these $SiO_4$ tetrahedra are the basic units from which $SiO_2$ forms as shown in Fig.5.

12. They bond together by sharing the briding oxygen atoms and these bridging atoms allow one tetrahedron to rotate with respect to its neighbours and lose long range order and thus become amorphous

13. The oxide is under compressive stress due to the following reasons

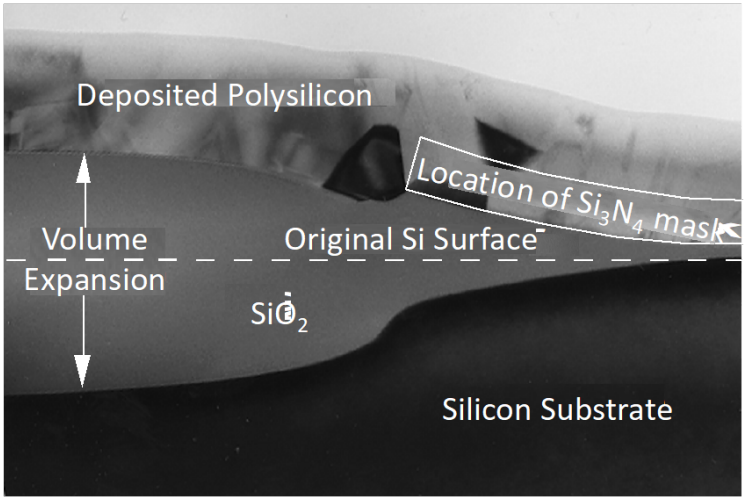


Figure 4: LOCOS

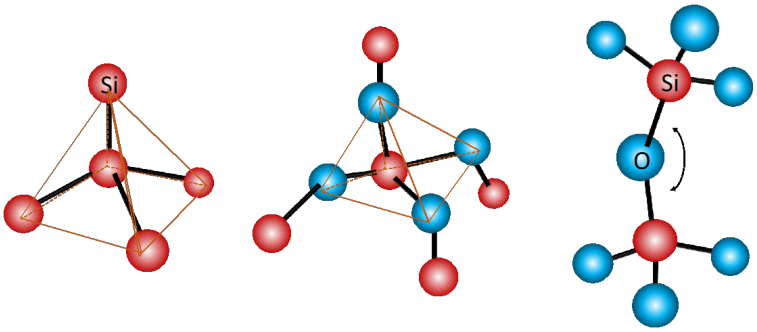


Figure 5: Amorphous Structure of $SiO_2$

- Requirement of Volume expansion
- Mismatch in thermal expansion coefficients

14. The high resolution transmission electron micrograph (TEM) image in Fig.6 shows the crystal structure in the silicon and an amorphous oxide layer, with an abrupt transition between the two.

**Slide #6**

15. The oxide grows by in-diffusion of the oxidizing species to the oxide/silicon interface where a simple chemical reaction occurs with $O_2$ and $H_2O$.

16. Dry oxidation

$$\boxed{Si + O_2 \rightarrow SiO_2} \tag{1}$$

17. Wet oxidation

$$\boxed{Si + 2H_2O \rightarrow SiO_2 + 2H_2} \tag{2}$$

18. Deal-Grove model (DG) is the standard model used for modeling oxidation processes.

19. DG model considered following fluxes

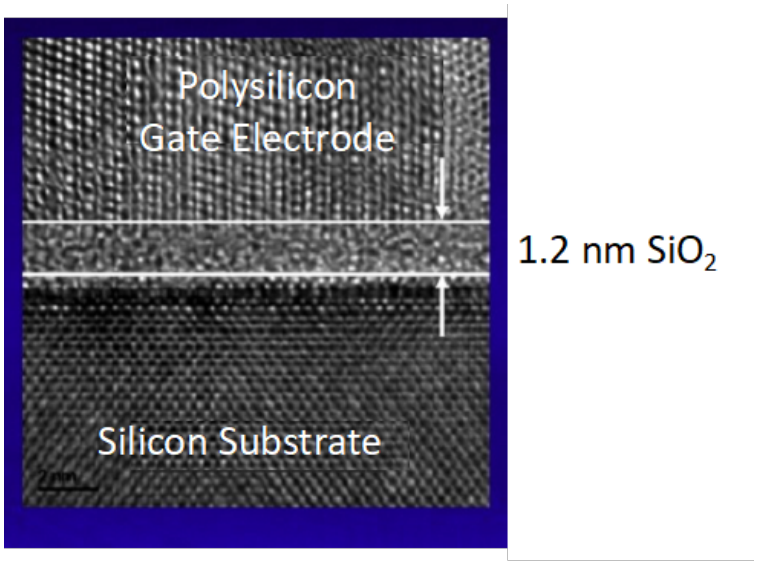


Figure 6: TEM Image of Si and its oxide

- $F_1$ : Transport of oxidant through the gas phase to the outer interface
- $F_2$ : Diffusive flux of oxidant through the oxide layer
- $F_3$ : Chemical reaction flux at the interface

20. Experimentally it is proven that gas phase transport and adsorption do not limit the rate at which oxidant enters oxide.

21. The basis of DG model can thus be simplified to the diffusion and reaction fluxes $F_2$ and $F_3$

22. Oxidant is available at the $SiO_2$ surface at an equilibrium concentration $C^*$ that is the solid solubility of the oxidant in $SiO_2$

23. Solid Solubility of $H_2O$ : $3 \times 10^{19} cm^{-3}$

24. Solid Solubility of $O_2$ : $3 \times 10^{16} cm^{-3}$

25. The oxidant diffuses through the existing oxide until it reaches the silicon interface where it reacts with the silicon to form $SiO_2$

**Slide #7**

26. The flux $F_2$ represents the diffusion of the oxidant through the oxide to the interface and can be expressed as

$$\boxed{F_2 = D\frac{dC}{dx} = D\left(\frac{C^* - C_i}{x_0}\right)} \tag{3}$$

27. $D$ is the oxidant diffusivity in the oxide. $C^*$ and $C_i$ are the concentrations at the oxide/ambient interface and oxide/silicon interface respectively

28. The linear expression is a simplification based on the assumption that there is no loss of oxidant as it diffuses through the oxide

29. The rate at which the oxidant is consumed at the interface is given proportional to the concentration and is given by

$$\boxed{F_3 \;=\; k_s C_i} \tag{4}$$

30. $k_s$ is the reaction rate and $C_i$ is the concentration of the oxidant at the interface.

31. The oxide growth rate is equal to the flux divided by the number of oxidant molecules $N_1$ that must be incorporated to form an unit volume of silicon

32. The molecular density of $SiO_2$ is $2.2 \times 10^{22}/cm^3$

33. $N_1$ for dry oxidation is $2.2 \times 10^{22}/cm^3$

34. $N_1$ for wet oxidation is $4.4 \times 10^{22}/cm^3$

35. Under steady state conditions, the fluxes are equal

$$\boxed{F_2 \;=\; F_3 \;\Rightarrow\; D\left(\frac{C^* \;-\; C_i}{x_0}\right) \;=\; k_s C_i} \tag{5}$$

36. $C_i$

$$\boxed{C_i \;=\; \frac{C^*}{k_s \frac{x_0}{D} \;+\; 1}} \tag{6}$$

37. The Growth Rate

$$\boxed{\frac{dx_0}{dt} \;=\; \frac{F_3}{N_1} \;=\; \frac{k_s \frac{C^*}{N_1}}{k_s \frac{x_0}{D} \;+\; 1}} \tag{7}$$

$$\boxed{\frac{dx_0}{dt} \;=\; \frac{B}{2x_0 \;+\; A}} \tag{8}$$

38. The linear growth coefficient B/A is

$$\boxed{B/A \;=\; k_s C^*/N_1} \tag{9}$$

39. The Parabolic growth coefficient B is

$$\boxed{B/A \;=\; 2DC^*/N_1} \tag{10}$$

40. Note that B depends only on mass transport and B/A depends only on kinetics

41. Integration Eqn.8, we have

$$\boxed{\frac{x_0^2}{B} \;+\; \frac{x_0}{B/A} \;=\; t \;+\; \tau} \tag{11}$$

42. $\tau$ is the time taken to grow initial oxide, if any,

$$\boxed{\tau \;=\; \frac{x_i^2}{B} \;+\; \frac{x_i}{B/A}} \tag{12}$$

43. The overall expression for thickness is given by

$$\boxed{x_0 = \frac{A}{2}\left[\sqrt{1 + \frac{t + \tau}{A^2/4B}} - 1\right]} \tag{13}$$

**Slide #8**

44. The limiting regimes are when $x_0$ is very small and $x_0$ is large as shown in Fig.7

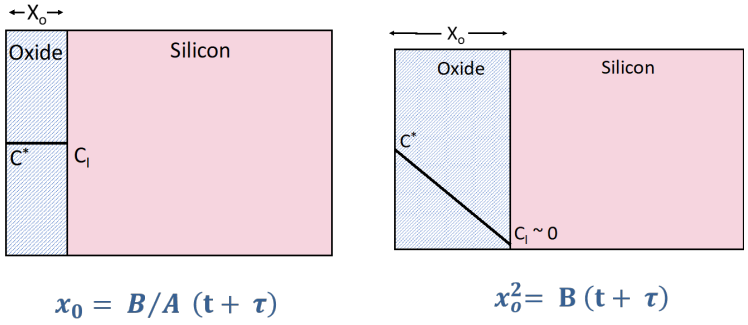


Figure 7: Kinetic Limited and Diffusion Limited Regimes

45. During the initial phase the growth can be approximated as

$$\boxed{x_0 = B/A(t + \tau)} \tag{14}$$

46. As thickness increases, diffusion through the already grown oxide becomes the limiting factor and the thickness can be modelled as

$$\boxed{x_0^2 = B(t + \tau)} \tag{15}$$

47. The model is not valid for ultra thin oxides

48. Higher doped substrates show faster growth rates

49. Experimentally both the linear and parabolic diffusion coefficients can be modeled as

$$\boxed{B = C_1 e^{(-E_1/kT)}} \tag{16}$$

$$\boxed{B = C_2 e^{(-E_2/kT)}} \tag{17}$$

50. $E_1$ and $E_2$ are the activation energies associated with the physical processes; $C_1$ and $C_2$ are activation energies

51. Fig.8 shows the values of the coefficients as a function of temperature

52. Table.1 shows the values of the coefficients for wet and dry oxidation processes

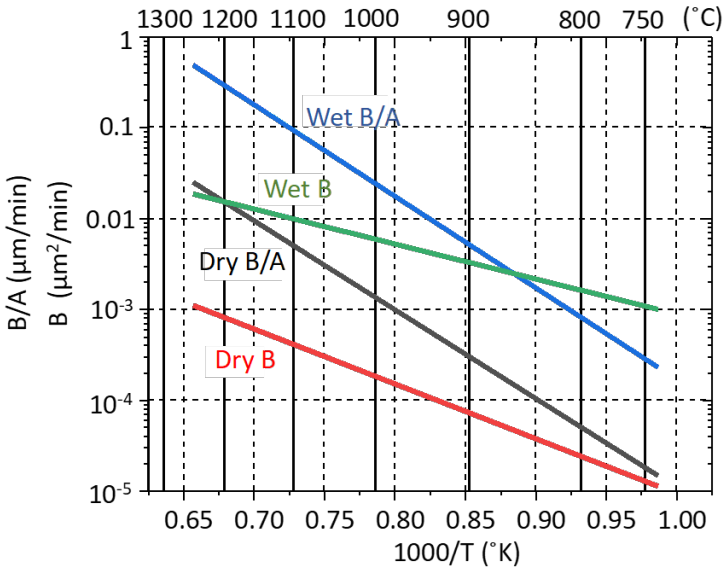


Figure 8: Arrhenius plots of diffusion coefficients

| Ambient | B/A | B |
|---|---|---|
| Dry $O_2$ | $1.04 \times 10^5\ e^{(-2.0eV/kT)}$ | $12.87\ e^{(-1.23eV/kT)}$ |
| $H_2O$ | $2.95 \times 10^5\ e^{(-2.05eV/kT)}$ | $7\ e^{(-0.78eV/kT)}$ |

Table 1: Linear and Parabolic Coefficients

- The activation values for parabolic coefficient are different for dry or wet oxidation
- The diffusion of $H_2O$ is lesser than oxygen in silicon dioxide
- The growth is faster in wet oxidation due to higher solid solubility of $H_2O$ despite the fact that diffusion of $H_2O$ is slower
- The activation values for linear coefficient are more or less the same for dry or wet oxidation
- The linear growth regime is kinetic limited. Hence the growth rates are almost the same in linear regime

**Slide #9**

# 3 Electrical Defects in the Silicon/Oxide System

1. There are four basic types of defects or charges that exist at the $Si/SiO_2$ interface as shown in Fig.11

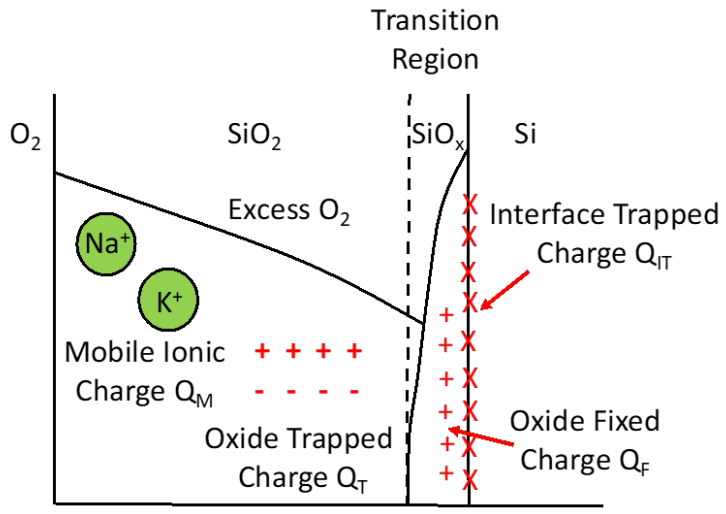


Figure 9: Various types of defects in silicon dioxide

2. **Fixed Oxide Charge $Q_f$:** A sheet of positive charge ($10^9 - 10^{11}\ cm^{-2}$) exists in the oxide very close to the interface and is attributed to partially oxidized silicon ($SiO_x$).

3. Variation of potential on the silicon surface has no impact on the fixed charge $Q_f$

4. $Q_f$ varies with process conditions. Oxidation at higher temperatures minimizes $Q_f$ due to faster kinetics which minimizes the partially oxidized silicon

5. Annealing in an inert ambient like $N_2$ or Ar drops the $Q_f$ to a low value

6. Equilibrium values for $Q_f$ after an $N_2$ anneal or Ar anneal are relatively independent of temperature

7. Annealing time for minimizing $Q_f$ depends on the temperature. Longer annealing time is required at lower temperatures

8. **Mobile Oxide charge $Q_m$:** Mobile oxide charge which may be located anywhere in the oxide. This is due to the presence of mobile ions like $Na^+$ and $K^+$ in the gate oxides

9. Even ppm of $Q_m$ due to $Na^+$ or $K^+$ can cause a shift in the threshold voltage $V_{TH}$ of the MOS devices

10. With proper cleaning procedure, these defects can be eliminated

11. **Oxide trapped Charge $Q_{ot}$:** This may be located anywhere in the oxide and is due to defects that are likely broken Si-O bonds in the bulk of the oxide, well away from the $Si/SiO_2$ interface

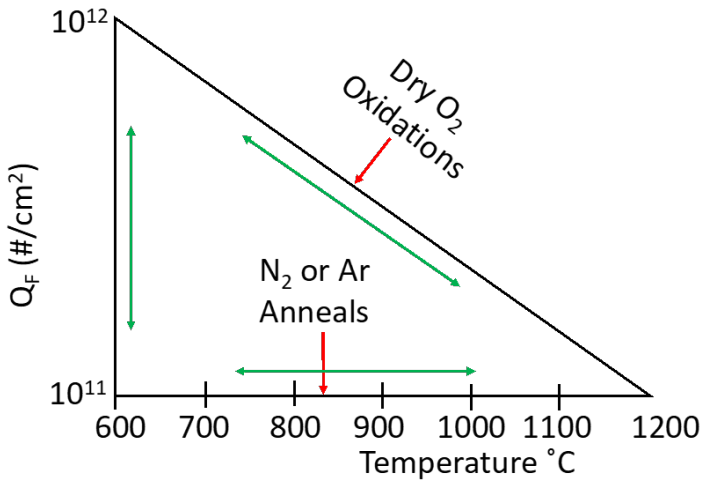


Figure 10: Fixed Charges and their behaviour as a function of temperature and annealing

12. These defects are normally repaired by a high temperature anneal before the fabrication is complete, which allows the broken bonds to repair themselves

13. If these defects are not repaired properly, these defects act as traps and can capture holes and electrons that may e injected into the oxide during device operation, resulting in trapped charge

14. The importance of oxide trapped charge $Q_{ot}$ increased with scaling of transistors. The high electric fields at lower nodes, result in more energetic or hot carriers that can achieve energies high enough to be injected into the gate oxides of the modern MOS devices.

15. If oxide traps are present or if they are created by the energetic carriers themselves, charge trapping can occur. This results in device threshold shifts with time and reliability concerns

16. **Interface trapped charge $Q_{it}$:** The second type of charged defect present near or at the $Si/SiO_2$ interface is the interface trapped charge $Q_{it}$

17. The origin is very similar to that of fixed charges. The key difference is that unlike fixed charge, the charge associated with $Q_{it}$ may be positive, neutral or negative. Moreover it may change during the normal device operation because of the capture of holes or electrons

18. These are often called fast states because of their ability to quickly trap holes or electrons

19. Energy levels associated with $Q_{it}$ exist through out the forbidden band, although there are more traps at energy levels near the conduction and valence edges than there are in the middle of the band gap.

20. Oxidizing a silicon surface usually results in a density of $Q_{it}$ of the order of $10^9 - 10^{11}\ cm^{-2}$

21. $Q_{it}$ can be passivated through hydrogen anneal at a fairly low temperatures (300 - 500 °C) whereas $Q_f$ is unaffected by such an anneal

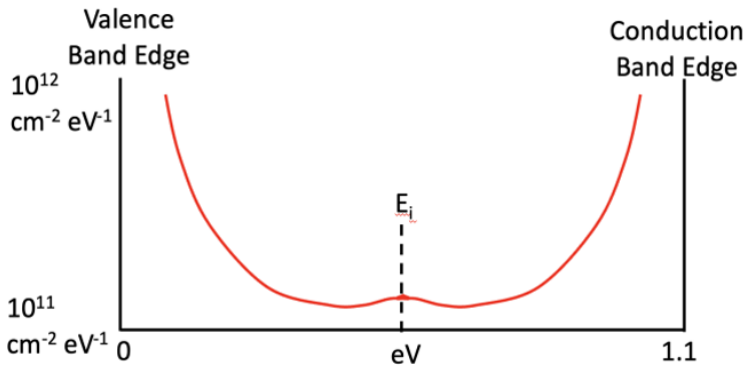


Figure 11: Interface trapped charge density

22. Once $Q_{it}$ traps are bonded with H atoms, they are no long electrically active and can no long act as trap carriers.

23. The mechanism of passivation is believed to be simply the diffusion of hydrogen through the $SiO_2$ layer to the $Si/SiO_2$ interface and reaction there to form Si-H bonds. Since the process takes place readily at temperatures that metal layers can tolerate, this "forming gas" anneal step is done at the end of a chip process

24. All the four types of defects can have deleterious effects on the device operation.

25. Great care is normally taken during fabrication to choose process sequence that will minimize these charges. Generally this is accomplished by high temperature inert anneals in Ar or $N_2$ in the process flow and by a moderate temperature (400 °C) anneal in $H_2$ or forming gas $N_2/H_2$ at the end of the process