Electrical Engineering
Indian Institute of Technology Hyd

CMOS VLSI Design

October 15, 2025

Deadline: 15 Oct 2025 | *Assignment # 5* | Maximum Marks: TBD

Instructions:

1. Use Cadence (with GPDK) for the simulations.

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1. Design a flip flop with
   - Static architecture
   - Dynamic architecture with transmission gates (ii) A Clock-Skew Insensitive Approach (iii) True Single-Phase Clocked Register (TSPCR)
2. Simulate and find delay time, setup time, and hold time for the architectures designed in Q1.
3. Design a shift register (8 bits) with the architectures designs in Q1.
4. Design a 8 bits (i) synchronous and (ii) asynchronous counters with the architectures designs in Q1. Find the maximum frequency of the counters designed.

Student's roll number: Ended here