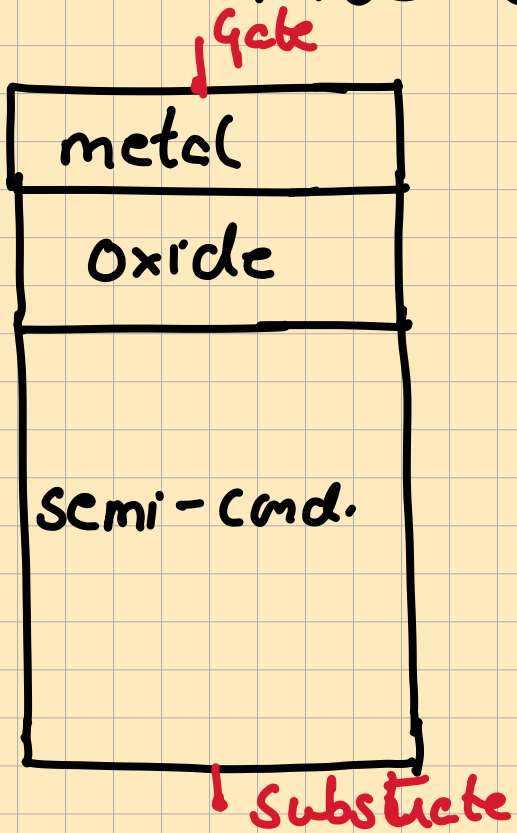
MOS Capacitor



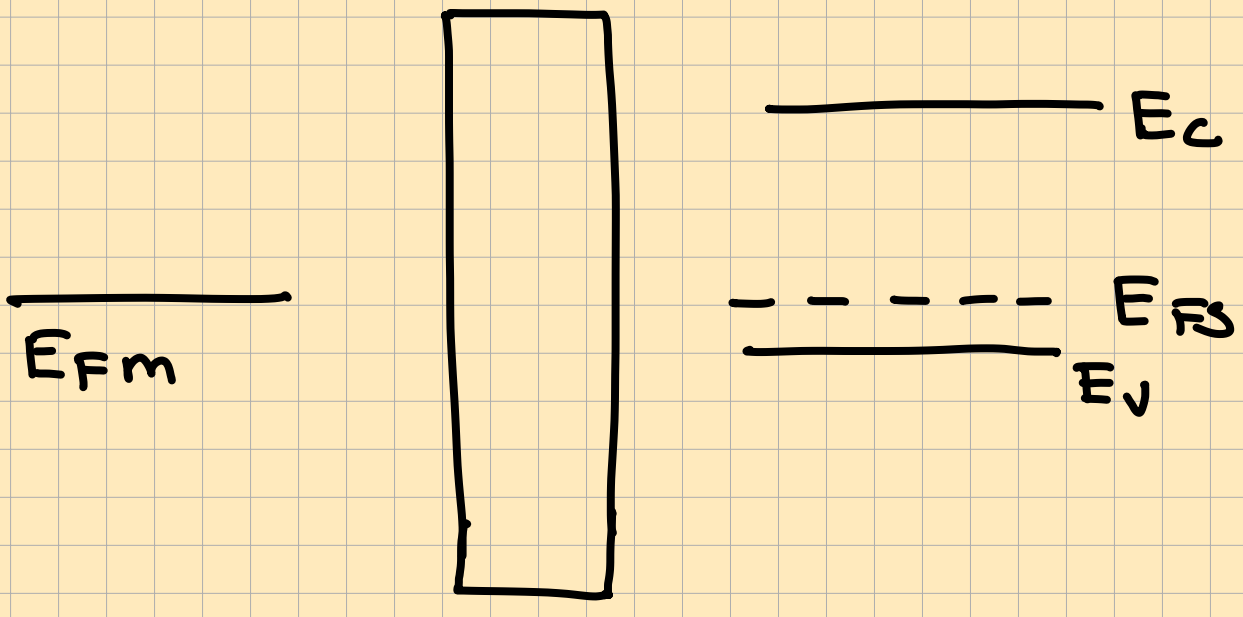
M

O

S (n-type / p-type)

M-O-S

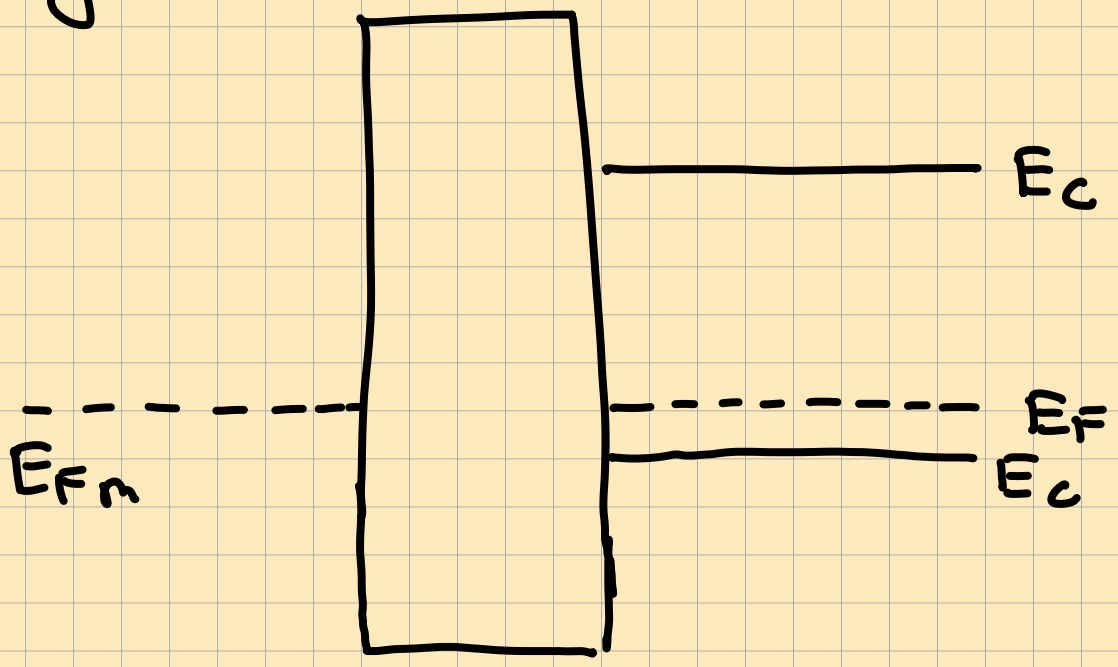
- p-type (n-MOS)
- n-type (p-MOS)



Assumption: $E_{Fm} = E_{FS}$

↳ ideal

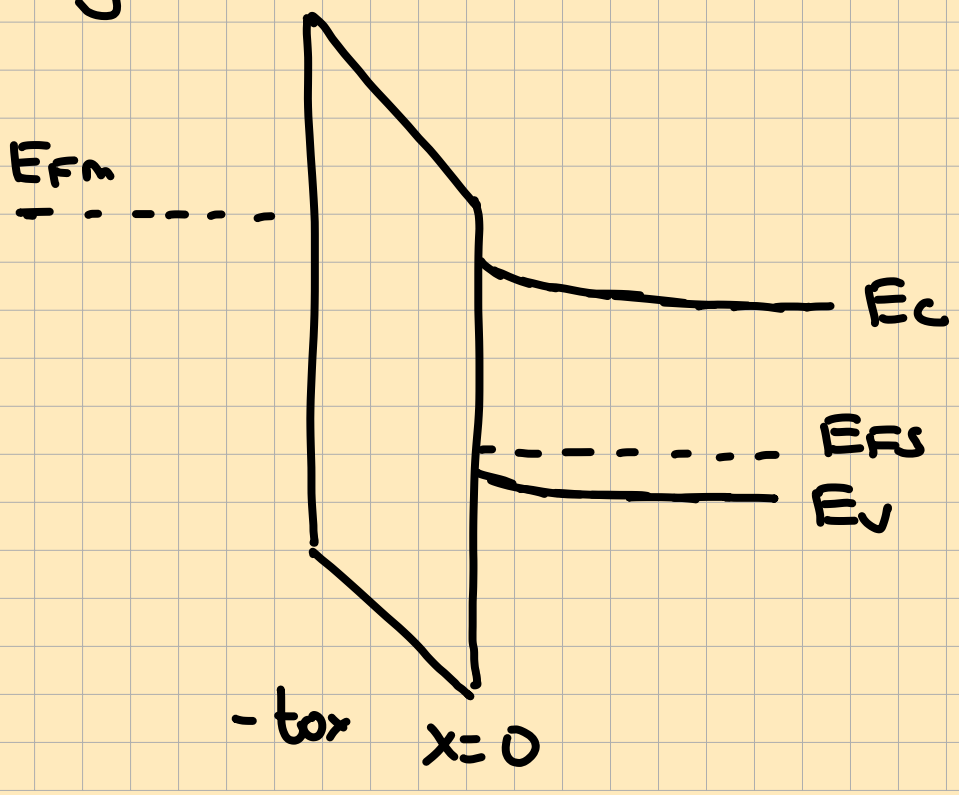
$V_g = 0$ Flat band condition



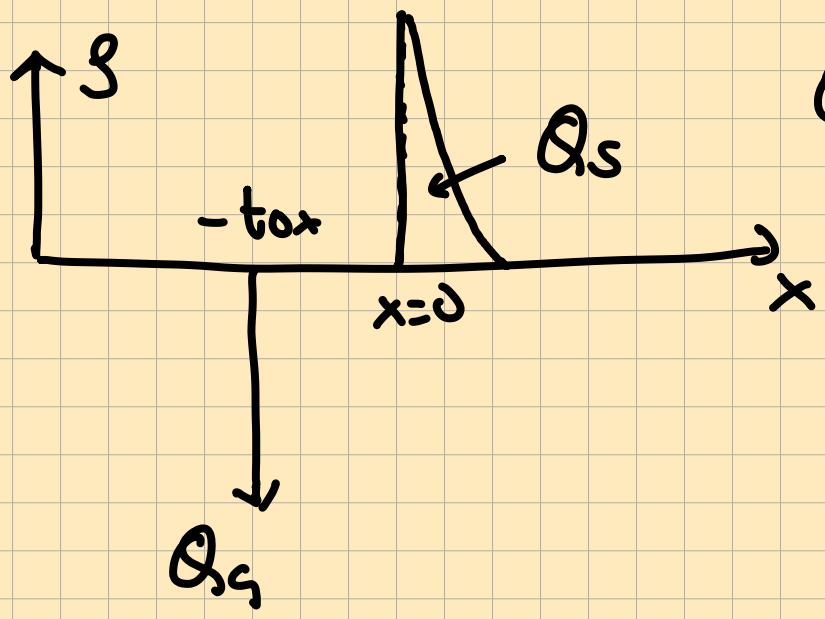
No electric field

No charges

$V_g < 0$ Accumulation

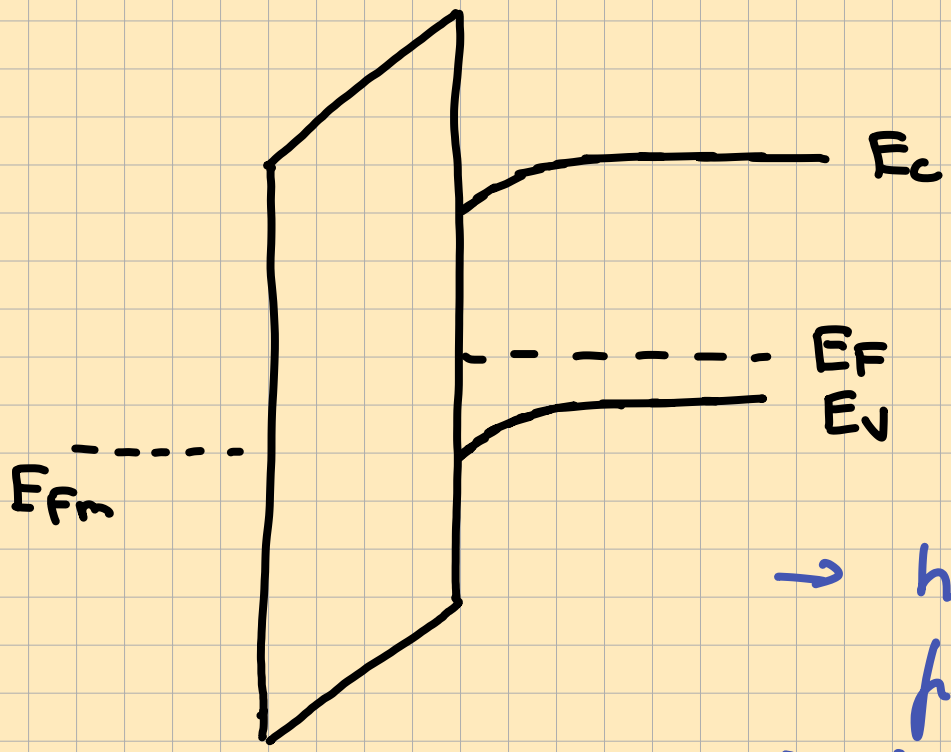


holes get accumulated at the oxide semiconductor interface



$Q_G = -Q_s$

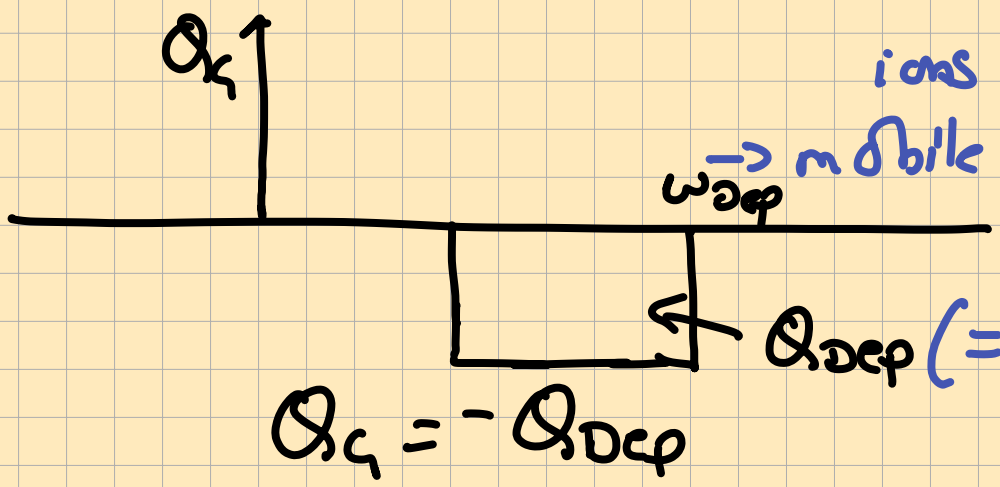
$V_g > 0$ & small Depletion region



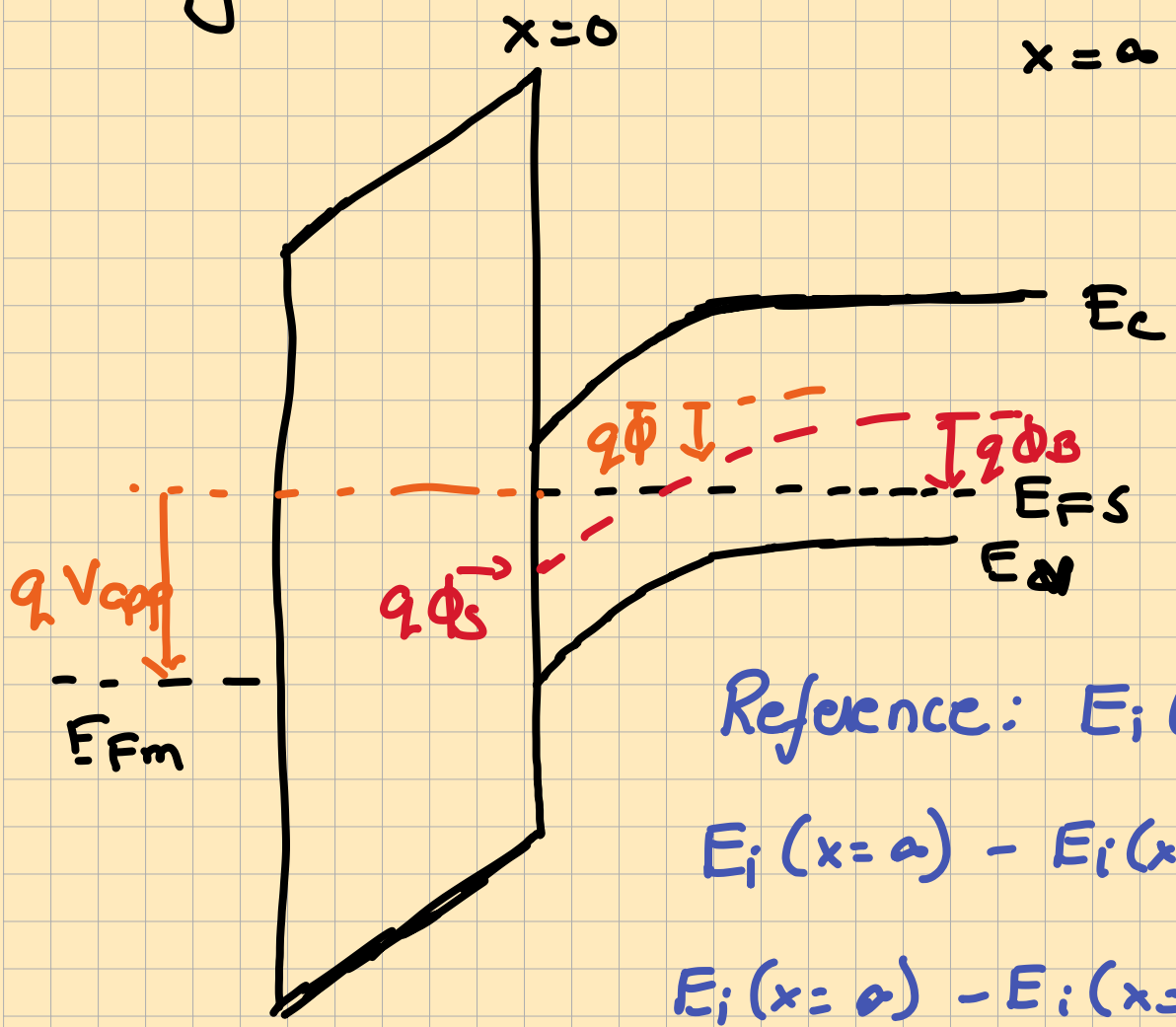
→ hole are repelled from interface

→ immobile acceptors ions

→ mobile carriers are small



$V_g > 0$



Reference: $E_i(x=a)$

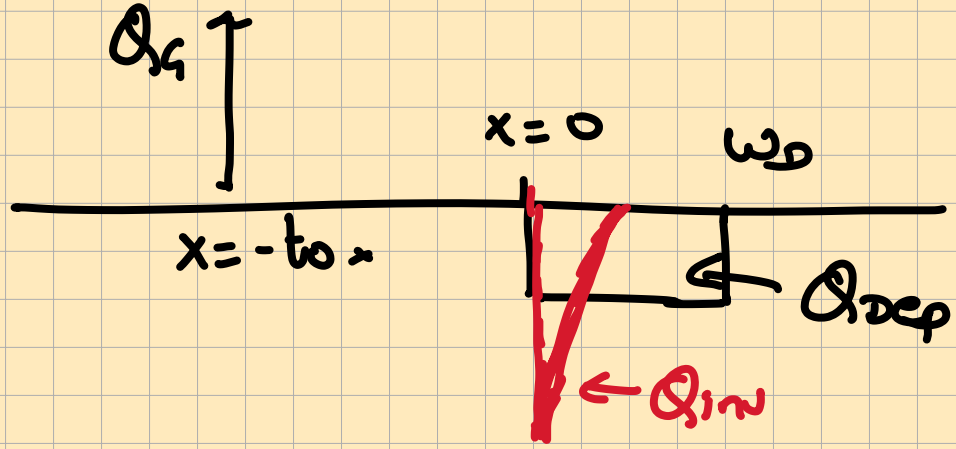
$E_i(x=a) - E_i(x) = q\phi$

$E_i(x=a) - E_i(x=0) = q\phi_s$

ϕ_s → Surface potential (bending downward is +ve)

$V_{app} = V_{ox} + \phi_s$

drop across oxide — drop across semiconductor



$$Q_G = -[Q_{Dep} + Q_{inv}]$$

$\phi_S = 2\phi_B$ $\quad n(x=0) = N_A$

→ Threshold voltage definition

i.e. the surface has inverted
→ become p-type

Q_{inv} → due to mobile electrons at the interface.

How does the charge in the semiconductor vary as a function of gate bias?

$$Q_S = \pm \frac{\sqrt{2}\, k_B T}{L_D\, q} \left[\left(\exp\left(-\frac{\phi_S}{V_T}\right) + \frac{\phi_S}{V_T} - 1 \right) + \frac{n_0}{p_0} \left(\exp\left(+\phi_S / V_T\right) - \frac{\phi_S}{V_T} - 1 \right) \right]^{1/2}$$

+ve → Accumulation

-ve → Depletion / Invasion.

L_D → Debye length

$p_0 = N_A \quad n_0 = \frac{n_i^2}{N_A}$

Accumulation → $\phi_s < 0$ → $\exp\left[-\phi_s/V_T\right]$ will dominate.

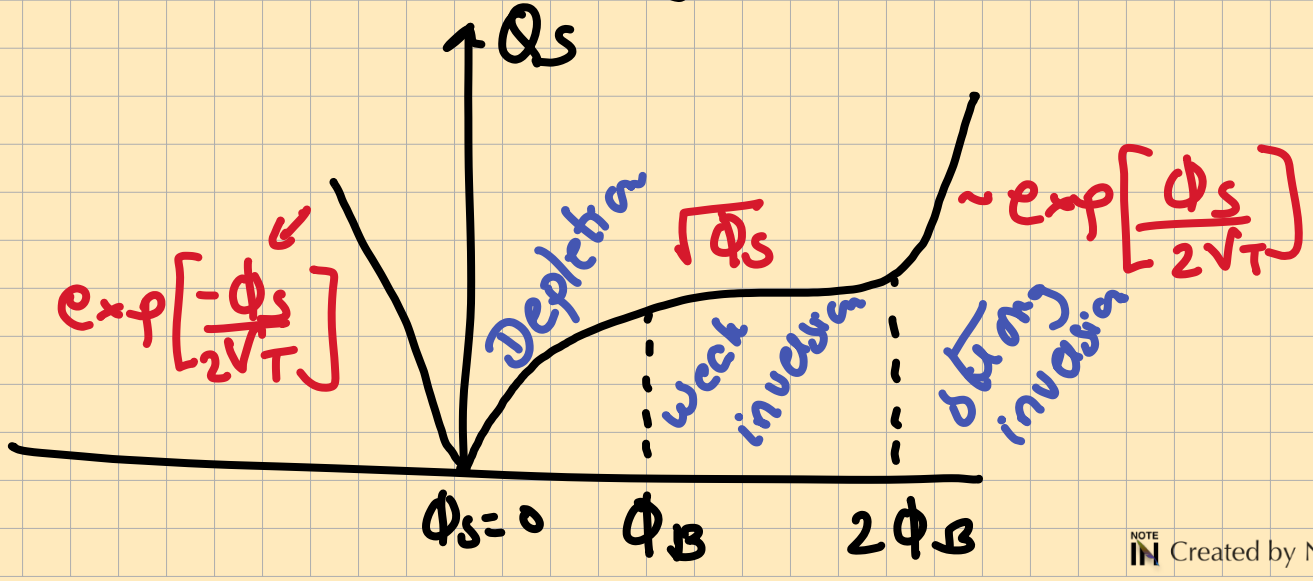
$Q_s \propto \exp\left[-\frac{\phi_s}{2V_T}\right]$

Depletion – $\phi_s > 0$ but not large enough to overcome $\frac{n_0}{p_0}$ term

thus $Q_s \propto \sqrt{\phi_s}$

Invasion → $\phi_s >> 0$ & $\exp\left[\frac{\phi_s}{V_T}\right]$ can compensate the n_0/p_0 term

$Q_s \propto \exp\left[\phi_s/2V_T\right]$



After strong inversion → further increase in gate bias leads to increase in mobile carriers & NOT in depletion charges

WHY ??

The depletion region width gets "pinned" to W_D at $\phi_S = 2\phi_B$

$$W_D = \sqrt{\frac{2\epsilon_{si}\phi_S}{qN_A}} \qquad W_{D,max} = W_D(\phi_S = 2\phi_B)$$

$$Q_D = -qN_A W_D = -\sqrt{2\epsilon_s qN_A \phi_S}$$

due to exponential increase in mobile carriers with ϕ_S → the surface potential gets also "pinned" to $2\phi_B$

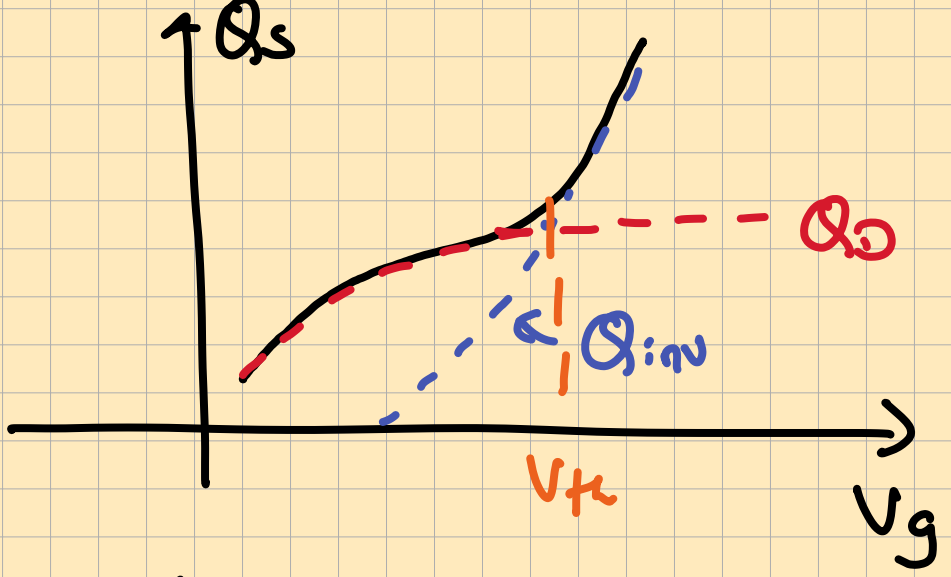
Relationship between V_G, ϕ_S & Q_S

$$V_G = V_{ox} + \phi_S$$

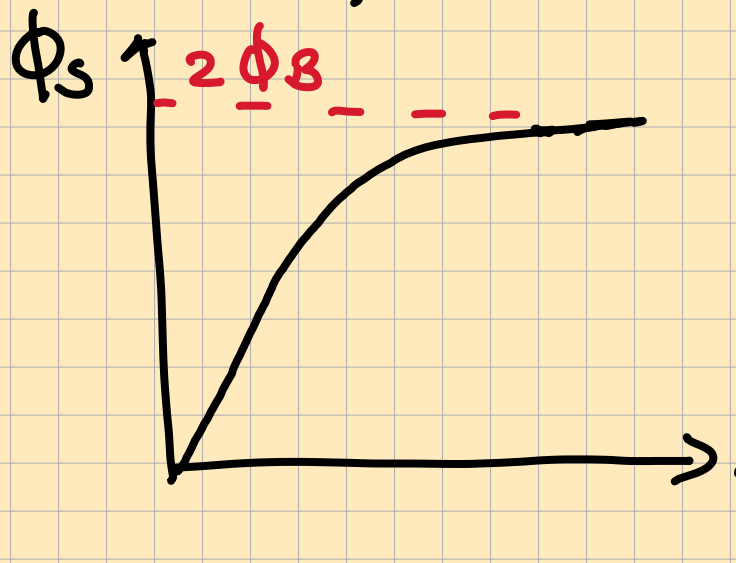
$$= \frac{Q_G}{C_{ox}} + \phi_S$$

$$= -\frac{Q_S}{C_{ox}} + \phi_S \quad - (1)$$

Numerically we can solve ① along with $Q_s - \phi_s$ to eliminate ϕ_s to get a relationship between Q_s & V_g



We can also use a similar process to write a relationship between V_g & ϕ_s

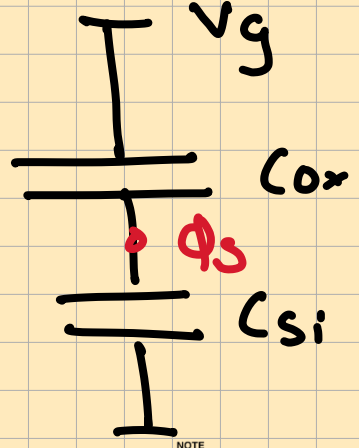


Mos Capacitance.

$$V_g = V_{ox} + \phi_s$$

$$= \frac{-Q_s}{C_{ox}} + \phi_s$$

$$\frac{dV_g}{d(-Q_s)} = \frac{1}{C_{ox}} + \frac{d\phi_s}{d(-Q_s)}$$



$$\frac{1}{C_{net}} = \frac{1}{C_{ox}} + \frac{1}{C_{Si}}$$

Accumulation : $\frac{1}{C_{net}} \approx \frac{1}{C_{ox}}$

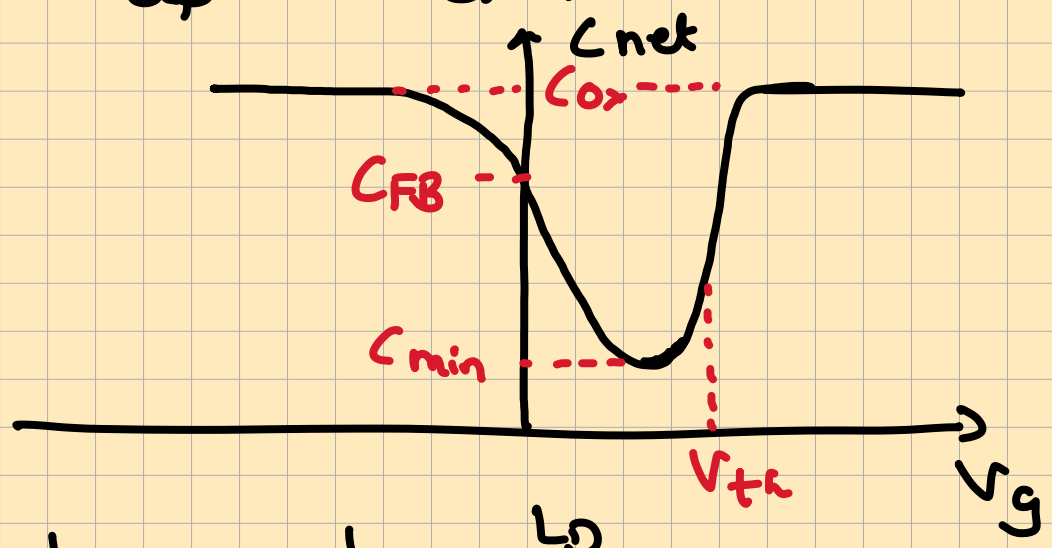
↳ Oxide - semiconductor interface acts as "metal" plate due to accumulation of hole.

Flat band: $\frac{1}{C_{net}} = \frac{1}{C_{ox}} + \frac{L_D}{\epsilon_{Si}}$

Depletion : $\frac{1}{C_{net}} = \frac{1}{C_{ox}} + \frac{W_{Dep}}{\epsilon_{Si}}$

$\frac{\epsilon_{Si}}{W_{Dep}} \Rightarrow C_{Dep}$

C_{Dep} would be smallest when $W_{Dep} \rightarrow W_{D,max}$



$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{L_D}{\epsilon_{Si}}$$

$$\frac{1}{C_{min}} = \frac{1}{C_{ox}} + \frac{1}{C_{DEP}}$$

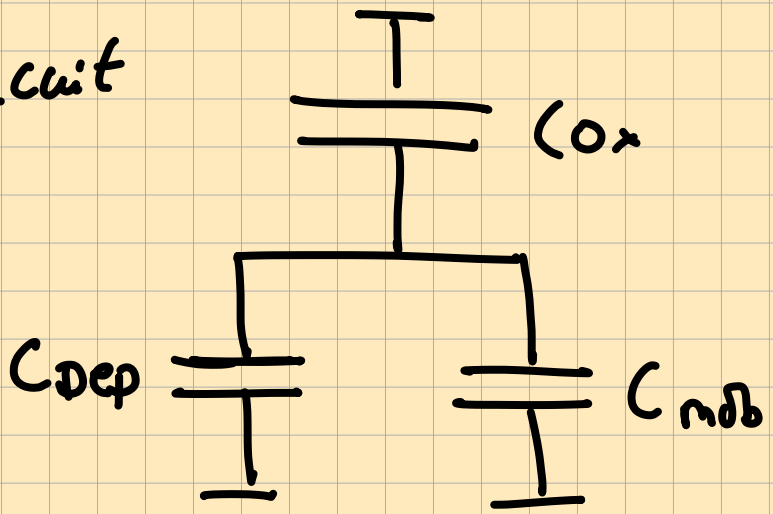
$$\frac{1}{C_{acc}} = \frac{1}{C_{ox}} + \frac{1}{C_{mob}}$$

C_{Si} is very large $\rightarrow C_{acc} \approx C_{ox}$

$$\frac{1}{C_{inv}} = \frac{1}{C_{ox}} + \frac{1}{C_{mob}}$$

C_{Si} is very large $\rightarrow C_{inv} \approx C_{ox}$

Equivalent Circuit



C_{mob} is the capacitance due to the presence of mobile carriers (in accumulation & inversion)

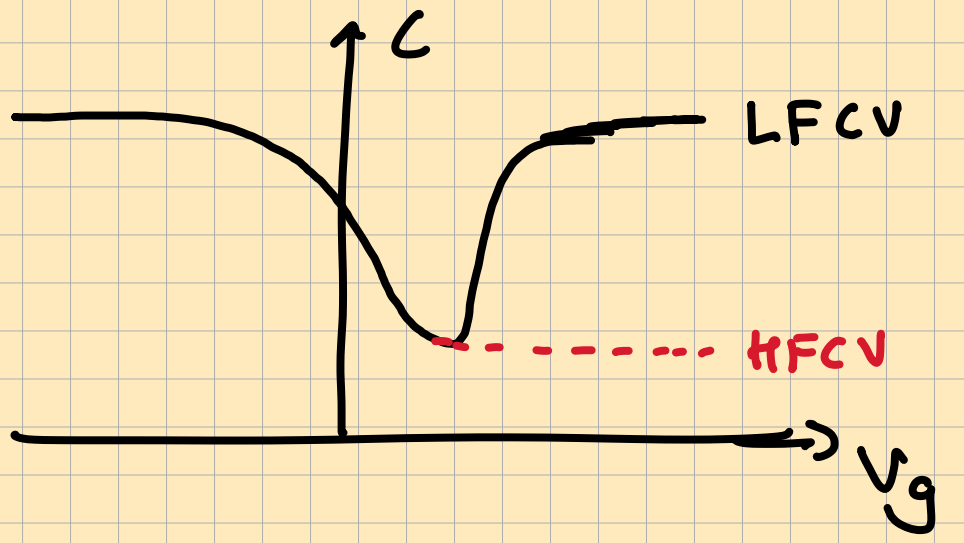
→ We have assumed that the carriers are able to respond to the change in bias

Recall : $C = \frac{\Delta Q}{\Delta V}$

But what if the carriers are not able to respond (i.e. generate / recombine)

Why is this important

↳ What is the source of the carriers (Generation near the oxide-semiconductor interface)



→ Note that the majority carriers are able to respond to the high frequency.

→ The minority carriers respond on the timescale of generation time (for silicon ~ 10^{-7} - 10^{-6} s)

→ Majority carriers respond on the timescale of dielectric relaxation time ($\tau_D = \rho\epsilon$)

Non ideal MOSFET

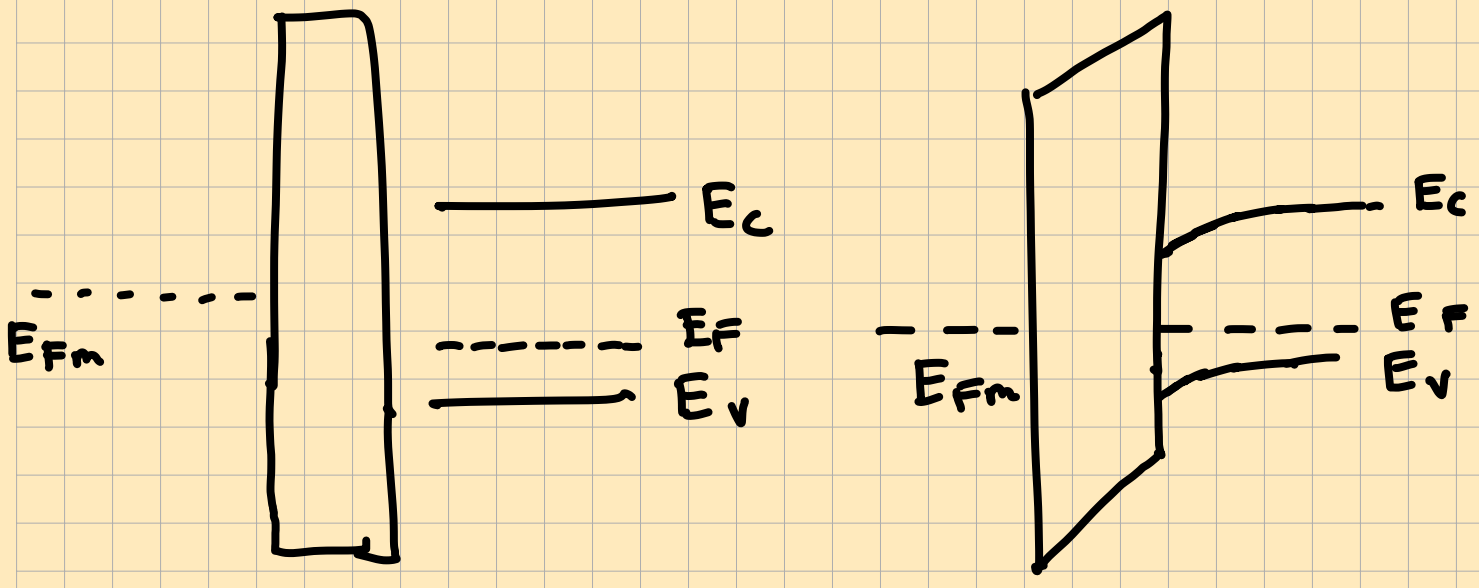
→ $E_{Fm} \neq E_{FS}$

→ Presence of oxide charges

→ Traps [We will not discuss it as a part of this course]

Case 1 $E_{Fm} < E_{FS}$ $\phi_{ms} < 0$

$$q\phi_m - q\phi_s < 0$$



$$\phi_m - \phi_s = \phi_{ms} < 0$$

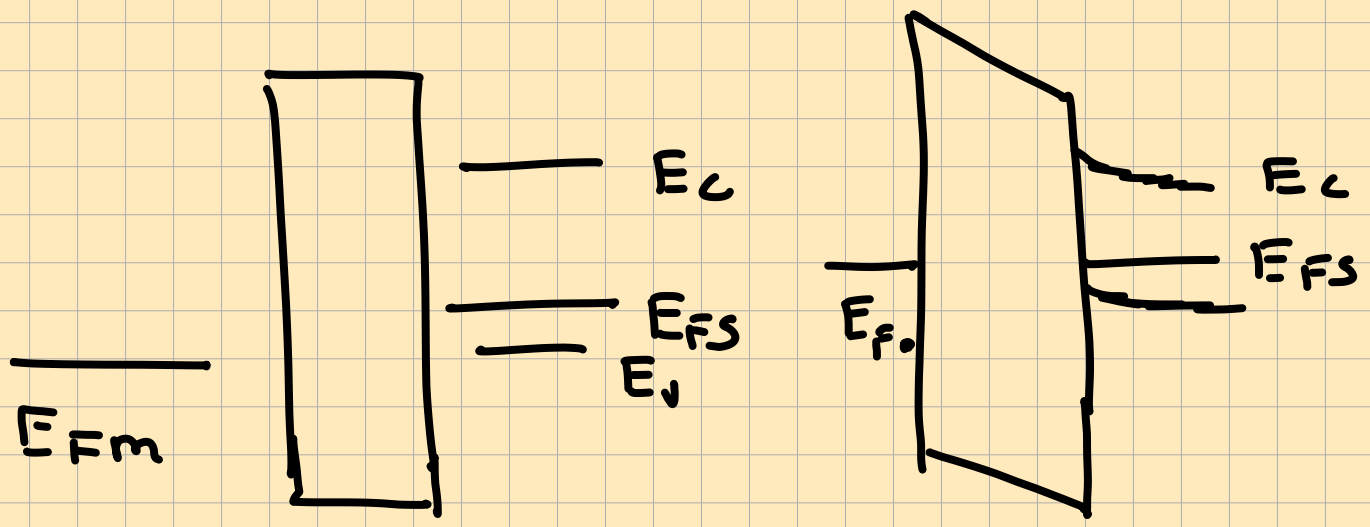
$V_g = 0$ the device is already in depletion

$$V_{th} - \phi_{ms} = 2\phi_B - \frac{Q_{Dep}}{C_{ox}}$$

$$V_{th} = 2\phi_B - \frac{Q_{Dep}}{C_{ox}} + \phi_{ms}$$

Case 2

$E_{Fm} > E_{FS}$



$\phi_{ms} > 0$

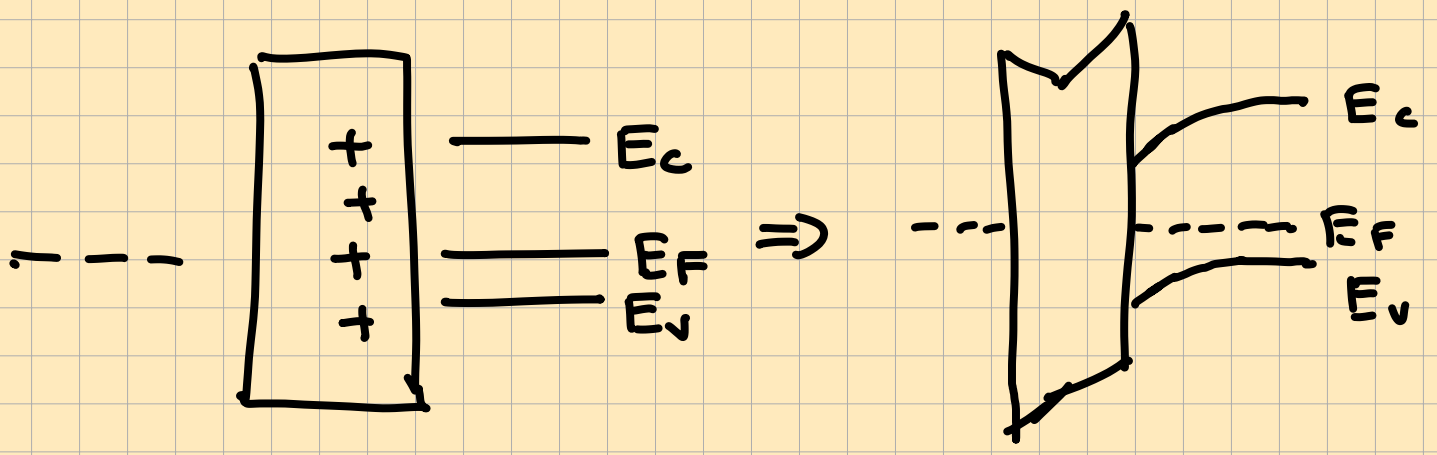
Here we see that the bands are bending as if the device is in accumulation at $V_g = 0$ so we have to apply an additional bias of ϕ_{ms} on gate to get it into flat band

$$V_{th} - \phi_{ms} = 2\phi_B - Q_D/C_{ox}$$

$$V_{th} = 2\phi_B - Q_D/C_{ox} + \phi_{ms}$$

Case 3 : Charges at the oxide semiconductor interface

$$\phi_m = \phi_s$$



$$V_{th} = \phi_{ms} - \frac{Q_{Dep}}{C_{ox}}$$

$$V_m - \frac{Q_G}{C_{ox}} = \phi_{ms} - \frac{Q_D}{C_{ox}}$$

$$Q_G = -Q_{ox}$$

$$V_{th} = \phi_{ms} - \frac{Q_D}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

Impact of nonidealities

$$V_{th} = \phi_{ms} - \frac{Q_D}{C_{ox}} - \underbrace{\frac{Q_{ox}}{C_{ox}} + \phi_{ms}}_{V_{fb}}$$

The threshold voltage shifts by

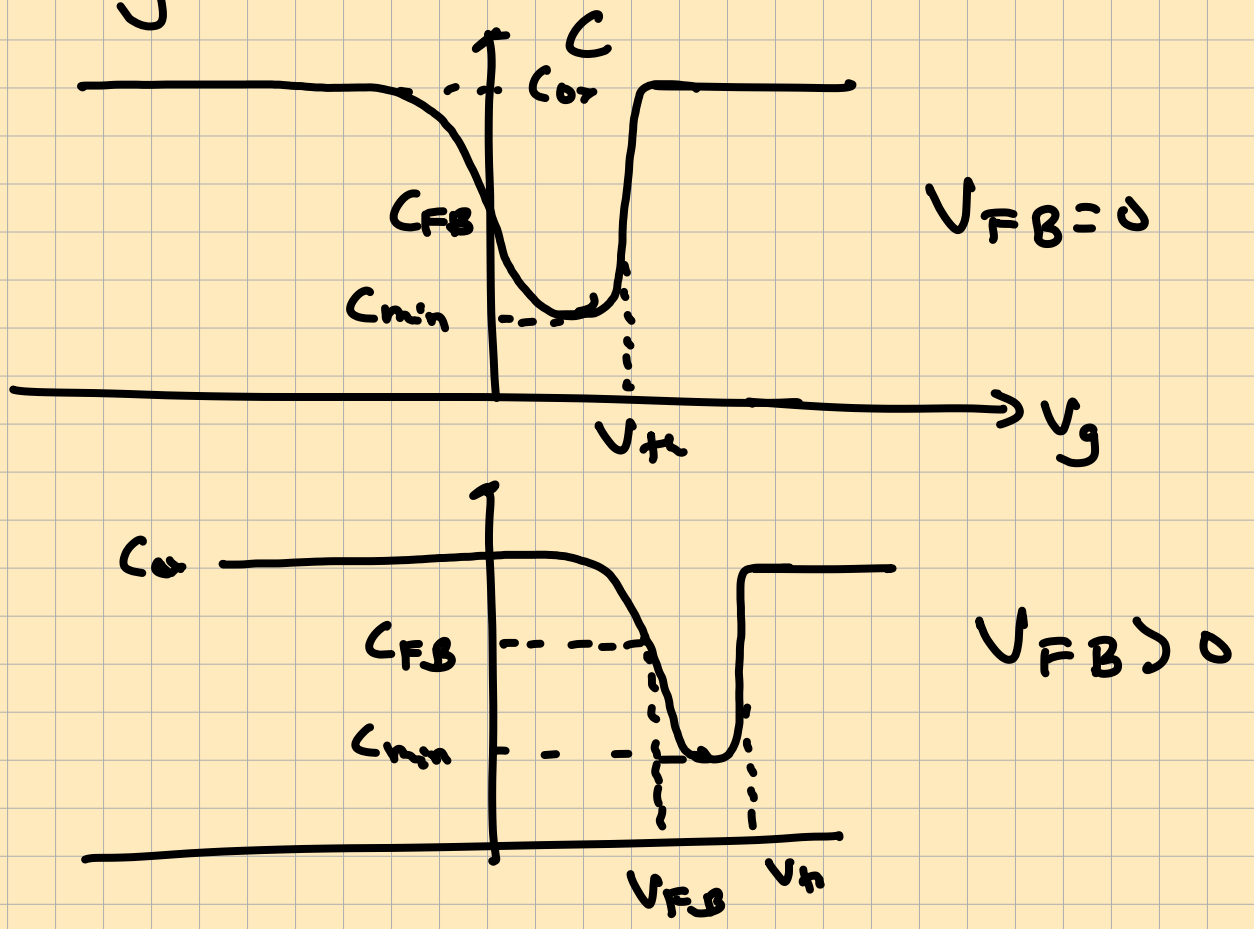
$$-\frac{Q_{ox}}{C_{ox}} + \phi_{ms} \equiv V_{FB}$$

What does it mean for $Q - \phi_s$ relationship

- NOTHING → WHY

$Q - V_g$ & $\phi_s - V_g$ they will shift to the right (if $V_{FB} < 0$) or left (if $V_{FB} > 0$)

C - V_g curve



In general the oxide charges need not lie at the oxide-semiconductor interface but are distributed throughout the oxide

(NOT PART OF THE COURSE)

↳ A more general expression to the shift in the threshold voltage can then be calculated (Refer: Fundamentals of modern VLSI Devices)