

The diagram illustrates a digital signal processing system for a 10-bit DAC. The main components and their connections are as follows:

- Prescaler (1MHz):** Receives `rst_n` and `clk50m`. Its output `en50_1m` is connected to the `en` input of the **prescaler adj** block.
- prescaler adj:** Receives `rst_n`, `clk50m`, and `en50_1m`. It has a `cnt[7:0]` output connected to the `cnt` input of the **counter up** block. It also has a `preval[7:0]` input connected to the `cnt` output of the **counter updn** block.
- counter up (10bit):** Receives `rst_n`, `clk50m`, and `en`. It has a `cnt[9:0]` output connected to the `address` input of the **memory** block.
- memory (16bit data, 10bit address):** Receives `address[9:0]` and `clock`. It has a `g[15:0]` output connected to the `din` input of the **DS DAC** block.
- DS DAC (16 bit):** Receives `clk`, `rst_n`, and `din[15:0]`. It has a `ce_out` output connected to the `ce` input of the **PWM DAC** block.
- PWM DAC (16 bit):** Receives `clk`, `rst_n`, and `ce`. It has a `dout` output.
- counter updn (8bit):** Receives `rst_n`, `clk50m`, and `en`. It has a `cnt[7:0]` output connected to the `preval` input of the **prescaler adj** block.
- comparator and multiplexer blocks:** There are two **compare** blocks and two **10bit** multiplexer blocks. The multiplexers receive `rst_n`, `clk50m`, and `sw` inputs. They have `sw_hi` and `sw_lo` inputs connected to the `sw` input of the **debounce** blocks. The comparators receive `bin[3:0]` and `hexn[6:0]` inputs connected to the `bin` and `hexn` inputs of the **sevensseg** block.

A green sine wave is shown at the bottom right, representing the output signal.

Projekt  
**DSM DAC**  
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