CSE/EEE 120

Lab 3 Answer Sheet

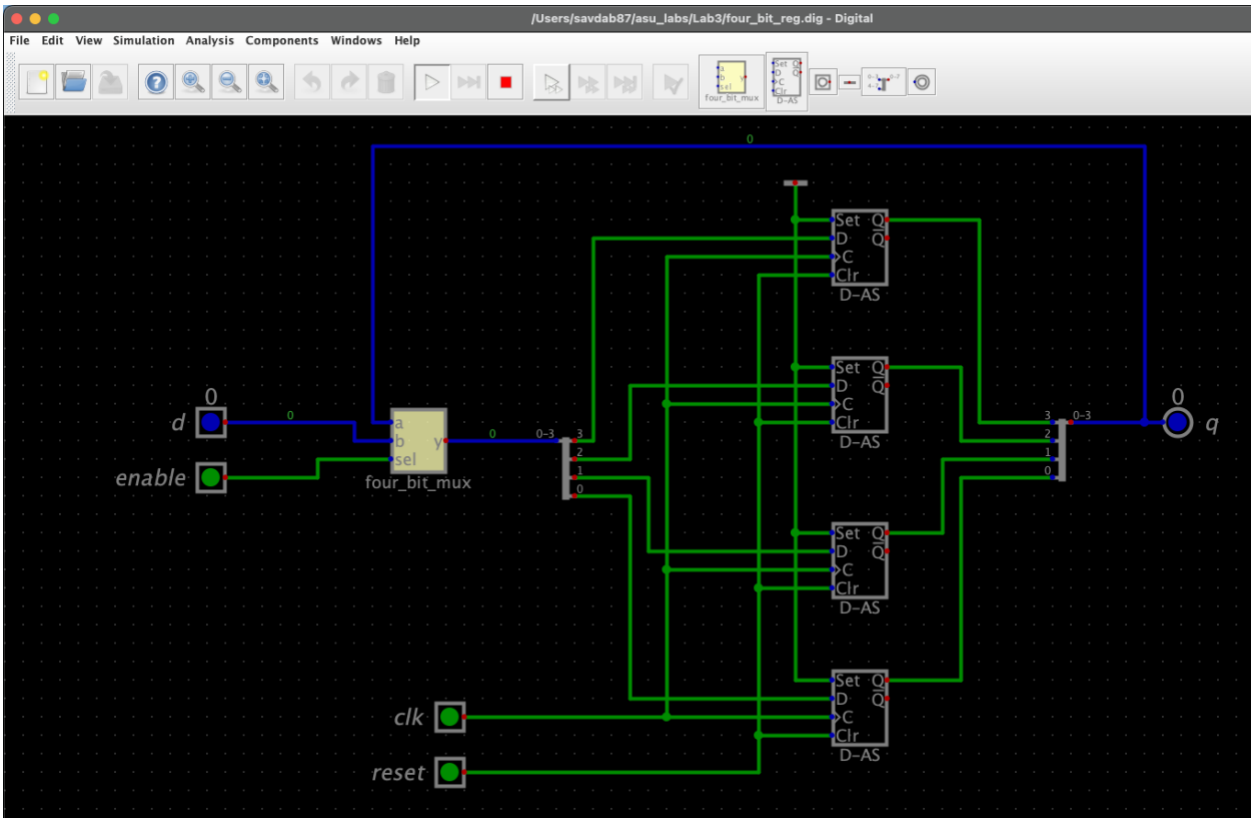
Registers, Counters and the “Brainless CPU”

Name: _Patrick Nelson_____

Date: 02/09/25

Task 3-1: Build and Test a 4-Bit D Register with Enable

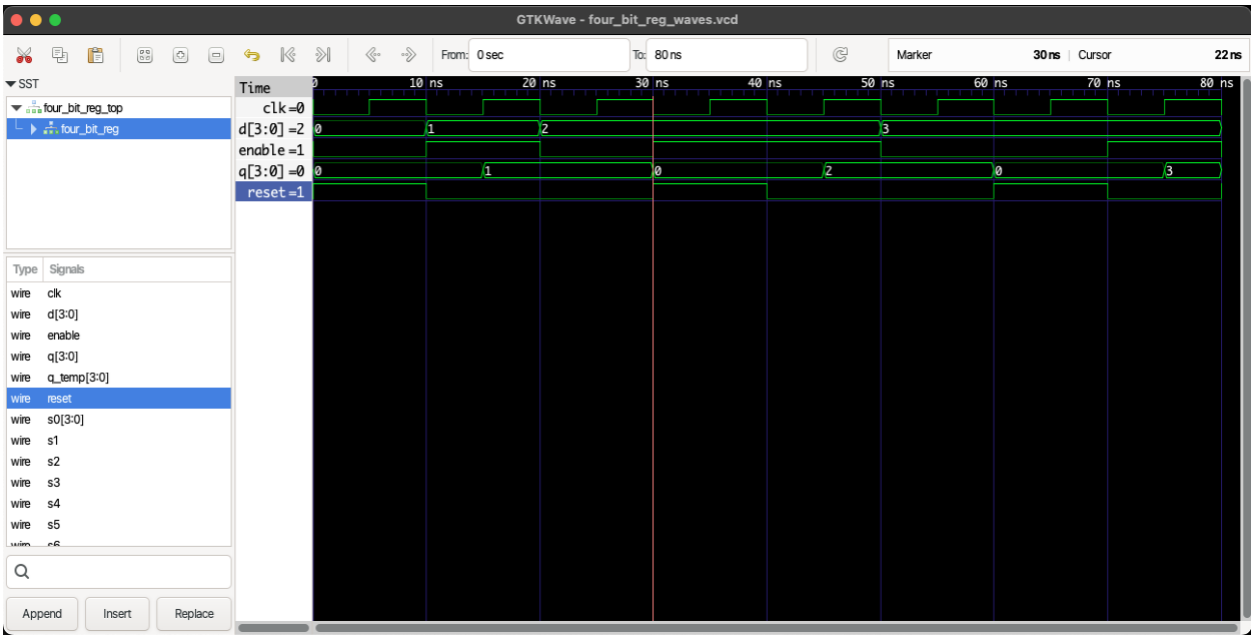
Include a picture of your Digital circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

No major issues were faced when designing this circuit.

Include a picture of your GTKWave waveforms (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

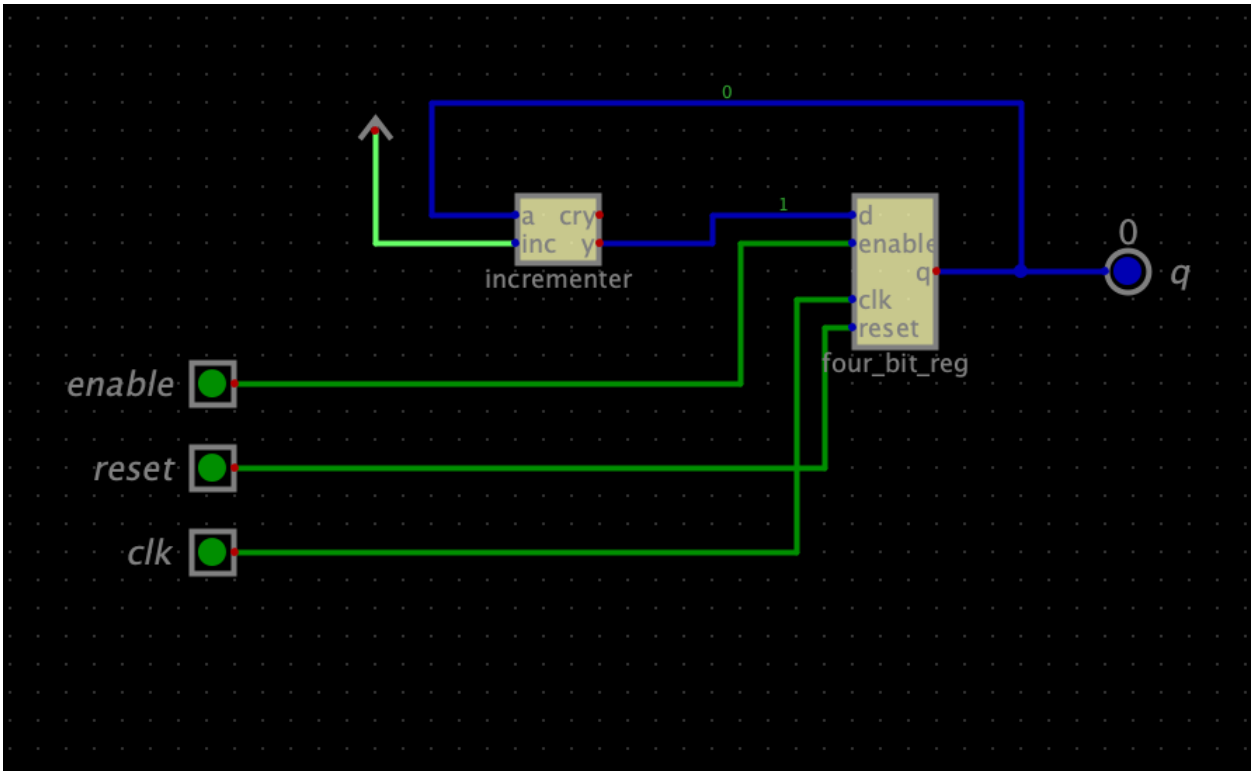
The circuit behaved as expected, although it took some trial and error to insure my test cases were accurate in lieu of the clock changes.

Please comment on the single biggest issue you were facing when simulating the circuit.

My understanding of how the four bit register should work was the only impediment I encountered when writing the simulation cases.

Task 3-2: Build and Test a 4-Bit UP Counter

Include a picture of your Digital circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

No issues when designing this circuit.

Did the circuit behave as expected? If no, what was wrong?

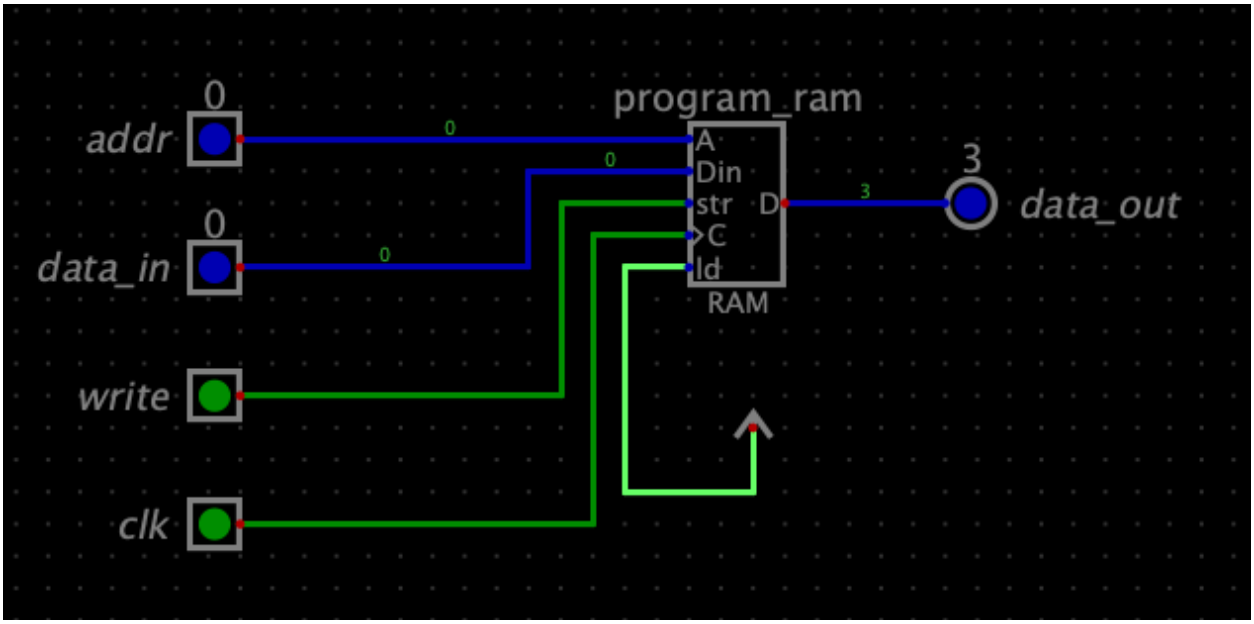
This circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

No issues were encountered when verifying the circuit behaved as expected. The lab did not include Verilog tests for this, so I manually tested increment worked as expected when enabled. Reset and clock also performed their function.

Task 3-3: Create a 4-Bit RAM with 16 4-Bit Words

Include a picture of your Digital circuit here:



Please comment on the single biggest issue you were facing when designing the circuit.

No issues designing this circuit.

Did the circuit behave as expected? If no, what was wrong?

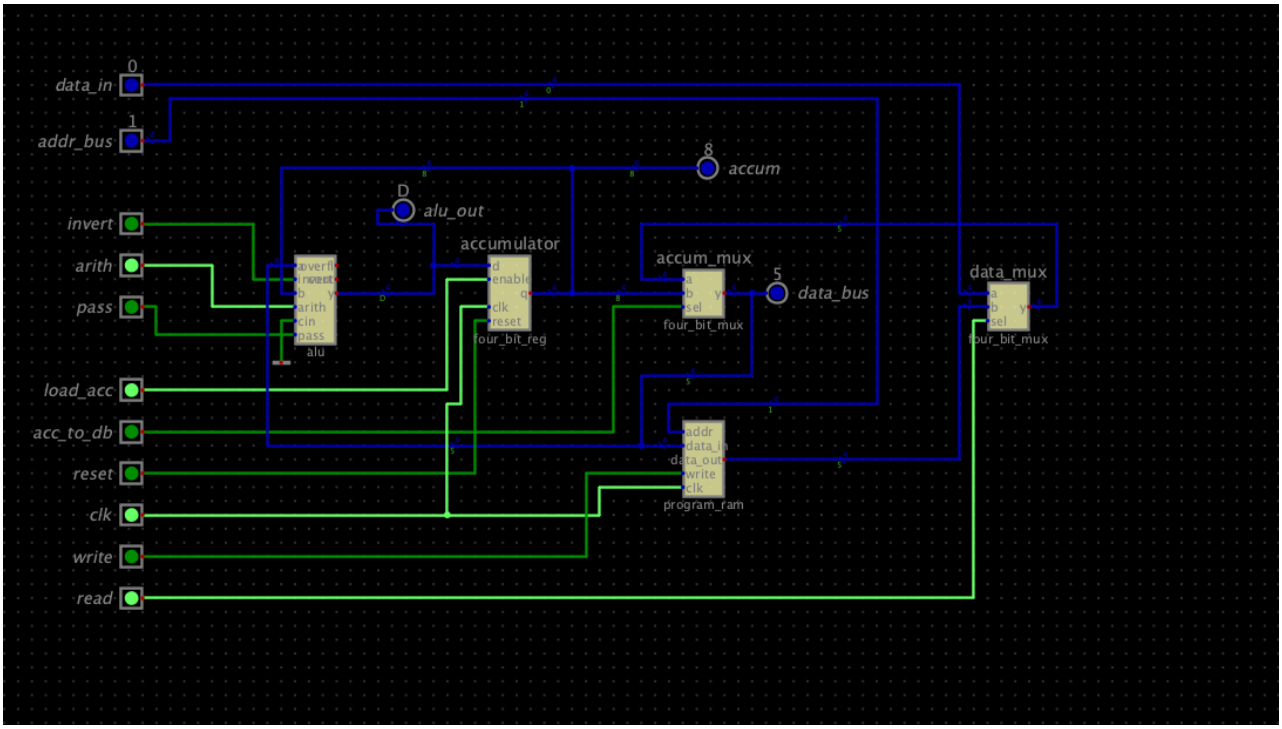
Yes it behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

No issues were encountered simulating this circuit. I was able to add the file to pre-load memory, increment the address, and verify write and clock are functional.

Task 3-4: Build and Test the Brainless Central Processing Unit

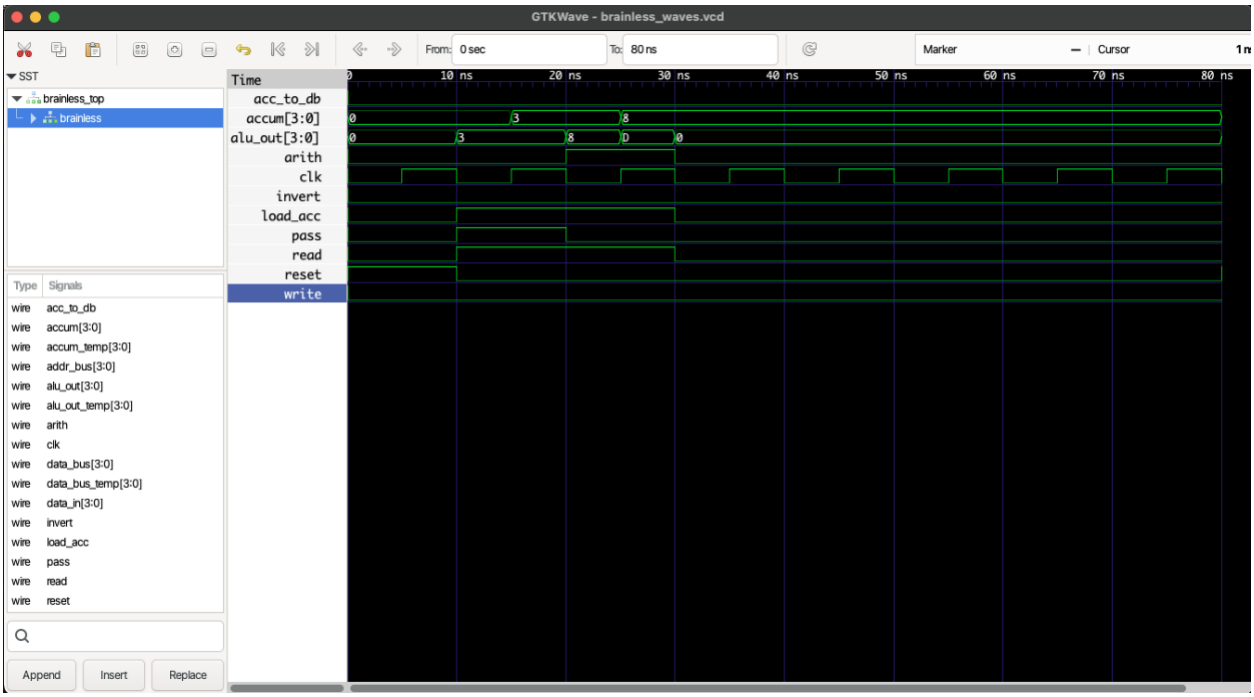
Include a picture of your Digital circuit here:



No issues were encountered when designing this circuit.

Task 3-5: Simulate the Brainless Central Processing Unit

Include a picture of your GTKWave waveforms (timing diagram) here:



Did the circuit behave as expected? If no, what was wrong?

I believe the circuit behaved as expected. I was able to follow the steps provided to add the values and the waveform reflected the expected output in this case.

Please comment on the single biggest issue you were facing when simulating the circuit.

No issues were faced while simulating this circuit.

Task 3-6: Create Additional Tests

As shown in the manual, paste the test_vals you used for each of the tests here. Be sure to note which each set of test_vals goes with each test.

If you changed your circuit since you took the screenshot for Task 3-4, take another and replace the screenshot in Task 3-4.

Include a picture of your GTKWave waveforms here (one per required test):

Brainless_ext_write

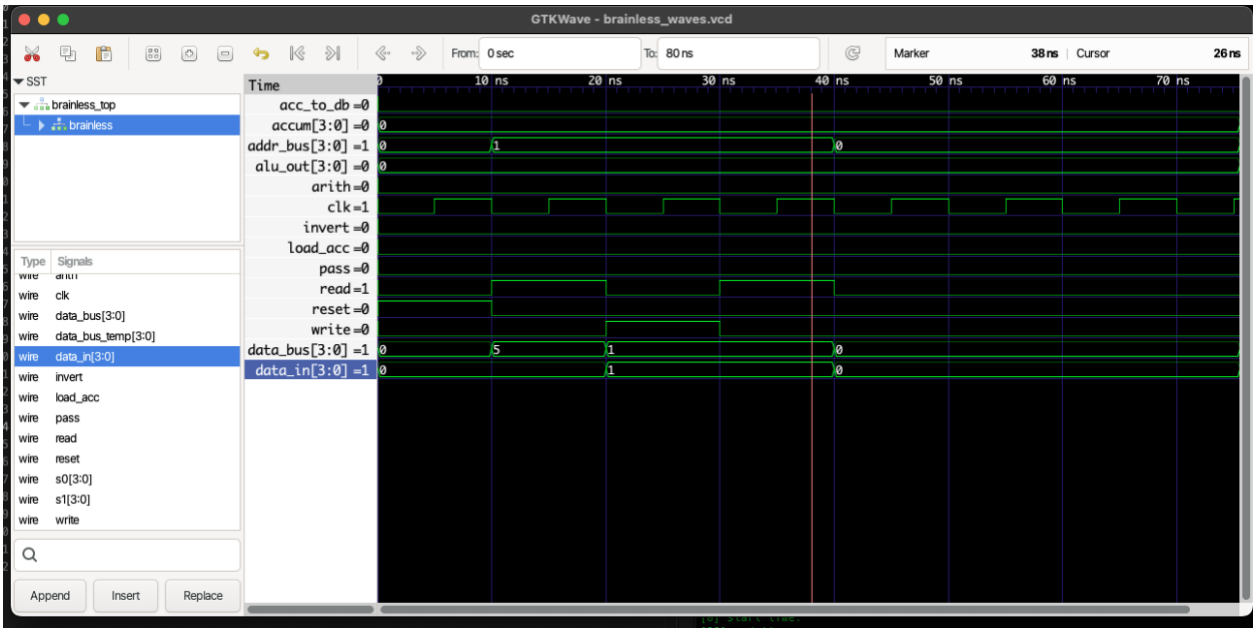


Figure 1 brainless_ext_write.v

```
test_vals[0] = 28'h0_0_0_0_0_0_4;    // reset this should always be the vector
test_vals[1] = 28'h0_5_0_0_1_0_1;    // read addr 1, expect 5
test_vals[2] = 28'h0_1_0_1_1_0_2;    // write 1 to addr 1
test_vals[3] = 28'h0_1_0_1_1_0_1;    // read addr 1, expect 1
test_vals[4] = 28'h0_0_0_0_0_0_0;
test_vals[5] = 28'h0_0_0_0_0_0_0;
test_vals[6] = 28'h0_0_0_0_0_0_0;
test_vals[7] = 28'h0_0_0_0_0_0_0;
```

Brainless_int_write

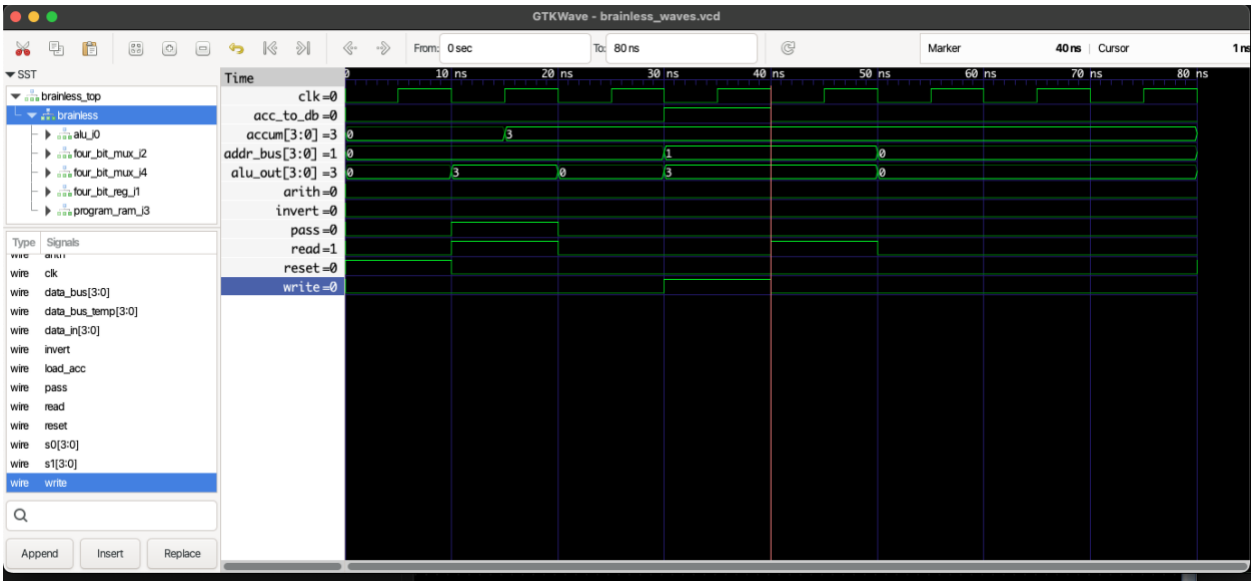


Figure 2 brainless_int_write

```
test_vals[0] = 28'h0_0_0_0_0_0_4;    // reset - this should always be the first vector
  test_vals[1] = 28'h3_3_3_0_0_3_1;    // get 3 into the accumulator
  test_vals[2] = 28'h3_0_0_0_0_0_0;    // leave 3 in accumulator
  test_vals[3] = 28'h3_3_3_0_1_0_A;    // acc_to_db ON, write 3 to the addr 1, expect 3
  test_vals[4] = 28'h3_3_3_0_1_0_1;    // read addr 1, expect 3
  test_vals[5] = 28'h3_0_0_0_0_0_0;
  test_vals[6] = 28'h3_0_0_0_0_0_0;
  test_vals[7] = 28'h3_0_0_0_0_0_0;
```

Brainless_alt_tests

I tested adding an external value with an internal value, and storing the result to a new address in memory

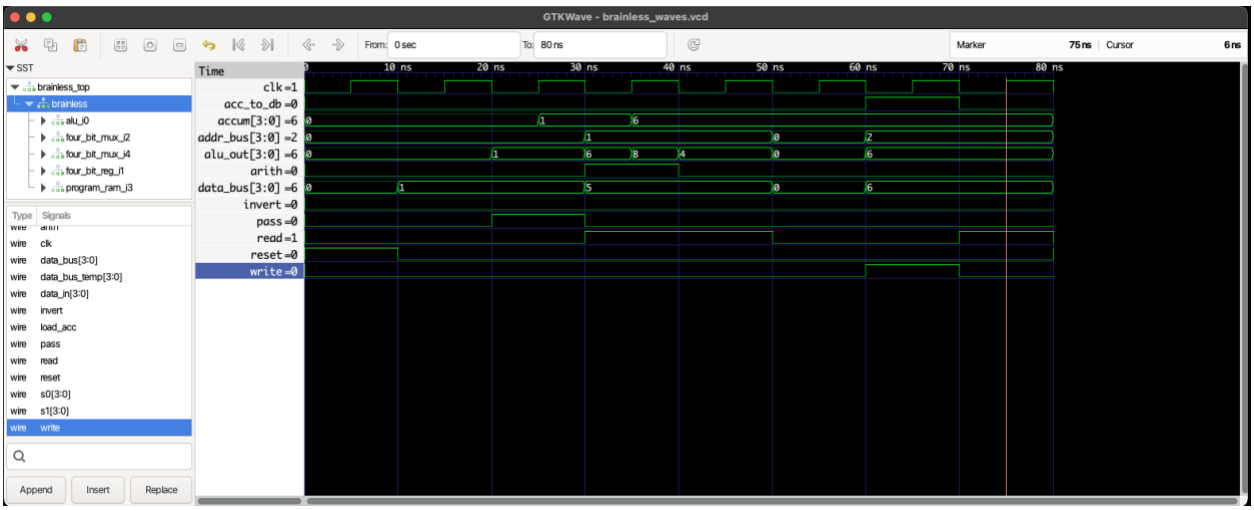


Figure 3 brainless_alt_tests.v

```
test_vals[0] = 28'h0_0_0_0_0_0_4;    // reset - this should always be the first vector
  test_vals[1] = 28'h0_1_0_1_0_0_0;    // get 1 into data bus
  test_vals[2] = 28'h1_1_1_1_0_3_0;    // pass 1 to accumulator
  test_vals[3] = 28'h6_5_B_1_1_5_1;    // add 5 and 1, load accumulator
  test_vals[4] = 28'h6_5_4_1_1_0_1;
  test_vals[5] = 28'h6_0_0_0_0_0_0;    // leave result in accumulator
  test_vals[6] = 28'h6_6_6_0_2_0_A;    // write to addr 2
  test_vals[7] = 28'h6_6_6_0_2_0_1;    // read addr 2 get 6
```

Please comment on the single biggest issue you were facing when designing the circuit.

I didn’t encounter any major issues when designing the circuit.

Did the circuit behave as expected? If no, what was wrong?

Yes as far as I can tell, the circuit is exhibiting expected behavior.

Please comment on the single biggest issue you were facing when simulating the circuit.

I think understanding the timing of the clock was difficult when writing my tests. I knew the steps but needed to break them down into smaller steps when writing the tests in Verilog.

Task 3-7: Create a video and submit your report (Optional)

[For students to learn how to present their work] Record a short video showing your schematics in Digital and your waveforms in GTKWave. Be sure to show yourself in the video and show your screen. Explain how your circuit works – you need to convince the grader you did the lab and understand it! **Copy and paste the link to your video below. Make sure the link is working and pointing to the correct video. Remember to include the password if required. Do NOT upload your video to Canvas. It is recommended that you use Zoom to record to the cloud, pasting the link and password below.** If your circuit is not working as expected, explain in the video how it is not working and why you think it is not working.

Video Link:

At the beginning of your recording, say your name and the lab name. Be brief in your recording. Submit the completed template to Canvas.

Make sure all your files are in the Lab3 directory. Create a zip file of the Lab3 directory. Remember to turn in the zip file and your completed template on Canvas!

Do not include the video in the zip file! This makes the file very large and you run the risk of the zip file not uploading or taking so long to upload that your submission will be late. Remember that the submission is dated at the time the upload completes, not when it starts!

LAB 3: LAB REPORT GRADE SHEET

Name _____

NOTE: You submit the zip file in order to show your work.
If the zip file is not submitted you will receive a 0 for this lab!

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 3-1: Build and Test a 4-Bit D Register with Enable	10	
Task 3-2: Build and Test a 4-Bit UP Counter	10	
Task 3-4: Build and Test the Brainless Central Processing Unit	20	
Task 3-5: Simulate the Brainless Central Processing Unit	20	
Task 3-6: Create Additional Tests	20	
Task 3-7: Create a video and submit your report (Optional)	0	
Lab Score (80 points total)	**Points Lost**	
	Late Lab	
	Lab Score	