Warren B. Nelms Institute for the Connected World
Patanjali SLPSK | Postdoctoral Research Fellow

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Bitbucket repo: https://bitbucket.org/patanjali/

Employment

Position	Institution	Duration
Postdoctoral Research Fellow	University of Florida	November 2019-Present
Research Intern	IBM Integrated Systems Development Lab, Bangalore	June 2015-December 2015

Education

Program	Institution	%/CGPA	Year of Completion
PhD. (CSE)	IIT Madras	**8.73**	November 2019
MS (CSE)	IIT Madras	**8.6**	2014
B.Tech. (CSE)	Pondicherry Engineering College (PEC)	**8.32**	2011
XII	Petit Seimnaire Higher Secondary School, Pondicherry	**94.17**	2007
X	Petit Seimnaire Higher Secondary School, Pondicherry	**89.74**	2005

Research Interests

- Hardware Security
- Computer Architecture
- Secure Systems Engineering, and
- Machine Learning

Current Projects

- **Automatic Implementation of Secure Silicon (Feb 2021-Current)**
  Program Manager
  The primary goal of the AISS project is to develop secure SoCs that can be widely used by designers with varying range of security expertise. However, it is also crucial to ensure that the security architectures are compliant with the power, performance, and area requirements.
  Critical Outcomes produced
  1. Developed and demonstrated a proof-of-concept implementation a complete SoC implementation with hardware and firmware support for integrating PUF, Logic Locking protocols, and IP watermarking techniques.
  2. Developed a standardized wrapper architecture for integrating IPs with diverse security objectives.
  3. Developed a secure boot methodology for provisioning critical assets during boot time.
  4. Developed a security specification language for describing security requirements at the user-level.
- **Lightweight Authentication Protocols for securing IoT Devices (June 2020- Current)**
  Counterfeit integrated circuits (ICs) have become a significant security concern in the semiconductor industry as a result of the increasingly complex and distributed nature of the supply chain. These counterfeit chips may result in performance degradation, profit reduction, and reputation risk for the manufacturer. Therefore, developing effective countermeasures against such malpractices is becoming severely crucial. As a part of our research effort we develop lightweight authentication techniques using Physically Unclonable Functions (PUFs) and watermarks for detecting counterfeit ICs.
  Critical Outcomes:
  1. Developed a challenge-vector free authentication technique using delay variations in boundary scan-chains.
  2. Developed a hybrid PUF protocol that combines the benefits of strong and weak PUFs by integrating bistable elements in design logic.
  3. Developed a lightweight watermarking technique for verifying IP provenance.

Publications

Patents

- Bhunia, Swarup, Christopher Vega, Shubhra Deb Paul, Parker Difuntorum, Reiner Dizon, and **Patanjali Sristi Lakshmiprasanna Sriramakumara.** "Defense of jtag i/o network." U.S. Patent Application 17/303,648, filed December 16, 2021.
- Bhunia, Swarup, Tamzidul Hoque, Abhishek Anil Nair, and **Patanjali Sristi Lakshmiprasanna Sriramakumara.** "Framework for obfuscation based watermarking." U.S. Patent Application 17/224,559, filed October 14, 2021

Publications (Contd.)

Journals

- Zhang, Fengchao, Shubhra Deb Paul, **Patanjali Slpsk**, Amit Ranjan Trivedi, and Swarup Bhunia. "On Database-Free Authentication of Microelectronic Components." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 29, no. 1 (2020).
- Vega, C., **SLPSK, P.**, Paul, S. D., Bhunia, S. (2020). MeLPUF: Memory in Logic PUF. arXiv preprint arXiv:2012.03162.
- Nair, A., **SLPSK, P.**, Rebeiro, C., Bhunia, S. (2020). SIGNED: A Challenge-Response Based Interrogation Scheme for Simultaneous Watermarking and Trojan Detection. arXiv preprint arXiv:2010.05209.
- Rahul Bodduna, Vinod Ganesan, **Patanjali Slpsk**, Chester Rebeiro and V. Kamakoti, "BRUTUS: Refuting the Security Claims of the Cache Timing Randomization Countermeasure proposed in CEASER," IEEE Computer Architecture Letters (2020).
- Hoque, Tamzidul, **Patanjali Slpsk**, and Swarup Bhunia. "Trust issues in microelectronics: The concerns and the countermeasures." IEEE Consumer Electronics Magazine 9, no. 6 (2020): 72-83.
- Krishnakumar, Gnanambikai, **Patanjali SLPSK**, Prasanna Karthik Vairam, Chester Rebeiro, and Kamakoti Veezhinathan. "GANDALF: A fine-grained hardware-software co-design for preventing memory attacks." in IEEE Embedded Systems Letters (2018).
- **Patanjali, SLPSK**, Milan Patnaik, Seetal Potluri, and V. Kamakoti. "MLTimer: Leakage Power Minimization in Digital Circuits Using Machine Learning and Adaptive Lazy Timing Analysis." in Journal of Low Power Electronics (2018).

Conferences

- S. Yang, P. Chakraborty, **P. SLPSK** and S. Bhunia, "Trusted Electronic Systems with Untrusted COTS," 2021 22nd International Symposium on Quality Electronic Design (ISQED), 2021, pp. 198-203, doi: 10.1109/ISQED51717.2021.9424257.
- Hoque, Tamzidul, **Patanjali SLPSK**, and Swarup Bhunia. "Trust Issues in COTS: The Challenges and Emerging Solution." In Proceedings of the 2020 on Great Lakes Symposium on VLSI, pp. 211-216. 2020.
- Mitra, Gargi, Prasanna Karthik Vairam, **Patanjali Slpsk**, Nitin Chandrachoodan, and V. Kamakoti. "Depending on HTTP/2 for Privacy? Good Luck!." In 2020 50th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), pp. 278-285. IEEE, 2020.
- Milind Srivatsava, **Patanjali SLPSK**, Indrani Roy, Chester Rebeiro, and Swarup Bhunia. "SOLOMON: An Automated Framework for Detecting Fault Attack Vulnerabilities in Hardware", **To appear in DATE 2020**
- **Patanjali Slpsk**, Prasanna Karthik Vairam, Chester. Rebeiro and V. Kamakoti, "Karna: A Gate-Sizing based Security Aware EDA Flow for Improved Power Side-Channel Attack Protection," in IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2019"
- Gargi Mitra, Prasanna Karthik Vairam, **Patanjali SLPSK**, Nitin Chandrachoodan, and Kamakoti V. " White Mirror: Leaking Sensitive Information from Interactive Netflix Movies using Encrypted Traffic Analysis." In ACM SIGCOMM 2019 Conference Posters and Demos.
- Gautham, Ashok, Kunal Korgaonkar, **Patanjali Slpsk**, Shankar Balachandran, and Kamakoti Veezhinathan. "The Implications of Shared Data Synchronization Techniques on Multi-Core Energy Efficiency." In HotPower. 2012.

Posters

- **Patanjali SLPSK**, Prasanna Karthik Vairam, Chester Rebeiro,and Kamakoti Veezhinathan. Karna: A Security Aware EDA Flow for Improved Side-Channel Attack Protection, In Proceedings of the 2019 Design Automation Conference (DAC 2019) under the Work-In-Progress section.
- Patanjali SLPSK, Seetal Potluri, and Kamakoti Veezhinathan. FastReplace: Efficient Vt Replacement Technique for Leakage Power Minimization . In Proceedings of the 2014 Design Automation Conference (DAC 2014)under Work-In-Progress section.
- Patanjali SLPSK, Seetal Potluri and Kamakoti Veezhinathan. HALTimer: A Fast Vt Replacement Heuristic for. Leakage Power Minimization. In Proceedings of 2015 Design Automation conference (DAC'15) under Work-In-Progress section.

Students Mentored

- **Milind Srivatsava**
  Dual Degree, IIT Madras.
  Project Title: SOLOMON: An Automated Framework for Detecting Fault Attack Vulnerabilities in Hardware.
- **Harish Reddy**
  Dual Degree, IIT Madras.
  Project Title: Privacy in Deep Learning.
- **Pritwish Basu Roy**
  MS, IIT Madras.
  Project Title: Fault attack countermeasures using EDA transformations.
- **Reiner Dizon**
  Ph.D. student, University of Florida.
  Project Title: Autonomous navigation of Drones for emergency applications
- **Christopher Vega**

Ph.D., University of Florida.
Project Title: A fully synthesizable and configurable random number generator for low-power IoT applications

- **Abhishek Anil Nair**
  Dual Degree, IIT Madras.
  Project Title: A low-overhead challenge-response based watermarking framework for IP protection.
- **Archit Jaiswal**
  Research Intern, University of Florida.
  Project Title: A low-overhead watermarking framework for preventing software piracy

Reviewing Experience

- **Journals:** Reviewer for HASS, JETC, IOT Journal, TIFS, TECS, Embedded System Letters.
- **Conferences:**Program Comittee member for ICCAD 2020, ICCAD 2021. External expert reviewer for DAC 2020,DAC 2019, Eurosys 2021. Artefact Reviewer for Eurosys 2021.

In other media

- Our work on Memory-In-Logic PUF was featured in the news. Click here for the article.
- Our article on Privacy issues on Video Streaming Applications was featured in Wired Magazine. Click here for the article
- Our work on the CSAW 2016 challenge was featured in Business Insider. Click here for the article.

Achievements

- My Thesis was accepted to the SIGDA Ph.D. Forum at DAC 2020.
- Winner and Runner-up in Applied Research Competition in CSAW 2020. (Along with Gargi Mitra and Prasanna Karthik Vairam).
- Selected for Richard Newton Young Fellow Program, DAC 2019.
- Winner 1st place. Applied Research contest Shaastra 2019.
- One of the top-100 (rank:40) of the technical writing challenge conducted by Department of Science and Technology, India.
- **Winner, First Place** in Embedded Systems Challenge in CSAW 2016.
- **Winner, Second Place** in HackU 2013 at IIT Madras. Click here for demo
- Our article on Privacy issues was featured in Wired Magazine. Click here for the article

Teaching Experience

- Computer Organization and Architecture: 2013, 2014 and 2015
- Operating Systems: 2015, 2016.
- Digital Systems Testing and Testable Design: 2014, 2015, 2016, 2017, 2018, and 2019.
- CAD for VLSI: 2016, 2017, and 2018.
- Digital Design Verification: 2016, 2017.
- Secure Systems Engineering: 2016, 2017, 2018, and 2019
- GPU Programming: 2018
- **Labs** Set up CTF for Secure Systems Engineering courses in the years 2016-2019.
- Set up an X86 lab using Intel Atom and Galileo Boards for the years 2013-2015.

References

- Dr. V. Kamakoti, IIT Madras.
- Dr. Swarup Bhunia, University of Florida.
- Dr. Sandip Ray, University of Florida.
- Dr. Chester Rebeiro, IIT Madras.