CCPS590 Lab 1 – Instruction Cycle, Interrupts, Memory Hierarchy

Preamble

There is no code to write for this lab. Instead, you will work through some problems related to examples we saw this week in class. Each of these can be solved using the lecture slides as a reference.

Lab Description

1) Consider the hypothetical processor with instruction format seen below:

In class, we saw an example that considered the following instruction op-codes:

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

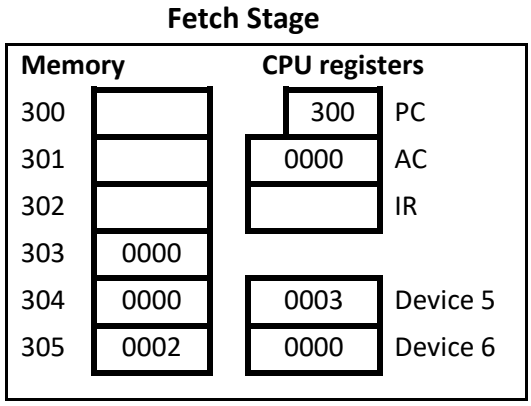
For this question, consider two additional op-codes:

0011 = Load AC from I/O device
0111 = Store AC to I/O device

For these new op-codes, the address field in the instruction refers to some external I/O device, rather than a location in main memory. Show the execution for a program that does the following:

1. Load AC from device 5 (address 705).
2. Add contents of memory location 305.
3. Store AC to device 6 (address 706).

In your answer, it is enough to show the contents of the registers at each step. The initial state of the CPU, in the same format we saw in class, can be seen below. You must fill in the memory and register values for this initial fetch stage and all remaining instruction cycles.



2) Suppose three interrupts, I1, I2, and I3, occur at times t=10, t=20, and t=30 as shown in the table below. Also in the table are the priorities of each interrupt (bigger number, higher priority), and the time required for the handler to process each interrupt.

Interrupt number	Interrupt time	Interrupt priority	time required
I1	t = 10	3	30
I2	t = 20	2	10
I3	t = 30	4	50

a) When does each of the three interrupts finish if the OS *disables* interrupts while an interrupt is being processed?

b) When does each of the three interrupts finish if the OS processes *multiple* interrupts using a priority scheme?

3) Consider the multi-level memory profile below:

Level 1: 1000 bytes 0.5t access time
Level 2: 1000 KB 1.0t access time

Below what hit ratio is this multi-level scheme doing more harm than good? Put another way, at what hit ratio would we be better off with *just* level 2 memory? Refer to the hit ratio example in the slides to get started.

Submission

Labs are to be submitted ***individually***! Submit your answers on D2L using any common digital format (PDF, doc, txt, etc). Make sure your answers are formatted cleanly and are easy to read.