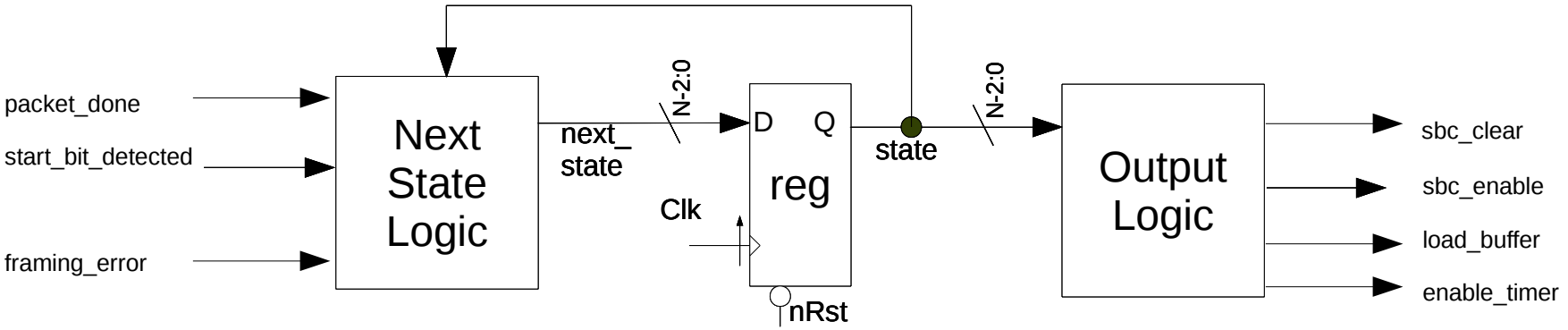
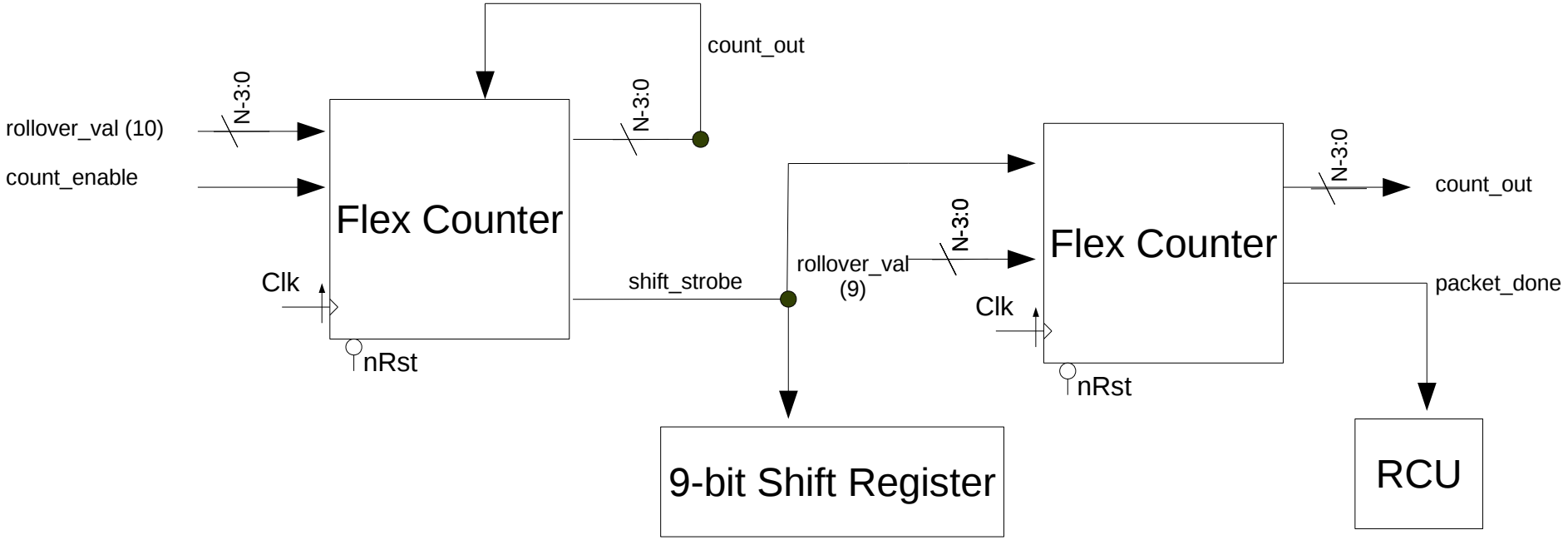
RCU RTL DIAGRAM



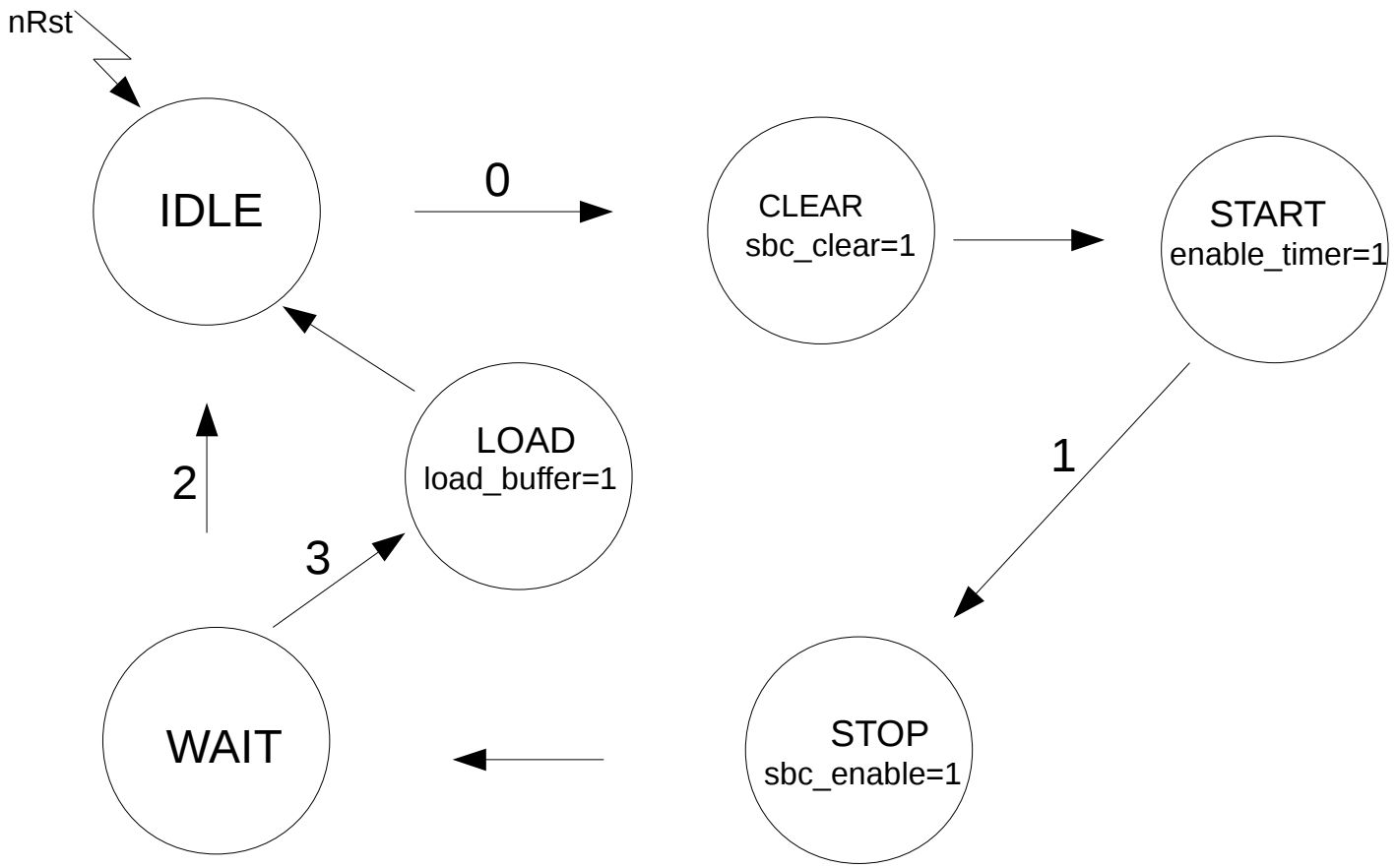
TIMER CONTROLLER RTL DIAGRAM



RCU STATE DIAGRAM

INPUT LEGEND

start_bit_detected=1 → 0
packet_done=1 → 1
framing_error=1 → 2
framing_error=0 → 3



DEFAULT OUTPUTS

sbc_clear = 0
sbc_enable = 0
load_buffer = 0
enable_timer = 0