DIGITAL DESIGN LAB 1

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B20EE082

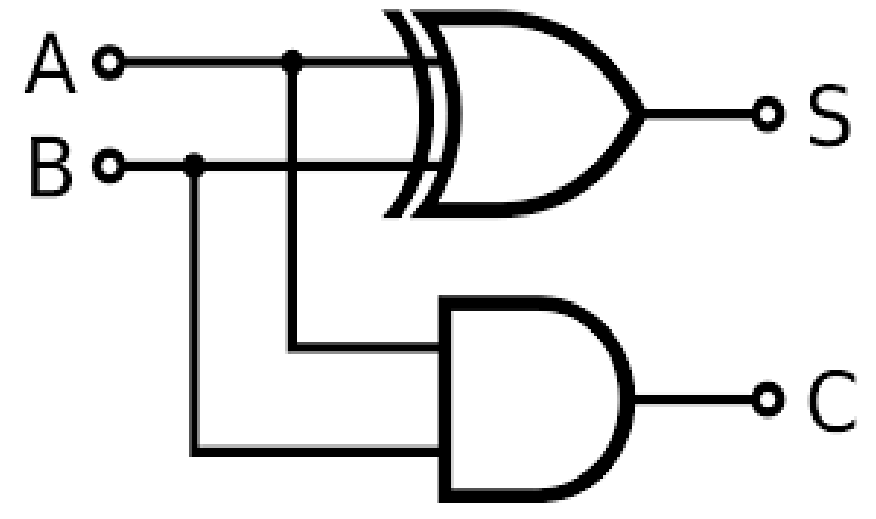
Work 1: Create a Half Adder. Write its test bench and Simulate

Project Summary | half_adder.v *

D:/YEAR 2/SEMESTER 2/DIGITAL DESIGN/LABS/LAB 1/half_adder.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 11.01.2022 15:48:03
7  // Design Name:
8  // Module Name: half_adder
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21
22
23 module half_adder(A,B,Sum,Carry);
24 input A, B;
25 output Sum, Carry;
26
27 assign Sum = A ^ B;
28 assign Carry = A & B;
29 endmodule
```

```
module half_adder(A,B,Sum,Carry);
input A, B;
output Sum, Carry;
assign Sum = A ^ B;
assign Carry = A & B;
endmodule
```



HALF ADDER TRUTH TABLE

INPUT		OUTPUT	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

TEST BENCH
HALF ADDER

Project Summary | half_adder.v * | test_half_adder.v *

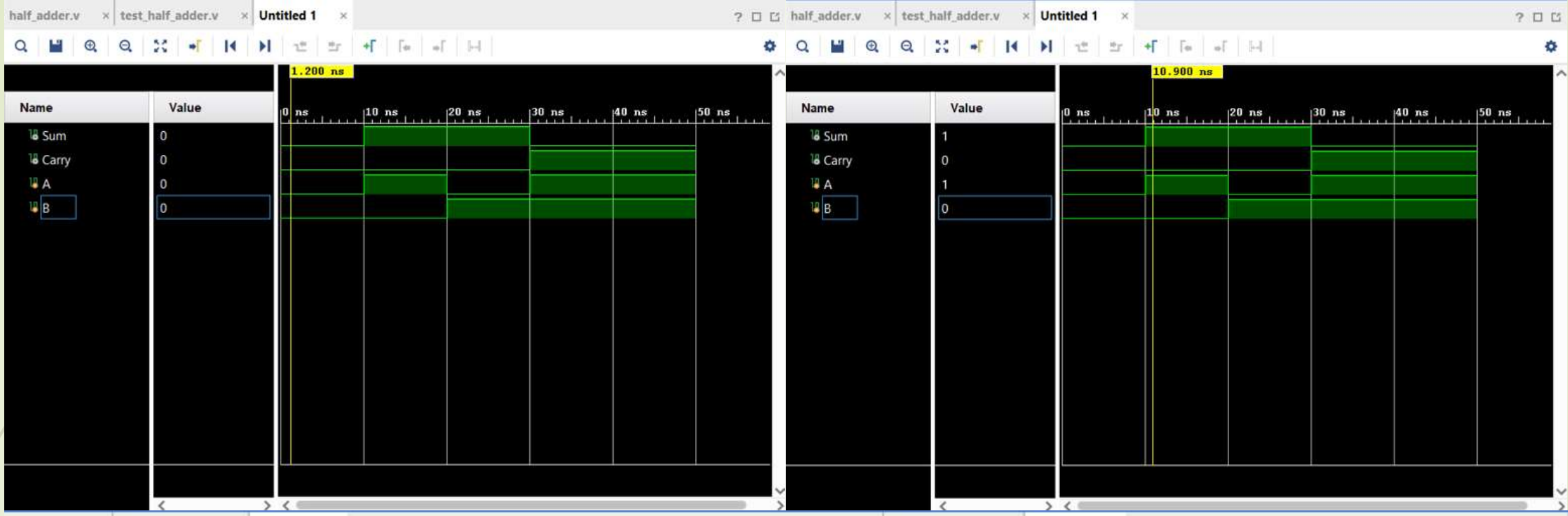
D:/YEAR 2/SEMESTER 2/DIGITAL DESIGN/LABS/LAB 1/test_half_adder.v

```
7  // Design Name:
8  // Module Name: test_half_adder
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////
21
22 module test_half_adder;
23 wire Sum,Carry;
24 reg A,B;
25 half_adder H1(A,B,Sum,Carry);
26
27 initial
28 begin
29     A = 1'b0; B = 1'b0;
30     #10 A = 1'b1;
31     #10 B = 1'b1; A = 1'b0;
32     #10 A = 1'b1;
33 end
34
35 initial #50 $finish;
36
37 endmodule
```

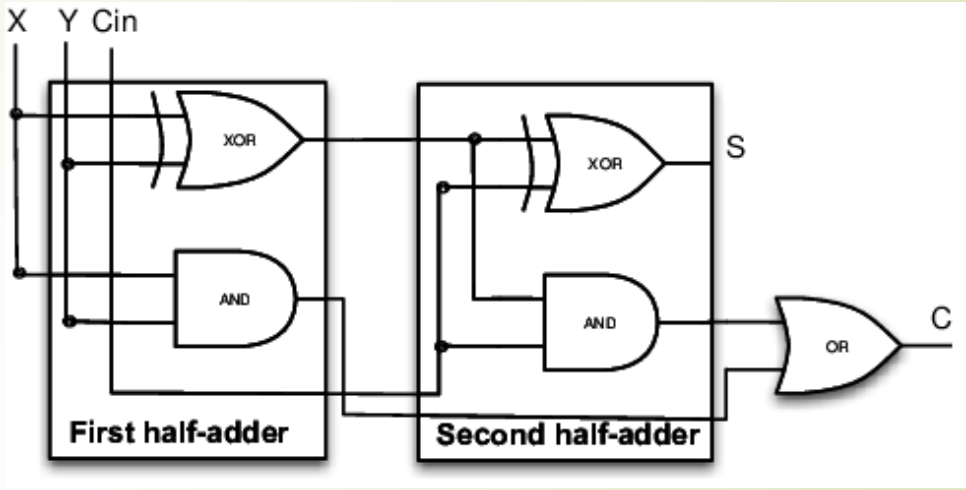
TEST BENCH - HALF ADDER

```
module test_half_adder;
wire Sum,Carry;
reg A,B;
half_adder H1(A,B,Sum,Carry);

initial
begin
    A = 1'b0; B = 1'b0;
    #10 A = 1'b1;
    #10 B = 1'b1; A = 1'b0;
    #10 A = 1'b1;
end

initial #50 $finish;

endmodule
```

SIMULATION


half_adder.v
test_half_adder.v
Untitled 1
Name
Value
Sum
Carry
A
B
0
0
0
0
1.200 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
1
0
1
0
10.900 ns
1
0
1
1
21.300 ns
0
1
1
1
30.700 ns

Work 2: Use Half Adder to Create a Full Adder



TRUTH TABLE FOR FULL ADDER

INPUT			OUTPUT	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Project Summary | half_adder.v * | test_half_adder.v * | full_adder.v

D:/YEAR 2/SEMESTER 2/DIGITAL DESIGN/LABS/LAB 1/full_adder.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 11.01.2022 16:00:07
7  // Design Name:
8  // Module Name: full_adder
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21
22
23 module full_adder(A,B,C,Sum,Carry);
24 input A,B,C;
25 output Sum, Carry;
26 wire Sum1, Carry1, Carry2;
27 half_adder H1(A,B,Sum1,Carry1);
28 half_adder H2(Sum1,C,Sum,Carry2);
29 assign Carry = Carry1|Carry2;
30
31 endmodule
```

```
module full_adder(A,B,C,Sum,Carry);
input A,B,C;
output Sum, Carry;
wire Sum1, Carry1, Carry2;
half_adder H1(A,B,Sum1,Carry1);
half_adder H2(Sum1,C,Sum,Carry2);
assign Carry = Carry1|Carry2;

endmodule
```

Work 3: Use Full Adder to Create a Four Bit Adder. Write its test bench and S...

Project Summary | test_four_bit_adder.v | four_bit_adder.v

D:/YEAR 2/SEMESTER 2/DIGITAL DESIGN/LABS/LAB 1/four_bit_adder.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////...
21
22
23 module four_bit_adder(A,B,S,Carry);
24 input [3:0]A,B;
25 output [3:0]S;
26 output Carry;
27 reg C0 = 1'b0;
28 wire C1,C2,C3;
29 full_adder FA1(A[0],B[0],C0,S[0],C1);
30 full_adder FA2(A[1],B[1],C1,S[1],C2);
31 full_adder FA3(A[2],B[2],C2,S[2],C3);
32 full_adder FA4(A[3],B[3],C3,S[3],Carry);
33
34 endmodule
```

```
module four_bit_adder(A,B,S,Carry);
input [3:0]A,B;
output [3:0]S;
output Carry;
reg C0 = 1'b0;
wire C1,C2,C3;
full_adder FA1(A[0],B[0],C0,S[0],C1);
full_adder FA2(A[1],B[1],C1,S[1],C2);
full_adder FA3(A[2],B[2],C2,S[2],C3);
full_adder FA4(A[3],B[3],C3,S[3],Carry);

endmodule
```

test_four_bit_adder.v | test_four_bit_adder_behav.wcfg

D:/YEAR 2/SEMESTER 2/DIGITAL DESIGN/LABS/LAB 1/test_four_bit_adder.v

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
21
22
23  module test_four_bit_adder;
24  reg [3:0]A,B;
25  wire [3:0]S;
26  wire Carry;
27
28  four_bit_adder FBA1(A,B,S,Carry);
29  initial
30  begin
31      A = 4'b0000; B = 4'b0000;
32      #10 A = 4'b0001; B = 4'b0010;
33      #10 A = 4'b0101; B = 4'b0111;
34      #10 A = 4'b0110; B = 4'b1000;
35      #10 A = 4'b1001; B = 4'b1010;
36      #10 A = 4'b1010; B = 4'b1011;
37      #10 A = 4'b1101; B = 4'b1110;
38      #10 A = 4'b1111; B = 4'b1111;
39  end
40
41  initial #80 $finish;
42  endmodule
```

TEST BENCH – FOUR BIT ADDER


```
module test_four_bit_adder;
reg [3:0]A,B;
wire [3:0]S;
wire Carry;

four_bit_adder FBA1(A,B,S,Carry);
initial
begin
    A = 4'b0000; B = 4'b0000;
    #10 A = 4'b0001; B = 4'b0010;
    #10 A = 4'b0101; B = 4'b0111;
    #10 A = 4'b0110; B = 4'b1000;
    #10 A = 4'b1001; B = 4'b1010;
    #10 A = 4'b1010; B = 4'b1011;
    #10 A = 4'b1101; B = 4'b1110;
    #10 A = 4'b1111; B = 4'b1111;
end

initial #80 $finish;
endmodule
```

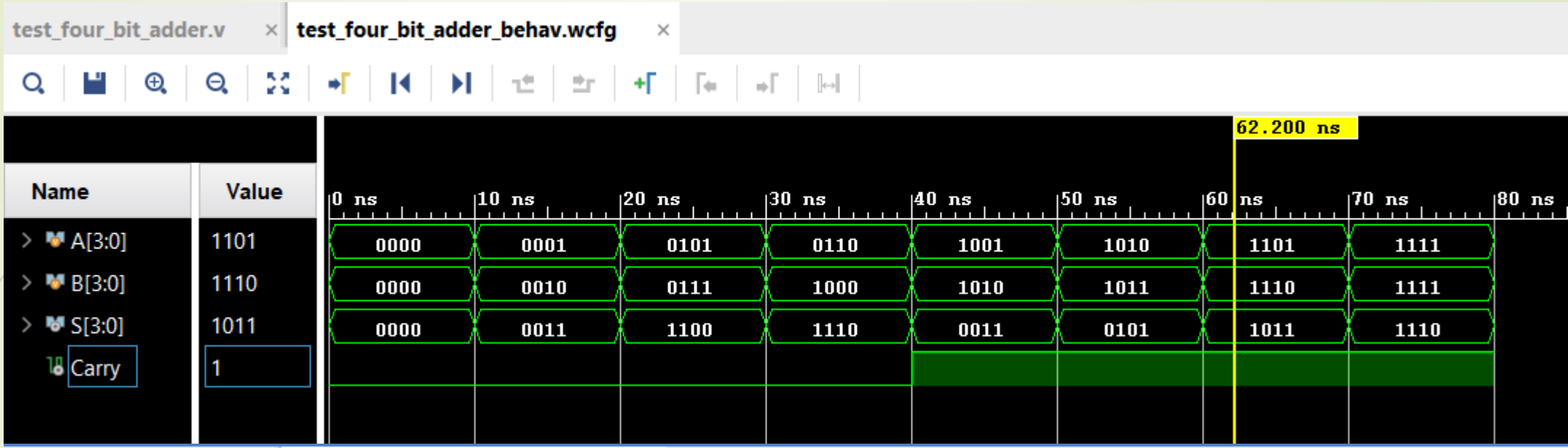
SIMULATION

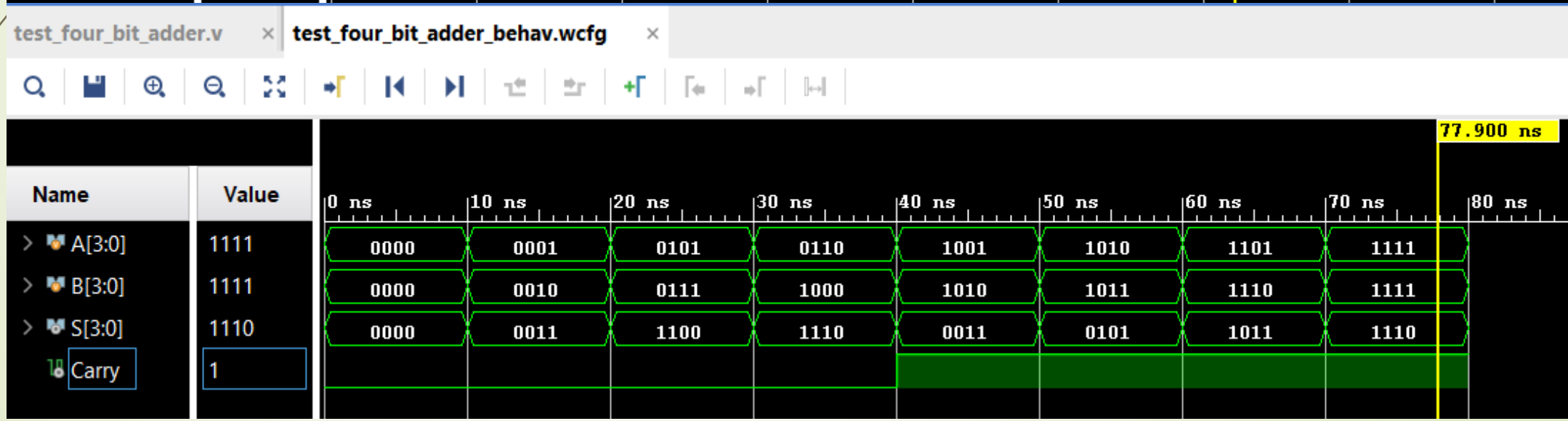

2.200 ns
Name
Value
A[3:0]
0000
B[3:0]
0000
S[3:0]
0000
Carry
0
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
0000 0001 0101 0110 1001 1010 1101 1111
0000 0010 0111 1000 1010 1011 1110 1111
0000 0011 1100 1110 0011 0101 1011 1110
12.500 ns
Name
Value
A[3:0]
0001
B[3:0]
0010
S[3:0]
0011
Carry
0
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
0000 0001 0101 0110 1001 1010 1101 1111
0000 0010 0111 1000 1010 1011 1110 1111
0000 0011 1100 1110 0011 0101 1011 1110
28.400 ns
Name
Value
A[3:0]
0101
B[3:0]
0111
S[3:0]
1100
Carry
0
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
0000 0001 0101 0110 1001 1010 1101 1111
0000 0010 0111 1000 1011 1110 1111
0000 0011 1100 1110 1001 0101 1011 1110

SIMULATION


Name
Value
A[3:0]
0110
B[3:0]
1000
S[3:0]
1110
Carry
0
32.000 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
0000
0001
0101
0110
1001
1010
1101
1111
0000
0010
0111
1000
1010
1011
1110
1111
0000
0011
1100
1110
0011
0101
1011
1110
Name
Value
A[3:0]
1001
B[3:0]
1010
S[3:0]
0011
Carry
1
48.900 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
0000
0001
0101
0110
1001
1010
1101
1111
0000
0010
0111
1000
1010
1011
1110
1111
0000
0011
1100
1110
0011
0101
1011
1110
Name
Value
A[3:0]
1010
B[3:0]
1011
S[3:0]
0101
Carry
1
50.900 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
0000
0001
0101
0110
1001
1010
1101
1111
0000
0010
0111
1000
1010
1011
1110
1111
0000
0011
1100
1110
0011
0101
1011
1110

SIMULATION


test_four_bit_adder.v
test_four_bit_adder_behav.wcfg
Name
Value
A[3:0]
1101
B[3:0]
1110
S[3:0]
1011
Carry
1
62.200 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
0000 0001 0101 0110 1001 1010 1101 1111
0000 0010 0111 1000 1010 1011 1110 1111
0000 0011 1100 1110 0011 0101 1011 1110


test_four_bit_adder.v
test_four_bit_adder_behav.wcfg
Name
Value
A[3:0]
1111
B[3:0]
1111
S[3:0]
1110
Carry
1
77.900 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
0000 0001 0101 0110 1001 1010 1101 1111
0000 0010 0111 1000 1010 1011 1110 1111
0000 0011 1100 1110 0011 0101 1011 1110

THANK YOU