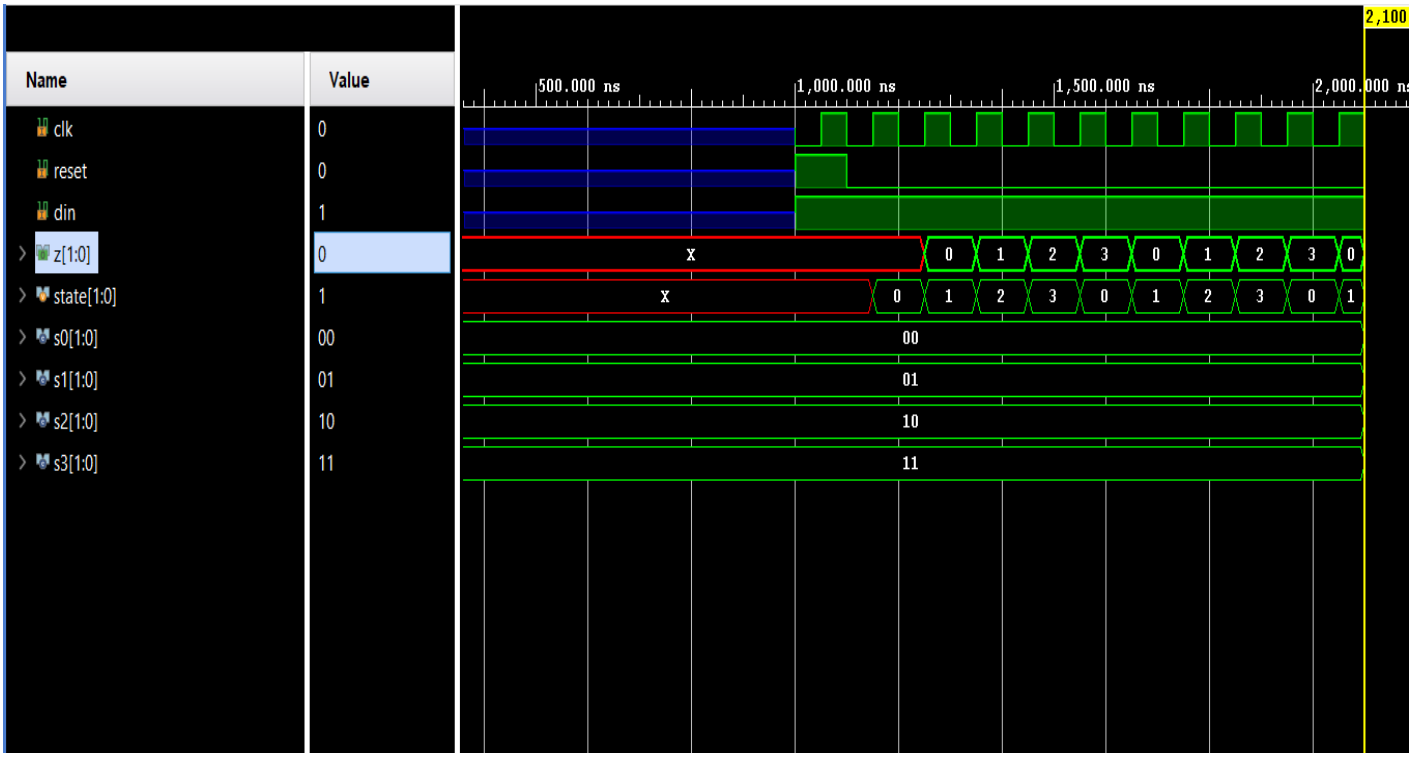
FSM COUNTER:

```
23      module FSM(clk,reset,din,z);
24          input wire clk,reset,din;
25          output reg [1:0] z;
26          reg [1:0] state;
27          parameter s0=2'b00,s1=2'b01,s2=2'b10,s3=2'b11;
28          always @(posedge clk)
29          begin
30              if(reset==0)
31              state<=s0;
32              else
33              state<=state;
34          end
35          always @(posedge clk)
36          begin
37          case(state)
38          s0: begin
39              if (din==1)
40              state<=s1;
41              else
42              state<=state;
43              end
44          s1: begin
45              if (din==1)
46              state<=s2;
47              else
48              state<=state;
49              end
50          s2: begin
51              if (din==1)
52              state<=s3;
53              else
54              state<=state;
55              end

56           s3: begin
57               if (din==1)
58               state<=s0;
59               else
60               state<=state;
61               end
62           endcase
63           z<=state;
64           end
65      endmodule
```


Name
Value
clk
0
reset
0
din
1
z[1:0]
0
state[1:0]
1
s0[1:0]
00
s1[1:0]
01
s2[1:0]
10
s3[1:0]
11
500.000 ns
1,000.000 ns
1,500.000 ns
2,000.000 ns
2,100
x
0 1 2 3 0 1 2 3 0
x
0 1 2 3 0 1 2 3 0 1
00
01
10
11