

1. Description

1.1. Project

Project Name	AD9834
Board Name	NUCLEO-G474RE
Generated with:	STM32CubeMX 6.7.0
Date	04/07/2023

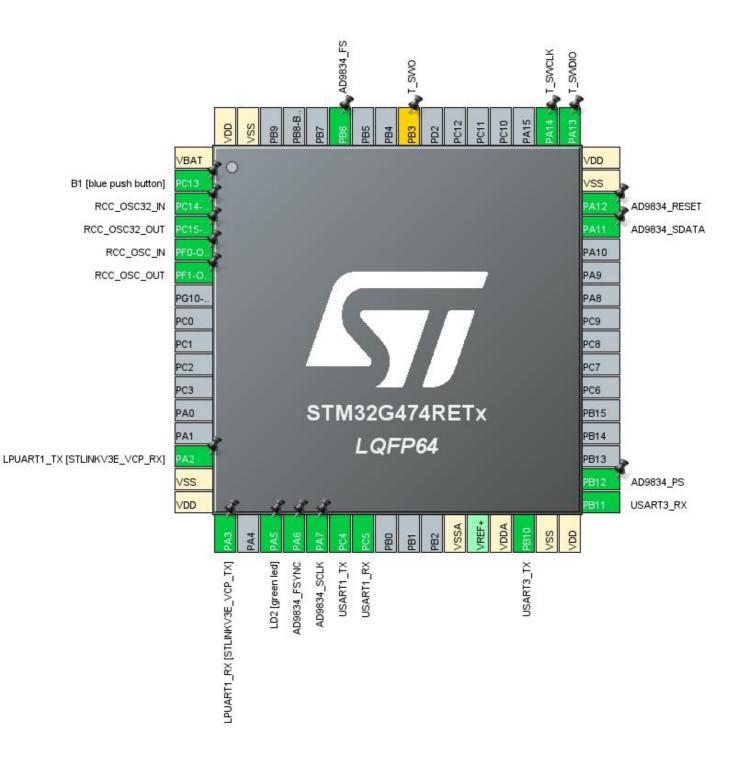
1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x4
MCU name	STM32G474RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration



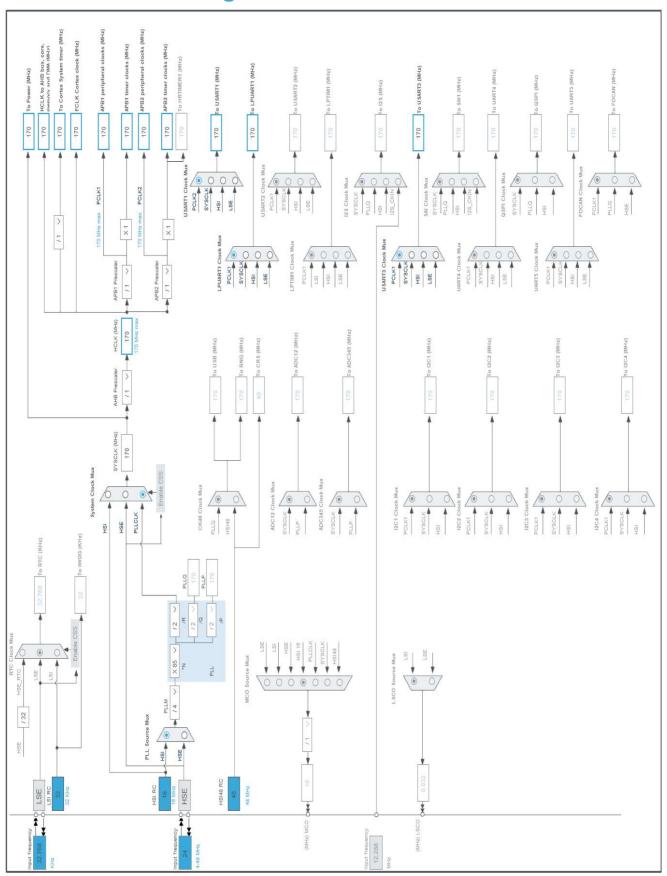
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after	" ' ' ' '	Function(s)	Labor
LQII 04	,		i dilettori(s)	
	reset)	_		
1	VBAT	Power		5.5.
2	PC13	I/O	GPIO_EXTI13	B1 [blue push button]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
14	PA2	I/O	LPUART1_TX	LPUART1_TX [STLINKV3E_VCP_RX]
15	VSS	Power		
16	VDD	Power		
17	PA3	I/O	LPUART1_RX	LPUART1_RX [STLINKV3E_VCP_TX]
19	PA5 *	I/O	GPIO_Output	LD2 [green led]
20	PA6 *	I/O	GPIO_Output	AD9834_FSYNC
21	PA7 *	I/O	GPIO_Output	AD9834_SCLK
22	PC4	I/O	USART1_TX	
23	PC5	I/O	USART1_RX	
27	VSSA	Power		
29	VDDA	Power		
30	PB10	I/O	USART3_TX	
31	VSS	Power		
32	VDD	Power		
33	PB11	I/O	USART3_RX	
34	PB12 *	I/O	GPIO_Output	AD9834_PS
45	PA11 *	I/O	GPIO_Output	AD9834_SDATA
46	PA12 *	I/O	GPIO_Output	AD9834_RESET
47	VSS	Power		
48	VDD	Power		
49	PA13	I/O	SYS_JTMS-SWDIO	T_SWDIO
50	PA14	I/O	SYS_JTCK-SWCLK	T_SWCLK
56	PB3 **	I/O	SYS_JTDO-SWO	T_SWO
59	PB6 *	I/O	GPIO_Output	AD9834_FS
63	VSS	Power		
64	VDD	Power		

*	The	pin	is	affected	with	an	I/O	function
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^{**} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value	
Project Name	AD9834	
Project Folder	C:\Users\Lenovo\STM32CubelDE\workspace_1.11.0\AD9834	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_G4 V1.5.1	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_LPUART1_UART_Init	LPUART1
4	MX_USART1_UART_Init	USART1
5	MX_USART3_UART_Init	USART3

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x4
мси	STM32G474RETx
Datasheet	DS12288_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

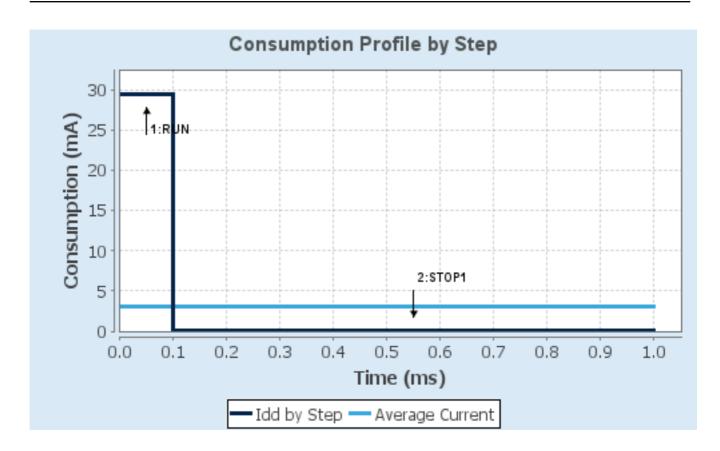
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/DualBank/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	29.5 mA	80.5 μA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	124.25	129.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	3.02 mA
Battery Life	1 month, 16 days,	Average DMIPS	212.5 DMIPS
	9 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. LPUART1

Mode: Asynchronous

7.1.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Single Sample Disable ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Advanced Features:

TX Pin Active Level Inversion

RX Pin Active Level Inversion

Disable

Data Inversion

Disable

TX and RX pins Swapping

Overrun

Enable

DMA on RX Error

MSB First

Disable

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value (64
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration TRUE

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

7.4. **USART1**

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Data Inversion Disable TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

7.5. USART3

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable Disable Data Inversion Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LPUART1_TX [STLINKV3E_VCP_RX]
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LPUART1_RX [STLINKV3E_VCP_TX]
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	T_SWDIO
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	T_SWCLK
USART1	PC4	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	T_SWO
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1 [blue push button]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green led]
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	AD9834_FSYNC
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	AD9834_SCLK
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	AD9834_PS
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	AD9834_SDATA
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	AD9834_RESET
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High	AD9834_FS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
USART3 global interrupt / USART3 wake-up interrupt through EXTI line 28	unused		
FPU global interrupt	unused		
LPUART1 global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line[15:10] interrupts	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32g4_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32g4_ibis.zip

System View https://www.st.com/resource/en/svd/stm32g4_svd.zip

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