UNIT-4

Memory: Basic concept and hierarchy, semiconductor RAM memories, 2D & 2 1/2D memory organization. ROM memories. Cache memories: concept and design issues & performance, address mapping and replacement Auxiliary memories: magnetic disk, magnetic tape and optical disks Virtual memory: concept implementation.

Q 1. (i)What do you mean by Cache Memory? What is cache hit? What is its importance? Define hit ratio.

(ii)Explain the following mapping process

(a) Associative Mapping (b). Direct Mapping (c) Set- Associative Mapping

Q2. What is cache memory? Discuss the different mapping process while considering the organization of cache memory.

Q3. Discuss Static and Dynamic RAM. Explain 2 D and $2^{1/2}$ D RAM organization.

Q4. Explain the need of memory hierarchy with the help of block diagram? What is the reason for not having one large memory unit for storing all information at one place?

Q5. Discuss the concept and implementation of virtual memory. Also describe a suitable scheme for translation from logical address to physical address.

Q6. Discuss the construction and working of a magnetic disk. Also discuss various components of disk access time.

Q7. What do you mean understand by level of memory hierarchy? Discuss various design considerations of memory hierarchy.

Q8. Discuss RAM and ROM chips with Block diagram.

Q9. What are page replacement policies? Explain FIFO and LRU page replacement policies.

Q10. What do you mean by address map?

Q11. Define Hit ratio.

Q12.Explain FIFO and LRU page replacement algorithms with example.

Q13. Explain various cache memory mapping technique.

Q14. Discuss address mapping and associate memory page table used in case of virtual memory.

Q15.Define ROM,PROM,EPROM,EEPROM.

Q16.Explain in detail how data is written onto and read from a magnetic disk?

Q17.Explain the cache memory principle using three level cache organizations.

Q18. What are the different auxiliary memories?

NUMERICAL PROBLEMS

Q1 a. How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes?

b. How many lines of the address bus must be used to access 2048 bytes of memory? How many these lines will be common to all chips?

c. How many lines must be decoded for chip select? Specify the size of the decoders.

Q2. A computer uses RAM chips of 1024*1capacity.

a. How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?

b. How many chips are needed to provide a memory capacity of 16k bytes? Explain in words how the chips are to be connected to the address bus.

Q3. Discuss different types of RAM. How many 128bytes RAM chips are required to provide a memory of 2048 bytes? Show details of connections, clearly indicating address, data and decoder configuration.

Q4. 1k*4 RAM chips are used to construct 1k*8 RAM. How many chips are required? Draw a connection diagram?

Q5. 16k*8 RAM chips are used to construct 64k*16 RAM . Find how many chips will be needed. Also draw diagrams showing connections of chip to address lines.

Q6. What is the transfer rate of an eight-track magnetic tape whose speed is 120inches per second and whose density is 1600 bits per inch?

Q7. A two-way set associative cache memory uses block of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128k*32.

a. Formulate all pertinent information required to construct the cache memory.

b. What is the size of the cache memory?

Q8. The access time of a cache memory is 100 ns and that of main memory 1000ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write. The ratio for read accesses only is 0.9. A Write through procedure is used.

a. What is average access time of the system considering only memory read cycles?

b. What is the average access time of the system for both read and write requests?

c. What is the hit ratio taking into consideration the write cycles?

Q9. A four-way set-associative cache memory has four words in each set. A replacement procedure based on the least recently used (LRU) algorithm is implemented by means of 2-bit counters associated with each word in the set. A value in the range 0 to 3 is thus recorded for each word. When a hit occurs, the counter associated with the referenced word

is set to 0, those counters with values originally lower than the referenced one are incremented by 1, and all others remain unchanged. If a miss occurs, the word with counter value 3 is removed, the new word is put in its place, and its counter is set to 0.The other three counters are incremented by 1. Show that this procedure works for the following sequence of word reference: A,B,C,D,B,E,D,A,C,E,C,E.(Start with A,B,C,D as the initial four words, with word A being the least recently used.)

Q10. A digital computer has a memory unit 64k*16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

a. How many bits are there in the tag, index, block, and word fields of the address format?

b. How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.

c. How many blocks can the cache accommodate?

Q11. An address space is specified by 24 bits and corresponding memory space by 16 bits.

a. How many words are there in the address space?

b. How many words are there in the memory space?

c. If a page consists of 2k words. How many pages and blocks are there in the system?

Q12. A virtual memory has a page size of 1K words. There are eight pages and four blocks. The Associative memory page table contains the following entries:

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses (in decimal) that will cause a page fault if use by the CPU.

Q13. A virtual memory system has an address space of 8k words, a memory space of 4k words, and page and block sizes of 1k words. The following page reference changes occurs during a given time interval. (Only page changes are listed. If the same page is referenced again, it is not listed twice.)

4 2 0 1 2 6 1 4 0 1 0 2 3 5 7

Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is (a) FIFO (b) LRU

Q14. The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4k words in each. Physical memory consists of 4k blocks of 4k words in each. Formulate the logical and physical address formats.

Q15. Extend the memory system of 128*8 RAM chips and 512*8 ROM chips to 4096 bytes of RAM and 4096 of ROM . List the memory address map and indicate what size of decoders are needed.

Q15. Draw a structure of an 8M*8 bit DRAM chip. Also explain its specification.