Accurate Institute of Management & Technology, Greater Noida
First Sessional Exam (Odd Semester 2020- 21)
Course: - MCA Year: - First Year Semester:-1st
Subject Name: - Computer Organization and Architecture Maximum Marks: -30
Paper Code: - KCA-105 Time Duration:-90 minutes
Roll No…….

Note- Attempt all questions.

SECTION - A

Q1.Attempt all Questions (5×2 = 10 marks)

(a). Represent the following conditional control statement by two register transfer statements With control function.

If (P=1) then (R1←R2) else if (Q=1) then (R1←R3)

(b).What is RPN?

(c). What is Bus? What are different types of Buses?

(d). What is microoperation?

(e) . let SP= 000000 in the stack. How many items are there in the stack if:

a. FULL = 1 and EMTY = 0?

b. FULL= 0 and EMTY = 1?

SECTION – B

Q2.Attempt any *one* part of the following (1 × 3 = 3 marks)

(a). Draw the block diagram for the hardware that implements the following statements

X+YZ:AR←AR+BR

Where AR and BR are two n-bit registers and x,y and z are control variables include the logic gates for the control function.

(b). What is Register organization? Show the block diagram of the hardware that implements the

Following register Transfer statement:

yT2: R2 ←R1, R1 ← R2

Q3. Attempt any *one* part of the following (1 × 3 = 3 marks)

(a). What is bus Arbitration? Explain serial and parallel bus arbitration?

(b). Discuss the advantages and disadvantages of Polling and daisy chaining bus Arbitration schemes.

Q4. Attempt any *one* part of the following (1 × 3 = 3 marks)

(a). What is Bus Architecture? Explain the following Bus:

i. ISA ii. EISA iii.MCA iv. SCSI v. AGP vi. PCI

b). What is Bus Architecture? Explain.

Q5.Attempt any *one* part of the following (1 × 3 = 3 marks)

(a). A stack is organized such that SP always points at the next empty location on the stack. This means that SP can be initialized to 4000 and the first item in the stack is stored in location 4000. List the microoperations for the PUSH and POP.

(b). What is memory transfer? The following transfer statements specify a memory. Explain the memory
operation in each case.

a. R2←M[AR]
b. M[AR] ← R3
c. R5 ←M[R5]

SECTION – C

Q6. Attempt any *one* part of the following (1 × 4 = 4 marks)

A bus-organized CPU has 16 registers with 32 bits in each, and an ALU and a destination decoder.

(a). How many multiplexers are there in the A bus, and What is the size of each multiplexer?
(b). How many selection inputs are needed for MUX A and MUX B?
(c). How many inputs and outputs are there in the decoder?
(d).How many inputs and outputs are there in the ALU for data, including input and output carries ?
(e).Formulate a control word for the system assuming that the ALU has 35 operations.

(b). What is register transfer ? Explain with suitable example ?

Q7. Attempt any *one* part of the following (1 × 4 = 4 marks)

(a). What is Stack Organization? Convert the following numerical arithmetic expression into reverse polish notation and show the stack operation for evaluating the numerical result.

(3+4)[10(2+6)+8]

(b).Draw 8-to1 Mux and 3*8 Decoder.