INDEX

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Sr. No	Name of the Experiment	Page No	Date of Experiment	Date of Submission	Remarks
1	Study of the logic Gate & verify the Truth Table	1-5	05/01/2021	05/01/2021	
2	Design & implimentation of Half & Full Adder	6-8	12/01/21	12/01/21	
3	Design & implimentation of Half & full Subtractor	9-10	19/01/2021	19/01/2021	
4	Design & implimentation of MUX & DeMUX	11-13	22/01/21	22/01/21	

Study of logic Gates & verify their Truth Table.

* AIM: Verification & interpretation of truth table for AND, OR, NOT, NAND, NOR, XOR & XNOR Gates.

* APPARATUS REQUERIED :

SL NO.	Component	Specification	Quantity
1	AND Gate	IC 7408	1
2	OR Gate	IC 7432	1
3	NOT Gate	IC 7404	1
4	NAND Gate	IC 7400	1
5	NOR Gate	IC 7402	1
6	X-OR Gate	IC 7486	1
7	ICTrainer Kit	-	1
8	Patch card	-	As Per Require

Theory: Logic Gates are electronic circuits which Perform logical functions on one or more I/P to Produce 1 o/P.

There are 7 Logic gates. when all i/P combinations of a logic gate are written in a series are their corresponding o/P written along them, this I/O combination is called Truth Table.

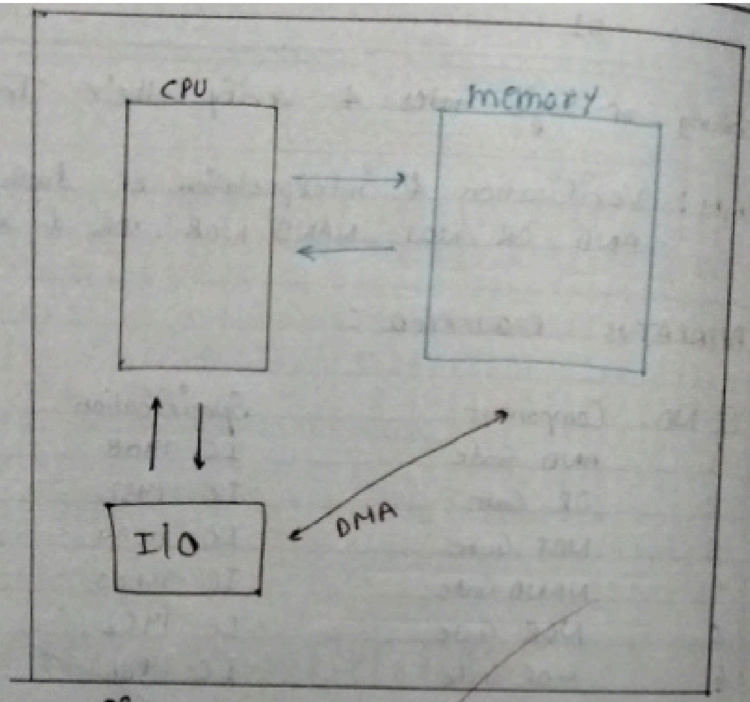


Fig. Structure of computer

* Program :- A Sequence of instruction for the computer is called a Program.

* Logic Gates :- Logic gates are the basic building blocks of any digital system.

⇒ It is an electronic circuit having one or more than one I/P & 1 O/P only.

⇒ The relationship b/w the I/O is based on a certain logic.

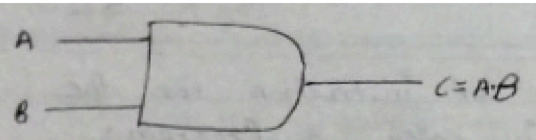
⇒ Gates are blocks of hardware that Produce Signals of binary 1 or 0 when input logic requirements are Satisfied.

TYPES OF LOGIC GATES

(I) AND Gate
(II) OR Gate
(III) NOT Gate
} → Basic GATES

(IV) NAND Gate
(V) NOR Gate
} → Universal Gates

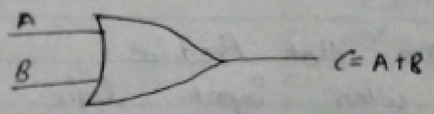
(VI) XOR Gate
(VII) XNOR Gate
} → Exclusive / Special GATES



Truth Table

A	B	C=A·B
0	0	0
0	1	0
1	0	0
1	1	1

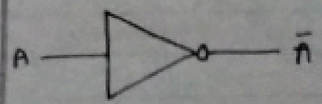
OR GATE



Truth Table

A	B	C=A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE



Truth Table

A	$\bar{A}$
0	1
1	0

i) AND GATE :- In AND gate, if it has one false value i.e 0, then the o/p is 0 otherwise true i.e 1.

Boolean expression :- $C = A \cdot B$

→ The algebric operation symbol of the AND function is the same as the multiplication symbol of ordinary airthmetic.

ii) OR GATE :- In OR gate, the o/p will be false i.e 0 if & only if both the i/p are 0 otherwise true i.e 1.

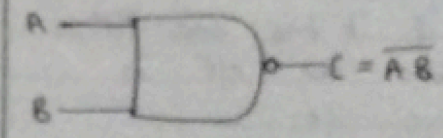
Boolean Expression :- $C = A + B$

→ The algebraic operation symbol of the OR function is the same as the addition operation.

iii) NOT GATE :- It is also known as inverter. It produces the NOT or the complement function. If the o/p is 1 then i/p must be 0 & vice-versa.

Boolean Expression :- $C = \bar{A}$

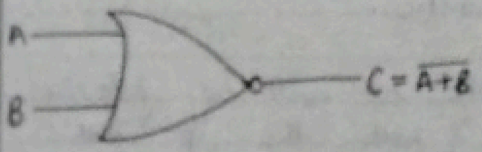
Teacher's Signature :



NAND Gate

Truth Table

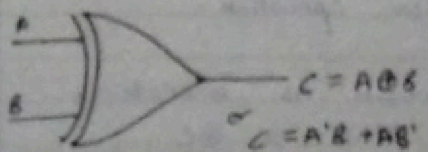
A	B	$C=\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



NOR Gate

Truth Table

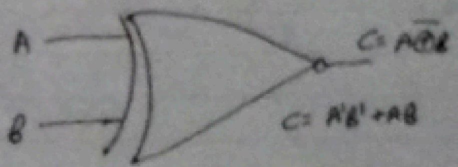
A	B	$C=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



XOR Gate

Truth Table

A	B	$C = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



A	B	$C = \overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

iv) NAND gate : It is the complement of AND Gate.

* The NAND Gate gives an o/p 0 if both i/p are 1. otherwise 1.

Boolean Expression :- $C = \overline{A \cdot B}$

v) NOR gate → It is the complement of OR gate.

* If both are same i.e 0. then otherwise 0 even in case of both i/p 1 each.

Boolean Expression :- $C = \overline{A+B}$

vi) XOR gate :- If both input are same then o/p is 0 otherwise 1.

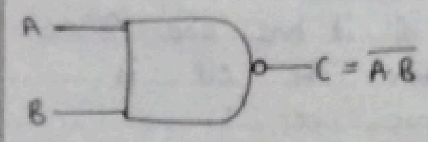
Boolean Expression :- $C = A \oplus B$

vii) XNOR Gate → It is also known as equivalence. It is the reverse of XOR gate.

If both i/p are same then true 1 otherwise false 0.

Boolean Expression :- $C = \overline{A \oplus B}$

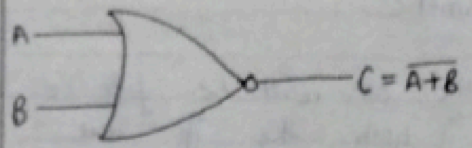
Teacher's Signature : ____________



NAND Gate

Truth Table

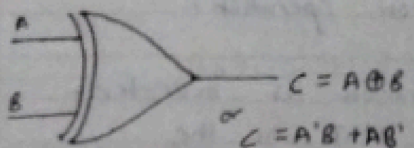
A	B	$C = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



NOR Gate

Truth Table

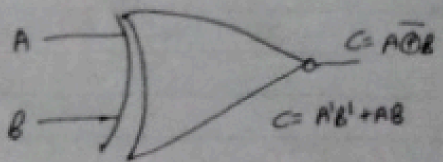
A	B	$C = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



XOR Gate

Truth Table

A	B	$C = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0



A	B	$C = \overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

iv) NAND gate :- It is the complement of AND Gate.

→ The NAND Gate gives an o/p 0 if both i/p are 1. otherwise 1.

Boolean Expression :- $C = \overline{A \cdot B}$

v) NOR gate → It is the complement of OR gate.

→ If both are same i.e 0. then otherwise 0 even in case of both i/p 1 each.

Boolean Expression :- $C = \overline{A+B}$

v) XOR gate :- If both input are same then o/p is 0 otherwise 1.

Boolean Expression :- $C = A \oplus B$

vi) XNOR Gate → It is also known as equivalence. It is the reverse of XOR gate.

If both i/p are same then true 1 otherwise false 0.

Boolean Expression :- $C = \overline{A \oplus B}$

Teacher's Signature : ____________

Date 05/01/21

Expt. No. 01 Page No. 05

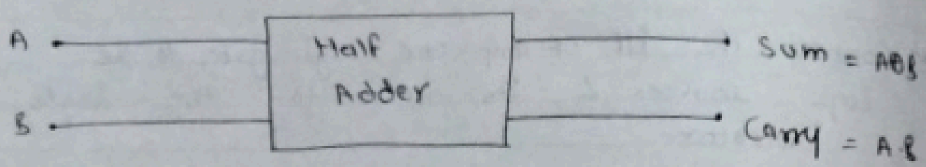
Procedure :

* Connect the trainer kit to ac power supply.
* Connect the i/p of any one logic gate to the logic sources & its o/p to the logic indicator.
* Apply various i/p combinationation & observe o/p for each one.
* Verify the truth table for each I/O combination.
* Repeat the process for all logic gates.
* Switch off the ac power supply.

Teacher's Signature :

Half - Adder

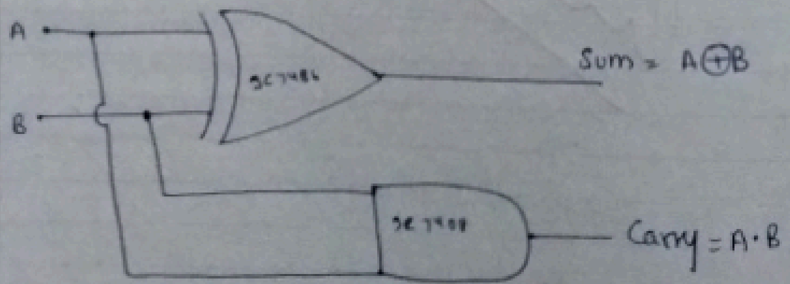
- Block Diagram



- Truth Table

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- Logic Diagram



Design & Implementation of full / half adder.

- Aim :- To design & very half & full adder using logic gates.

- Apparatus Required -

  IC 7404 (NOT) gate
  IC 7408 (AND Gate)
  IC 7486 (XOR Gate)
  IC 7432 (OR Gate)
  Patch cards & trainer Kit

- Theory :-

1) Half - Adder - It is a combinational circuit that performs the addition of two data bits, A & B.

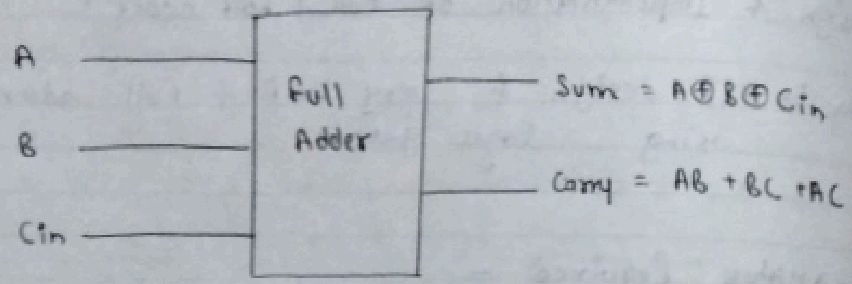
→ Addition will result in two o/p bits; 1 of which is the sum bit, S and the other is the carry bit, C.

→ The Boolean functions describing the half adder are -

$$Sum = a \oplus b$$
$$Carry = a \cdot b$$

Teacher's Signature : ____________

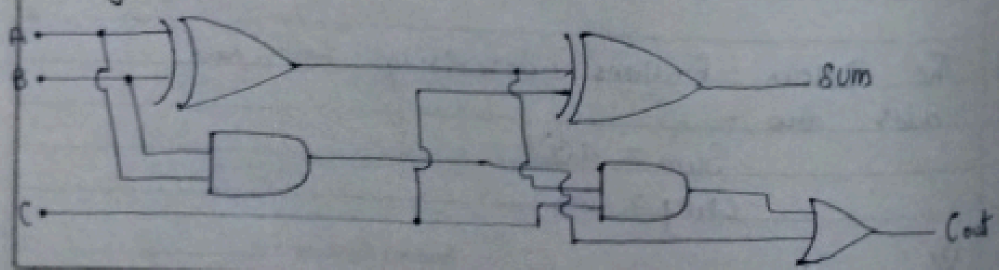
④ BLOCK DIAGRAM : FULL ADDER



• Truth Table

Input			Output	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

• Logic Diagram ·



2 Full Adder

The half adder does not take the carry bit from its previous stage into a/c.

* This carry bit from its previous stage is called Carry-in bit.

* A combinational logic circuit that adds two data bits, A & B. and a carry-in bit, Cin is called Full Adder.

⇒ Logical expression for sum

$A'B'C_{in} + A'BC_{in} + AB'C_{in} + ABC_{in}$

$C_{in}(A'B' + AB) + C_{in}(A'B + AB')$

C_{in} XOR (A XOR B)

⇒ K-map for carry

	00	01	11	10
0			1	
1		1	1	1

Carry = AB + BC + AC

Teacher's Signature :

Expt. No. 02 Date 19/01/21
Page No. 09

Procedure -

ⓐ Connections are given as per circuit diagram.

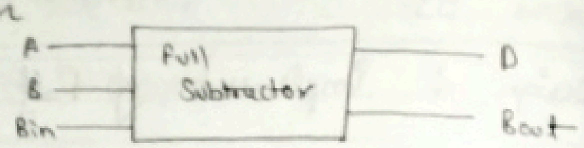
ⓑ Logical inputs are given as per circuit diagram

ⓒ Observe the output are verify the truth table.

Teacher's Signature :

b) Full-Subtractor -

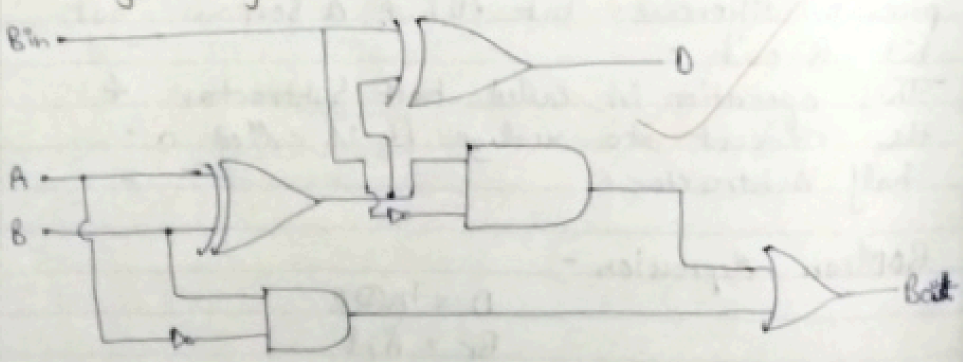
• Block Diagram



• Truth Table

Input			Output	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

• Logic Diagram



• K-Map for Bout -

A \ BBin	00	01	11	10
0		1	1	1
1			1	

Date 17/01/21

Expt. No. 03 Page No. 101

b) Full Subtractor -

It is a combinational circuit that perform subtraction of two bits A & B, with Borrow Bin & produce a difference (D), Borrow

• Boolean Expression -

$A'B'Bin + ABBin + AB'Bin' + ABBin$
$Bin(A'B' + AB) + Bin'(AB' + A'B)$
$Bin(A \text{ XOR } B)' + Bin'(A \text{ XOR } B)$
$Bin \text{ XOR } (A \text{ XOR } B)$
$(A \text{ XOR } B) \text{ XOR } Bin$

• Procedure -

i) Connections are given as per circuit diagram.

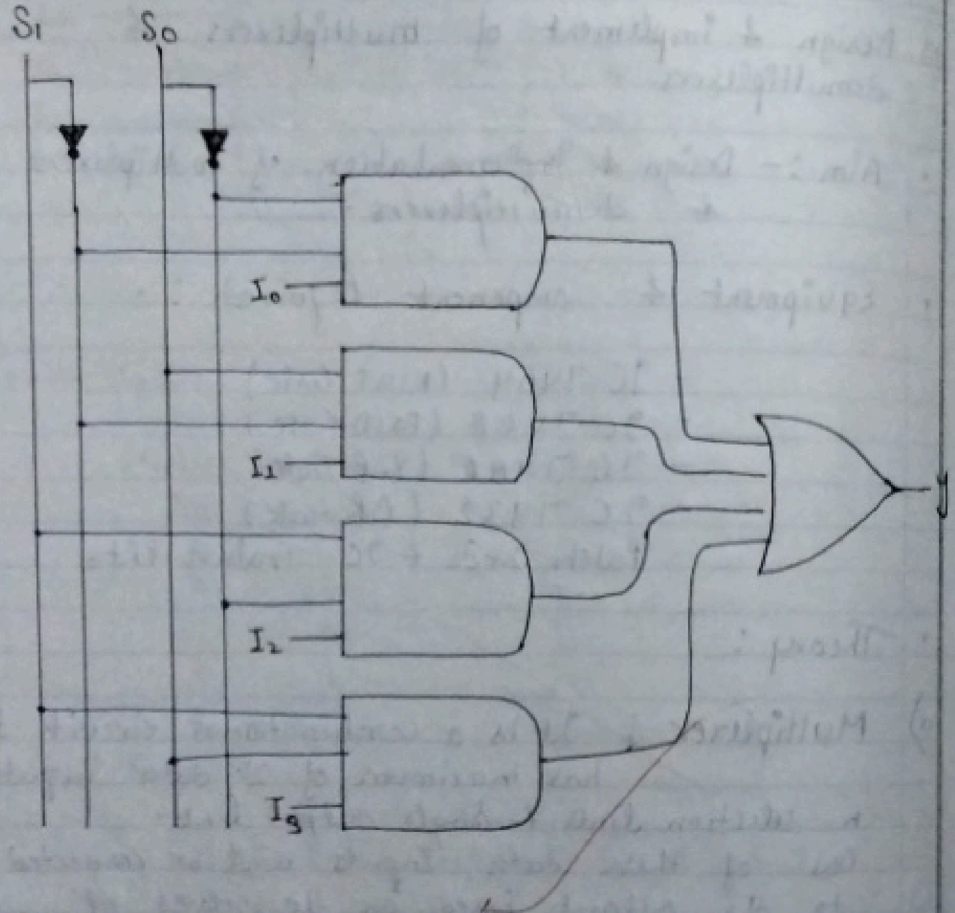
ii) Logical Input are given as per circuit diagram.

iii) Observe the output & verify the truth table.

$\boxed{Bout = A'Bin + A'B + BBin}$

Teacher's Signature : ____________

Fig: - Logic circuit of 4x1 multiplexer

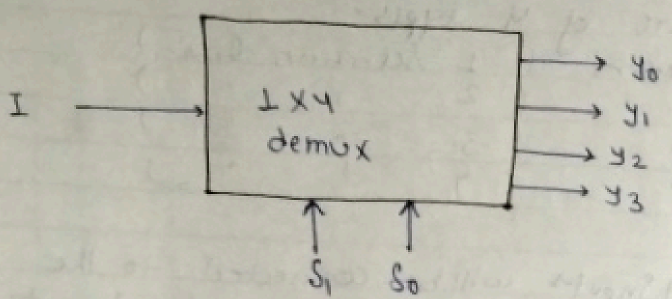


→ Multiplexers are of 4 types-

a) 2x1 multiplexers (1 Selection line)
b) 4x1 " (2 " ")
c) 8x1 " (3 " ")
d) 16x1 " (4 " ")

→ One of these 4 inputs will be connected to the output based on the combination of input present at these two selection lines.

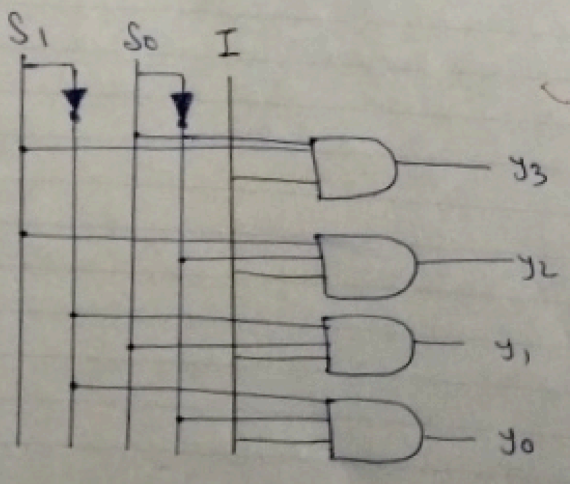
→ We can implement the Boolean function of 4x1 mux using inverters AND gates & OR gates.



• Truth Table

selection input		output			
S_1	S_0	y_3	y_2	y_1	y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

• Circuit diagram



2 **Demultiplexer** - It is a combinational circuit that performs the reverse operation of multiplexer. It has single input, "n" selection lines & maximum of 2^n outputs.
The input will be connected to one of these outputs based on the values of selection lines.

→ Since, there are 'n' selection lines there will be 2^n possible combinational of zeros & ones. so each combination can select only one output.
Demultiplexer is also called as DeMux.

1×4 De-Multiplexer - 1×4 demultiplexer has 1 input I, 2 selection lines S_1 & S_2 & 4 outputs y_3, y_2, y_1, y_0.

* The single input I will be connected to one of the 4 outputs, y_3 to y_0 based on the values of selection line S_1 & S_0.
we can implement these boolean functions using inverters & 3 inputs AND gates.

Teacher's Signature : ____________

Expt. No. 04

Date 22|01|21

Page No. 14

• Procedure -

1 check for the proper working of the Gate.
2 connect the circuit as per circuit diagram
3 verify it with truth table

Result 1 - Study of 4X1 mux & verify truth table.

Result 2 - Study of 1x4 demux & verify TT

Precautions -

1 All IC's should checked before starting the experiment.
2 All the connection should be tight.

3 Always connect the ground first & then connect Vcc.
4 Suitable type of wire should be used

5 The Kit should be off before change.

Teacher's Signature :