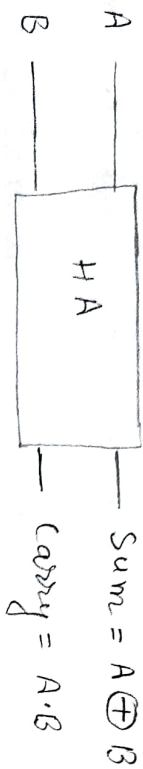


① Half-Adder

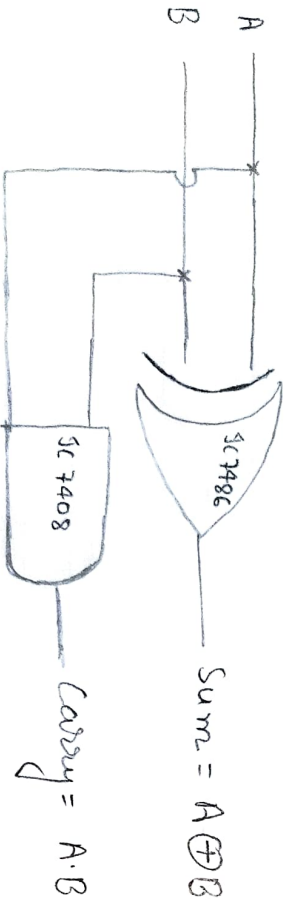
• Block diagram



• Truth table

| A | B | Sum | Carry |
|---|---|-----|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

• Logic diagram :-



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Page No.

* Design and Implementation of Full / Half adder.

- Aim:- To design and verify half and full adder using logic gates.

• Apparatus Required :-

- IC 7404 (NOT gate)
- IC 7408 (AND gate)
- IC 7486 (XOR gate)
- IC 7432 (OR gate)
- Patch cards and Trainer kit.

• Theory :-

- ① Half-Adder:- It is a combinational circuit that performs the addition of two data bits, A and B.

- Addition will result in two output bits; one of which is the Sum bit, S and the other is the carry bit, C.

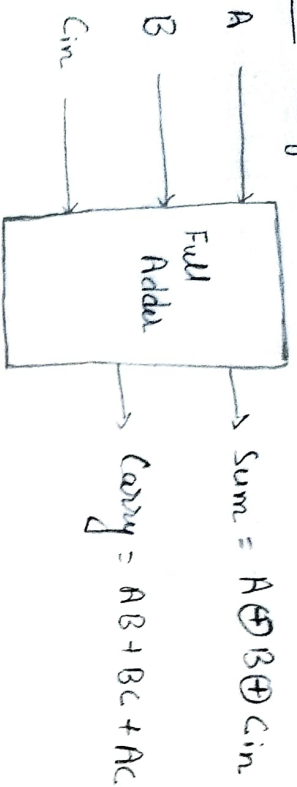
- The Boolean functions describing the half adder are:-

$$\text{Sum} = a \oplus b$$

$$\text{Carry} = a \cdot b$$

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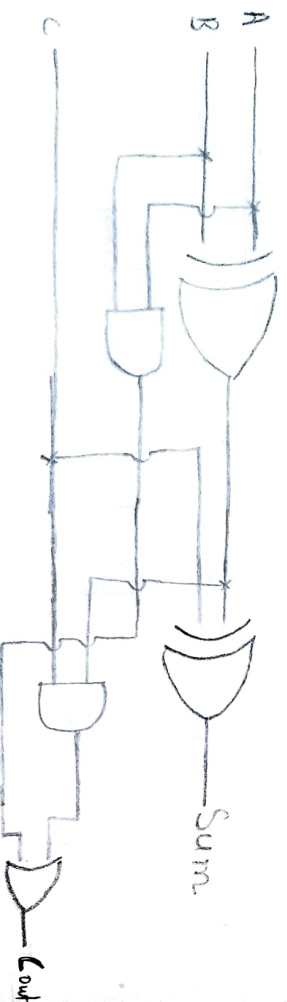
② Block Diagram :- (Full-adder)



• Truth Table :-

| Input | | | Output | |
|-------|---|-----|--------|-------|
| A | B | Cin | Sum | C-out |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

• Logic Diagram



② Full-Adder :- The half-adder does not take the carry bit from its previous stage into account.

→ This carry bit from its previous stage is called carry-in bit.

A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin, is called full adder.

• Logical expression for Sum :-

$$= A'B'C_{in} + A'B'C_{in} + A'BC_{in} + AB'C_{in}$$

$$= C_{in} (A'B' + A'B + A'C + AB)$$

$$= C_{in} \text{ XOR } (A \text{ XOR } B)$$

• K-map for carry :-

| A \ BC | 00 | 01 | 11 | 10 |
|--------|----|----|----|----|
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |

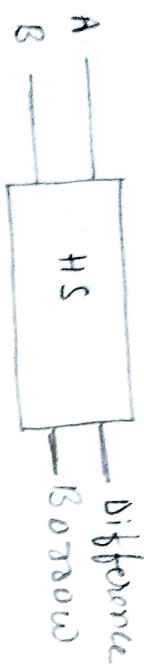
$$\text{Carry} = AB + BC + AC$$

- Procedure:-

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

@ Half-Subtractor

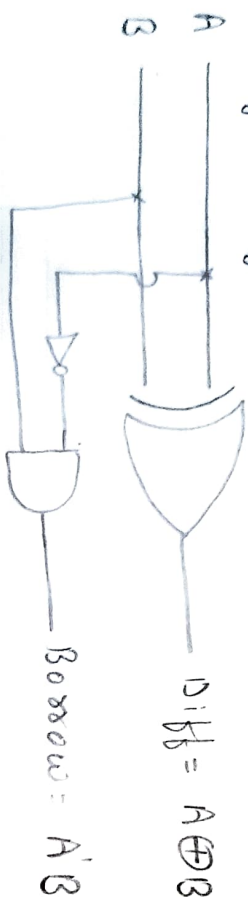
- Block Diagram:-



- Truth table

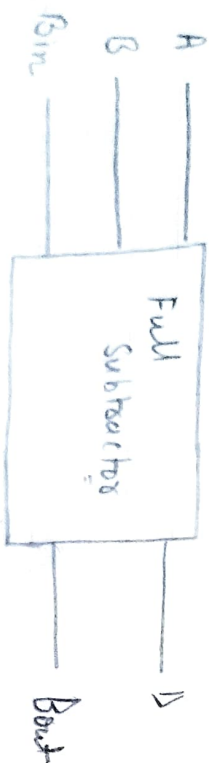
| A | B | Difference | Borrow |
|---|---|------------|--------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

- Logic diagram



- Full-Subtractor

- Block Diagram:-



Expt. No. 03

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Date _____

* Design and implement of half / full subtractor

- Aim:- To design and verify half and full subtractor using logic gates.

- Apparatus required:-

- 1 IC 7404 (NOT gate)
- 1 IC 7408 (AND gate)
- 1 IC 7486 (XOR gate)
- 1 IC 7432 (OR gate)
- Patch cords and IC trainer kit.

- Theory:-

(a) Half-subtractor:- Subtracting a single-bit binary value B from another A (i.e. A-B) produces difference bit D, and a borrow out bit B-out. This operation is called half-subtraction and the circuit to realize it is called a half-subtractor.

- Boolean expression:-

$$D = A \oplus B$$

$$B_o = \bar{A} \cdot B$$

- (b) Full subtractor:- It is a combinational circuit that perform

subtraction of two bits A and B, with Borrow, Bin and produce a difference D & Borrow.

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• Truth Table

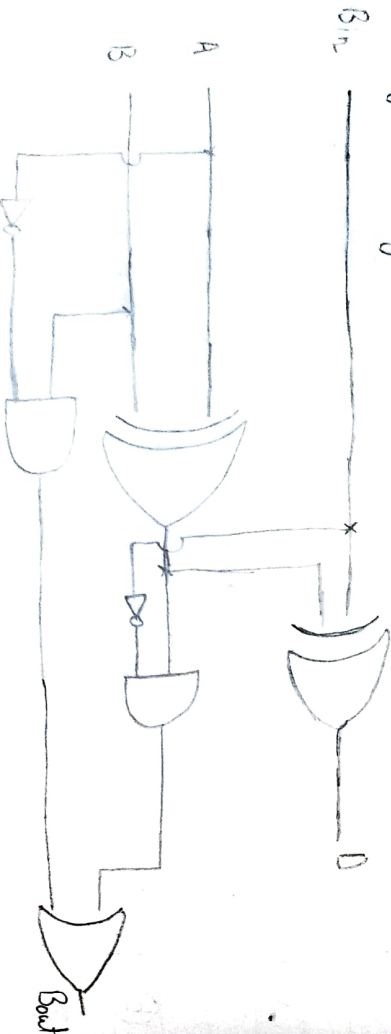
| Input | | Output | |
|-------|---|--------|------|
| A | B | D | Bout |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

• K-map for Bout

| AB | | 00 | 01 | 11 | 10 |
|----|---|----|----|----|----|
| 0 | 1 | | 1 | 1 | 1 |
| 1 | 0 | | | 1 | |

$$B_{out} = A'B_{in} + AB + BB_{in}$$

• Logic diagram :-



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• Boolean expression

$$\begin{aligned}
 &= A'B_{in} + AB_{in} + AB'B_{in} + AB_{in} \\
 &= B_{in}(A'B + AB) + B_{in}'(AB + A'B) \\
 &= B_{in}(A \times OR B) + B_{in}'(A \times OR B) \\
 &= B_{in} \times OR (A \times OR B) \\
 &= (A \times OR B) \times OR B_{in}
 \end{aligned}$$

• Procedure :-

- Connections are given as per circuit diagram.
- Logical inputs are given as per circuit diagram.
- Observe the output and verify the truth table.

Teacher's Signature : _____