UNIT-1

Introduction: Functional units of digital system and their interconnections, buses, bus architecture, types of buses and bus arbitration. Register, bus and memory transfer.

Processor organization: general registers organization, stack organization and addressing modes.

1.What is Bus? What are different types of Buses? Explain.
2.What is Bus Architecture? Explain.
3.Explain the following Bus:
i. ISA ii. EISA iii.MCA iv. SCSI v. AGP vi. PCI
4. What is register transfer language? Explain with suitable example ?
5. What is microoperation? Explain the arithmetic, logical, shift microoperation with example
6.Show the block diagram of the hardware that implements the following register Transfer statement:

yT2: R2 ←R1, R1 ← R2

7. Represent the following conditional control statement by two register transfer statements With control function.

If (P=1) then (R1←R2) else if (Q=1) then (R1←R3)

8. The following transfer statements specify a memory. Explain the memory operation in each case.

a. R2←M[AR]
b. M[AR] ← R3
c. R5 ←M[R5]

9. What is bus Arbitration? Explain serial and parallel bus arbitration?
10. Explain Register organization with Example.
11. Explain Stack organization with example.
12. A computer has 16 registers, an ALU (arithmetic logic unit) with 32 operations, and a shifter with eight operations, all connected to a common bus system.
a) Formulate a control word for a microoperation.
b). specify the number of bits in each field of the control word and give a general encoding scheme.
c). show the bits of the control word that specify the microoperation R4←R5+R6.

13). A bus-organized CPU has 16 registers with 32 bits in each, and an ALU and a destination decoder.
(a). How many multiplexers are there in the A bus, and What is the size of each multiplexer?
(b). How many selection inputs are needed for MUX A and MUX B?
(c). How many inputs and outputs are there in the decoder?
(d).How many inputs and outputs are there in the ALU for data, including input and output carries ?
(e).Formulate a control word for the system assuming that the ALU has 35 operations.

14. Explain Stack Organization with example?
15. Convert the following numerical arithmetic expression into reverse polish notation and

show the stack operation for evaluating the numerical result.

(3+4)[10(2+6)+8]

16.let SP= 000000 in the stack. How many items are there in the stack if:

a. FULL = 1 and EMTY = 0?

b. FULL= 0 and EMTY = 1?

17. A stack is organized such that SP always points at the next empty location on the stack. This means that SP can be initialized to 4000 and the first item in the stack is stored in location 4000. List the microoperations for the PUSH and POP.

18. Explain different functional unit of digital computer.

19.What is RPN?

20.Draw the block diagram for the hardware that implements the following statements

X+YZ:AR←AR+BR

Where AR and BR are two n-bit registers and x,y and z are control variables include the logic gates for the control function.

21.What is bus transfer?

22.Discuss the advantages and disadvantages of Polling and daisy chaining bus Arbitration schemes.

23.What do you mean by Processor Organization? Explain various types of Processor Organization.

24.What is wrong with the following register transfer statements?

a. xT: AR ← AR', AR ←0

b. yT: R1←R2, R1←R3

c. zT : PC ←AR, PC←PC+1

25. Write a program to evaluate the arithmetic statement:

X= A*[B+C*(D+E)]/F*(G+H)

(a).Using a general register computer with three address instructions.

(b).Using a general register computer with two address instructions.

©. Using an accumulator type computer with one address instructions.

(d).Using a stack organized computer with zero-address operation instructions

26. What is Addressing modes ? Describe different kind of Addressing modes ?

(27). A two- word instruction is stored in memory at an address designated by the symbol W. The address Field of the instruction (stored at W+1) is designated by the symbol Y. The operand used during the Execution of the instruction is stored at an address symbolized by Z. An index register contains the Value X. State how Z is calculated from the other addresses if the addressing mode of the instruction Is

a. Direct
b. Indirect
c. Relative
d. Indexed

(28). An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a).direct (b) immediate (C) relative (d) register indirect (d) Index with R1 as the index register.

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