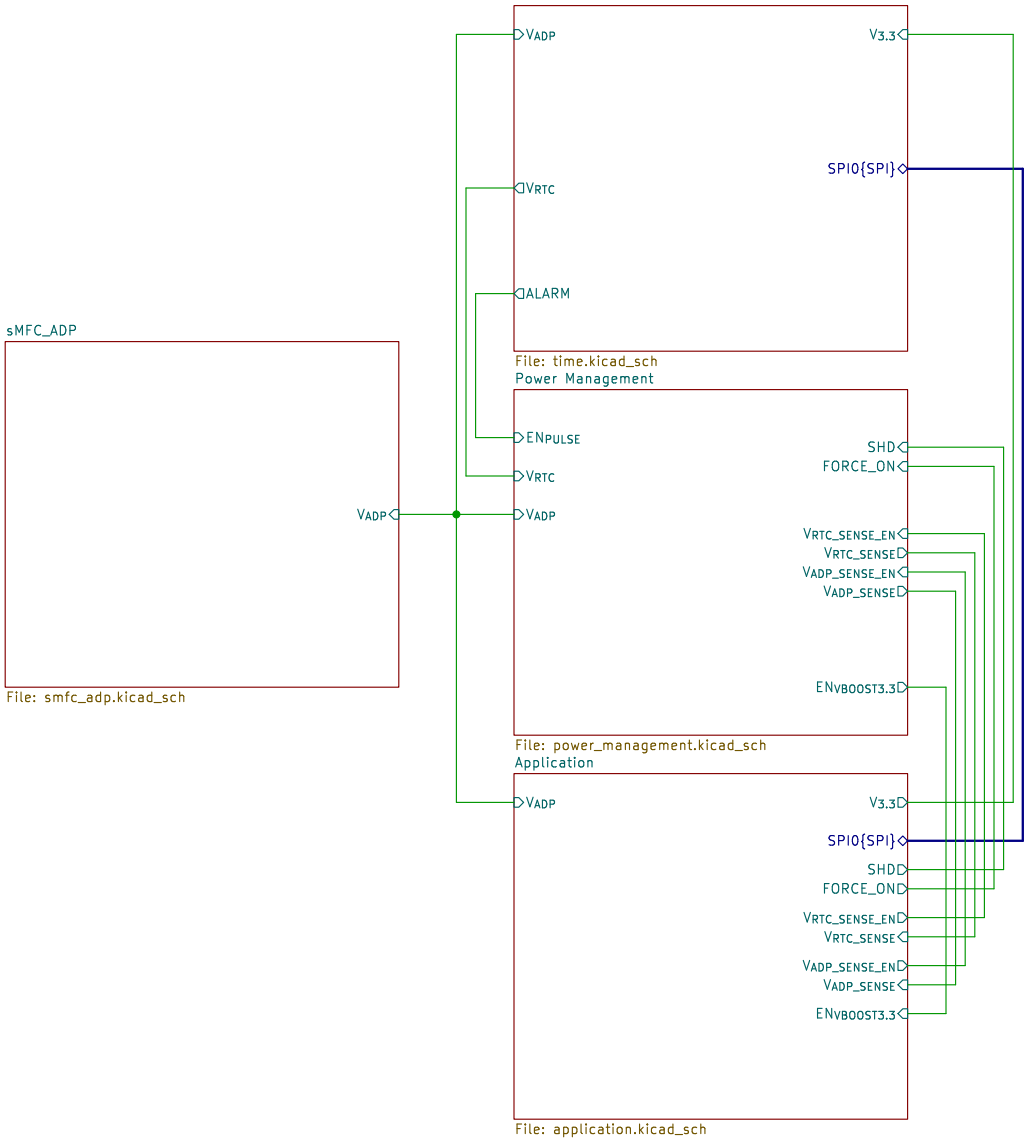


This is the implementation of Artemia as done for ASPLOS on breadboards.
Author: Gabriel Marcano
UC San Diego

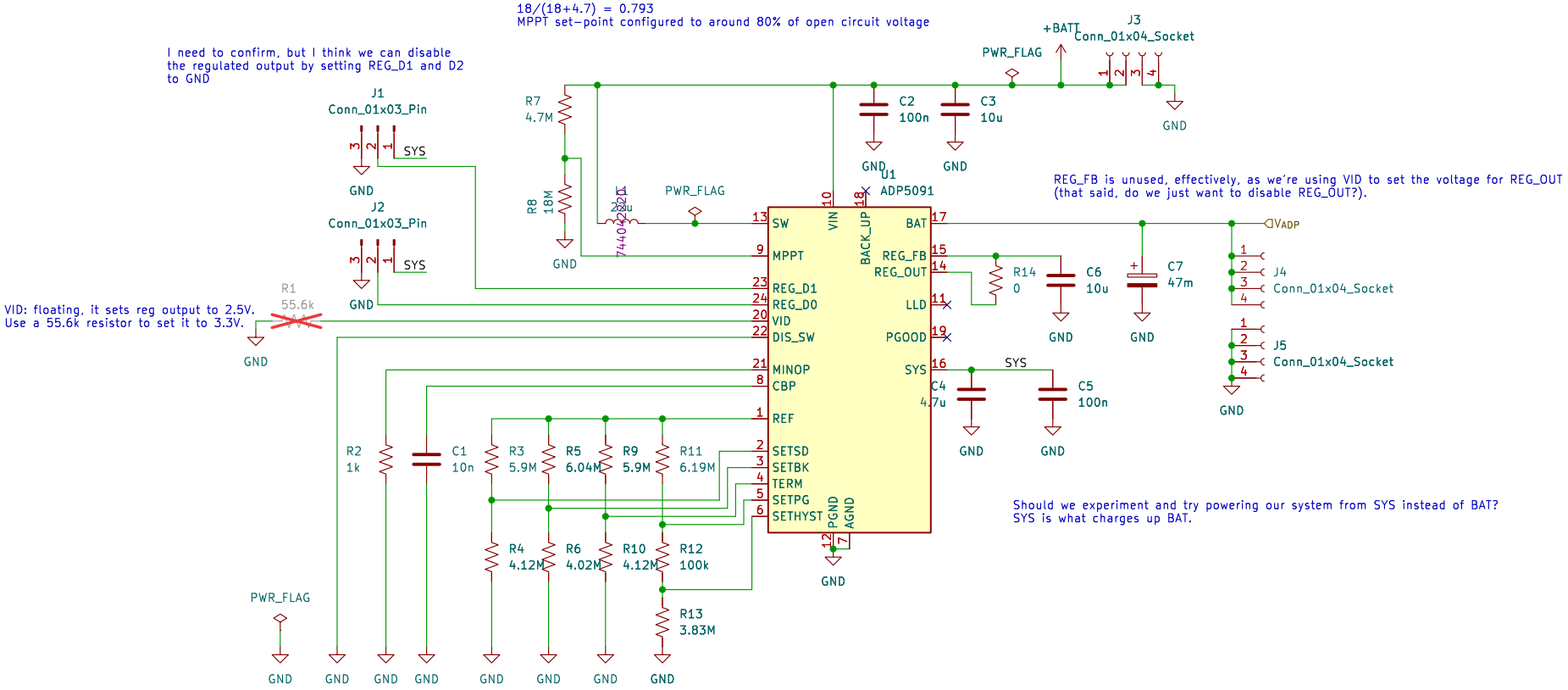
Sheet: /
File: artemia.kicad_sch

Title: Artemia

Size: USLetter	Date: 2023-09-13	**Rev: A**
KiCad E.D.A. kicad 7.0.8		Id: 1/6

This is the equivalent circuit of the ADP5091-1-EVALZ schematic, with the jumpers set to what we used for Artemia.

BAT is the lines coming from the sMFCs.



Settings for all of the control pins:
SETSD – Sets shutdown discharge voltage on BAT pin – ~1.011 * (5.9 / 4.12 + 1) = between 2.32, 2.59 V due to V_{INT_REF} tolerance
    While BAT voltage < SETSD setpoint, converter is in async mode
SETBK – Sets backup voltage enable threshold – ~ 1.011 * (6.04/4.02 + 1) = between 2.39 and 2.67 V due to V_{INT_REF}
    While BAT voltage < SETBK setpoint, backup battery is used
TERM – Sets max BAT voltage – 3/2 * ~1.011 * (5.9 / 4.12 + 1) = between 3.48, 3.89 V due to V_{INT_REF}
    Once BAT voltage reaches TERM, disables boost converter
SETPG – Set PGOOD falling threshold – ~1.011 * (6.19 / (0.1 + 3.83) + 1) = between 2.46, 2.75 V due to V_{INT_REF}
SETHYST – Set PGOOD rising threshold – ~1.011 * (6.19 / (0.1 + 3.83) + 1) = between 2.52 and 2.82 V due to V_{INT_REF}
    PGOOD goes high once SYS voltage goes above SETHYST setpoint, and low once it goes below SETPG threshold

Author: Gabriel Marcano
UC San Diego

Sheet: /sMFC_ADP/
File: smfc_adp.kicad_sch

Title: Artemia: Energy Harvester

Size: USLetter	Date: 2023-09-13	**Rev: A**
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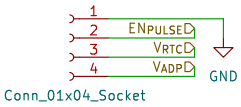
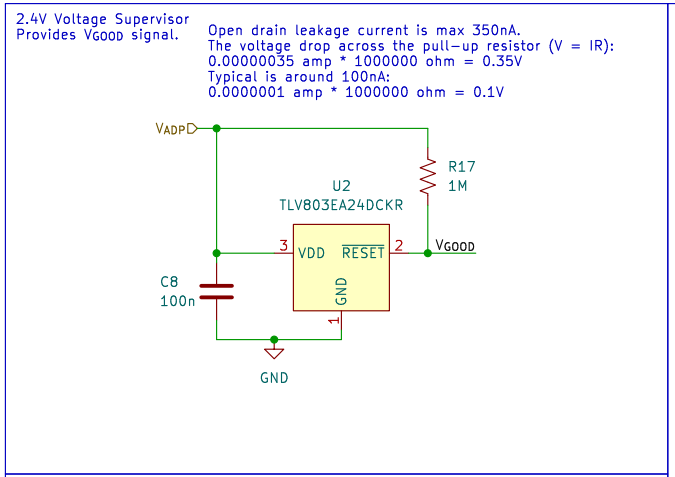
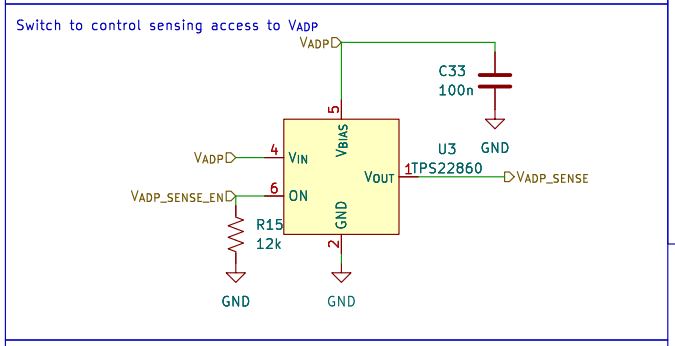
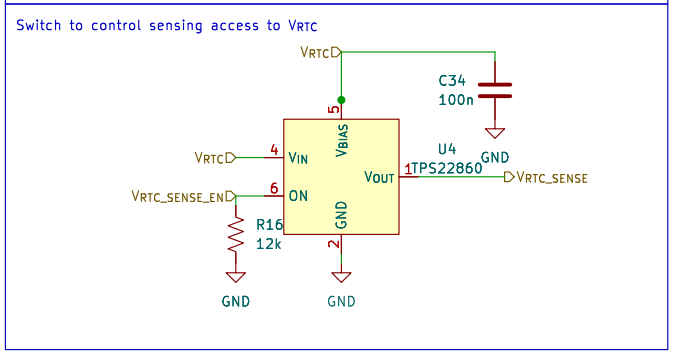
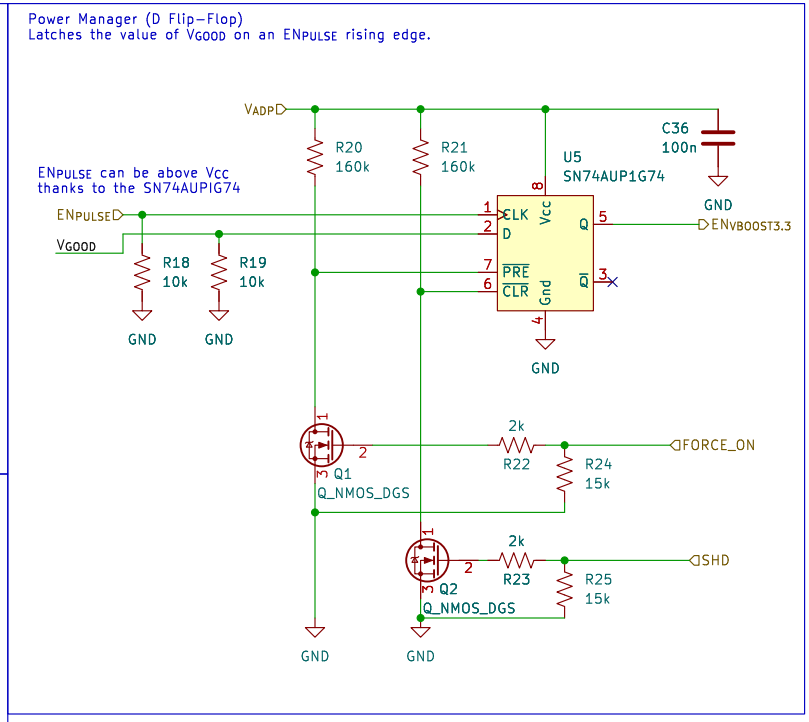
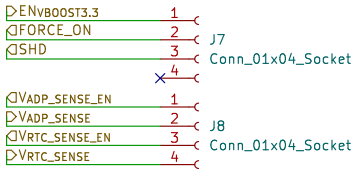












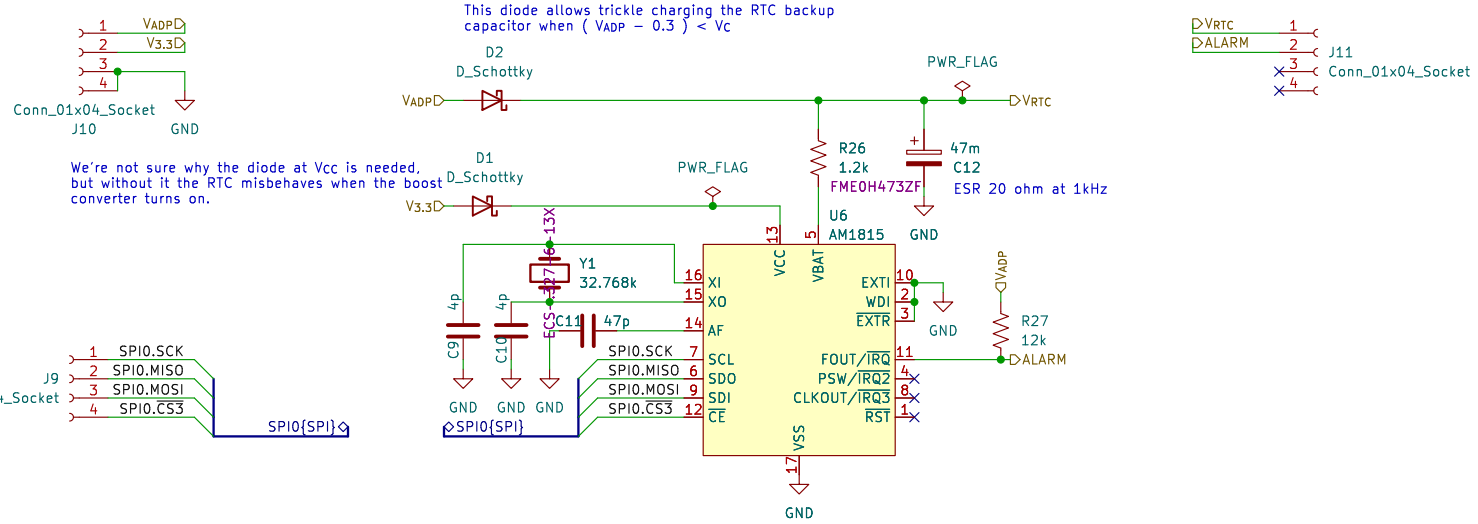
Author: Gabriel Marcano
UC San Diego
Sheet: /Power Management/
File: power_management.kicad_sch

Title: Artemia: Power Management

Size: USLetter	Date: 2023-09-13	**Rev: A**
KiCad E.D.A. kicad 7.0.8		Id: 3/6

This schematic capture of the Artasie RTC eval board is done partially from inspecting the board, our modifications, and the suggested circuit layout from Ambiq documentation.

In particular, the crystal network is unknown, exactly. Hardware design guide says caps aren't necessary, just use the internal calibration stuff to adjust the input capacitance, but the eval board uses two caps.



I've noticed something strange with Vcc with the diode in place. It looks like internally there may be something going on between Fout and Vcc. At very low Fout levels, I'm sometimes seeing traces of a voltage on Vcc and these are proportional to the voltage on Fout. Maybe we need to drive Fout from the battery??? That sounds wasteful.

What prompted this is that with the power supply, if I increased the voltage from 0 to 2V quickly in steps of 0.10V, at around 1.3V the system actually woke up for a second, and then the RTC completely forgets its state.

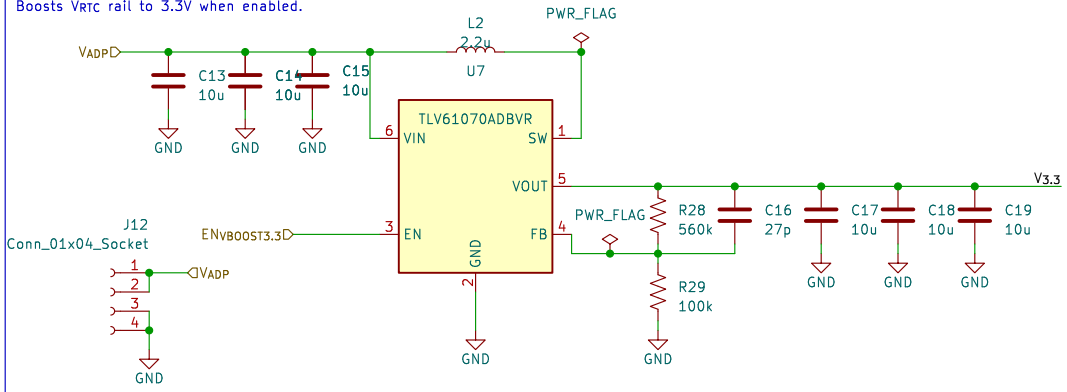
Author: Gabriel Marcano
UC San Diego

Sheet: /Time/
File: time.kicad_sch

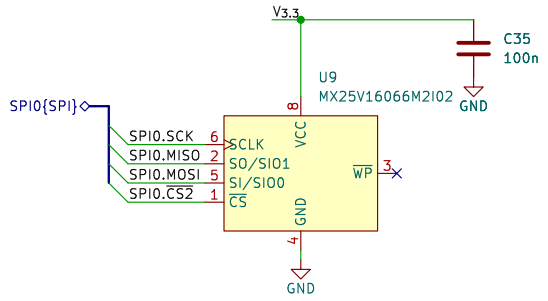
Title: Artemia: Time

Size: USLetter	Date: 2023-09-13	**Rev: A**
KiCad E.D.A. kicad 7.0.8		Id: 4/6

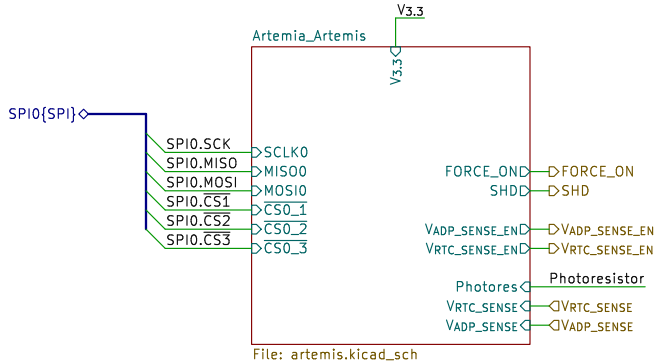
3.3V Boost Converter
Boosts VRTC rail to 3.3V when enabled.



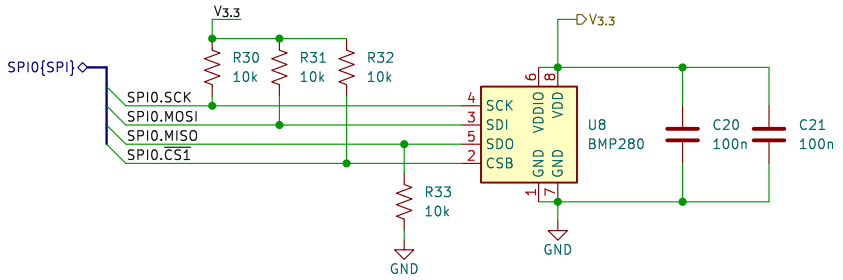
2 MB of Flash Memory



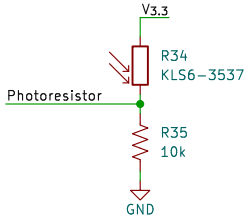
Sparkfun Redboard Artemis ATP
Application microcontroller using
an Ambiq Apollo3.

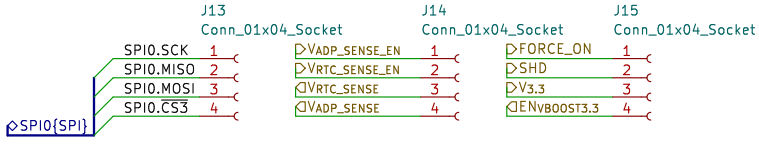


BMP280 temperature and atmospheric pressure sensor.



Light Intensity Sensor
Photoresistor in a voltage divider configuration.





Author: Gabriel Marcano
UC San Diego

Sheet: /Application/
File: application.kicad_sch

Title: Artemia: Application

Size: USLetter	Date: 2023-09-13	**Rev: A**
KiCad E.D.A. kicad 7.0.8		Id: 5/6

External 5V and 3.3V domain
Powered from USB

J16
USB_C_Receptacle_USB2.0
PWR_FLAG
VBUS
A4/B9
VBUS_5V
R38 5.1k
CC1
A5
CC2
B5
R39 5.1k
GND
D-
A7
D-
B7
USBDM
D+
A6
D+
B6
USBDP
SHIELD
GND
SBU1
A8
SBU2
B8
USB4105-GF-A
S1
A1/B12
GND

D3
LED
R40
1k?
GND
J17
Conn_01x02_Pin
VREG3.3

Internal 3.3V domain
Could be powered not from USB

D4
LED
R41
1k?
GND
J22
Conn_01x02_Pin
V3.3

J24
Conn_02x05_Odd_Even
V3.3
SWDIO
SWDCK
SWO
RESET
GND

U11
AP7366EA-33W5-7
VBUS_5V
IN
OUT
EN
GND
C25
1u
C27
1u
VREG3.3
J18
Conn_01x02_Pin
V3.3

U12
Sparkfun Artemis
C28
100n
C29
100n
V3.3
GND
VDD
SWDCK
A_RX
A_TX
SWDIO
SCLK0
MOSI0
CS0_2
MISO0
CS0_3
GPIO20/SWDCK
GPIO49/RX0
GPIO039
GPIO040
GPIO9
GPIO010
GPIO48/TX0
GPIO21/SWDIO
GPIO8
GPIO5
GPIO7
GPIO035
GPIO4
GPIO24
GPIO22
GPIO018
GPIO23
GPIO14
GPIO28
GPIO6
GPIO032
GPIO025
GPIO012
GPIO026
GPIO013
GPIO015
GPIO047/BOOT
GPIO033
GPIO034
GPIO011
GPIO029
GPIO019
GPIO018
GPIO016
GPIO017
GPIO031
GPIO041
GPIO045
GPIO2
GPIO1
GPIO0
GPIO043
GPIO042
GPIO3
GPIO036
GPIO038
GPIO037
GPIO044
XO
XI
nRESET
SWO
VRTC_SENSE
VADP_SENSE
Photores
CS0_1
VADP_SENSE_EN
VRTC_SENSE_EN
FORCE_ON
SHD
GPIO11 is CS0_0,
but also an ADC pin
Clock max drive level: 1uW
FIXME how to size load resistor? Do we need it?
R43
0
C31
4u
Y2
32.768k
C32
4u
ECS-327-16-19X
SW1
SW_SPST
C30
500n
RESET
RST has an internal pullup
and a debounce circuit already
J23
Conn_01x02_Pin
V3.3
BOOT
R42
10k
When BOOT is low,
bootloader skips programmer
I'm guessing internal pull-up resisto
due to GPIO pull up specified as 20k
Min reset pulse required = 4.5 ms.
RC constant = 500nC * 20kOhm = 1

VREG3.3
C24
100n
C26
100n
GND
U10
FT230XS
3V3OUT
VCC
VCCIO
TXD
RXD
RTS
CTS
CBUS0
CBUS1
CBUS2
CBUS3
USBDM
USBDP
RESET
GND
R36
27
R37
27
C22
47p
C23
47p
J19
Conn_01x02_Pin
A_RX
J20
Conn_01x02_Pin
A_TX
J21
Conn_01x02_Pin
RESET

Apparently the 47p caps on the USB
data lines aren't mandatory-- they
just seem to help with noise.

If there's no USB power, the jumpers connected to
the FT230XS should be disconnected.

Sheet: /Application/Artemia_Artemis/
File: artemis.kicad_sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 7.0.8
Id: 6/6