

Government College of Engineering, Amravati
(An Autonomous Institute of Government of Maharashtra)

Fourth Semester B. Tech. (Electronics and Telecommunication)

Summer – 2013

Course Code: ETU403

Course Name: Microprocessor and Interfacing

Time: 2 Hrs. 30 Min.

Max. Marks: 60

Instructions to Candidate

- 1) All questions are compulsory.
- 2) Assume suitable data wherever necessary and clearly state the assumptions made.
- 3) Diagrams/sketches should be given wherever necessary.
- 4) Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
- 5) Figures to the right indicate full marks.

**Q1 a) Specify the contents of H-L pair after executing 04
the following code snippet**

LHLD 3000h;	Address	Contents
MOV E,M;	3000	02
INX H;	3001	30
MOV D,M;	3002	00
LDAX D;	3003	30
MOV L,A;		
INX D;		
LDAX D;		
MOV H,A;		

**b) Justify the statement: “The ALE signal of 8085 04
plays a key role in preserving the contents of the
lower order address bus.”**

- c) Distinguish between TRAP and HOLD signals in 8085. 04

Q2 Solve any two

- a) Write an assembly language program to transfer a block of 5 elements from C000h to E000h. 06
- b) Write an assembly language program to find out the number of odd numbers present in a block of 5 elements. 06
- c) What are the similarities and differences in PUSH-POP and CALL-RET instructions and specify the contents of SP & PC after execution of the following code 06

LXI SP, 8000h;
CALL 2006h;
POP H;
LXI B, 4050h;
PUSH B;
RET;

- Q3** a) Distinguish between memory mapped IO and IO mapped IO scheme 06
- b) Expand the memory capacity up to 32KB using a 8KB memory chip whose starting address is 8000h. Specify the address map and draw the memory organization. 06

Q4 Solve any two

- a) Explain the serial data transmission and reception using SID and SOD lines with suitable example. 06

- b) Explain the Direct memory access data transfer scheme with the help of flowchart. 06
- c) Write a note on interrupts in 8085. 06

Q5

Solve any two

- a) Explain the transmitter and receiver section of USART. 06
- b) Explain the architecture of 8237 DMAC 06
- c) Draw Interface an 8-bit ADC 0809 with 8085 using 8255 PPI. The digital data is accepted on port A, port C is used for channel selection. The line PC3 Is used for sending the SOC pulse and EOC is read on PC7 06

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1 a) With an appropriate bit assignment, explain the PSW of 04 8085. Given below is a code snippet, write the step-wise execution and specify the contents of Accumulator and status flags:

MVI A, 45h;
MOV B, A;
STC;
CMC;
RAR;
XRA B;

b) ‘The ALE signal is an important factor in preserving the 04 contents of A0-A7 lines’; Justify the statement with suitable diagram.

Contd..

c) Contrast between the TRAP and HOLD signals of 8085.

2 Solve any two (2)

a) Write an assembly language program to find out the number of even numbers stored in an array of 10 numbers.

b) Draw and explain the opcode fetch machine cycle.

c) Execute the following code snippet sequentially and specify the contents of SP after execution of last instruction:

LXI SP, EFFFh;
CALL 3000h;
3000: LXI H, 3CF4h;
PUSH PSW;
SPHL;
POP PSW;
RET;

3 a) Expand the memory capacity upto 32KB using 4KB memory chip whose starting address is 0000h. Specify the address map and draw the memory organization.

b) Discuss the address space portioning schemes with the advantages and disadvantages.

4 Solve any two (2)

a) Explain with a suitable example, how the serial data transmission and reception is carried out in 8085?

b) Write a note on Interrupts in 8085.

c) Discuss the direct memory access data transfer scheme using flowchart.

5

Solve any two (2)

- a) Enlist the operating modes of 8253 Programmable timer/counter, and explain any three in details. 06
- b) Interface an 8-bit ADC 0809 with 8085 using 8255 PPI. 06
The digital data is accepted on port A, port C is used for channel selection. The line PC3 Is used for sending the SOC pulse and EOC is read on PC7.
- c) Discuss the operation of a DMA controller in a microprocessor system with suitable diagram 06

Government College of Engineering, Amravati
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Winter – 2014

Course Code: ETU403

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Time: 2 Hrs. 30 Min.

Max. Marks: 60

Instructions to Candidate

- 1) All questions are compulsory.
- 2) Assume suitable data wherever necessary and clearly state the assumptions made.
- 3) Diagrams/sketches should be given wherever necessary.
- 4) Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
- 5) Figures to the right indicate full marks.

- 1 a) Explain the bit pattern for flag register and specify the contents of accumulator and status flags after executing the following code

06

MVI A, 45h;

MOV B, A;

STC;

RAL;

06

- b) "It is very essential to preserve the contents of lower order address bus and the address latch enable signal plays an important role in doing so." Justify the statement with suitable example.

2 Solve any two (2)

06

- a) Draw and explain the timing diagram for 'MOV r1, r2' instruction.

06

- b) Write an assembly language program to count the number of even numbers present in an array of 10 elements.

06

- c) Differentiate the PUSH-POP pair with the CALL-RETURN pair of instructions and specify the step-by-step contents of SP and PC after execution of following snippet

LXI SP, C000h;

CALL 8006h;

POP H;

LXI B, A050h;

PUSH B;

RET;

- 3 a) Expand the memory capacity upto 8kB, using 2kB memory chips having initial address from 2000h.

06

- b) Write a subroutine to generate a delay of 1.5s using 8085 having a clock period of 0.33 μ s.

06

4

- a) Define data transfer scheme and explain the direct memory access data transfer scheme using flow chart. 06

- b) What do you mean by serial data transfer? Explain with a suitable example how data can be serially transmitted or received in 8085? 06

5

Solve any two (2)

- a) Discuss the working of a DMAC operates in a microprocessor system with suitable example. 06

- b) Interface an 8-bit ADC0809 with 8085; digital data accepted on port B, port C used for channel selection PC3 used for sending SOC and PC7 used to read EOC. 06

- c) Explain the transmitter and receiver section of USART 06

Government College of Engineering, Amravati
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B. Tech. Fourth Semester
(Electronics and Telecommunication Engineering)

150 04056 .

Summer - 2017

April 15

Course Code: ETU403

Course Name: Microprocessor and It's Interfacing

Time: 2 hr. 30 min.

Max. Marks: 60

Instructions to Candidate

- 1) All questions are compulsory; solve any two sub-questions from Q2.
 - 2) Assume suitable data wherever necessary and clearly state the assumptions made.
 - 3) Diagrams/sketches should be given wherever necessary.
 - 4) Use of logarithmic table, drawing instruments and non programmable calculators is permitted.
 - 5) Figures to the right indicate full marks.
1. a) i. Classify the given instructions on the basis of 08 length ADD D, ADI 25H, DCR C, MOV A, B
ii. What is the duration of one T-state in the 8085 microprocessor that uses a crystal of 5 MHz?
iii. An 8085 microprocessor based system uses a $4k \times 8$ bit RAM whose starting address is AA00 H. What will be the address of last byte in this RAM?
iv. How the content of accumulator in an 8085 microprocessor is altered or not after execution of the following instructions
CMP C, CPI 3A, ANI 5C and ORA A

- b) Consider an 8085 microprocessor system, the 04 following program starts at location 0100H
- LXI SP, 00FF
LXI H, 0107
MVI A, 20H
SUB M
- What will be the content of accumulator when the program counter reaches 0109H?
 - If in addition code exists from 0109H onwards ORI 40H, ADD M. What will be the result in the accumulator after the last instruction is executed?
2. a) Explain the interrupts TRAP, INTR, RST 7.5 and 06 RST 6.5.
- An 8085 assembly language program is given below. The execution time of each instruction is given against the instruction in terms of T-state. What is the execution time of program in terms of T-states?
- | Instruction | T-state |
|----------------|---------|
| MVI B,0AH | 7T |
| LOOP:MVI C,05H | 7T |
| DCR C | 4T |
| DCR B | 4T |
| JNZ LOOP | 10T/7T |
- b) Design a seven-segment LED output port with the 06 device address F5H, using 3-to-8 decoder, 4-input NAND gate, a NOR gate and a common-anode seven-segment LED. Write a program to display digit 7 at the output port.
- c) Two unsigned binary numbers are stored at 06 consecutive data memory locations X, X+1. Write a program for computing $(X+1) - X$. The magnitude of the result should be stored at Y and

the sign (00 if positive, 01 if negative) at Y+1.

3. a) Write a program to exchange the contents of 06 memory location X, X+1 with the contents of Y and Y+1. Use minimum number of instructions. 06
- b) Explain the serial data transfer scheme in 8085 06 through SID and SOD lines using RIM and SIM instructions.
4. a) Draw and explain mode register format of 8251. 04
- b) Explain the function of 8255 pins that are used for 04 interfacing with microprocessor.
- c) What is FIFO/sensor RAM? Describe its use in 04 8279. Explain how a location of FIFO/sensor RAM can be read?
5. a) Interface a temperature sensor using an A/D converter and port A of 8255. Write instruction to read the temperature so that fan and heater is controlled. If temperature is less than 10°C, turn on heater and if temperature is higher than 35°C, turn on fan. 08
- b) How to interface DAC 0808 with 8085 04 microprocessor.

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- 5) Figures to the right indicate full marks.

Q1 a) Discuss the HOLD and interrupt signal in 8085 04 and distinguish between them.

b) Explain the bit pattern for flag register and specify 04 the contents of accumulator and status flags after executing the following code

MVI A, 45h;
MOV B, A;
STC;
RAL;

c) Draw the architecture of 8085 and explain the sequential execution of an instruction 04

Q2

Solve any two

- a) Discuss the addressing modes of an 8085 06 instruction set with suitable example.
- b) Write an assembly language program to find out 06 the number of 1's present in an 8-bit number stored in accumulator.
- c) Draw and explain the opcode fetch machine cycle. 06

Q3

- a) Write a subroutine to generate a delay of 1.5s 04 using 8085 having a clock period of $0.5\mu s$.
- b) Explain the mechanism used for preserving the contents of lower order address/data bus when being used to carry the data. 04
- c) A system needs 4KB of EPROM and 4KB of 04 RAM. The EPROM address starts at 0000h and the RAM address starts at 2000h, the available chips are 2KB EPROM and 2KB RAM. Draw the organization of memory interfaced with 8085.

Q4

Solve any three

- a) Define interrupt in 8085 and explain the 04 categories in which the interrupts can be classified.
- b) What do you mean by the data transfer scheme? 04 Explain the interrupt driven data transfer scheme with flow-chart.
- c) Explain the serial data transmission /reception in 04 8085 with suitable example.

d) Explain the BSR mode of 8255 PPI.

04

Q5

Solve any two

- a) What are the various modes of operation of IC 8253, explain any three with waveforms. 06
- b) Discuss the operation of a DMA controller in a microprocessor system with suitable diagram. 06
- c) Draw Interface an 8-bit ADC 0809 with 8085 using 8255 PPI. The digital data is accepted on port A, port C is used for channel selection. The line PC3 Is used for sending the SOC pulse and EOC is read on PC7. 06