Government College of Engineering, Amravati

(An Autonomous Institute of Government of Maharashtra)

Seventh Semester B. Tech.
(Computer Science and Engineering)

Winter – 2017

Course Code: CSU702

Course Name: Microprocessor & Interfacing

Time: 2 Hrs. 30 Min. **Max. Marks: 60**

Instructions to Candidate

1) All questions are compulsory.
2) Assume suitable data wherever necessary and clearly state the assumptions made.
3) Diagrams/sketches should be given wherever necessary.
4) Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
5) Figures to the right indicate full marks.
6) (Other special instruction, if any)

1. **Solve: (any two)**

a) Draw the architectural diagram of 8086 and explain the function of each block in detail. **6**

b) Explain the use of segmentation in different applications. Explain how segmentation provides effective task switching mechanism. **6**

c) Explain the following signals **6**

i) $\overline{DEN}$ ii) $\overline{LOCK}$ iii) $\overline{BHE}$ iv) $\overline{RQ}/\overline{GT}$

Contd..

2. **Solve: (any two)**

a) Draw the block diagram of 8255 and explain each block. 6

b) What is BSR mode of operation? How it is useful in controlling the interrupt initiated data transfer for mod1 and mode2? 6

c) Suppose that the beginning address of an 8255 is 0900H and write a program sequence that will, (i) Put both groups A and B in mode 0 with ports A and C being input ports and port B as an output port. (ii) Put group A in mode 1 with port A being an input and PC6 and PC7 being outputs and group B in mod 1 with ort B being an input. 6

3. **Solve: (any two)**

a) Explain the importance of 8259 interrupt controller and explain how it handles the interrupt. 6

b) Interface 8259 with 8086 at address 074X. Write an alp to initialize 8259 in single level triggered mode with call address interval of 4 non buffered, no special fully nested modes. Then set the 8259 to operate with IR6 masked. IR4 as bottom priority level with special EOI mode 6

c) Draw & explain in detailed the functional block diagram of 8254 6

4. **Solve**

a) Will it be possible to interface more than 16 7-segment display units using 8279? If yes then justify the answer. 6

b) What do you mean by cascade operation of 8237? Why it is required? **6**

5. **Solve in one statements:** **12**

i) What is T-state?

ii) What are the operations performed by logical instructions?

iii) What is difference between CALL and JUMP instruction?

iv) What is vector table? Where is it located?

v) What is the need for an interrupt controller?

vi) How is 8259 programmed?

vii) Write the format of ICW1 of 8259.

viii) What is synchronous data transfer scheme?

ix) What are the operating modes of port-A of 8255?

x) How is DMA initiated?

xi) What are the programmable registers of 8237?

xii) What is USART?