Government College of Engineering, Amravati
(An Autonomous Institute of Government of Maharashtra)

Sixth Semester B. Tech.
(Computer Science and Engineering)

Summer – 2016

Course Code: Switching Theory and Logic Design

Course Name: CSU601

Time: 2 Hrs. 30 Min. **Max. Marks: 60**

Instructions to Candidate

1) All questions are compulsory.
2) Assume suitable data wherever necessary and clearly state the assumptions made.
3) Diagrams/sketches should be given wherever necessary.
4) Use of logarithmic table, drawing instruments and non-programmable calculators is permitted.
5) Figures to the right indicate full marks.

1. **Solve any two:**

(a) Show type classification available in VHDL and explain scalar data type in brief. 6m

(b) Explain case, wait and loop sequential statements in detail with example. 6m

(c) Design VHDL code for 9 bit parity generator circuit 6m

2. Solve:

(a) Write short note on: 4m
i) Explicit visibility with clauses
ii) Operator overloading

(b) Write VHDL code for: 8m
i) 1bit full adder using dataflow modeling
ii) synchronous D-type flip-flop triggered on the rising edge of the clock signal using behavioural modelling

3. **Solve:**

(a) Simplify the following Boolean function: 4m
$F(A,B,C,D) = \Sigma_m(1,2,4,7,8,11,13,14)$

(b) Find all the prime implicants for the Boolean functions given and determine which are essential PI $F(A,B,C,D) = \Sigma m(0,1,3,4,5,7,13,15)$, using Tabulation method 6m

(c) Prove that the compliment of a function is equal to complementing a function using dual method. 2m

4. **Solve any one:**

(a) Design BCD to 7 segment LED code convertor. 12m

(b) (i) Design BCD to Excess-3 code convertor 6m

(ii) Design VHDL code for 3:8 decoder using Data flow modeling and logic circuit along with its truth table 6m

5. **Solve**

(a) Design 3 bit synchronous up counter using J-K flip flop. 6m

(b) What are shift register? Explain bi-directional shift register with parallel load in detail 6m

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1. Solve any two:

(a) Explain the following sequential statements: if, case, null and exit. 6m

(b) Design VHDL code for 9 bit parity generator circuit 6m

(c) What are signal assignment statements? Elaborate them in detail. 6m

2. Solve:

(a) Write down VHDL code for given circuits: 6m
   i) 1 bit full adder using mixed modeling.
   ii) 2:4 decoder using behavioural modeling.

Contd..

(b) Write short note on: 6m
i) Functions
ii) Overloading & Visibility
iii) Use clause & Generic constants.

3. Solve:

(a) Simplify the following Boolean function: 6m
i) $F(w,x,y,z)= \Sigma_m(0,1,2,4,5,8,10,12,14)$
ii) $F(a,b,c,d)= \Sigma_m(0,2,6,8,12,13,15)+d_m(3,4,9)$

(b) Minimize the given logic functionusing Tabulation method and determine Prime implicants& essential PI, 6m
$F(A,B,C,D)= \Sigma_m(0,1,2,3,5,7,8,10,12,13,15)$

4. Solve any two:

(a) Design BCD to Excess-3 code convertor 6m

(b) Explain Adders in detail with its types and implementation. 6m

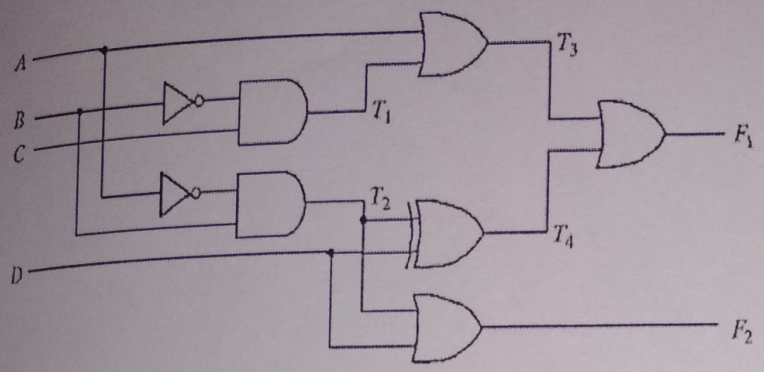
(c) Consider the combinational circuit shown below: 6m
i) Derive the Boolean expressions for T_1 through T_4. Evaluate the outputs of F_1 and F_2 as a function of the four inputs.
ii) List the truth table with 16 binary combinations of the four inputs variables. Then list the binary values for T_1 through T_4 and outputs F_1 and F_2 in the table.
iii) Plot the output Boolean functions obtained in part on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).

A
B
C
D

5. (a) Solv
Des
flip

(b)
Expl
as it

(c)
Wha
brief



5. (a) Solve any two: 6m

Design 3 bit synchronous down counter using T flip flop.

(b) 6m

Explain synchronous counters with BCD counter as its type.

(c) 6m

What are shift register? Explain serial transfer in brief with example.