**Government College of Engineering, Amravati**
**Department of Computer Science and Engineering**
CLASS TEST-II (Winter 2015) B. Tech. Second Year
**Course**: Electronic Devices and Circuits **Code**: ETU311 **Time**: 1 hrs. **Marks**: 15

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**Note: 1. Solve any three of the following. (5 marks each)**
**2. Assume the data whenever necessary.**

**Que1.** What is the use of multistage amplifier? Hence explain working of RC coupled transistor amplifier with its frequency response.

**Que2.** Analyze the transistor hybrid model for common emitter configuration to find out h-parameters.

**Que3.** What is biasing? What are the different biasing methods for JFET? Hence explain self bias method for n-channel JFET to find out of $I_D$ and $V_{DS}$.

**Que4.** A JFET has a) $I_D = 15mA$, $I_{DSS} = 25mA$ and $V_P = 5V$, find $V_{GS}$. (2 marks)
b) $I_D = 2.5mA$, $I_{DSS} = 10mA$ and $V_P = -4.5V$, find transconductance $g_m$. (3 marks)

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$h_{11} = h_{ie}$
$h_{12} = h_{re}$
$h_{21} = h_{fe}$
$h_{22} = h_{oe}$

**Government College of Engineering, Amravati**
**Department of Information Technology**
**Class Test-II (W-17)**

**Sub: ETU 311 COA** **Marks: 15** **Time: 1 hour**

**Solve Any Three**

*Q.1 Explain working of Common base Amplifier with its input and output characteristics.*

*Q.2 How operating point is ensured/ calculated in Voltage divider biasing method? Explain with diagram.*

*Q.3 Explain working of RC coupled amplifier with its advantages and limitations.*

*Q.4 Derive the expression for Input impedance and Voltage gain for Common emitter configuration using H-parameter model.*



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**Government College of Engineering, Amravati**

Department of Information Technology

Class Test-II

Course Code: ETU311 Date: 07/10/2016

Course: Electronic Devices and Circuits Time: 9:00-10:00AM

Note: Attempts any three from Q.1 to Q.4 Max. Marks: 15

**Q.1** Describe in brief working of n-channel JFET. Also draw its V-I Characteristics. 5

**Q.2** Derive general expression for stability factor .Determine Q point and stability factor of the shown figure 1 , assume transistor to be a silicon transistor and $\beta$=100 5

**Q.3** Derive the expression of Ic and $V_{CE}$ for voltage divider bias with neat diagram. If $R_1$=47K, $R_2$=6.2K, $R_C$=2.7K, $R_E$= 1.5K, $\beta$=100, $V_{CC}$=20V. Calculate $I_C$, $I_B$, $V_{CE}$, and $V_E$. 5

**Q.4** Differentiate JFET and MOSFET. Also define the transconductance, drain resistance and amplification factor of FET. 5

10} and a relation R on S where

A + B