

GOVERNMENT COLLEGE OF ENGINEERING, AMRAVATI
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
CLASS TEST 1- SUMMER 2019

COURSE CODE: CSU602 – Operating System and Design TIME: 1hr

MAX MARK: 15

Solve any Two. Each question carries 5 marks.

Q1. Define Operating System? Explain in brief various services of operating system with example

Q2. What is the need of system call? List and explain the different categories of System call with example.

Q3. Draw and explain UNIX system structure

Solve

Q4. Consider the following five processes Compute and prepare comparison chart for waiting time, Turn Around Time of each process for FCFS,SJF,RR(Q=2)

Process	P0	P1	P2	P3	P4
Arrival Time	2	4	8	6	0
Burst time	5	9	6	3	8

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CSE Dept. – Summer 2018

CT- I

Course Name - STLD

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Q.1] Name and Explain the statement available in VHDL that suspends the execution of a process. [3m]
Solve any three: [4m each]

- Q.2] Mention data objects available in VHDL and describe them in short with proper example.
- Q.3] Design VHDL code for AND-OR invert circuits.
- Q.4] What is a loop statement? Justify its iteration scheme types with the help of factorial example.
- Q.5] Write down VHDL code for Hierarchical 1 bit Full adder circuits.

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Q.1] Specify the use of assertion & report statement in VHDL

[2m]

Q.2] Write down VHDL code for 1 bit full adder

[3m]

Q.3] What is delay model? Explain its types in detail

[5m]

Q.4] Solve any one:

[5m]

A) Design VHDL code for 9 bit parity generator circuit

B) How many operators are available in VHDL? Evaluate each in detail with a proper example