# Government College of Engineering, Amravati

**(An Autonomous Institute of Government of Maharashtra)**

## Fourth Semester B. Tech.
## (Computer Science and Engineering)

**Summer – 2016**

**Course Code: ETU411**

**Course Name: Analog and Digital IC'S**

**Time: 2 hr. 30 min.** **Max. Marks: 60**

**Instructions to Candidate**

1) All questions are compulsory; solve any two sub-questions from **Q2.**
2) Assume suitable data wherever necessary and clearly state the assumptions made.
3) Diagrams/sketches should be given wherever necessary.
4) Use of logarithmic table, drawing instruments and Non-programmable calculators is permitted.
5) Figures to the right indicate full marks.

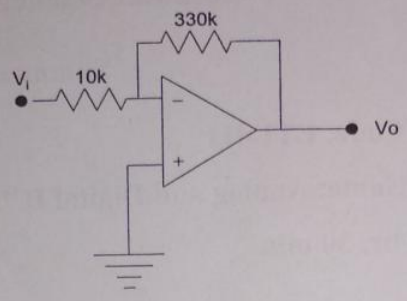
**1** a) **i.** An op-amp has an output signal of 2V for an input of 50mV. Find its $A_v$ and $A_{v\,(\text{in dB})}$? **08**

**ii.** The input signal Vi is 0.04 sin $1.13\times10^5$t (V) is to be amplified to the maximum extent. How much maximum gain can be had by using op-amp with slew rate of 0.4 V/ μsec?

**iii.** Which oscillator is used in the audio range from 20Hz to 100 kHz and what is $\left|\frac{d\phi}{d\omega}\right|$ for an ideal oscillator?

**iv.** Why hysteresis is desirable in a Schmitt trigger?

b) Determine whether the output will be distorted due to slew rate limitation in each case as shown in below. The operational amplifier has a slew rate of 0.5V/μsec. **04**




**4.**

i. $V_1 = 0.01 \sin 10^6 t$ (V)
ii $V_2 = 0.05 \sin 350 \times 10^6 t$ (V)
iii $V_3 = 0.1 \sin 200 \times 10^3 t$ (V)
iv $V_4 = 0.2 \sin 50 \times 10^3 t$ (V)

**5.**

**2.** a) Explain the working of a Wien bridge oscillator. Derive the expression for the frequency of operation. **06**

b) With the help of neat diagram and waveform, explain positive and negative clipper circuit using op-amp. **06**

c) Explain with waveforms how IC 555 function as astable multivibrator. **06**

**3.** a) **i.**In the given logic equation **04**
$A(A+\bar{B}\bar{C}+C) + \bar{B}(\bar{C}+\bar{A}+BC) + (A+\bar{B}C+A\bar{C}) = 1$,
If $C = \bar{A}$ then find simplified form of it.
**ii.**Find the minterms expansion of $f(P, Q, R) = PQ + Q\bar{R} + P\bar{R}$

b) Minimize the following function in both SOP and POS forms using K-maps **04**
$\Sigma$ m(1,3,4,7,11) + d(5,12,13,14,15)

c) Implement $f$ (X,Y,Z) = $\Sigma$ m(0,3,4,5,7) using NOR logic. **04**

**4.** a) Implement the following Boolean function using 8:1 multiplexer. **06**
F(A,B,C,D)=$\overline{A}\,\overline{C}\,D + \overline{B}CD + \overline{A}\,B\overline{D} + ACD$

b) Design a full-subtractor and implement it using basic logic gates. **06**

**5.** a) Design a synchronous BCD counter using J-K flip flops. **04**

b) If a counter having 10 FF's is initially at 0, what count will it hold after 2060 pulses? Compare Synchronous and Asynchronous counter. **04**

c) Explain any four operating characteristics and applications of flip-flops. **04**

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**Q1.** **Solve**

**a)** What are the specifications of ideal OP-AMP? How the ideal characteristics of OP-AMP are approach in an actual OP-AMP? Draw ideal V/I characteristics of OP-AMP **06**

**b)** The input to an OP-AMP differentiator circuit is a sinusoidal voltage of peak value of 10 μV and frequency 2kHz. Determine the output voltage if R=50kΩ and C=2μF **06**

**Q2.** **Solve any Two**

**a)** Explain voltage controlled oscillator (VCO) Using timer 555. Can we change the output frequency of **06**

*Contd..*

VCO? How?

b) In Monostable multivibrator using IC555, when $R_A$=10 kΩ and output pulse width tp=2.2ms determine the value of C to be required. **06**

c) Draw the circuit diagram of 555 timer connected as an astable multivibrator and explain its operation. **06**

**).3 Solve any two**

a) Compare ECL, TTL and CMOS logic families and Why are CMOS Ics preferred in low power applications? **06**

b) Output one appears in the truth table for following input conditions ABCD = 0001,0100,1011. Find output minimized expression and implement it using logic gates. **06**

c) Minimize the following logic functions and realize it using NOR gate. **06**
$F(A,B,C,D)= \pi M(1,2,3,8,9,10,11,14) \cdot d(7,15)$

**).4 Solve**

a) Design two bit comparator using gates. **06**

b) Design full subtractor using 2:1 MUX Ics **06**

**).5 Solve any two**

a) Design synchronous MOD 12 UP counter using T flip flop **06**

b) Design ripple Decade counter using JK flip-flop **06**

c) Design 3 bit Bi-directional shift register **06**

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| | | | |
|---|---|---|---|
| 1. | a) | Enlist the features of IC741. | 6 |
| | b) | Elaborate the terms: Input offset voltage, input offset current, Input bias current, CMRR, slew rate, Gain-bandwidth product. | 6 |
| | c) | Derive an expression for open-loop gain as a function of frequency. Plot the graph of open-loop gain and phase versus frequency. And comment on the result. | 6 |
| 2. | a) | Discuss basic negative clipper circuit. Modify this | 6 |

*Contd.*

circuit to work as half wave rectifier.

b) Design a phase shift oscillator so that $f_o = 200Hz$. What are the problems associated with basic differentiator circuit? How they are corrected? Draw the frequency response of basic and practical differentiator. 6

3. a) State and prove the DeMorgan's Laws and give its importance. 6

b) Describe the methods of conversion of SOP to POS form. Convert the SOP form equation to its equivalent POS form equations. 6

$$f = A\bar{B}CD + \bar{A}\bar{B}CD + ABC\bar{D} + AB\bar{C}\bar{D} + A\bar{B}\bar{C}D + ABCD$$

4. a) Reduce the equation given in Q3 b) by using k-map. Describe the role of don't care condition in k-map reduction, considering d(7,13) in the same function. 6

b) Design a 4-bit parallel subtractor using logic gates that utilizes the 1's complement method for subtraction 6

c) What is the difference between encoder and multiplexer? Draw and explain the working of 8:3 encoder and 8:1 multiplexer to point out the differences. 6

5. a) Enlist the types of shift registers. Describe parallel-in-serial-out shift register. 6

b) Design Mod-10 counter using JK flip-flops. Can this counter be used for BCD counting? 6

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**Q1.** **Solve any two**

**a)** What are the factors that contribute to the propagation delay in digital gate devices? Compare the propagation delays of various logic families. **06**

**b)** A Boolean function has four input variables. The first seven outputs are true and the next three are false and others are don't cares. Find out the minimize expressions and implement it using logic gates. **06**

*Contd..*

c) Minimize the following logic function and realize using NAND gates 06
$f(A,B,C,D)= \Sigma m(1,3,5,8,9,11,15)+d(2,13)$

**Q2. Solve**

a) Design 40:1 MUX using 8:1 MUX(S) 06

b) Implement the following multi output combinational logic circuit using 4 line to 16 line decoder 06

$F1 = \Sigma m(1,2,5,7,8,11,13)$
$F2 = \Sigma m(3,4,9,11)$
$F3 = \Sigma m(10,13,14)$
$F4 = \Sigma m(6,9,12,15)$

**Q3. Solve Any Two**

a) Design synchronous MOD 7 UP-DOWN counter using JK flip-flop and one control input N for UP-DOWN counting 06

b) Explain the operation of Bi Directional shift register with its circuit diagram 06

c) Design the following ripple counter using T flip flops 06
1. Divide- by -5
2. Divide-by-7

**Q4. Solve**

a) An inverting amplifier has $R_f$=500kΩ and $R_1$=5 kΩ. Determine the amplifier circuit voltage gain, input resistance and output resistance. Determine also the output voltage and input current if the 06

**Q5.**

input voltage in 0.1 V. Assume OP/AMP to be ideal one.

b) "The gain of differential amplifier is same as inverting amplifier" elaborate and prove the above statement. **06**

**Q5. Solve any Two**

a) Explain the working principal of Monostable multi vibrator using Timer. **06**

b) What are the essential building blocks of IC 555? Explain. What do you mean by grounded load? And why normally control terminal of IC 555 Timer is connected to ground through 0.01 μf by pass capacitor **06**

c) Design astable multivibrator with an output signal frequency of 800 Hz and 60% duty cycle. **06**

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**1. a)** Elaborate the term 'Operational Amplifier'. Draw and explain the building blocks of Operational Amplifier. **6**

**b)** Enlist the electrical characteristics of an ideal op-amp. **6**

**c)** Design a compensating network for op-amp. The op-amp uses $\pm 10V$ supply voltages. The $V_{io}$ is specified as 10mV. **6**

**2. a)** Discuss basic positive and negative clampers. Also draw an inverting comparator with positive **6**

feedback. This circuit should convert an irregular-shaped waveform to a square wave or pulse. Name this circuit.

b) Design a Wein bridge oscillator so that $f_o = 965Hz$. What are the problems associated with basic integrator circuit? How they are corrected? Draw the frequency response of basic and practical integrator. 6

3. a) Design Ex-or gate using universal gates Brief the needs of universal gates. 6

b) Describe noise margin, propagation delay and Q-factor of digital ICs. 6

4. a) Design 4-bit BCD adder using 4-bit binary adder IC. 6

b) Describe working of 4-bit magnitude comparator. Design 5-bit magnitude comparator using 4-bit magnitude comparator IC. 6

5. a) Design a 16:1 multiplexer using minimum number of 4:1 multiplexer. 6

b) What do you mean by Race-around condition? How it is taken care in JK flip-flop? 6

c) Describe the working of universal counter along with necessary timing diagram. 6

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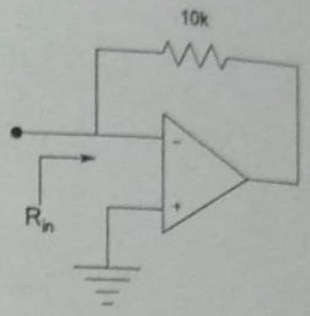
1 a) **i.** What is the use of difference amplifier stage in an op-amp? The ideal Op-Amp has Ri =? , A=? and Ro=? **12**

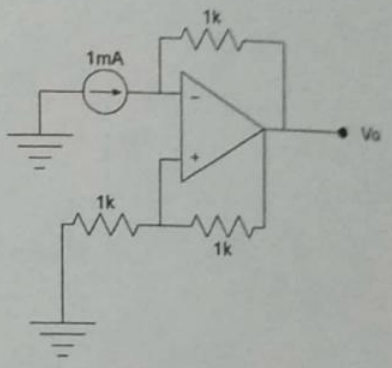
**ii.** In response to a square wave input, the output of an op-amp changed from -3V to +3V over a time interval of 0.25µsec. Determine the slew rate of the op-amp?

**iii.** What is the purpose of compensating networks?

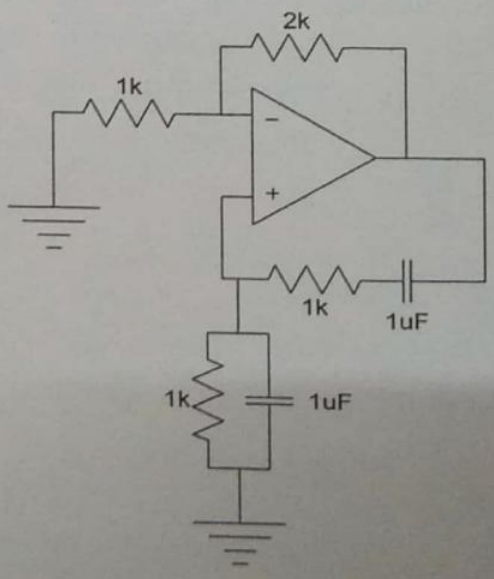
**iv.**Find $R_{in}$ if open loop gain is 10




**v.**What is the output voltage $V_0$ shown in circuit?




**vi.**Recognize the type of oscillator and find the oscillating frequency




**2.** a) Design a phase shift oscillator to oscillate at 0.1 kHz and how frequency of oscillation depends upon RC components? **06**

b) A Schmitt trigger with hysteresis width $V_H = 2V$ and lower threshold level $V_{LT} = -1.5V$ converts a 1kHz sine wave of amplitude 5 V pp into a square wave. Calculate the time duration of the negative and positive portion of the output waveform. **06**

c) Draw and explain the functional diagram of a 555 timer as monostable multivibrator. **06**

3. a) **i.**Apply Demorgans theorem to expression $f = \overline{\overline{AB}(CD + \bar{E}F)\,(\overline{AB} + \overline{CD})}$ **04**

**ii.**Reduce the expression $f = \overline{\overline{AB} + \bar{A} + AB}$

b) Make a K-map of F = AB + A$\bar{C}$ +C + AD + A$\bar{B}$C + ABC and obtain minimal expression in SOP and POS form. **04**

c) Compare TTL, ECL, $I^2L$ and CMOS logic families with the help of noise margin, fan-out, power dissipation and propagation delay **04**

4. a) Design a combinational circuit using logic gates which compares 2-bit. The circuit should have less than, greater than and equal to outputs. **04**

b) Design a 4-digit BCD adder using 7483 adders **04**

c) Implement 3-input XOR logic gate using a multiplexer. **04**

5. a) Design a 4-bit binary UP/DOWN ripple counter with a control for UP/DOWN counting **06**

b) Derive the characteristic equations of JK, SR, D and T flip-flop. **06**