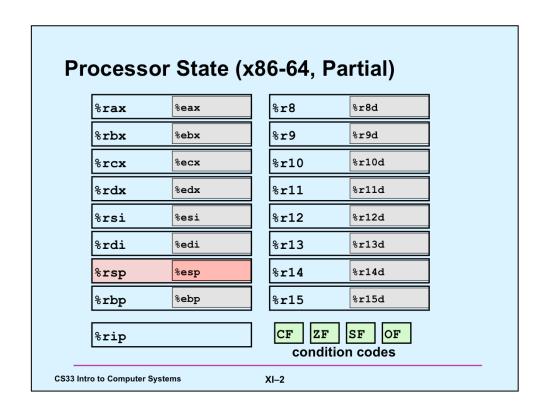


Most of the slides in this lecture are either from or adapted from slides provided by the authors of the textbook "Computer Systems: A Programmer's Perspective," 2nd Edition and are provided from the website of Carnegie-Mellon University, course 15-213, taught by Randy Bryant and David O'Hallaron in Fall 2010. These slides are indicated "Supplied by CMU" in the notes section of the slides.



Condition Codes (Implicit Setting)

· Single-bit registers

```
CF carry flag (for unsigned) SF sign flag (for signed)

ZF zero flag OF overflow flag (for signed)
```

Implicitly set (think of it as side effect) by arithmetic operations

```
example: add1/addq Src,Dest \leftrightarrow t = a+b CF set if carry out from most significant bit (unsigned overflow) ZF set if t == 0 SF set if t < 0 (as signed) OF set if two's-complement (signed) overflow (a>0 && b>0 && t<0) || (a<0 && b<0 && t>=0)
```

Not set by lea instruction

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Condition Codes (Explicit Setting: Compare)

• Explicit setting by compare instruction

```
cmpl/cmpq src2, src1
cmpl b,a like computing a-b without setting destination
```

CF set if carry out from most significant bit (used for unsigned comparisons)

```
ZF set if a == b

SF set if (a-b) < 0 (as signed)

OF set if two's-complement (signed) overflow

(a>0 \&\& b<0 \&\& (a-b)<0) \mid \mid (a<0 \&\& b>0 \&\& (a-b)>0)
```

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Condition Codes (Explicit Setting: Test)

· Explicit setting by test instruction

```
test1/testq src2, src1
test1 b,a like computing a&b without setting destination
```

- sets condition codes based on value of Src1 & Src2
- useful to have one of the operands be a mask

```
ZF set when a&b == 0
SF set when a&b < 0
```

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Reading Condition Codes

- SetX instructions
 - set single byte based on combinations of condition codes

SetX	Condition	Description	
sete	ZF	Equal / Zero	
setne	~ZF	Not Equal / Not Zero	
sets	SF	Negative	
setns	~SF	Nonnegative	
setg	~(SF^OF)&~ZF	Greater (Signed)	
setge	~(SF^OF)	Greater or Equal (Signed)	
setl	(SF^OF)	Less (Signed)	
setle	(SF^OF) ZF	Less or Equal (Signed)	
seta	~CF&~ZF	Above (unsigned)	
setb	CF	Below (unsigned)	

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Reading Condition Codes (Cont.) · SetX instructions: - set single byte based on combination of condition codes · Uses one of 8 addressable byte registers - does not alter remaining 7 bytes - typically use movzbl to finish job int gt (int x, int y) %rax %eax %ah %al return x > y; **Body** cmpl %esi, %edi # compare x : y setg %al # %al = x > ymovzbl %al, %eax # zero rest of %eax/%rax CS33 Intro to Computer Systems XI-7

Jumping

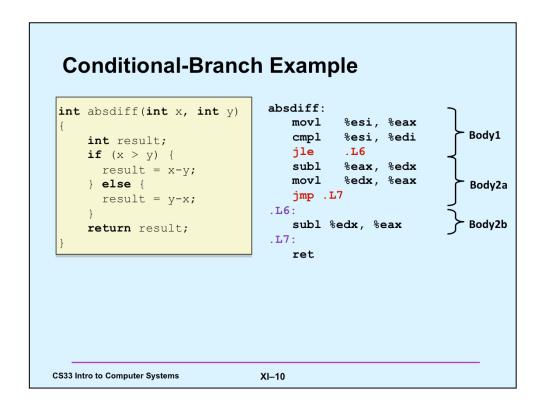
- jX instructions
 - Jump to different part of code depending on condition codes

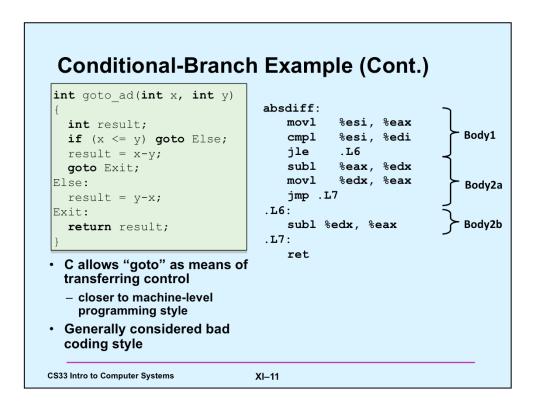
jΧ	Condition	Description	
jmp	1	Unconditional	
je	ZF	Equal / Zero	
jne	~ZF	Not Equal / Not Zero	
js	SF	Negative	
jns	~SF	Nonnegative	
jg	~(SF^OF)&~ZF	Greater (Signed)	
jge	~(SF^OF)	Greater or Equal (Signed)	
jl	(SF^OF)	Less (Signed)	
jle	(SF^OF) ZF	Less or Equal (Signed)	
ja	~CF&~ZF	Above (unsigned)	
jb	CF	Below (unsigned)	

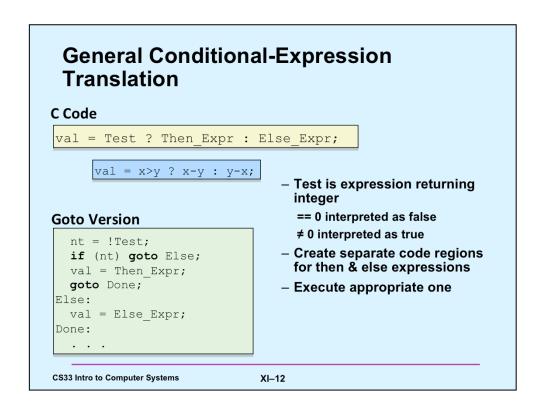
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Jumping • jX instruction – Jump to differ	, (e.ga.)		f the		
jΧ	Condition	Description			
jmp 1	1	Unconditional			
je 2	ZF	Equal / Zero			
jne ^	~ZF	Not Equal / Not Zero			
js S	SF	Negative			
jns	~SF	Nonnegative			
jg	~(SF^OF)&~ZF	Greater (Signed)			
jge ^	~(SF^OF)	Greater or Equal (Signed)			
jl	(SF^OF)	Less (Signed)			
jle	(SF^OF) ZF	Less or Equal (Signed)			
ja ^	~CF&~ZF	Above (unsigned)			
jb	CF	Below (unsigned)			
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Using Conditional MovesConditional move instructions

- instruction supports:
 - if (Test) Dest ← Src
- supported in post-1995 x86 processors
- gcc does not always use them
 - » wants to preserve compatibility with ancient processors
 - » enabled for x86-64
 - » use switch -march=686 for IA32

· Why use them?

- branches are very disruptive to instruction flow through pipelines
- conditional moves do not require control transfer

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```
C Code
```

```
val = Test
   ? Then_Expr
   : Else_Expr;
```

Goto Version

```
tval = Then_Expr;
result = Else_Expr;
t = Test;
if (t) result = tval;
return result;
```

Supplied by CMU.

Note that, as shown in the goto version, both the then_expr and the else_expr are computed before the test is done.

Conditional Move Example: x86-64 int absdiff(int x, int y) { int result; **if** (x > y) { result = x-y; } else { result = y-x; return result; absdiff: x in %edi movl %edi, %eax subl %esi, %eax # result = x-y y in %esi movl %esi, %edx subl %edi, %edx # tval = y-x %esi, %edi # compare x:y cmpl cmovle %edx, %eax # if <=, result = tval</pre> ret **CS33 Intro to Computer Systems** XI-14

Bad Cases for Conditional Move Expensive Computations val = Test(x) ? Hardl(x) : Hardl(x); both values get computed only makes sense when computations are very simple Risky Computations val = p ? *p : 0; both values get computed may have undesirable effects

Computations with side effects val = x > 0 ? x*=7 : x+=3;

both values get computed

· must be side-effect free

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"Do-While" Loop Example

C Code

```
int pcount_do(unsigned x)
{
  int result = 0;
  do {
    result += x & 0x1;
    x >>= 1;
  } while (x);
  return result;
}
```

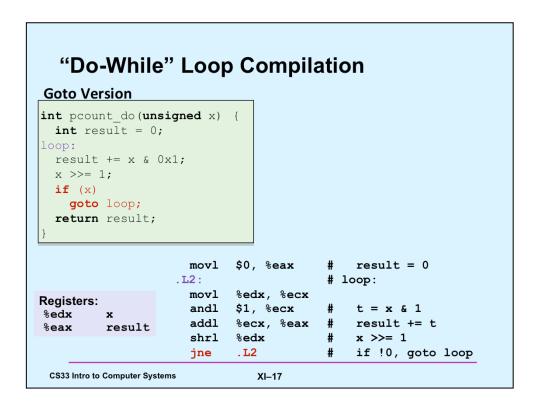
Goto Version

```
int pcount_do(unsigned x)
{
  int result = 0;
loop:
  result += x & 0x1;
  x >>= 1;
  if (x)
    goto loop;
  return result;
}
```

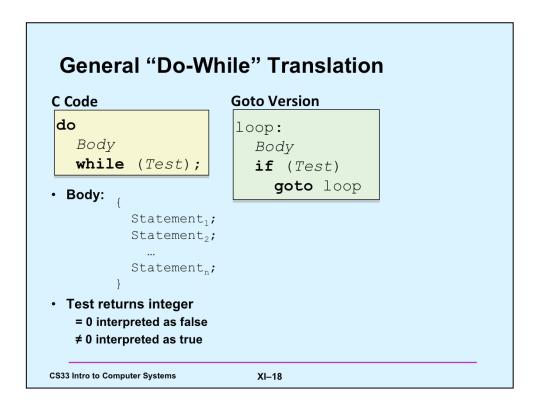
- Count number of 1's in argument x ("popcount")
- Use conditional branch either to continue looping or to exit loop

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Note that the condition codes are set as part of the execution of the shrl instruction.



"While" Loop Example

C Code

Goto Version

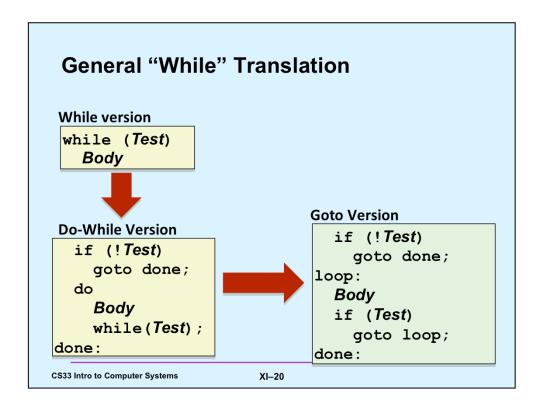
```
int pcount_while(unsigned x) {
  int result = 0;
  while (x) {
    result += x & 0x1;
    x >>= 1;
  }
  return result;
}
```

```
int pcount_do(unsigned x) {
  int result = 0;
  if (!x) goto done;
loop:
  result += x & 0x1;
  x >>= 1;
  if (x)
    goto loop;
done:
  return result;
}
```

- Is this code equivalent to the do-while version?
 - must jump out of loop if test fails

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"For" Loop Example

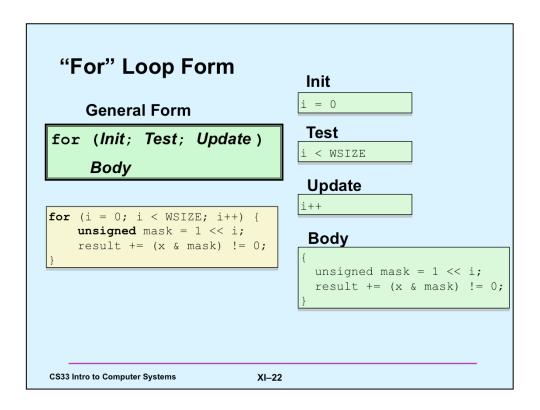
C Code

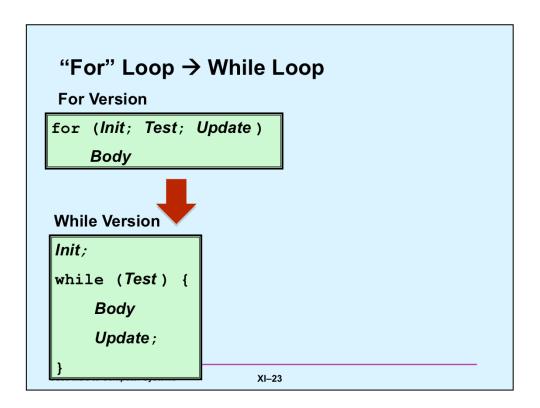
```
#define WSIZE 8*sizeof(int)
int pcount_for(unsigned x) {
   int i;
   int result = 0;
   for (i = 0; i < WSIZE; i++) {
      unsigned mask = 1 << i;
      result += (x & mask) != 0;
   }
   return result;
}</pre>
```

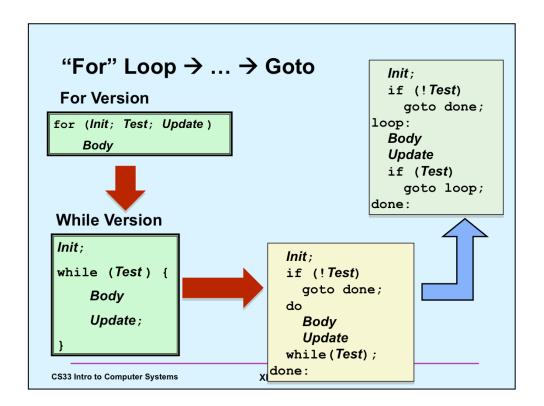
• Is this code equivalent to other versions?

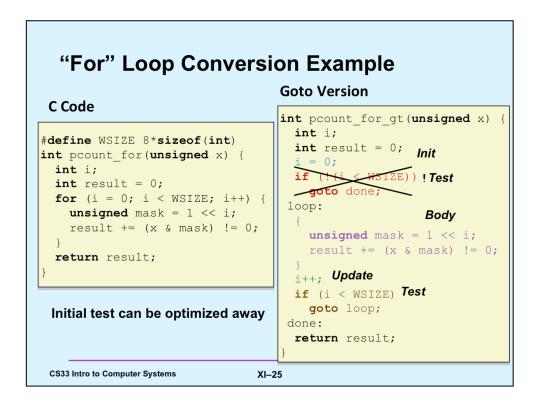
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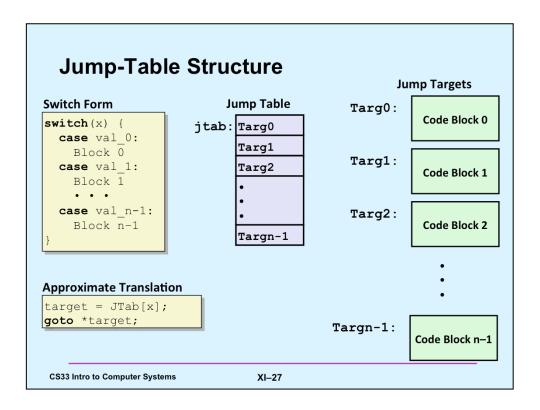


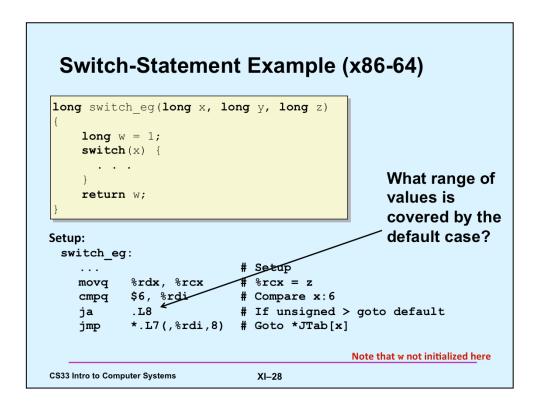


```
Switch-Statement
long switch_eg
                                   Example
   (long x, long y, long z) {
   long w = 1;
   switch(x) {
   case 1:
                                     · Multiple case labels
      w = y * z;
                                        - here: 5 & 6
      break;
   case 2:
                                     · Fall-through cases
       w = y/z;
/* Fall Through */
                                        - here: 2
   case 3:

    Missing cases

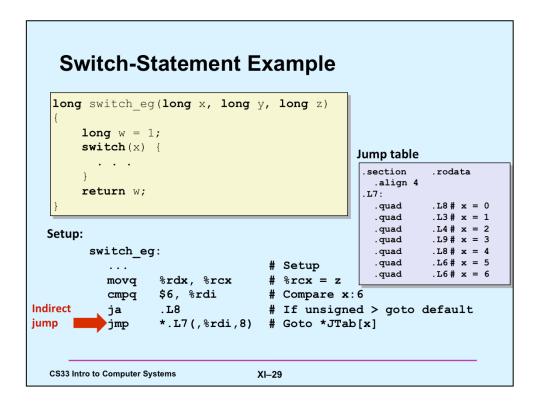
       w += z;
       break;
                                        - here: 4
   case 5:
       w -= z;
      break;
   default:
       w = 2;
   return w;
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                                XI-26
```





Note that the ja in the slide causes a jump to occur if the previous comparison is interpreted as being performed on unsigned values, and the result is that x is greater than (above) 6. Given that x is declared to be a *signed* value, for what range of values of x will ja cause a jump to take place?

Note that the assembler code shown in the examples was produced by compiling the C code using gcc with the "-O1" flag.



Assembly-Setup Explanation

- Table structure
 - each target requires 8 bytes
 - base address at .L7
- Jumping

```
direct: jmp .L8
```

- jump target is denoted by label .L8

```
indirect: jmp *.L7(,%rdi,8)
```

- start of jump table: .L7
- must scale by factor of 8 (labels have 8 bytes on x86-64)
- fetch target from effective address .L7 + rdi*8 $\,$
 - » only for $0 \le x \le 6$

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Jump table

.align 4

. quad

. quad . quad

. quad . quad

.section .rodata

.quad .L3 # x = 1 .quad .L4 # x = 2

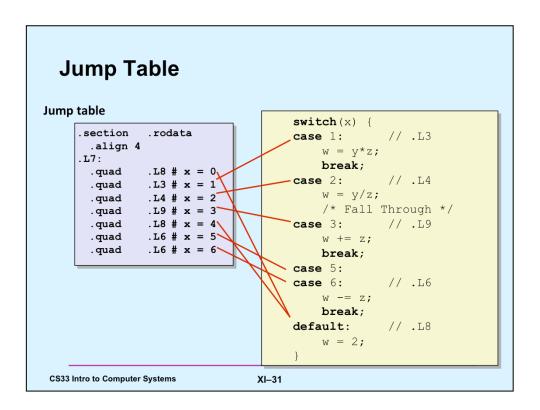
. L8 # x = 0

. L9 # x = 3

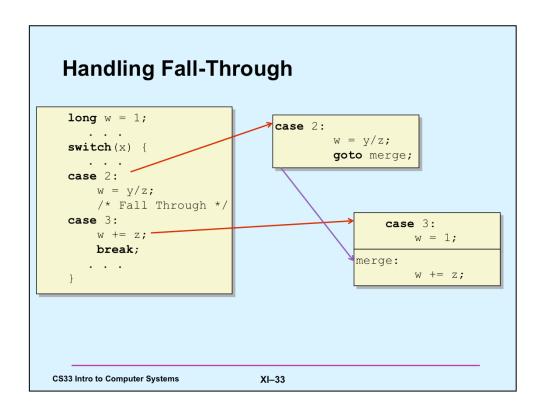
. L8 # x = 4

.L6 # x = 5

.L6 # x = 6



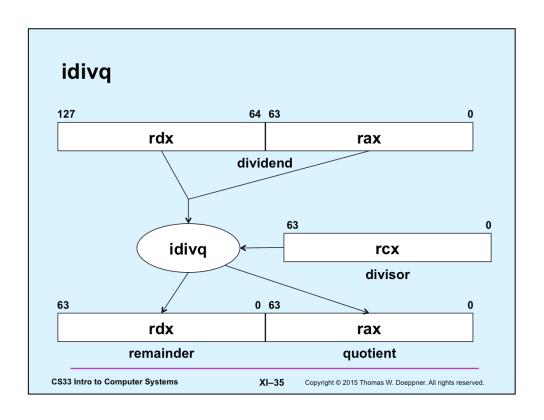
Code Blocks (Partial) switch(x) { # x == 1movl %rsi, %rax # y **case** 1: // .L3 W = y * z;imulq %rdx, %rax # w = y*z break; # x == 5, x == 6movl \$1, %eax # w = 1 subq %rdx, %rax # w -= z break; # Default default: // .L8 mov1 \$2, %eax # w = 2w = 2;ret **CS33 Intro to Computer Systems** XI-32



Code Blocks (Rest) # x == 2switch(x) { movq %rsi, %rax case 2: // .L4 movq %rsi, %rdx w = y/z;sarq \$63, %rdx /* Fall Through */ idivq %rcx case 3: // .L9 jmp w += z; break; movl \$1, %eax L5: # merge: addq %rcx, %rax # ret **CS33 Intro to Computer Systems** XI-34

Supplied by CMU, but converted to x86-64.

The code following the .L4 label requires some explanation. The idivq instruction is special in that it takes a 128-bit dividend that is implicitly assumed to reside in registers rdx and rax. Its single operand specifies the divisor. The quotient is always placed in the rax register, and the remainder in the rdx register. In our example, y, which we want to be the dividend, is copied into both the rax and rdx registers. The sarq (shift arithmetic right quadword) instruction propagates the sign bit of rdx across the entire register, replacing its original contents. Thus, if one considers rdx to contain the most-significant bits of the dividend and rax to contain the least-significant bits, the pair of registers now contains the 128-bit version of y. The idivq instruction computes the quotient from dividing this 128-bit value by the 64-bit value contained in register rax (containing z). The quotient is stored register rax (implicitly) and the remainder is stored in register rdx (and is ignored in our example). This illustrated in the next slide.



```
x86-64 Object Code

    Setup

       - label .L8 becomes address 0x4004e5
       - label .L7 becomes address 0x4005c0
Assembly code
switch_eg:
   . . .
          .L8
                        # If unsigned > goto default
   jа
          *.L7(,%rdi,8) # Goto *JTab[x]
   jmp
Disassembled object code
00000000004004ac <switch_eg>:
                                ja
 4004b3: 77 30
                                       4004e5 <switch_eg+0x39>
 4004b5: ff 24 fd c0 05 40 00 jmpq
                                       *0x4005c0(,%rdi,8)
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                             XI-36
```

Disassembly was accomplished using "objdump –d". Note that the text enclosed in angle brackets ("<", ">") is essentially a comment, relating the address (4004e5) to a symbolic location (0x39 bytes after the beginning of *switch_eg*).

x86-64 Object Code (cont.)

- Jump table
 - doesn't show up in disassembled code
 - can inspect using gdb

```
gdb switch
```

(gdb) x/7xg 0x4005c0

- » examine 7 hexadecimal format "giant" words (8-bytes each)
- » use command "help x" to get format documentation

 0x4005c0:
 0x0000000004004e5

 0x4005d0:
 0x0000000004004c4

 0x4005e0:
 0x00000000004004e5

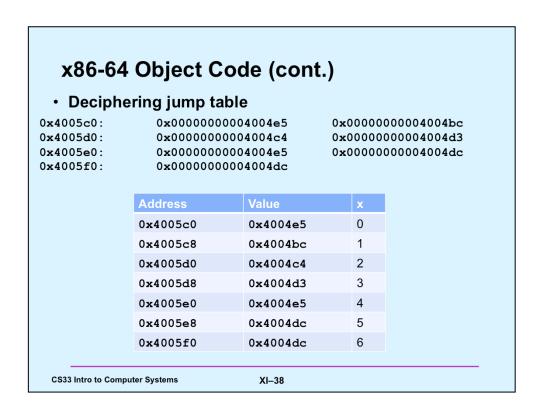
 0x4005f0:
 0x000000000004004dc

 0x4005c0: 0x00000000004004e5 0x00000000004004bc 0x00000000004004d3 0x00000000004004dc

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Supplied by CMU, but converted to x86-64. We assume that the switch_eg function was included in a program whose name is switch. Hence, gdb is invoked from the shell with the argument "switch".



Disassembled Targets

```
(gdb) disassemble 0x4004bc,0x4004eb
Dump of assembler code from 0x4004bc to 0x4004eb
  0x00000000004004bc <switch_eg+16>: mov
                                             %rsi,%rax
                                     imul
                                              %rdx,%rax
  0x00000000004004bf <switch_eg+19>:
  0x000000000004004c3 <switch_eg+23>:
                                      retq
  0x00000000004004c4 <switch eg+24>:
                                      mov
                                              %rsi,%rax
  0x00000000004004c7 <switch eg+27>:
                                              %rsi,%rdx
                                      mov
  0x00000000004004ca <switch eg+30>:
                                              $0x3f,%rdx
                                     sar
  0x00000000004004ce <switch eg+34>:
                                     idiv
                                              0x4004d8 <switch_eg+44>
  0x000000000004004d1 <switch eg+37>:
                                     jmp
                                     mov
  0x00000000004004d3 <switch eg+39>:
                                              $0x1,%eax
  0x00000000004004d8 <switch_eg+44>:
                                      add
                                              %rcx,%rax
  0x00000000004004db <switch_eg+47>:
                                       retq
  0x000000000004004dc <switch eg+48>:
                                              $0x1,%eax
                                       mov
  0x00000000004004e1 <switch eg+53>:
                                       sub
                                              %rdx,%rax
  0x00000000004004e4 <switch eg+56>:
  0x00000000004004e5 <switch_eg+57>:
                                              $0x2,%eax
                                       mov
  0x00000000004004ea <switch_eg+62>:
                                      retq
```

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